Homework 4 Written

Points: 35

The pdf you submit must look exactly like this with the answers and all supporting works shown on the the page with the question.

Last Name	First Name	Student ID
Ahmed	Fareeha	999307203
Partner Last Name	**Partner First Name**	**Partner Student ID**

1. (3) Given that you have a Fully Associative cache of size 2^10 bytes with a line size of 16 bytes show how an Address of 29 bits would be partitioned.

$S = 1$ set $\quad LS = 16$

set bits = $\log_2(S) = \log_2(1) = 0$

offset bits = $\log_2(\text{linesize}) = \log_2(16) = 4$

tag = leftover

29 -

Tag	Set	Offset
28-4	none	3-0

32768 bits 256 bits

2. (3) Given that you have Direct Mapped cache of size 2^12 bytes with a line size of 32 bytes show how an Address of 50 bits would be partitioned.

$W = 1$

$\#set = \frac{\#\ lines}{W} = 128$

$\#lines = \frac{c}{linesize} = \frac{32768}{256} = 128$

$\#set\ bits = \log_2(s) = \log_2(128) = 7$

$\#offset\ bits = \log_2(32) = 5$

tag	set	offset
49 – 12	11 – 5	4 – 0

3. (3)Given that you have a 5 way Set Associate cache of size 5242880 bytes with a line size of 64 bytes show how an Address of 64 bits would be partitioned.

$W = 5 \rightarrow 5$ lines / set

$\#\text{ lines} = \frac{C}{\text{linesize}} = \frac{5242880}{64} = 81920$

$\#\text{set} = \frac{\#\text{lines}}{W} = \frac{81920}{5} = 16384$

$\#\text{ setbits} = \log_2(16384) = 14$

$\#\text{ offsetbits} = \log_2(\text{linesize}) = \log_2(64) = 6$

Tag	set	offset
63 - 20	19 - 6	5 - 0

8 bits 00000001

4. (3 per) Here is a string of hex address references given as byte addresses: 1, 2, 3, 1A, A,1B, 16, 14, 3, 12, 9, 23 ,3A, 5, 19, 1, 9
   1. Assuming a **direct mapped cache** with a **total size of 16 bytes** and a **line size that is 1 byte**. that is initially empty, label each reference in the list as a hit or miss and show the final contents of the cache tag bits for each line. If a line is not written to leave its tag bits blank. Compute the hit rate for this example.

W=1

$\#\text{lines} = \frac{C}{\text{linesize}} = 16$

$\#\text{set} = \frac{\#\text{lines}}{W} = 16$

$\#\text{set bits} = \log_2(16) = 4$

$\#\text{offset bits} = 0$

Address

Tag	set	offset
7-4	3-0	X

	set	tag	Value
0	0000		
1	0001	0000	1
2	0010	0001	12
3	0011	0010	23
4	0100	0001	14
5	0101	0000	5
6	0110	0001	16
7	0111		
8	1000		
9	1001	0000	9
10	1010	0011	3A
11	1011	0001	1B
12	1100		
13	1101		
14	1110		
15	1111		

HR: 2/17

1	2	3	1A	A	1B	16	14	3	12	9	23	3A	5	19	1	9
M	M	M	M	M	M	M	M	H	M	M	M	M	M	M	H	M

2. Repeat 4.1 but for a **direct mapped cache** that is **16 bytes big** and has a **line size of 4 bytes**

$W = 1$

$\# lines = \frac{C}{line\ size} = \frac{16}{4} = 4$

$\# set = \frac{\# lines}{W} = \frac{4}{1} = 4$

$\# setbits = \log_2(\# set) = \log_2(4) = 2$

$\# offsetbits = \log_2(line\ size) = \log_2(4) = 2$

Address

Tag	set	offset
7-4	3-2	1-0

set	Tag	Val 00	Val 01	10	11
00	0000	0	1	2	3
01	0000	4	5	6	7
10	0000	10	9	A	B
11	0				

HR: 4/17

1	2	3	1A	A	1B	16	14	3	12	9	23	3A	5	19	1	9
M	H	H	M	M	M	M	H	H	M	M	M	M	M	M	M	M

	tag	s	o
1	0000	00	01
2	0000	00	10
3	0000	00	11
1A	0001	10	10
A	0000	10	10
1B	0001	10	11
16	0001	01	10
14	0001	01	00
12	0001	00	10
9	0000	10	01
23	0010	00	11
3A	0011	10	10
5	0000	01	01
19	0001	10	01

$k=2$

3. **Repeat 4.1 but for a two way set associative cache that is 16 bytes big and has a line size of 1 byte. Assume an LRU replacement strategy is used.**

$W=2$

$\#\text{lines} = \frac{C}{\text{linesize}} = \frac{16}{1} = 16$

$\#\text{set} = \frac{\#\text{lines}}{W} = \frac{16}{2} = 8$

$\#\text{setbits} = \log_2(8) = 3$

$\#\text{offsetbits} = \log_2(\text{linesize}) = \log_2(1) = 0$

Address

Tag	Set	offset
7 - 3	2 - 0	X

	tag 1	Val 1	Age 1	Tag 2	Val 2	Age 2
000						
001	00001	9	~~1 1 0 0~~ 0	00000	9 1	~~0 1~~ 0
010	00111	3A	~~0 1~~ 0	00010	~~1A~~ 12	~~0 1 0~~ 1
011	00100	23	~~1~~ 0	00011	1B	~~0~~ 1
100	00010	14				
101	00000	5				
110	00010	16				
111						

HR : 1/17

1	2	3	1A	A	1B	16	14	3	12	9	23	3A	5	19	1	9
M	M	M	M	M	M	M	M	H	M	M	M	M	M	M	M	M

16 8 4 2 1

00001 = 1

00111 = 7

00100 = 4

10 = 2

11 = 3

4. Repeat 4.1 but for a **fully associative** cache that is **16 bytes big** and has a **line size of 1 byte**. Assume an **LRU replacement strategy** is used.

$S = 1$ $C = 16$ $LS = 1$

#set bits = $\log_2(1) = 0$

#offset bits = $\log_2(1) = 0$

Address

Tag	set	offset
Ø	x	x

tag	Val
00000001	1
00000010	2
00000011	3
00011010	1A
00001010	A
00011011	1B
00010110	16
00010100	14
00010010	12
00001001	9
00100011	23
00111010	3A
00000101	5
00011001	19

1	2	3	1A	A	1B	16	14	3	12	9	23	3A	5	19	1	9
M	M	M	M	M	M	M	M	H	M	M	M	M	M	M	H	H

HR = 3/17

5. Repeat 4.1 but for a **fully associative** cache that is **16 bytes big** and has a **line size of 4 bytes**. Assume an **LRU replacement strategy** is used.

$S = 1 \rightarrow$ # set bits $= 0$

$LS = 4$, # offset bits $= \log_2(4) = 2$

Address

Tag	offset
7 - 2	1 - 0

3

tag	00	01	10	11	Ages
000110	18	19	1A	1B	~~1 2 3 0 1 2 3 0 1~~ 2
000000	0	1	2	3	~~0 1 2 3 0 1 2 3 0~~ 1
000010	8	9	A	B	~~0 1 2 3 0 1 2 3~~ 0
000001	4	5	6	7	~~0 1 2 3 0 1 2~~ 3

1	2	3	1A	A	1B	16	14	3	12	9	23	3A	5	19	1	9
M	H	H	M	M	H	M	M	H	M	H	M	M	M	M	M	M

HR: 5/17.