Homework 3 Written

The pdf you submit must look exactly like this with the answers and all supporting works shown on the the page with the question.

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Partner Last Name	**Partner First Name**	**Partner Student ID**

1. (5 points) Create a JK Flip-Flop using only a T Flip-Flop and basic logic gates.

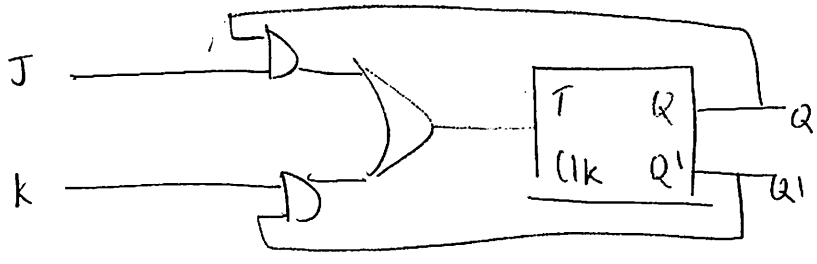
J	k	Q^1
0	0	Q
0	1	0
1	0	1
1	1	$\bar{Q}$

T	Q^1
0	Q
1	$\bar{Q}$

J	k	Q	T
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

Q \ Jk	00	01	11	10
0	0	0	1	1
1	0	1	1	0

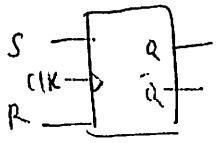
$T = J\bar{Q} + KQ$



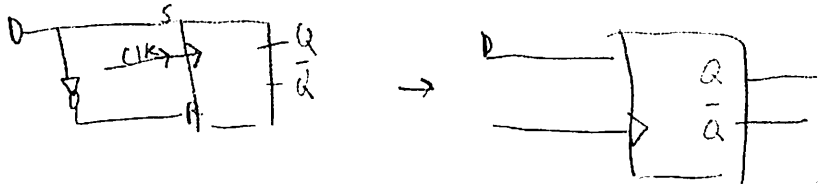
2. (5 points) Create an SR Flip-Flop using only a D Flip-Flop and basic logic gates.

SR

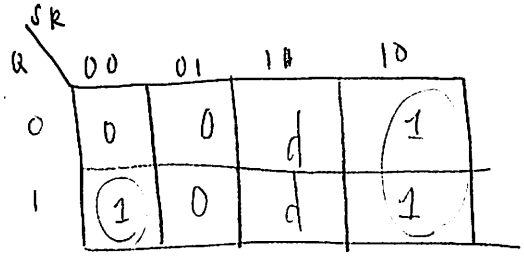
CLK	S	R	Q	$\bar{Q}$
0	X	X	Q	$\bar{Q}$
1	0	0	Q	$\bar{Q}$
1	0	1	0	1
1	1	0	1	0
1	1	1	E	E



CLK	D	Q	$\bar{Q}$
0	0	Q	$\bar{Q}$
0	1	Q	$\bar{Q}$
1	0	0	1
1	1	1	0

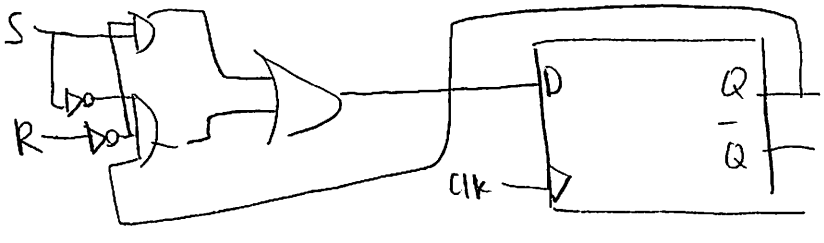


CLK	S	R	Q	D
0	X	X	Q	Q
1	0	0	Q	Q
1	0	1	0	0
1	1	0	1	1
1	1	1	E	X

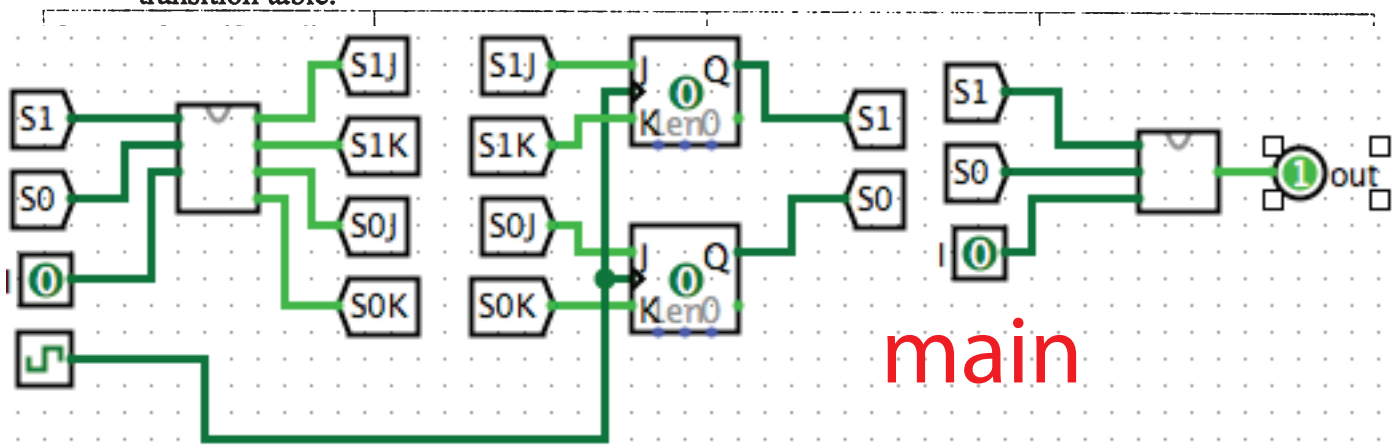


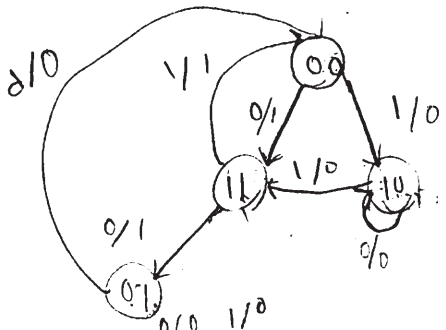
$D = S\bar{R} + \bar{S}\bar{R}Q$

S	R	Q	D
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	d
1	1	1	d



3. (5 points) Implement the **simplest** circuit possible using **JK Flip-Flops** based on the following transition table.





0/1, 1/1

(S_{11}, S_{00})

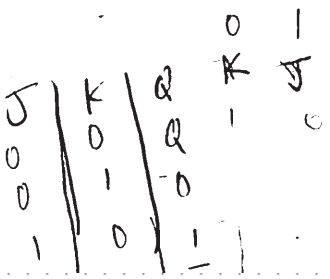
A

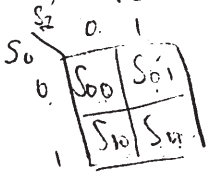
0/0 1/0

(S_{10}, S_{00}, S_{01})

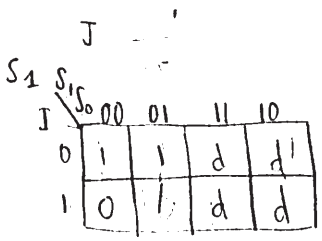
B

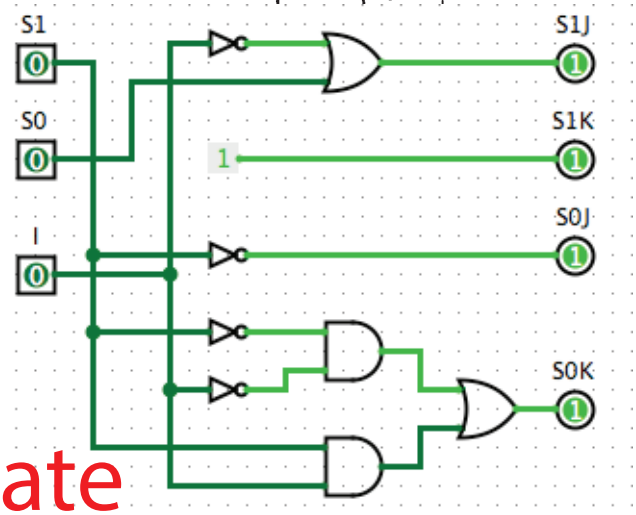
AA (S_{11}) AB (S_{00}) BA (S_{10}) (S_{01})

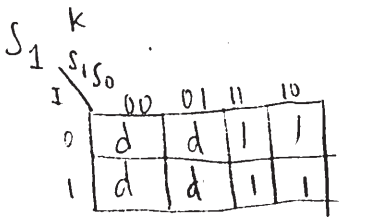


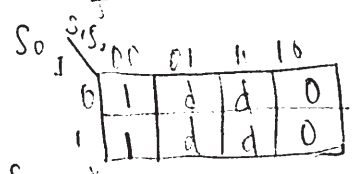


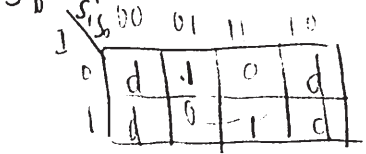
next state

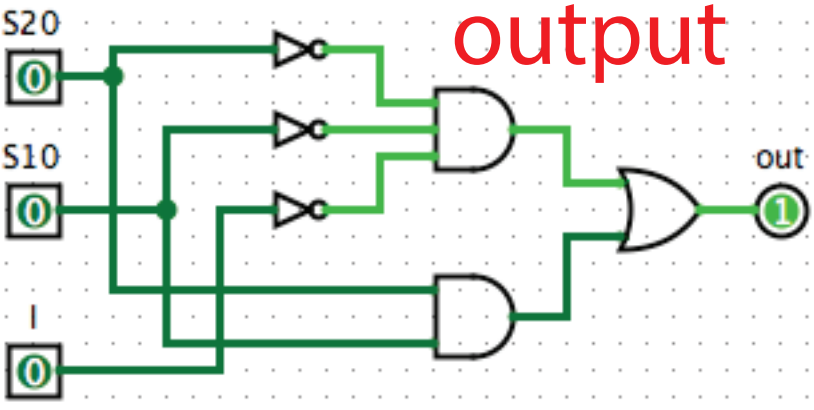




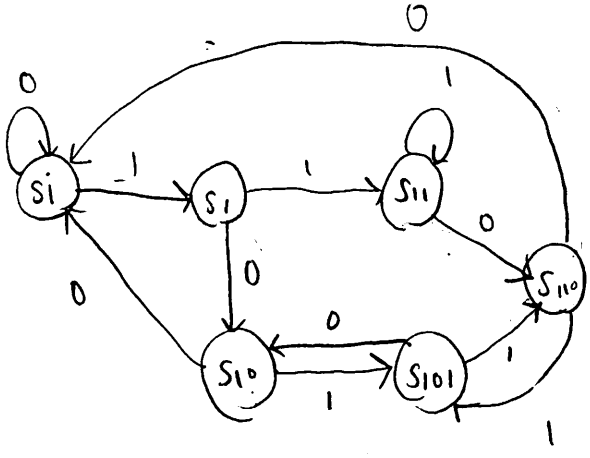






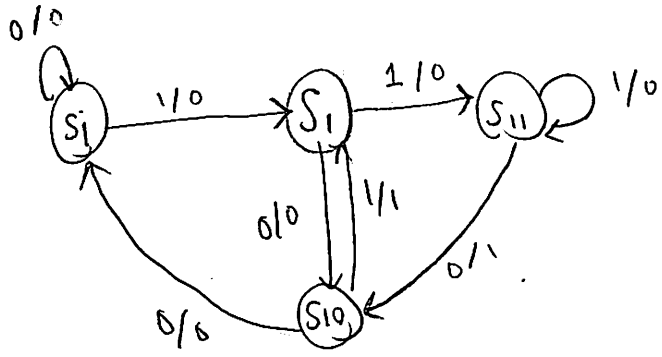


4. (5 points) Derive the **minimal** state table for a single input, single output **Moore** model FSM that outputs 1 whenever it detects either 110 or 101 in the input sequence. Overlapping sequences should be detected. For example if the input is 1101 then the output would be 00011 (Don't forget that the output of a Moore is delayed 1 clock cycle behind the input.



current state	input	next state	output
S_i	0	S_i	0
S_i	1	S_1	0
S_1	0	S_{10}	0
S_1	1	S_{11}	0
S_{10}	0	S_i	0
S_{10}	1	S_{101}	0
S_{11}	0	S_{110}	0
S_{11}	1	S_{11}	0
S_{101}	0	S_{10}	1
S_{101}	1	S_{11}	1
S_{110}	0	S_i	1
S_{110}	1	S_{101}	1

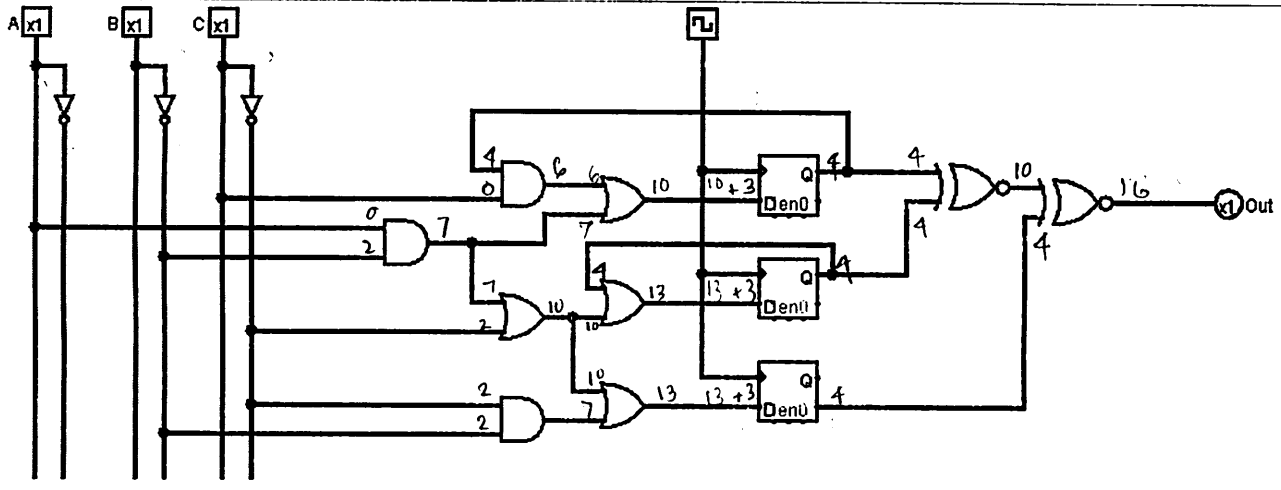
5. (5 points) Repeat number 4 but for a **Mealy** model FSM.



current state	input	next state	output
S_i	0	S_0	0
S_i	1	S_1	0
S_1	0	S_{10}	0
S_1	1	S_{11}	0
S_{10}	0	S_i	0
S_{10}	1	S_1	1
S_{11}	0	S_{10}	1
S_{11}	1	S_{11}	0

6. (5 points) Given the propagation delays contained in the table below and that the setup time for a D Flip-Flop is 3ns determine the length of the worst case path **and** the maximum clock frequency for the following circuit.

Gate	Propagation Delay
AND	5ns
OR	3ns
NOT	2ns
XNOR	6ns
D Flip-Flop	4ns



length: 16 ns

max clock frequency: $\frac{1}{16ns} = \frac{10^9}{16}$ Hz