A New Simplified Space-Vector PWM Method for Three-Level Inverters

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Abstract – **In this paper, a newly developed simplified space vector PWM(SVPWM) method for three-level inverter is presented. The space vector diagram of the three-level inverter is simplified into that of two-level inverter. So the selection of switching sequence and the calculation of the dwelling time is done as conventional two-level SVPWM method. The control of DC link neutral-point potential is easy to implement. And the proposed SVPWM method can be applied to the multi-level inverter. The validity of the new SVPWM method is verified by simulation and experiment with a three-level IGBT inverter.**

I. INTRODUCTION

Recently, with the dramatic improvements in high voltage technology, HVIGBT(High Voltage Insulated Gate Bipolar Transistor) and GCT(Gate Commutated Thyristor) are expanding the area of their application.

For the high performance AC drive systems at increased power levels, high quality inverter output is necessary for the low harmonic losses and torque pulsation. In the conventional two-level inverter configurations, the reduction of the harmonic contents of the inverter ouput current is achieved mainly by raising the switching frequency.

However in the field of high voltage, high power application, the switching frequency of the power devices has to be restricted below 1khz, due to the increased switching losses, even in case of the HVIGBT and GCT. So the harmonic reduction by raised switching frequency of the two-level inverter becomes more difficult in high power applications.

In addition, in two-level configurations, the DC link voltage of the two-level inverter is limited by the voltage ratings of the switching devices, so the problematic series connection of the switching devices is required to raise the DC link voltage. By series connection, the maximum allowable switching frequency has to be more lowered, thus the harmonic reduction becomes more difficult.

From the aspect of the harmonic reduction and the higher voltage level, three-level approach seems to be most promising alternative.

The harmonic contents of the three-level inverter is less than that of two-level inverter at the same switching frequency and the blocking voltage of the switching device is half of the DC-link voltage. So the three-level inverter topology is generally used in realizing the high performance, high voltage AC drive systems.

However, the inherent neutral-point potential variation of the three-level inverter has to be effectively suppressed to utilize the above mentioned advantages of the three-level inverter.

So the many PWM strategies have been proposed to solve the neutral-point potential unbalance problem. But many of them is focused mainly on the neutral-point potential control, while using complicated dwell-time calculation and voltage vector selection procedure.

In this paper, a simple SVPWM method for three-level inverter is proposed. By using the new PWM strategy, dwell-time calculation and voltage vector selection is easily done like that of two-level inverter. And the neutral-point voltage control by changing the sequence of the voltage vector is easy to implement.

The proposed three-level SVPWM method is verified using 2500V, three-level IGBT inverter system.

Ⅱ. Simplified Space Vector PWM Method

A. Basic principles of the proposed SVPWM Method

Fig. 1 is the circuit diagram of the NPC inverter and the switching states of one phase of the inverter are listed in table I. There are 3 kinds of switching states P, O and N in one phase, so the 27 switching states are exist for three phase inverter.

The principles of the proposed SVPWM method is easily explained using space vector diagram of a three-level inverter. The space vector of a three-level inverter, which is shown in fig. 2, can be thought that it is composed of six space vector diagrams of two-level inverter. Each space vector of two-level inverter is centered at the six apexes of the inner hexagon. So, if each of the six small hexagons is moved toward the center of the inner hexagon by Vdc/3

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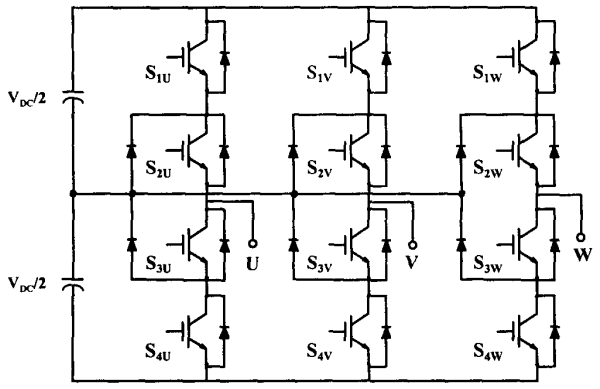


Fig. 1. Configuration of three-level inverter

TABLE I
SWITCHING STATES AND TERMINAL VOLTAGE(X=U,V,W)

Switching Symbols	Switching States				Terminal Voltage
	S_{1X}	S_{2X}	S_{3X}	S_{4X}	
P	ON	ON	OFF	OFF	$V_{DC}/2$
O	OFF	ON	ON	OFF	0
N	OFF	OFF	ON	ON	$-V_{DC}/2$

according to their location, the space vector diagram of a three-level inverter is simplified to that of two-level inverter. This is achieved by correcting the reference voltage vector, which will be explained in the following section. Then the determination of switching sequence and the calculation of duration time of three voltage vectors, surrounding the voltage reference vector, is done as like that of two-level SVPWM method.

The proposed SVPWM method is same as that of conventional two-level SVPWM in principle, so various techniques, which are used in two-level SVPWM, can be adopted to this method.

B. Simplification of Three-level Space Vector

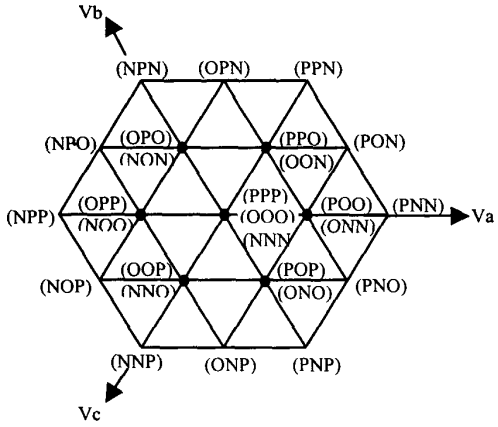
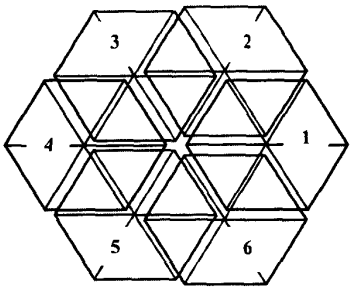
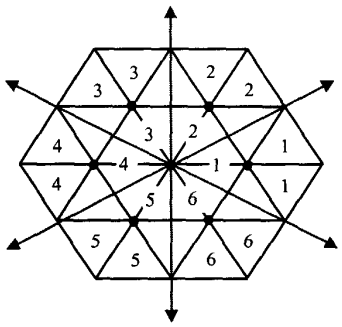


Fig. 2. Space Vector Diagram of Three-level Inverter



(a)



(b)

Fig. 3. Basic Principles of the Proposed PWM Method

As explained in the previous section, the space vector of three-level inverter can be simplified to that of two-level inverter. The number in fig. 3, represented as *s*, is the index that denotes the six small hexagons, constituting the three-level space vector diagram. As there exist the regions which are shared by adjacent small hexagons in the three-level space vector diagram, the criteria of determining the value of index *s* can be various as is shown in fig. 3 (a) and (b). If the three level space vector diagram is divided as in fig. 3(b), the index *s* of the shaded region of fig. 2 has the value of 1 or 2.

If the value of index s is determined according to the magnitude and the location of the voltage reference vector,

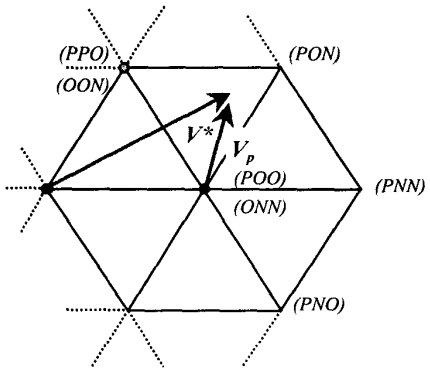


Fig.4. Simplification of the Three-level Space Vector to Two-level Space Vector

TABLE II

Redefinition of Reference Voltage Vector

S	Vas_ref =	Vbs_ref =
1	Vas_ref – Vdc/3.	Vbs_ref + Vdc/6.
2	Vas_ref – Vdc/6.	Vbs_ref - Vdc/6.
3	Vas_ref + Vdc/6.	Vbs_ref – Vdc/3.
4	Vas_ref + Vdc/3.	Vbs_ref - Vdc/6.
5	Vas_ref + Vdc/6.	Vbs_ref + Vdc/6.
6	Vas_ref – Vdc/6.	Vbs_ref + Vdc/3.

(*) Vcs_ref= -Vas_ref – Vbs_ref

the reference voltage vector is corrected by subtracting the center vector of the corresponding small hexagon from the original reference vector, as shown in fig.4. This is summarized in table II.

C. Calculation of the dwelling times

If the reference voltage vector is changed as explained in the previous section, the calculation of the dwelling times is same as two-level SVPWM method. Using the method of [2], the dwelling time calculation can be done more efficiently as shown in the following example. In calculating the dwelling time, the only difference between the two-level SVPWM and three-level SVPWM is the factor 2 appearing in the first three lines in the following example.

```
Ta=2.*Vas_ref*Tsamp/V_DC;
Tb=2.*Vbs_ref*Tsamp/ V_DC;
Tc=-(Ta+Tb);

if( Ta>Tb ) { a=Ta;   b=Tb; }
else        { a=Tb;   b=Ta; }
if( Tc>a )  a=Tc;
if( Tc<b )  b=Tc;

T0=Tsamp-(a-b);
a=T0*0.5-b;
Ta+=a;   Tb+=a;   Tc+=a;
if(Flag_on_off)
        Ta=Tsamp-Ta;
        Tb=Tsamp-Tb;
        Tc=Tsamp-Tc; }
```

Once the small hexagon is identified by the location of the reference voltage vector, the selection of the voltage vectors and their switching sequence is done on the basis of the center vector of the small hexagon. For example, if the reference vector is given as in fig. 4, the switching sequence will be (POO)-(PON)-(OON)-(ONN). This means that among the four switches in phase A, only the first and the third switches are enabled to change their states. In cases of phase B and C, only the second and the fourth switches have to be enabled to change their states. The enable signal is produced by the simple digital circuits using the index *s*.

D. Neutral-point potential control

It is well known that there are two methods that control the neutral-point potential of the three-level inverters. The first is changing the switching sequence and the second is rearranging the time distribution of the voltage vectors. These two methods are also used in the proposed SVPWM method. Changing the switching sequence is easily done using the index *s*.

i) Method 1 : changing the switching sequence

If the voltage reference vector stays at region B in fig. 5(a), the neutral-point potential can be controlled by changing the switching sequence. As explained in the preceding sections, the index s can have the value 1 or 2 in this region. In this case as shown in figure 5(a), switching sequence can be given in the order (POO)-(PON)-**(OON)**-(ONN) or (PPO)-**(POO)**-(PON)-(OON). The former sequence is the case when the index s has the value of 1, and the latter is the case when the index *s* has the value of 2. If the former switching sequence is selected and the load current flows out from DC-link capacitors, the load current will discharge the upper capacitor, while charging the lower capacitor of the dc-link. But on the contrary, if the latter switching sequence is selected, the upper capacitor is charged and the lower capacitor is discharged. So if the value of index *s* is changed according to the voltage error and the direction of the power, the neutral-point potential is controlled. This is realized by subtracting or adding 1 to the index **s**. The method, explained in the preceding paragraph is also applied to the region A in fig. 5.

ii) Method 2 : he time distribution of the voltage vectors

If the voltage reference vector stays at the region C as in fig. 5(b), the switching sequence is given as in the following. T_{1P}, T_2, T_3 and T_{1N} are dwelling times of the corresponding vectors.

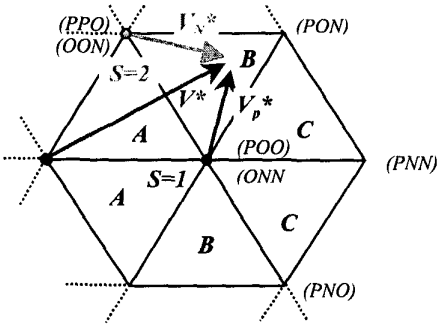
(POO) - (PNO) - (PNN) - (ONN)

T_{1P} - T_2 - T_3 - T_{1N}

In this case, the neutral-point voltage is controlled by adjusting the control factor f in response to the voltage error and to the load condition[3]. As the vector (POO) and (OON) are same in magnitude and in phase, changing the dwelling times of the two vector has no effect on the output voltage vector only if the following equations are satisfied.

$$T_{1n} + T_{1p} = T_1 , \; T_{1n} = T_1*(1+f)/2, \; T_{1p} = T_1*(1-f)/2$$

$$[-1 \le f \le -1]$$



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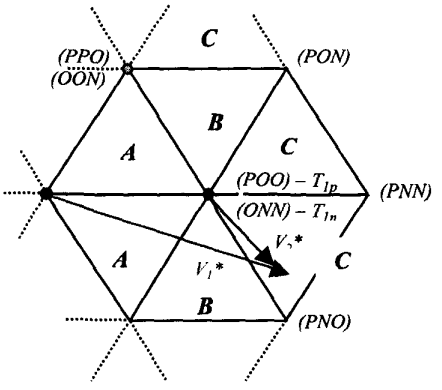


(b)

Fig. 5. Neutral-Point Potential Control

This technique is also used in the region B.

E. Application to the multi-level SVPWM

The proposed SVPWM method can be applied to multi-level SVPWM. For example, the four or five-level space-vector can be simplified to the three-level space vector on the same principles as explained in this paper. This is illustrated in figure 6. If it is simplified to the three-level space vector plane, the SVPWM is done like that of the proposed three-level SVPWM method.

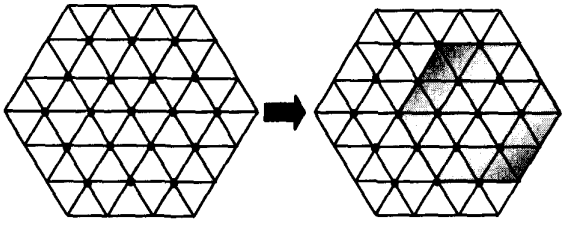


Fig. 6. Application to the multi-level SVPWM

III. SIMULATION AND TEST RESULTS

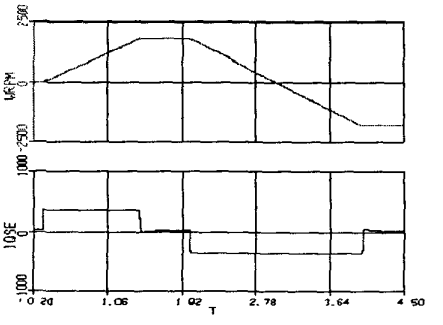
To verify the validity of the proposed SVPWM method, simulation and the experiment are executed. The three-level PWM converter, inverter are used to simulate the proposed SVPWM method. The simulation and test conditions are shown in table III.

Table III

Simulation and test conditions

	Simulation	Test
DC-link Voltage	3800[Vdc]	3700[Vdc]
Inverter Capacity	2,000[kVA]	2000[kVA]
Switching Frequency	500[Hz]	500[Hz]
DC-link Capacitance	6000[uF]	5700[uF]
Converter Type	PWM converter	Diode rectifier

Fig. 7 shows the performance of the three level PWM converter and the vector controlled inverter systems. From the simulation results, we can know that the voltage balancing of the DC link capacitor is controlled fairly well.



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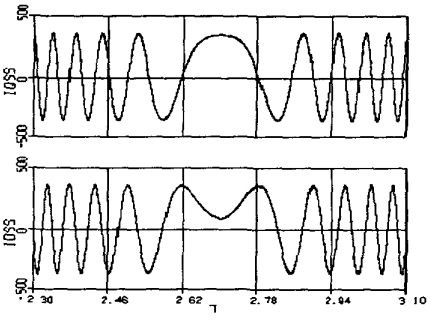

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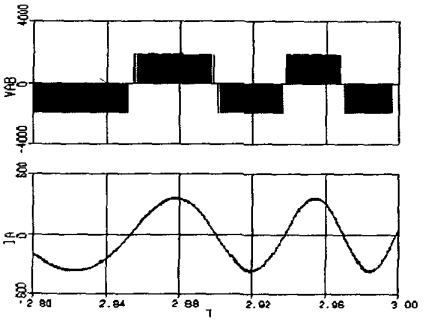

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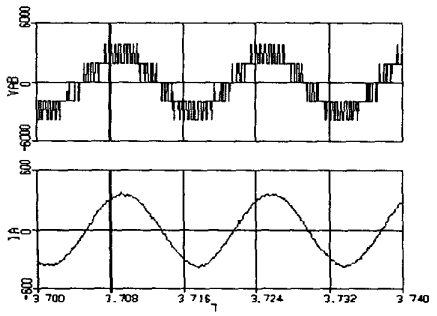

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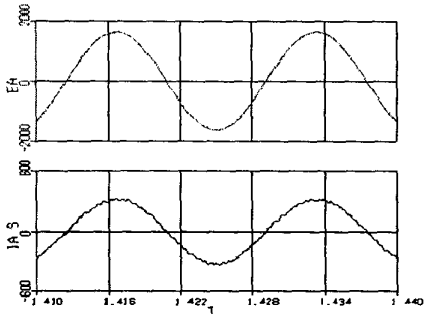

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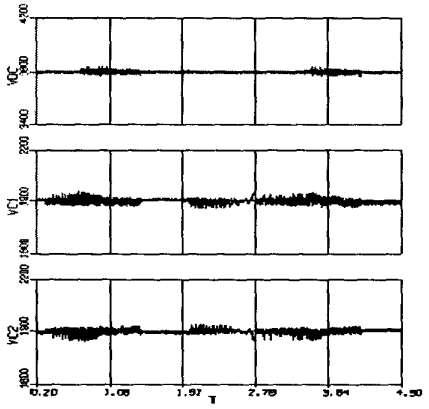


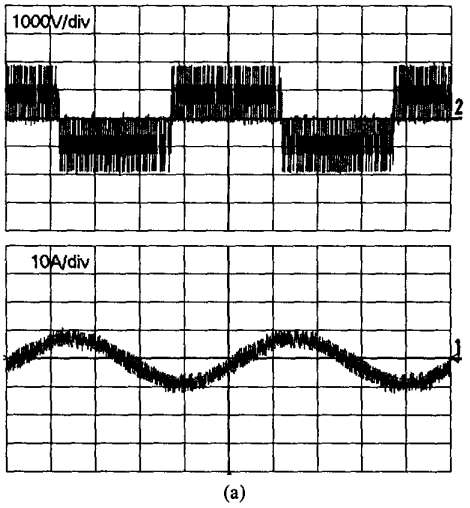
(f)

(a) Wrpm, Iqse (b) Iqss, Idss (c) line-to-line voltage and phase current at low speed regions (d) line-to-line voltage and phase current at high speed region (e) Source voltage and current (f) DC-link capacitor voltage

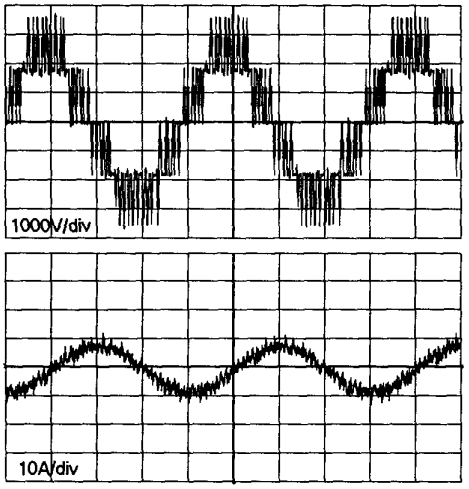
Figure 7. Simulation results of the proposed three-level SVPWM method

The steady state and dynamic performances of the inverter are also verified from the simulation results. Test of the proposed SVPWM method was carried out using diode rectifier and three level IGBT PWM inverter. The 3300V, 100kw squirrel cage induction motor was used as a load of the three-level IGBT PWM inverter. The test results of the developed system are shown in fig.8. From the test results, we can know the neutral-point potential of the three level inverter is controlled well at various motor speeds.

From the results of simulation and experiment, we can know that the proposed space-vector PWM methods is simple in its structure and effective in suppressing the neutral-point potential of dc-link voltage.



(a)



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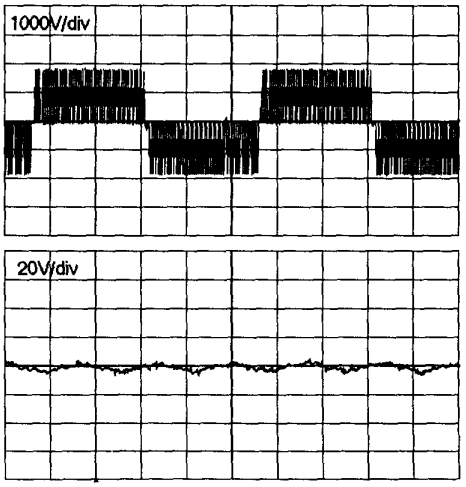

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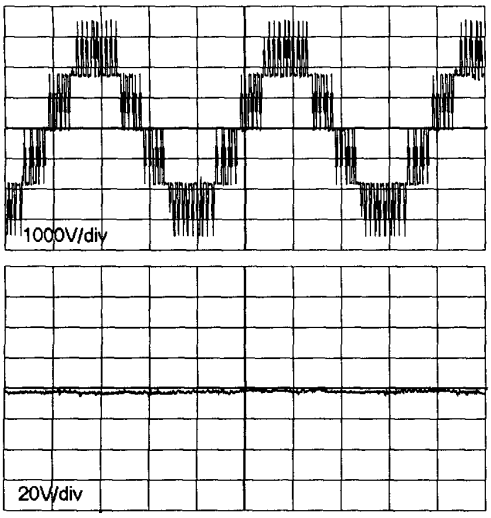

(d)

(a) line-to-line voltage and phase current at f_0=20[hz], time : 10ms/div (b) line-to-line voltage and phase current at f_0=50[hz], time : 5ms/div (c) line-to-line voltage and DC-link voltage error(Vc1-Vc2) at f_0=20[hz], time : 10ms/div (d) line-to-line voltage and DC-link voltage error(Vc1-Vc2) at f_0=20[hz], time : 5ms/div

Fig. 8. Test results of the proposed SVPWM method

IV. CONCLUSION

The more promising field of the three level IGBT voltage source inverter seems to be that of very high power with high DC link voltage. In this paper, a new simplified space-vector PWM method was proposed and described in detail. The proposed SVPWM method has the following features.

i) The selection of the switching sequence is done without look-up table, so the memory of the controller can be saved.

ii) The calculation of the dwelling time of voltage vector is done at the same manner as two-level SVPWM. - Thus it reduces the execution time of the three-level SVPWM.

iii) the neutral-point potential control algorithm is easy to implement.

The validity of the presented SVPWM method is verified by simulation and experiment.

High performance three-level IGBT inverter systems have been developed to drive the high voltage, high power induction motor.

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