Development of a New Voltage Source Inverter (VSI) Average Model Including Low Frequency Harmonics

S. Ahmed[1], D. Boroyevich[1], F. Wang[2], and R. Burgos[3]

[1]Center for Power Electronic Systems (CPES)
The Bradley Department of Electrical and Computer Engineering
Virginia Polytechnic Institute and State University
Blacksburg, VA
sahassan@vt.edu

[2]Oak Ridge National Lab
University of Tennessee
Knoxville,TN
fred.wang@utk.edu

[3]ABB U.S. Corporate Research Center
Raleigh, NC
rbugos@ieee.org

***Abstract*— This paper presents an enhanced average model of a voltage source inverter (VSI) that can accurately predict some of the low frequency phenomena only seen by the switching models. These phenomena include the dead time, voltage drop across switching devices (switch & diode), different modulation and minimum pulse width. Simulation and experimental results with a 2 kW prototype is used for validation purposes. The paper shows the simulation results of both complete switching and proposed average model depicting a great match between the two. The enhanced average model showed very good matching with the switching model, about 2% difference in time domain and also harmonic spectrum analysis.**

I. INTRODUCTION

Analysis of power electronics systems is complicated when using complete switching models. The switching models are detailed accurate models that can predict the actual and transient behavior. However, power electronics systems can have hundreds of power electronics converters and motor drive systems which if presented with detailed component models will result in practical constraints in the size of the simulation system that can be achieved. In addition, it will place constraints on the computing time and will also increase the computer storage [1]. Therefore, the demand for the development of the accurate, time-efficient models becomes very strong.

This paper presents accurate average model of a voltage source inverter (VSI) that can predict some of the phenomena only seen by the switching models. The paper first presents the ideal average model of the VSI model which has been presented in literature and then adds some of the low frequency phenomena that is usually only seen with the switching model in order to reach a more realistic model. From these phenomena are the various types of modulation [2-3], dead time that is inevitable to prevent the shoot-through phenomenon [4-8] analyzing the non-linearities, voltage and current distortion due to that, minimum pulse-width constraint [9-11] and other phenomena due to the inherent characteristics of the switching devices as the voltage drop, and the turn on/off time of the switches. Research concentrated on developing compensation methods for these types of phenomena in a switching model but none actually implemented them in an average model. In this paper, some of the methods developed in the research are used in a reverse way to introduce the low frequency harmonics into the proposed average model to become more realistic as the switching model and then compensate for that. The paper then shows the simulation results of both complete switching and proposed average model depicting a great match between the two. Then finally, it verifies the results experimentally with a prototype that matches the simulation model implemented. The paper also discusses the saving in simulation time introduced by this enhanced average model.

II. PROPOSED VOLTAGE SOURCE INVERTER AVERAGE MODEL

Fig. 1 shows the circuit schematic of the VSI model considered in this paper, comprised of a power stage, controller, modulation and passive elements. The power stage is modeled as an ideal average model with the set of equations (1) in the *abc*-coordinates. However, a diode bridge is added in parallel as shown in Fig. 1 to reveal the converter real phase-leg operation. The controller is in the *dq*-frame.

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} d_a \\ d_b \\ d_c \end{bmatrix} v_{dc} \;\&\; i_{dc} = i_a d_a + i_b d_b + i_c d_c \quad (1)$$

The inverter parameters is as follows, it is a 2 kW prototype implemented in Saber running at about 1kW, the dc link voltage V_{dc}=300 V, the output phase RMS voltage is 60 V_{rms}, phase current is 4 A_{rms} and the load resistor is 15 Ω. Fig. 2 shows some of the simulation results for the ideal VSI average model defined here. It shows the output voltage with an RMS voltage of 59.897 V, RMS current of phase A of 3.9932 A and duty cycle of the three phases respectively.

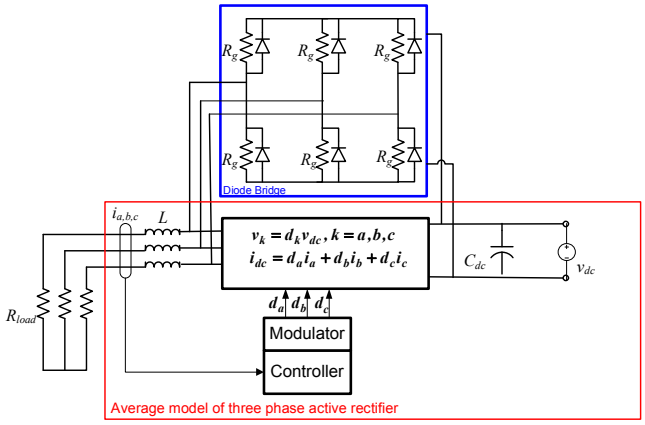


Figure 1 Circuit schematic of VSI topology considered in this paper.

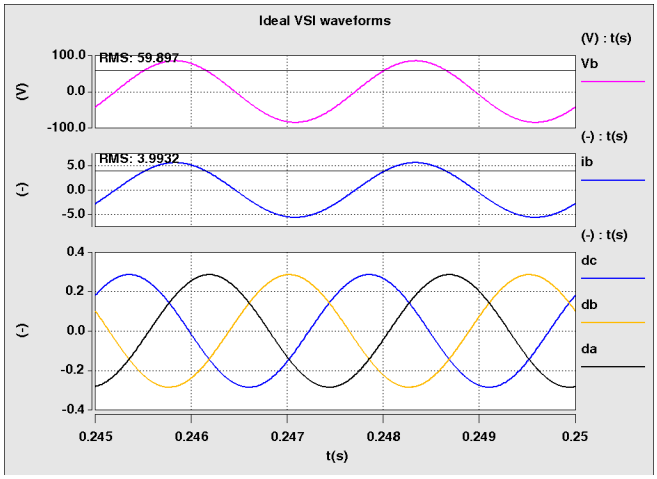


Figure 2 Simulation results for ideal VSI average model proposed.

III. Different Low Frequency Phenomena Modeled

A. Modulation Control Methods

The ideal inverter simulation in the previous section shows pure sinusoidal PWM waveforms where it just represents the fundamental signals with no injected harmonics. The first modification for the model to be more realistic is to include the zero-sequence into the PWM waveforms. This signal depends on the distribution of the zero vector and the type of modulation control used [2]. In [2] a unified representation for the zero-sequence signal $e_i(t)$ is given in (2):

$$e_i = k_o(1-u_{\max}) + (1-k_o)(-1-u_{\min}),\ 0 \le k_o \le 1 \quad (2)$$

and u_i is the fundamental sinusoidal waveforms, u_{min} and u_{max} is the minimum and maximum of the three phases respectively.

For continuous symmetrical PWM (SYPWM), $k_o = 0.5$ and this means the two zero vectors are equally distributed. Fig. 3 shows the modulation signals for one phase, with the injected zero sequence. For discontinuous PWM, there were different ones implemented as the two extremes, the DPWMMAX where the zero vector (111) is used for the six sectors and the DPWMMIN where the zero vector (000) is used in this case for the six vectors. In addition to those two, the 2-phase right aligned (2-Φ RA) SVM presented in Fig. 4 is also implemented.

TABLE I shows the zero-sequence representations and space voltage vectors used for all six sectors to achieve this discontinuous 2-Φ RA. In addition, to the zero sequence injection the model is capable of discrete sampling and for this case it is 20 kHz. The effect of the sampling can be seen in the staircase steps effect on the modulation signal as shown in Fig. 3. Fig 5 compares the continuous and discrete sampling effect on phase A current.

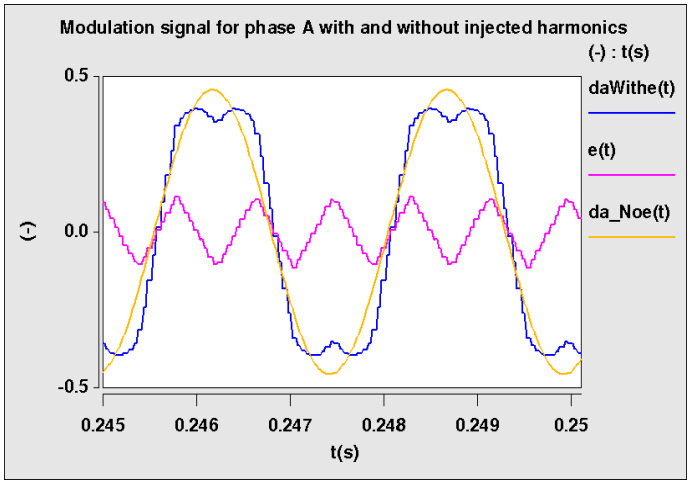


Figure 3 Modulation signals for continuous symmetrical PWM.

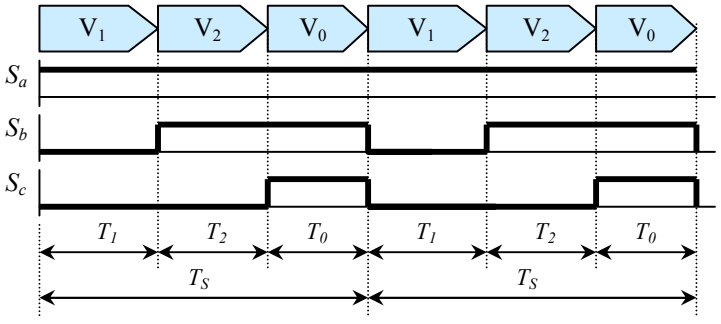


Figure 4 Discontinuous 2-Φ RA modulation in sector 1.

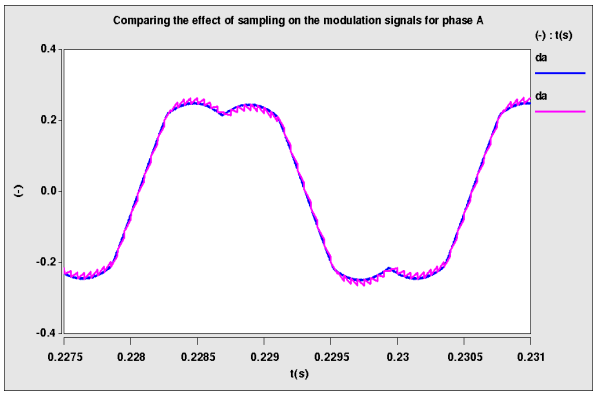


Figure 5 Comparing the phase A duty cycle with continous and discrete sampling of 20kHz.

TABLE I. THE ZERO SEQUENCE CALCULATED FOR EACH SECTOR FOR 2 2-Φ RA MODULATION

Sector NO.	Space voltage vectors	Zero sequence $e_i(t)$
I	T_s=T_1 (100)+T_2 (110)+T_0 (111)	$e_i(t)=\frac{T_0}{Ts}+\frac{1}{3}\frac{T_2}{Ts}-\frac{1}{3}\frac{T_1}{Ts}$
II	T_s=T_1 (110)+T_2 (010)+T_0 (000)	$e_i(t)=\frac{-T_0}{Ts}-\frac{1}{3}\frac{T_2}{Ts}+\frac{1}{3}\frac{T_1}{Ts}$
III	T_s=T_1 (010)+T_2 (011)+T_0 (111)	$e_i(t)=\frac{T_0}{Ts}+\frac{1}{3}\frac{T_2}{Ts}-\frac{1}{3}\frac{T_1}{Ts}$
IV	T_s=T_1 (011)+T_2 (001)+T_0 (000)	$e_i(t)=\frac{-T_0}{Ts}-\frac{1}{3}\frac{T_2}{Ts}+\frac{1}{3}\frac{T_1}{Ts}$
V	T_s=T_1 (001)+T_2 (101)+T_0 (111)	$e_i(t)=\frac{T_0}{Ts}+\frac{1}{3}\frac{T_2}{Ts}-\frac{1}{3}\frac{T_1}{Ts}$
VI	T_s=T_1 (101)+T_2 (100)+T_0 (000)	$e_i(t)=\frac{-T_0}{Ts}-\frac{1}{3}\frac{T_2}{Ts}+\frac{1}{3}\frac{T_1}{Ts}$

B. Dead time and Non-linearities due to Turn On/off and Voltage Drop on Switching Devices

The second important phenomenon implemented is the dead time. The dead time is a blanking time to avoid the so-called shoot-through of the dc link. This time guarantee that both switches in an inverter leg never conduct simultaneously [4]. For switching model, dead time is generated by delaying the switching time as shown in Fig. 6. From Fig. 6, it can be seen that time error in the on time duration resulting from dead time is given by (3).

$$T_{err}=\left[\left(-\frac{T_{off}}{2}+\frac{T_{on}}{2}+T_d\right)\Big/T_s\right]sign\,(i)$$

$$\&\quad sign\,(i)=\begin{bmatrix}1:when\ i>0\\-1:when\ i<0\end{bmatrix} \qquad (3)$$

For the ideal average model, the error time is added to the commanded time duration T_{com} so that the effective time duration T_{eff} is the summation of both as given in (4):

$$T_{eff}=T_{com}+\left[\left(-\frac{T_{off}}{2}+\frac{T_{on}}{2}+T_d\right)\Big/T_s\right]sign\,(i) \qquad (4)$$

In addition to the effect of the dead time and the turn on and off time of the switches, there are some non-linearities caused by the voltage drop across the switch (V_{ce}) & the on voltage of the diode (V_d). This can be realized in the model by adding the error caused by the voltage drop to the error time in (3) giving the new effective duty cycle as in (5):

$$d_{eff}=d_{com}+\left[\left(\left(-\frac{T_{off}}{2}+\frac{T_{on}}{2}+T_d\right)\Big/T_s\right)+d_a(V_{ce}/V_{dc})+(1-d_a)(V_d/V_{dc})\right]sign\,(i) \qquad (5)$$

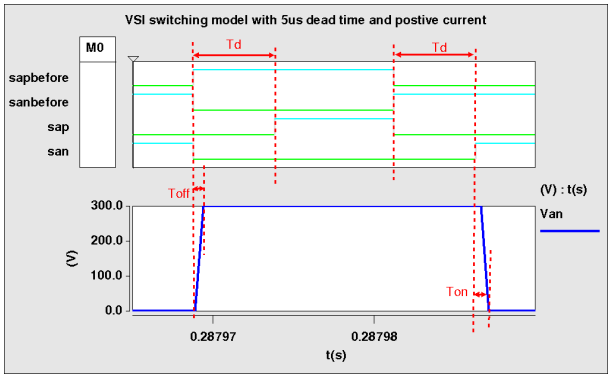
Fig 7 shows the phase A current with and without the effect of a dead time of 5μs.

C. Minimum Pulse-width

Another important source of distortion is the minimum pulse-width (MPW) limitations that result when small on-time duration of the switches can not be achieved. Such limitations may have to be enforced to prevent damage of the semiconductors switches as this MPW can be smaller than the on and off time of the switch [10]. In a switching model, this can be implemented easily by comparing the width of the pulse of the gating signal to the minimum pulse allowed duration and if it is smaller then it gets deleted. However, in the proposed average model, a limit is enforced on the duty cycle achievable. The minimum allowed duty cycle is given in (6) and if the duty cycle is smaller then it is clipped to the minimum one.

$$d_{\min}=(1/T_s)(T_{deadtime}+T_{MPW}) \qquad (6)$$

Fig. 8 depicts the difference between phase A current when the MPW phenomenon is added to the model.



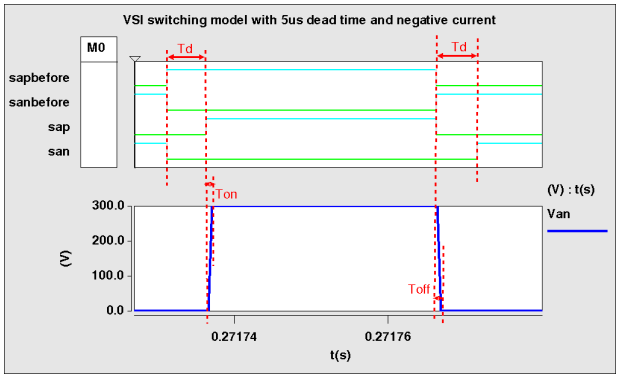


Figure 6 PWM voltage waveforms for positive current (top) and negative current (bottom). From the top for each one: phase A positive gate signal without dead time, negative gate signal without dead time, positive gate signal with dead time, negative gate signal with dead time and line to neutral phase A voltage.

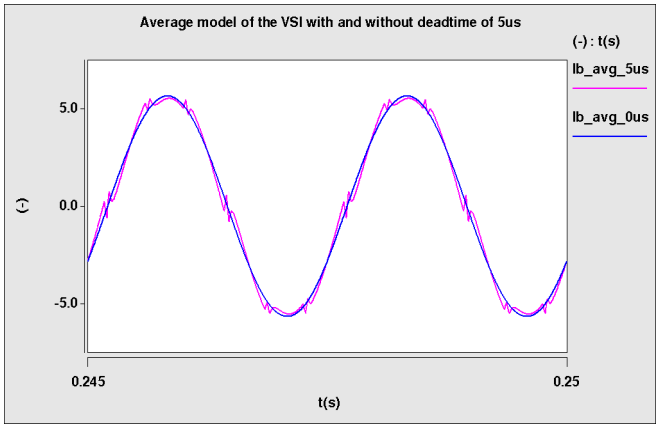


Figure 7 Phase A current for proposed model with and without dead time.

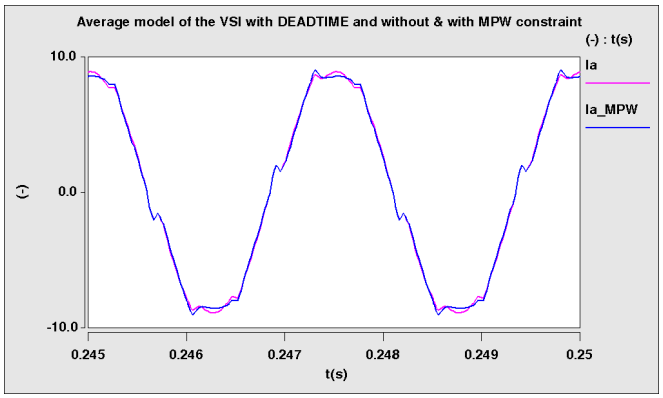


Figure 8 Phase A current with and without minimum pulse width.

IV. Comparing The Perofrmance Of Switching And Average Model

The average model proposed in the previous section with all the different low frequency harmonics phenomena discussed is compared to a switching model with the same exact parameters and the results are compared and shown in Fig. 9 and 10 respectively. Fig. 9 shows the comparison between the real switching and average model when no distortion is enforced. It compares phase B current. Fig. 10 shows the same current with distortion added: 5μs dead time, on and off time of 1μs, voltage drop across the switch of 0.2V, diode on voltage of 0.7V and 1μs minimum pulse width. Fig. 10 compares the average switching current waveform (averaged over one switching cycle) versus the average model current. From looking at the time domain waveform, it can be seen that the two waveforms matches very good. However, a more accurate way of verifying the results is to calculate the deviation percentage between both waveforms. This percentage is calculated using equation (7),

$$Deviation = \frac{1}{X_{RMS}} \sqrt{\frac{1}{N} \sum_{i=1}^{N} \left(x_{i\,swi} - x_{i\,avg} \right)^2} \qquad (7)$$

Using the above equation, each point is subtracted from the corresponding one and the relative error is calculated and normalized using RMS current. The percentage error between the two models is 2.32%.

In addition to comparison above, the models simulation time was compared for a 0.2s window. The ideal average model with no distortion has the least simulation time (1.7s) followed by the new enhanced average model with distortion (2.38min) and finally the switching model almost 4 times more than the enhanced average model time (8.1s). So although there is a penalty paid when using the enhanced average models on the simulation time, the benefit of low frequency modeling is more significant than the time in this case. This is because the enhanced average model still has much lower simulation time than the switching model almost halved and could predict well the performance as shown.

V. EXPERIMENTAL SETUP & RESULTS VERIFICATION

A. Setup

A 2 kW prototype experiment is conducted to verify the performance of the new developed model. Fig. 11 shows the construction. A 6-pack IGBT IPMs from Fuji (6MBP20RH060) (600V, 20A) is used. The output inductance per phase is 600μH. The control board is DSP-FPGA digital controller.

B. Verification

To validate the new average model, the model was compared to the real experimental model with exact the same parameters as mentioned above. The validation tests are divided into three sets, power quality verification, impedance measurement and EMI verification. However, this section will concentrate on the first one and the later two are beyond the scope of this paper. The power quality verification will include normal steady state verification where the ac output current waveforms are measured and compared versus the average simulation model as done in the previous section. The error percentage is again calculated the same way using equation (7) where now the waveforms compared is the averaged experimental versus the new developed average model. The second part of the power quality verification is the frequency characteristics. This part will include comparison between individual harmonics and the total percentage error is also calculated.

Fig. 12 compares both the experimental phase B current averaged over one cycle with the average simulation model current. The percentage error is given as 8.74% calculated with equation (7).

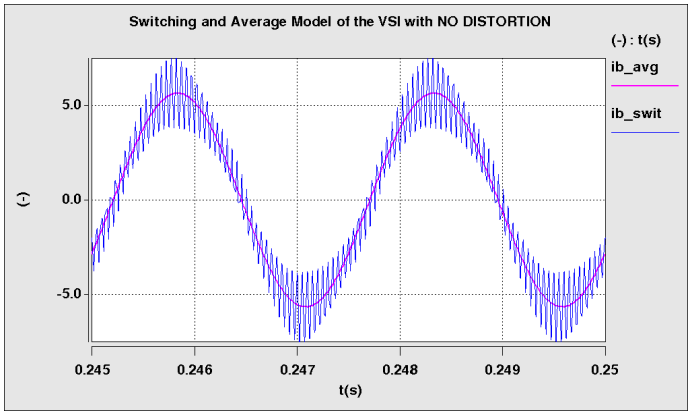


Figure 9 Average and switching model comparison without distortion.

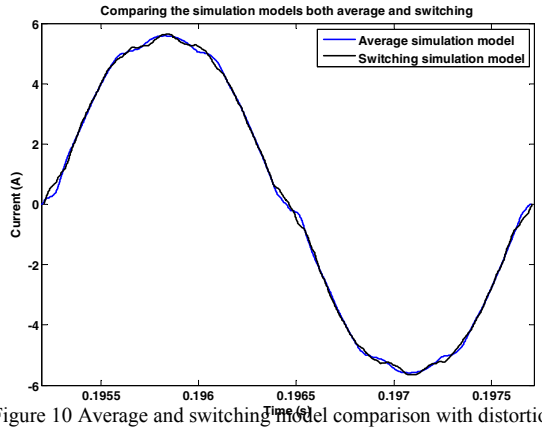


Figure 10 Average and switching model comparison with distortion.

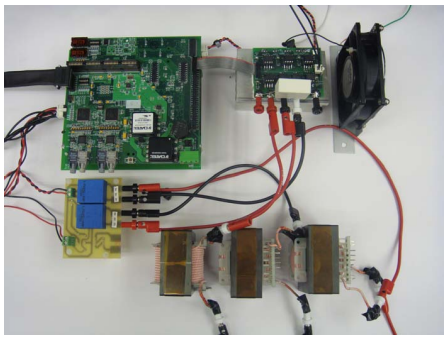


Figure 11 Experimental setup.

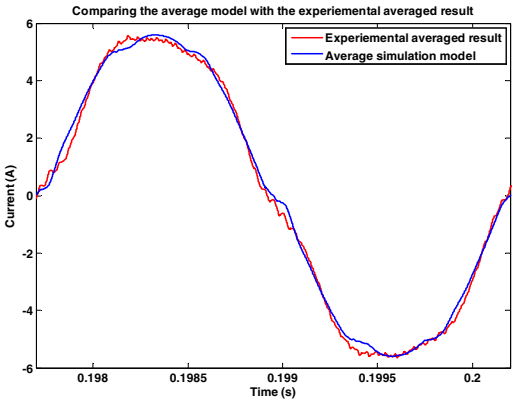


Figure 12 Average and switching model comparison with distortion.

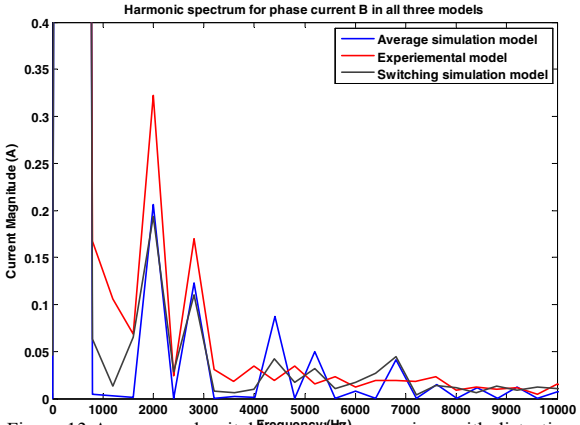


Figure 13 Average and switching model comparison with distortion.

Fig. 13 compares the harmonic spectrum of phase B current for the three models (real switching model, enhanced average model and experimental prototype). The fundamental harmonic is about 5.72A (magnitude) and the figure zooms on the sub harmonics that are high enough to be investigated, therefore, it concentrates from the 5th harmonic till half the switching frequency (10kHz) which is around the 23rd harmonic. It can be seen that the simulation models (average and switching) matches very well in most points while the experimental is little higher. Calculating the percentage of deviation or error using equation (7) and over the region given in Fig 13, it is found to be 0.82% between the experimental prototype and the enhanced average model and 1.85% between the real switching simulation model and the average model.

VI. CONCLUSIONS

This paper has presented a new average model for Voltage Source Inverter (VSI) model. This average model can capture low frequency harmonics that are usually phenomena modeled only with switching models. The paper discussed the process of implementing these different phenomena and compared the results of the proposed average model to a complete switching model. Experimental results obtained with a 2 kW Voltage Source Inverter prototype verified the proposed average model.

ACKNOWLEDGMENT

This work was conducted under the CPES project "Stability of AC Power Systems-Phase II" sponsored by The Boeing Company.

This work made use of Engineering Research Center Shared Facilities supported by the National Science Foundation under NSF Award Number EEC-9731677.

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