Average Modeling and Control Design for VIENNA-Type Rectifiers Considering the DC-Link Voltage Balance

Rixin Lai, *Student Member, IEEE*, Fei (Fred) Wang, *Senior Member, IEEE*, Rolando Burgos, *Member, IEEE*, Dushan Boroyevich, *Fellow, IEEE*, Dong Jiang, and Di Zhang, *Student Member, IEEE*

***Abstract*—This paper presents a new average d–q model and a control approach with a carrier-based pulsewidth modulation (PWM) implementation for nonregenerative three-phase three-level boost (VIENNA-type) rectifiers. State-space analysis and an averaging technique are used to derive the relationship between the controlled duty cycle and the dc-link neutral-point voltage, based on which an optimal zero-sequence component is found for dc-link voltage balance. By utilizing this zero-sequence component, the behavior of the dc-link voltage unbalance can be modeled in d–q coordinates using averaging over a switching cycle. Therefore, the proposed model is valid for up to half of the switching frequency. With the proposed model, a new control algorithm is developed with carrier-based PWM implementation, which features great simplicity and good dc-link neutral-point regulation. Space vector representation is also utilized to analyze the voltage balancing mechanism and the region of feasible operation. Simulation and experimental results validated the proposed model and control approach.**

***Index Terms*—Average d–q model, carrier-based pulsewidth modulation (PWM), operation region, space vector, VIENNA-type rectifier.**

I. Introduction

THE FAMILY of nonregenerative three-level boost rectifier is characterized by reduced number of active switching devices, high input power factor, and low device voltage stress, which make it a suitable topology for medium- and high-power applications with high power density [1]–[8]. Within this family, there are various circuit topologies proposed by different authors. Since VIENNA rectifier is among the earliest of this converter-type with good recognition [1], the term "VIENNA-type rectifier" is used to represent the whole nonregenerative three-level boost rectifier family, in this paper.

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The control of the VIENNA-type rectifier is relatively complex because of its three-level structure and dc-link neutral-point voltage regulation requirement. In the past several years, there has been a lot of research done on this aspect, including average model derivation and control scheme development [9]–[20]. Generally speaking, all rectifier models are based on the synchronous d–q frame representation. However, due to the intrinsic time-varying nature of the dc-link neutral-point current [3], it is difficult to directly obtain the equilibrium point with conventional d–q coordinate transformation. For this reason, a low-frequency state model [9]–[12] has been built by averaging the dc-link neutral-point operation in a complete ac-line cycle. Burgos *et al.* [13] present an average model for full frequency range by using equivalent switching functions. The approach provides a useful tool for system analysis and characterization, but is still difficult to implement in control design due to the complexity of the model and the coupling between the switching functions.

Several methods have been proposed for the control design of the VIENNA-type rectifier. Hysteresis current control [14] is simple to implement, as the switch-gating signals are generated by comparing the reference and measured currents. Hysteresis current control has the drawback of a varying switching frequency. Backman and Rojas [15] proposed a simple carrier-based control approach and discussed the inherent relationship between the space-vector modulation (SVM) and the carrier-based pulsewidth modulation (PWM), without a clear presentation on the zero-sequence component generation for the carrier-based implementation. Constant-frequency integration control [16] and unity power factor control [17] feature both simplicity and constant switching frequency, but they do not provide closed-loop regulation for the dc-link neutral-point voltage. Consequently, in order to limit the voltage unbalance of the dc link, bigger dc-link capacitors are needed. The three-level space-vector-based control scheme [18]–[20] provides a clear insight into system control and operation, as the redundant vectors can be utilized to regulate the neutral-point voltage. However, a large calculation effort is required for the implementation, which has limited its application for high–switching applications. In addition, a detailed control loop design methodology for voltage balance is absent in the existent control approaches due to the limited frequency range of the available models.

Section II of this paper proposes a new average d–q model for the VIENNA-type rectifier with an extended frequency range. This model is based on the state-space analysis and the concept

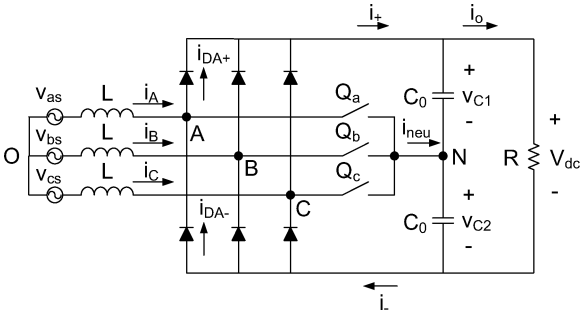

Fig. 1. Rectifier topology.

of optimal neutral-point current injection. First the state-space model for the system is built, and the relationship between the controlled duty cycle and the voltage unbalance is established through a differential equation. Based on this relationship, an optimal zero-sequence component for the duty cycle is found to achieve zero current injection to the dc-link neutral point, which indicates an equilibrium point of the dc-link voltage balance. By utilizing this optimal zero-sequence component into the duty cycle, the average model for neutral-point operation can be greatly simplified and represented in the d–q frame. A simple mathematical relationship between the voltage unbalance and the controlled zero-sequence component can be obtained, and therefore, the neutral-point voltage control loop can be easily designed.

Section III presents a new control algorithm based on the proposed average model. The voltage balance control is designed with the combination of a feed-forward component and a feedback loop, which can be easily incorporated into the conventional multiloop d–q controller for a two-level converter, and then implemented by carrier-based modulation. Compared to the previous methods, the new control approach features great simplicity and good dc-link voltage regulation. In Section IV, the voltage balance mechanism of the proposed approach is analyzed by space vector representation. The analysis shows that the proposed approach and the space-vector-based control approach are mathematically the same in terms of keeping the neutral point balance. Section IV contains an investigation of the feasible operating region with the proposed zero-sequence component, and the limits of the modulation index are found. In Section V, a field-programmable gate array-digital signal processor (FPGA-DSP)-controlled rectifier prototype is introduced, and the proposed model and control approach are verified by simulation and experiment.

II. Proposed Average Model

Without loss of generality, the circuit topology of the VIENNA-type rectifier is shown in Fig. 1. It consists of six diodes and three bidirectional switching units Q_a, Q_b, and Q_c. The three active switching units are controlled to ensure sinusoidal ac current and steady dc-link voltage. Since this type of rectifier is current force commutated, the rectifier pole voltage (V_{AN}, V_{BN}, V_{CN}) is determined by not only the controlled switch state but also the polarity of the ac phase current at the corresponding instance. For example, if the switch Q_a is off and the phase current i_A is positive, the phase leg A is clamped to the positive dc link, and therefore, V_{AN} is equal to $V_{\rm dc}/2$. Similarly, if Q_a is off and i_A is negative, then V_{AN} will be $-V_{\rm dc}/2$. If the Q_a is on, phase leg A will be clamped to the dc-link neutral point and V_{AN} will be zero, regardless of i_A polarity. The same operation principle applies to phase B and phase C. Based on this understanding, state-space representation can be obtained, and then used to analyze the system operation. For the input stage, the state-space equations are given by (1), where V_{NO} is the voltage across the neutral point of the dc-link and the neutral point of the three-phase input voltage, and L is the input inductance. V_{as}, V_{bs}, and V_{cs} are the input source voltages, which are given by (2) with V_m being the amplitude of the phase voltage

$$\begin{cases} V_{as} &= L\dfrac{di_A}{dt} + V_{AN} + V_{NO} \\ V_{bs} &= L\dfrac{di_B}{dt} + V_{BN} + V_{NO} \\ V_{cs} &= L\dfrac{di_C}{dt} + V_{CN} + V_{NO} \end{cases} \tag{1}$$

$$\begin{cases} V_{as} &= V_m\cos(\omega_0 t) \\ V_{bs} &= V_m\cos(\omega_0 t - 120^\circ) \\ V_{cs} &= V_m\cos(\omega_0 t + 120^\circ). \end{cases} \tag{2}$$

As mentioned above, the switch voltages V_{AN}, V_{BN}, and V_{CN} are determined by both the switching pattern and the current polarity, which, after some algebraic transformation, can be obtained by (3), where $V_{\rm dc} = v_{C1} + v_{C2}$, $\Delta v = v_{C1} - v_{C2}$, sgn is the signum function, and S_a, S_b, and S_c are the switching function defined as (4)

$$\begin{cases} V_{AN} = \dfrac{V_{\rm dc}}{2}\left[\mathrm{sgn}(i_A) + \dfrac{\Delta v}{v_{\rm dc}}\right](1 - S_a) \\ V_{BN} = \dfrac{V_{\rm dc}}{2}\left[\mathrm{sgn}(i_B) + \dfrac{\Delta v}{v_{\rm dc}}\right](1 - S_b) \\ V_{CN} = \dfrac{V_{\rm dc}}{2}\left[\mathrm{sgn}(i_C) + \dfrac{\Delta v}{v_{\rm dc}}\right](1 - S_c) \end{cases} \tag{3}$$

$$S_{a,b,c} = \begin{cases} 0, & \text{if } \mathrm{Q_{a,b,c}} \text{ is turned off} \\ 1, & \text{if } \mathrm{Q_{a,b,c}} \text{ is turned on.} \end{cases} \tag{4}$$

Normally Δv is much smaller than $V_{\rm dc}$, and therefore, the $\Delta v/V_{\rm dc}$ component in (3) can be ignored, which leads to

$$\begin{cases} V_{AN} &= \dfrac{V_{\rm dc}}{2\,\mathrm{sgn}}(i_A)(1 - S_a) \\ V_{BN} &= \dfrac{V_{\rm dc}}{2\,\mathrm{sgn}}(i_B)(1 - S_b) \\ V_{CN} &= \dfrac{V_{\rm dc}}{2\,\mathrm{sgn}}(i_C)(1 - S_c). \end{cases} \tag{5}$$

The phase leg average duty cycle is defined as

$$d_{a,b,c} = (1 - K_{a,b,c})\mathrm{sgn}(i_{A,B,C}) = d'_{a,b,c} + d_0 \tag{6}$$

where $K_{a,b,c}$ represents the average switch on-time for Q_a, Q_b, and Q_c in one switching cycle, respectively; and $d'_{a,b,c}$ and d_0 are

the sinusoidal components and the zero-sequence component, respectively.

In addition, for the three-phase three-wire system it follows that

$$i_A + i_B + i_C = 0. \tag{7}$$

Substituting (4)–(7) into (1), we can achieve the state-space average model for the VIENNA-type rectifier ac input stage, which is given by

$$\begin{cases} V_{as} &= L\dfrac{di_A}{dt} + \dfrac{V_{\rm dc}}{2}d'_a \\ V_{bs} &= L\dfrac{di_B}{dt} + \dfrac{V_{\rm dc}}{2}d'_b \\ V_{cs} &= L\dfrac{di_C}{dt} + \dfrac{V_{\rm dc}}{2}d'_c. \end{cases} \tag{8}$$

Equation (8) shows the same expression as the conventional two-level voltage source rectifier, since the impact of the voltage unbalance on the ac input stage is ignored in (5). With Park's transformation, the equivalent d–q representation of (8) is given by

$$\begin{cases} V_{sd} &= L\dfrac{di_d}{dt} - \omega_0 L i_q + \dfrac{V_{\rm dc}}{2}d'_d \\ V_{sq} &= L\dfrac{di_q}{dt} + \omega_0 L i_d + \dfrac{V_{\rm dc}}{2}d'_q. \end{cases} \tag{9}$$

For the dc output stage, the state-space model is given by

$$\begin{cases} C_0\dfrac{dv_{C1}}{dt} &= i_+ - \dfrac{V_{\rm dc}}{R} \\ C_0\dfrac{dv_{C2}}{dt} &= i_- - \dfrac{V_{\rm dc}}{R} \end{cases} \tag{10}$$

where i_+ and i_- are the currents through the positive dc bus and the negative dc bus, respectively. According to Kirchhoff's current law, i_+ and i_- are given by (11), where $i_{D(A,B,C)+}$ and $i_{D(A,B,C)-}$ are the currents through the top and bottom diodes for difference phases

$$\begin{cases} i_+ &= i_{DA+} + i_{DB+} + i_{DC+} \\ i_- &= i_{DA-} + i_{DB-} + i_{DC-}. \end{cases} \tag{11}$$

Due to the force commutation characteristics of the VIENNA-type rectifier, the current through the diode can be obtained as (12) and (13)

$$i_{D(A,B,C)+} = \begin{cases} (1 - K_{a,b,c})i_{A,B,C} & (i_{A,B,C} \geq 0) \\ 0 & (i_{A,B,C} < 0) \end{cases} \tag{12}$$

$$i_{D(A,B,C)-} = \begin{cases} 0 & (i_{A,B,C} \geq 0) \\ -(1 - K_{a,b,c})i_{A,B,C} & (i_{A,B,C} < 0). \end{cases} \tag{13}$$

Subtracting (12) from (13) leads to

$$i_{D(A,B,C)-} - i_{D(A,B,C)+} = -(1 - K_{a,b,c})i_{A,B,C}. \tag{14}$$

Considering the duty cycle definition in (6), the sum of (12) and (13) leads to (15)

$$i_{D(A,B,C)+} + i_{D(A,B,C)-} = d_{a,b,c}i_{A,B,C}. \tag{15}$$

With (7), (11), (14), and (15), the relationships between the average dc link current and the ac input current are given by

$$i_+ + i_- = d_a i_A + d_b i_B + d_c i_C \tag{16}$$

$$i_{\rm neu} = i_- - i_+ = K_a i_A + K_b i_B + K_c i_C. \tag{17}$$

After substituting (6), (16), and (17) into (10) and performing some algebraic manipulation, the state-space average model for the dc output stage can be given by

$$C_0\frac{dV_{\rm dc}}{dt} = d'_a i_a + d'_b i_b + d'_c i_c - 2\frac{V_{\rm dc}}{R} = d'_d i_d + d'_q i_q - 2\frac{V_{\rm dc}}{R} \tag{18}$$

$$\begin{aligned} C_0\frac{d\Delta v}{dt} &= -i_{\rm neu} \\ &= |i_A|\,d'_a + |i_B|\,d'_b + |i_C|\,d'_c + d_0(|i_A| + |i_B| + |i_C|). \end{aligned} \tag{19}$$

In order to maintain the dc-link voltage balance, the neutral-point injection current $i_{\rm neu}$ should always be zero within the pulse interval. Therefore, from the voltage balance standpoint, the optimal zero-sequence component is given by

$$d'_0 = -\frac{|i_a|\,d'_a + |i_b|\,d'_b + |i_c|\,d'_c}{|i_a| + |i_b| + |i_c|}. \tag{20}$$

Assuming

$$d_0 = d'_0 + \Delta d_0 \tag{21}$$

then (19) can be simplified as

$$C_0\frac{d\Delta v}{dt} = 2\Delta d_0\frac{|i_A| + |i_B| + |i_C|}{2}. \tag{22}$$

Actually $|i_A| + |i_B| + |i_C|\,/2$ is equal to the absolute value of the maximum instantaneous ac input current. For unity power factor case, the instantaneous input current is given by (23) with voltages given in (2), where I_M is the amplitude of the phase current

$$\begin{cases} i_A = I_M\cos(\omega_0 t) \\ i_B = I_M\cos(\omega_0 t - 120^\circ) \\ i_C = I_M\cos(\omega_0 t + 120^\circ). \end{cases} \tag{23}$$

Then the dc component of $|i_A| + |i_B| + |i_C|\,/2$ can be achieved by

$$\frac{6}{T}\int_{-\frac{T}{12}}^{\frac{T}{12}} I_M\cos(\omega_0 t)dt = \frac{3}{\pi}I_M. \tag{24}$$

Neglecting all the harmonic components, then (22) can be further simplified as (25) for unity power factor case

$$C_0\frac{d\Delta v}{dt} \approx \frac{6}{\pi}I_M\Delta d_0 = \frac{2\sqrt{6}}{\pi}i_d\Delta d_0. \tag{25}$$

Equation (25) establishes a simple relationship between the controlled zero-sequence component Δd_0 and the dc-link voltage unbalance Δv. Based on (9), (18) and (25), the corresponding equivalent circuit model is in Fig. 2. Since the model is

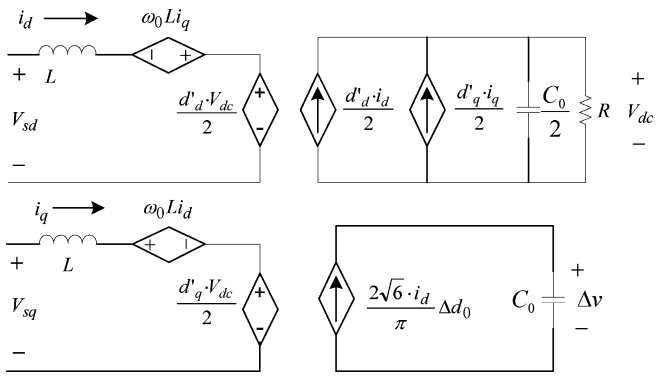

Fig. 2. State-space average model.

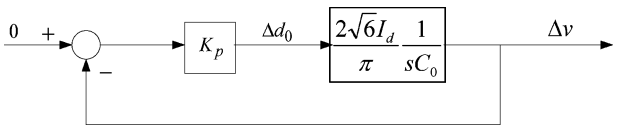

Fig. 3. Neutral-point voltage control block diagram.

averaged over one switching cycle, it is valid for up to half of the switching frequency. Therefore, the neutral-point voltage loop can be designed with higher bandwidth than used in previous work [9]–[12]. As shown in Fig. 2, the behavior of the dc-link unbalance is a simple first-order system, based on which the neutral-point voltage controller can be easily designed under a given operating point. Fig. 3 shows the control loop structure. A simple proportional compensator is utilized for feedback regulation. K_p is the proportional gain, which is given by

$$K_p = \frac{\pi \omega_n C_0}{2\sqrt{6} I_d} \tag{26}$$

where I_d is the steady-state d channel current and ω_n is the required control bandwidth. With (26), the loop gain for the neutral-point voltage regulation is obtained as

$$G(s) = \frac{\omega_n}{s}. \tag{27}$$

As can be seen in the derivation, the proposed d–q model is built on the equilibrium point where the dc-link voltage is balanced. Equation (20) indicates the condition to achieve the balanced operating point. Although the optimal zero-sequence component d'_0 is not shown in the model, its implementation is the basis for making the proposed model valid.

III. Carrier-Based Controller

The multiloop controller in the synchronous reference frame (d–q frame) [21], [22], and [25] is commonly used to control three-phase boost rectifiers with either two-level or three-level topologies. The basic structure of the multiloop controller is shown in Fig. 4. Typically, the outer loop is designed for dc-link voltage regulation and the inner loop is used to control the ac input current. The dc-link voltage error is fed to a proportional and integral (PI) regulator, and the output of the PI regulator is fed to the inner current loop as the d-channel current reference.

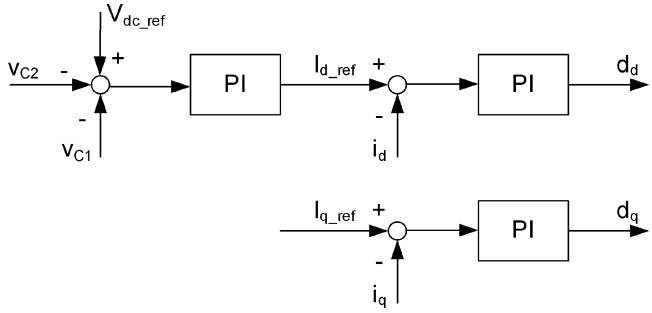

Fig. 4. Multiloop controller for two-level topologies.

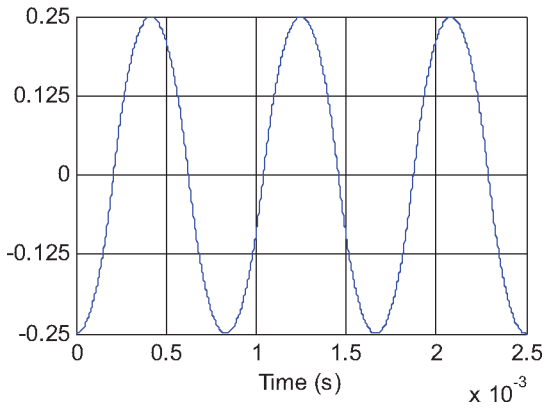

Fig. 5. Time-domain waveform of d'_0 ($M = 1, \omega_0 = 400\,\text{Hz}$).

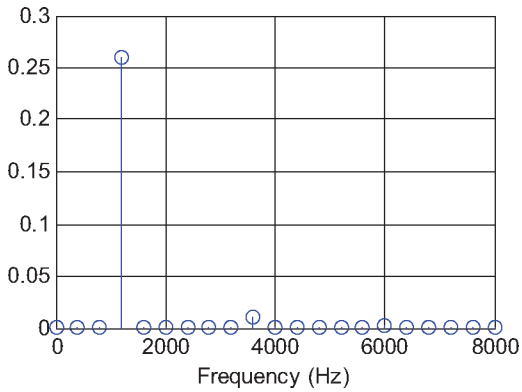

Fig. 6. Spectrum of d'_0 ($M = 1, \omega_0 = 400\,\text{Hz}$).

For the unity power factor case, the q-channel current reference is set to be 0. The required duty cycle can then be achieved by regulating the current error with another PI regulator. For the three-level neutral point clamping topology, an additional dc voltage balance control loop is required. Since the reference voltage is in the d–q frame, SVM is often used for implementation, which is complicated, especially for the VIENNA-type rectifier.

In Section II, the zero-sequence component is carefully studied when deriving the average model. There are opportunities to achieve the phase leg duty cycle without using a space vector modulator. The key point is to find the zero-sequence component d'_0 defined in (20). Neglecting the voltage drop across the inductor L, based on (2) and (8), the sinusoidal duty cycles can

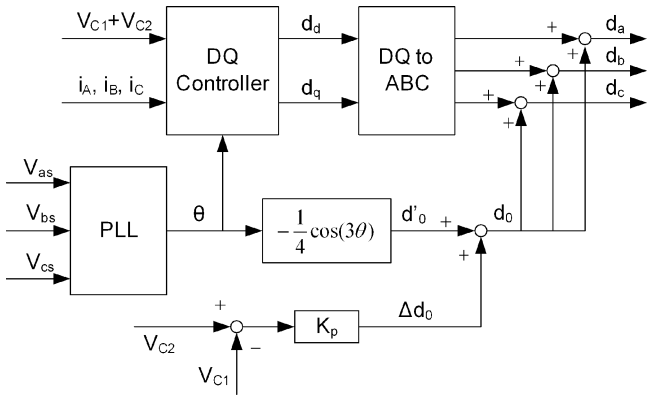

Fig. 7. Control scheme block diagram.

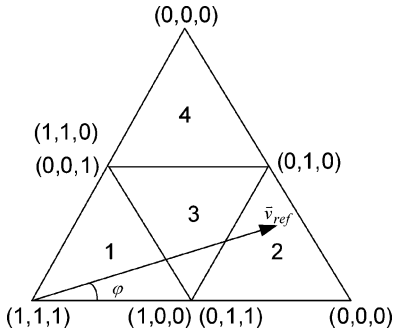

Fig. 8. Space vector diagram at 60°.

TABLE I
PARAMETERS USED IN SIMULATION

Source voltage	60 V_{rms}
Source frequency	400 Hz
Dc link voltage	180 V
Switching frequency	40 kHz
Input inductance L	160 μH
Dc link capacitor C_0	40 μF
Load resistance R	50 Ω

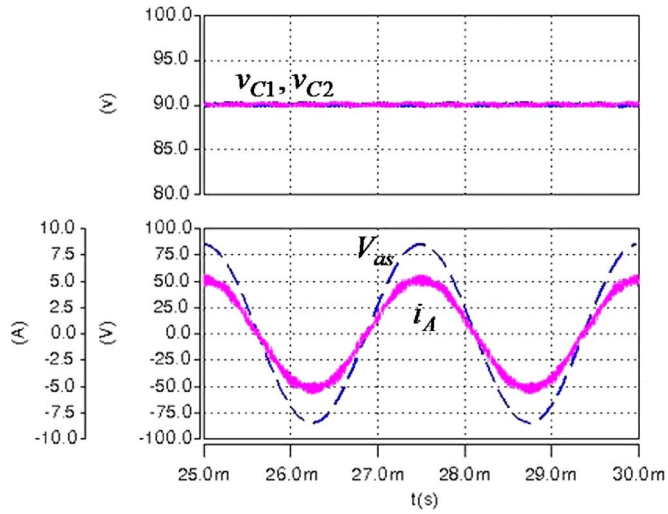

Fig. 9. Steady-state simulation results.

be given by

$$\begin{cases} d'_a = M\cos(\omega_0 t) \\ d'_b = M\cos(\omega_0 t - 120^\circ) \\ d'_c = M\cos(\omega_0 t + 120^\circ) \end{cases} \tag{28}$$

where M is the modulation index defined as the peak phase voltage over half of the dc-link voltage, and ω_0 is the frequency of the source voltage. By substituting (23) and (28) into (20), the optimal zero-sequence component can be given in (29) shown at the bottom of the page.

Figs. 5 and 6 show the time-domain waveform and the spectrum analysis of (29) when the modulation index is 1 with 400 Hz fundamental frequency. The results indicate that the optimal zero-sequence component can be approximated by

$$d'_0 \approx -\frac{M}{4}\cos(3\omega_0 t). \tag{30}$$

Based on the previous analysis, a new controller is proposed, as shown in Fig. 7. The basic idea of this controller is to implement the SVM scheme in a carrier-based way with the optimal zero sequence developed in this paper, which can guarantee zero current injection to the neutral point. In Fig. 7, the *DQ* controller represents the standard multiloop control for a two-level boost rectifier in d–q reference frame, as shown in Fig. 4. However, in this case, instead of using the complicated three-level space vector modulator, d_d and d_q are directly converted into *abc*-coordinates d_a, d_b, and d_c through the inverse Park's transformation. The dc-link neutral point voltage balance is regulated by the zero-sequence component d_0, which consists of two parts: a feed-forward component d'_0 and a feedback component Δd_0, where d'_0 is the optimal zero-sequence component given by (30). In real system, the ac-input voltage and the circuit parameters are not perfectly symmetrical. And delays exist in the digital controller. Therefore, the feed-forward component in the proposed scheme cannot guarantee zero current injection into the neutral point. The feedback component Δd_0 is used to compensate the nonidealities in the real system. The control calculations are significantly reduced when compared to the space-vector-based control scheme, and the neutral-point voltage is effectively regulated by the zero-sequence component.

As can be seen in Section II, the proposed model is developed based on balanced load condition. The proportional (P) regulator for the voltage balance control will perform well since the required neutral point injection is zero for this case. For the

$$d'_0 = -M\frac{|\cos(\omega_0 t)|\cos(\omega_0 t) + |\cos(\omega_0 t - 120^\circ)|\cos(\omega_0 t - 120^\circ) + |\cos(\omega_0 t + 120^\circ)|\cos(\omega_0 t + 120^\circ)}{|\cos(\omega_0 t)| + |\cos(\omega_0 t - 120^\circ)| + |\cos(\omega_0 t + 120^\circ)|}. \tag{29}$$

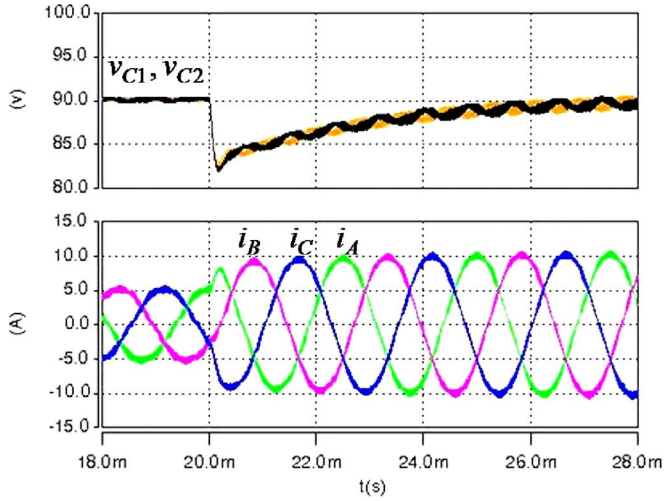

Fig. 10. Simulation results of load step-up transient.

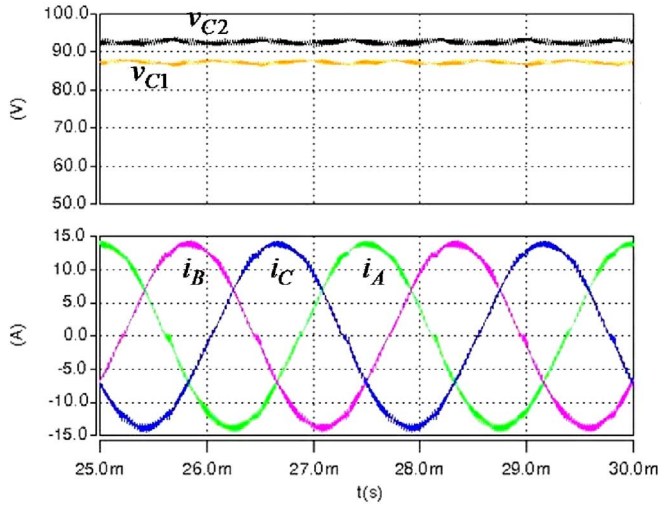

Fig. 12. Voltage unbalance with P regulator under unbalanced load condition.

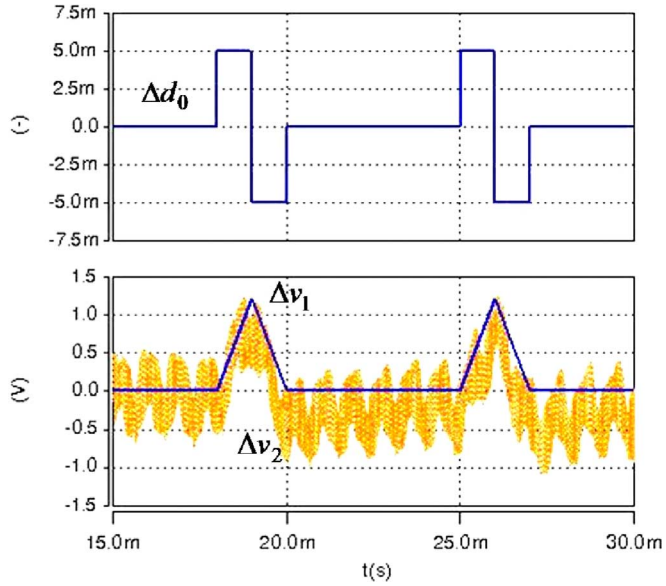

Fig. 11. Voltage unbalance behavior under pulsating Δd_0.

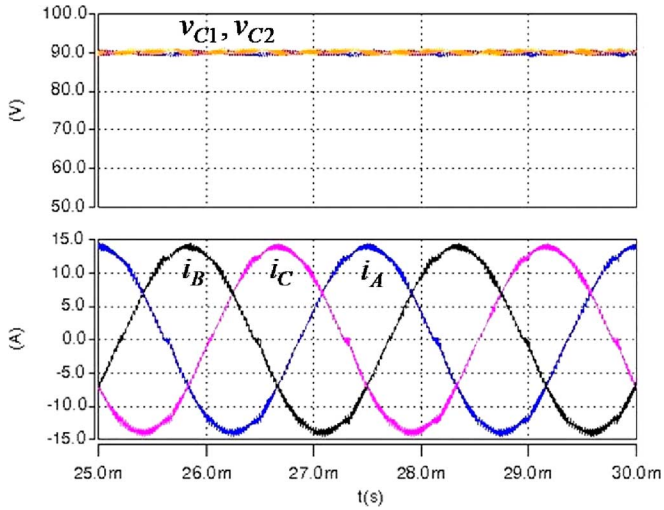

Fig. 13. Voltage unbalance with PI regulator under unbalanced load condition.

unbalanced load condition, a constant injection current is required for the neutral point in order to keep the voltage balance. That results in a constant voltage difference if only using a P regulator. For the unbalanced load case, a PI regulator will help to improve the control performance.

IV. Space Vector Analysis

Space vector analysis is carried out in this section to investigate the mechanism of the voltage balance. Then, the proposed control approach is compared with the space-vector-based approach. The feasible operating region while considering dc-link voltage balance is also studied.

According to the symmetry of space vectors, only 60° needs to be considered, as shown in Fig. 8. In the figure, 1 and 0 represent the on and off states of the corresponding switch, respectively; and φ is the angle between vector (0,0,0) and the reference voltage vector. In subsector 1, if φ is smaller than 30°, (1,0,0), and (0,1,1) point to the same vector. If φ is larger than 30°, (1,1,0), and (0,0,1) point to the same vector. Although these redundant vectors have the same voltage representation in the $\alpha-\beta$ plane, they can lead to thoroughly different current injections into the neutral point. For instance, in the first 30° region, (1,0,0) indicates the dc-link neutral point injecting current to be i_A, while (0,1,1) leads to $-i_A$. In the second 30° region, (0,0,1), and (1,1,0) indicate the current injection of i_C and $-i_C$, respectively. Assuming the ac line current is in phase with the reference voltage, the redundant vectors are always charging or discharging the dc link neutral point with the maximum line current. Therefore, the combination of these redundant vectors can be used to balance the neutral-point voltage as an extra control variable in the space-vector-based approach [18].

For example, if the reference voltage vector lies in subsector 2, the corresponding relative dwell times for the vectors are given by [19], where M is the modulation index and φ is defined in

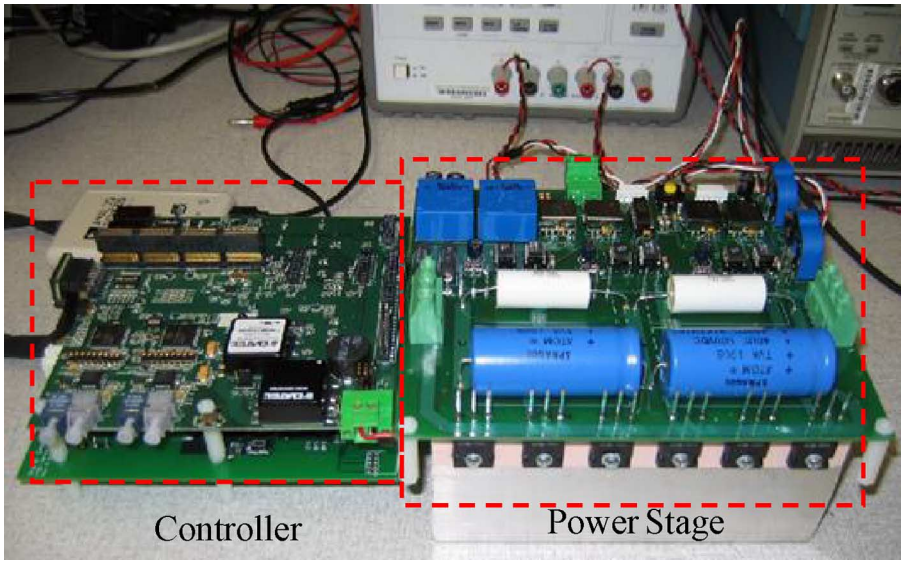

Fig. 14. Experimental system.

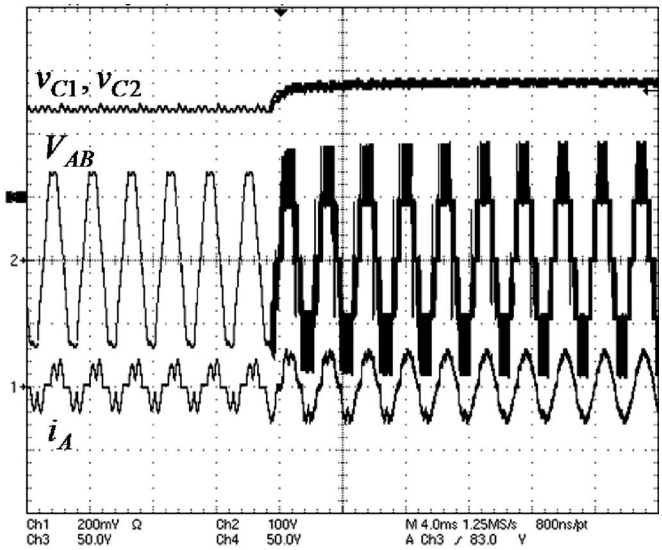

Fig. 15. Experimental waveform of the transient for operation mode transition. The traces from top-to-bottom are dc-link voltages, rectifier pole-to-pole voltage V_{AB}, and phase A current.

Fig. 8

$$\begin{cases} d_{(1,0,0)} + d_{(0,1,1)} = 2 - \sqrt{3}M\sin(\varphi + 60^\circ) \\ d_{(0,0,0)} = \sqrt{3}M\cos(\varphi + 30^\circ) - 1 \\ d_{(0,1,0)} = \sqrt{3}M\sin(\varphi). \end{cases} \tag{31}$$

Note that the first equation in (31) shows the redundant vectors (1,0,0) and (0,1,1) corresponding to subsector 2. There are infinite solutions to the equation. In order to achieve zero neutral-point current injection, the relative dwell times in (31) should be also subject to

$$d_{(0,1,0)}i_B + (d_{(1,0,0)} - d_{(0,1,1)})i_A = 0. \tag{32}$$

Using (31) and (32), the relative dwell times of the voltage vectors can be determined. Due to the characteristics of current forced commutation, the phase leg duty cycles can be given by

$$\begin{cases} d_a = (1 - d_{(1,0,0)})\mathrm{sgn}(i_A) \\ d_b = (1 - d_{(0,1,1)} - d_{(0,1,0)})\mathrm{sgn}(i_B) \\ d_c = (1 - d_{(0,1,1)})\mathrm{sgn}(i_C). \end{cases} \tag{33}$$

Then, the equivalent zero-sequence duty for the SVM scheme can be obtained through

$$d_{0\_\mathrm{SVM}} = \frac{d_a + d_b + d_c}{3}. \tag{34}$$

Using (23), (31)–(34), the optimal zero-sequence component for the SVM scheme in subsector 2 can be derived as

$$d_{0\_\mathrm{SVM}} = \frac{M}{2\cos\varphi}\left(\frac{1}{2} - \cos 2\varphi\right) \qquad 0 \le \varphi \le 30^\circ. \tag{35}$$

With the same assumption, substituting φ ($0 \le \varphi \le 30^\circ$) for $\omega_0 t$ in (29) leads to

$$d_0' = -M\frac{\cos^2\varphi - \cos^2(\varphi - 120^\circ) - \cos^2(\varphi + 120^\circ)}{\cos\varphi - \cos(\varphi - 120^\circ) - \cos(\varphi + 120^\circ)}. \tag{36}$$

After some trigonometric calculations, (36) can be further simplified as

$$d_0' = \frac{M}{2\cos\varphi}\left(\frac{1}{2} - \cos 2\varphi\right) \qquad 0 \le \varphi \le 30^\circ. \tag{37}$$

Equations (35) and (37) show that in subsector 2, the space-vector-based control scheme has the same zero-sequence component as the proposed carrier-based control scheme. Actually this conclusion stands for all the other subsectors. This analysis indicates that the proposed control approach is the same as the space vector modulation approach mathematically, but the zero sequence duty cycle in the carrier-based method is generated in a partially feed-forward way instead of going through the complicated space vector modulator.

As we know, for two-level converters, the zero-sequence injection technique is usually used to increase the possible modulation index [23]. However, the zero-sequence component in this

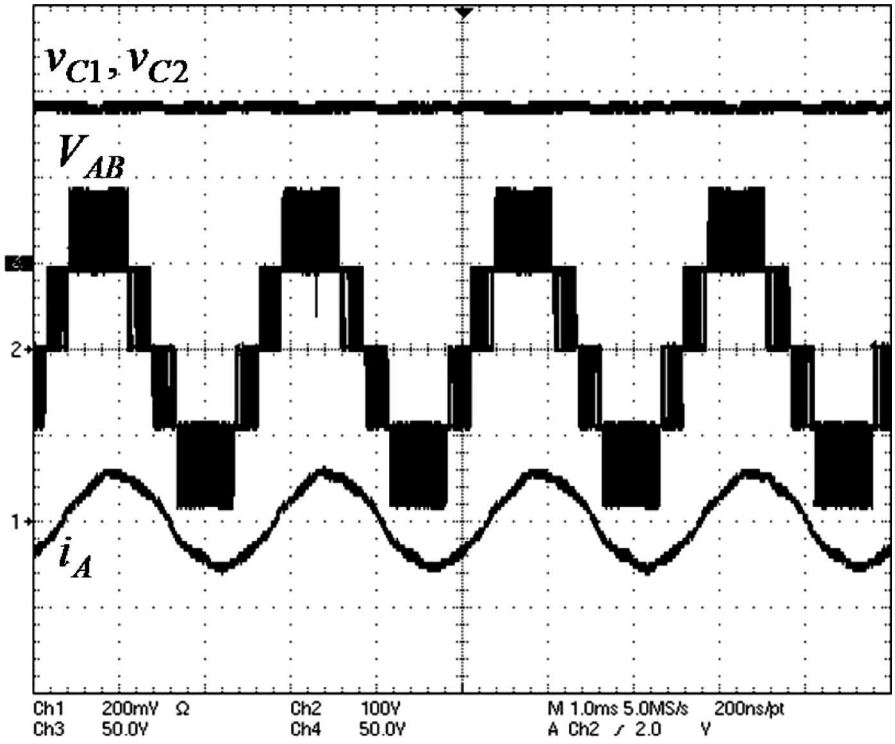

Fig. 16. Steady-state results with the carrier-based control scheme.

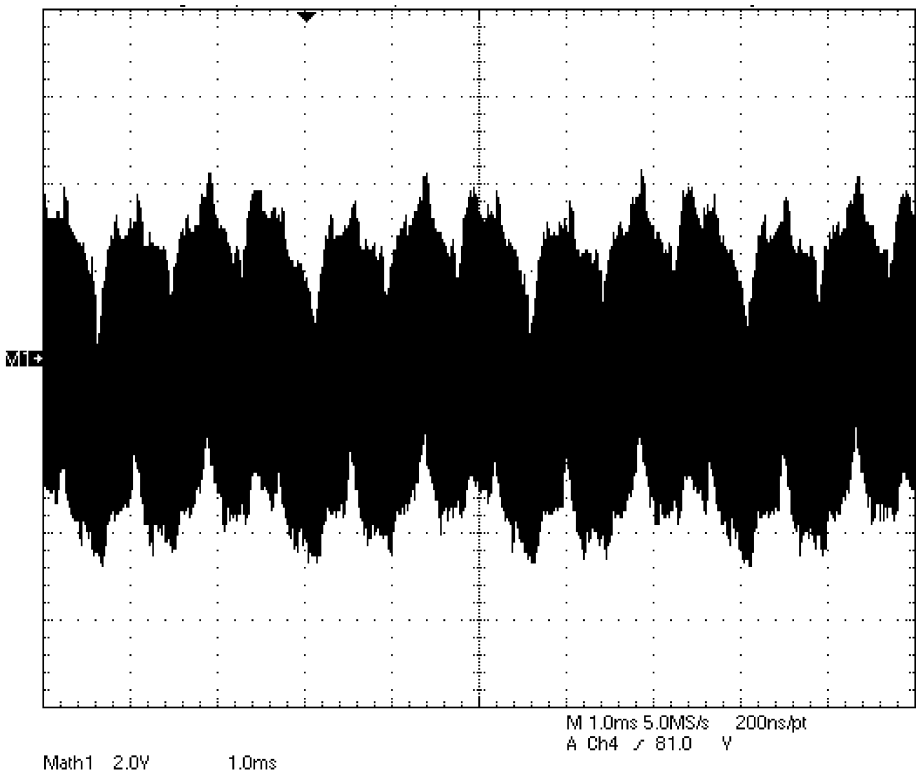

Fig. 17. DC-link voltage unbalance with the carrier-based control scheme.

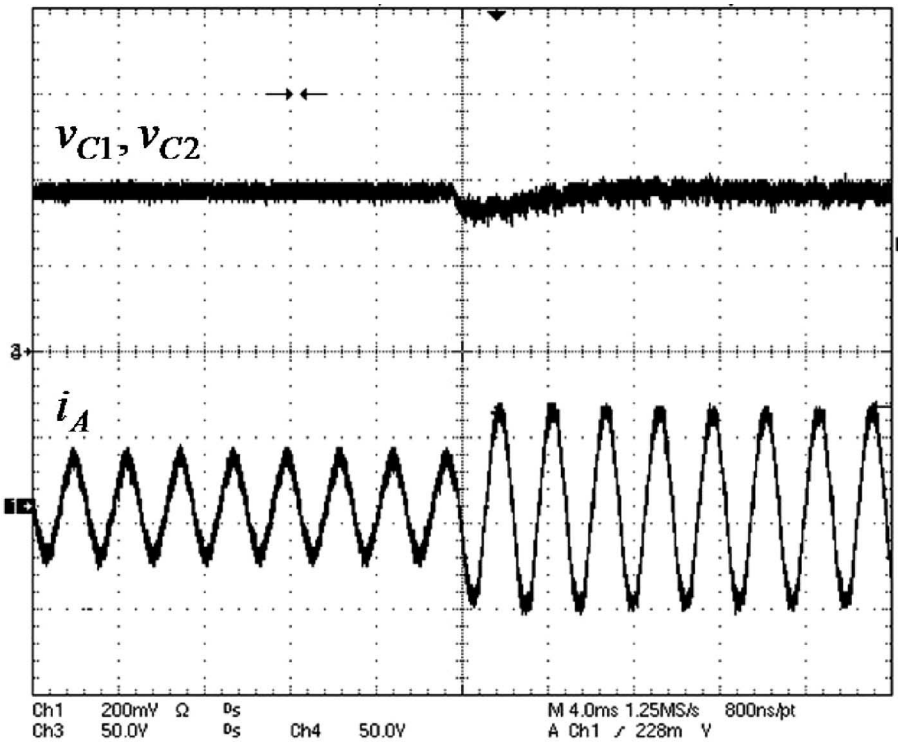

Fig. 18. Experimental waveform during load step change. The traces from top-to-bottom are dc-link voltages and phase A current.

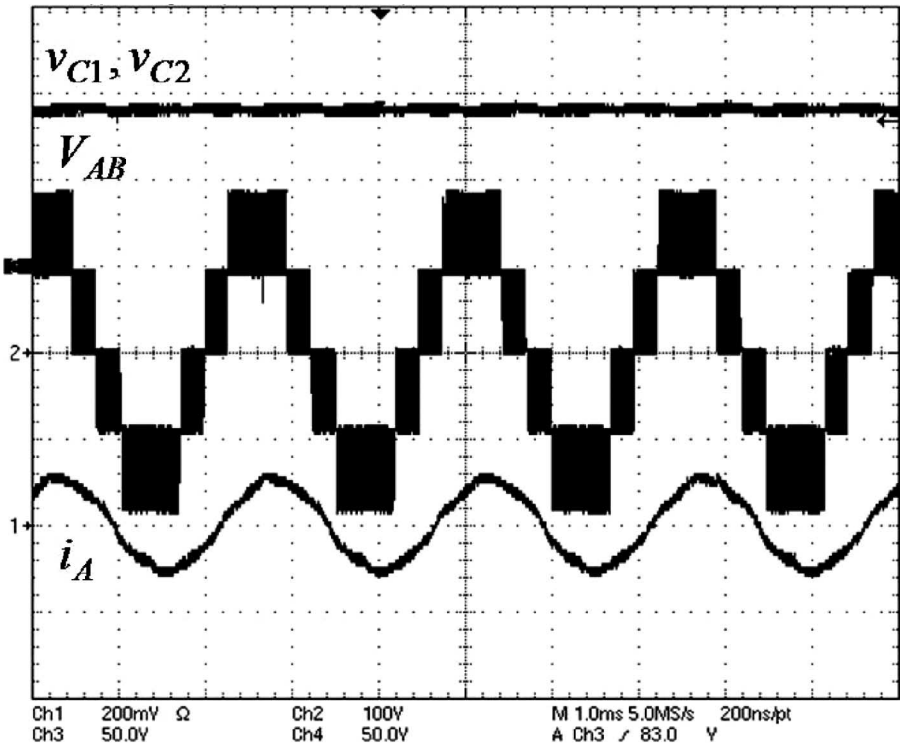

Fig. 19. Steady-state results with the space-vector-based control approach.

paper is derived from the neutral-point voltage balance standpoint instead. Therefore, its impact on the operating region, or the feasible modulation index, needs to be investigated.

The analysis can also be carried out based on vector synthesis equations. For example, if the target reference voltage is located in subsector 2 as shown in Fig. 8, we can define the distribution

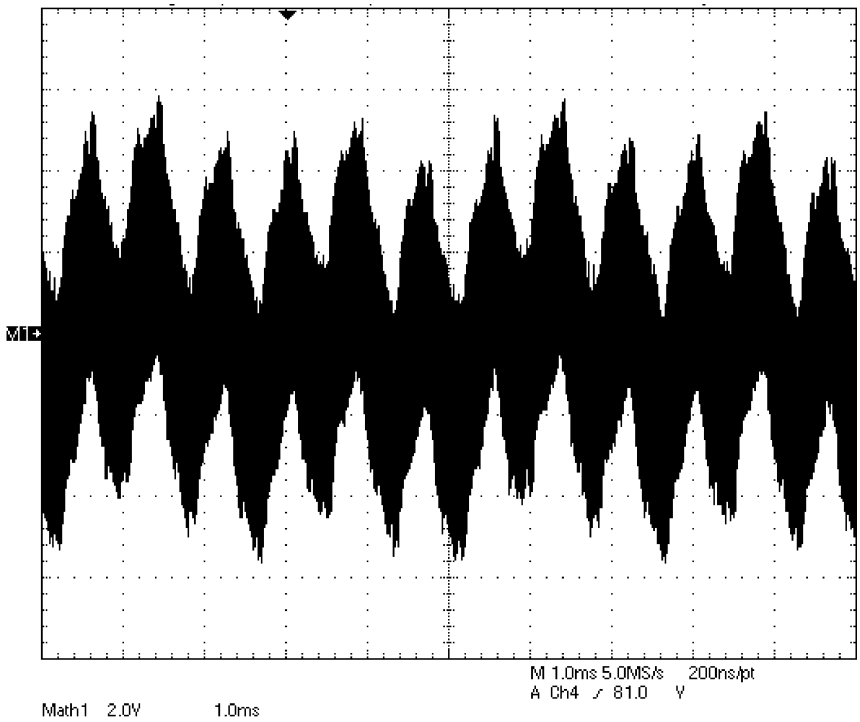

Fig. 20. DC-link voltage unbalance with the space–vector-based control approach.

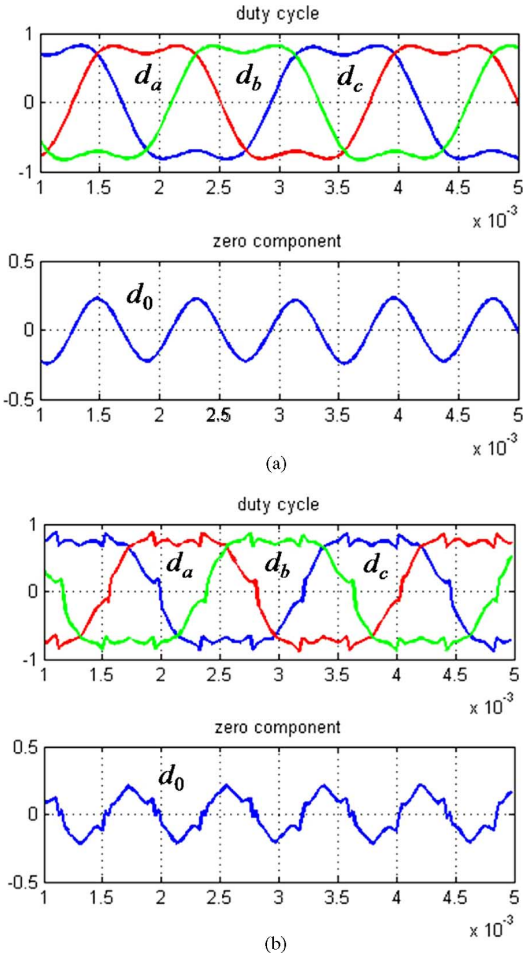

Fig. 21. Experimental duty cycle components for different approaches. (a) Carrier-based control scheme. (b) Space–vector based control scheme.

ratio of the redundant voltage vectors as

$$r = \frac{d_{(1,0,0)}}{d_{(1,0,0)} + d_{(0,1,1)}}. \tag{38}$$

After substituting (23) and (38) into (31) and (32) and performing some algebraic manipulation, the following relationship can be achieved

$$1 - 2r = \frac{\cos(\varphi - 120^\circ)}{\cos\varphi} \frac{\sqrt{3}M\sin\varphi}{2 - \sqrt{3}M\sin(\varphi + 60^\circ)}. \tag{39}$$

Since (32) is included in the derivation, (39) guarantees zero current injection into the dc-link neutral point. For a feasible solution, the distribution ratio r should be between 0 and 1, which leads to

$$-1 \le 1 - 2r \le 1. \tag{40}$$

Using (39) and (40), the upper boundary for the modulation index can be obtained as

$$M \le \frac{2\cos\varphi}{\sqrt{3}\sin(2\varphi + 60^\circ)}. \tag{41}$$

In subsector 2, $0 \le \varphi \le 30^\circ$, therefore, the minimum upper boundary in (41) can be achieved when $\varphi = 30^\circ$, as

$$M \le \frac{2}{\sqrt{3}}. \tag{42}$$

Equation (42) indicates that the full modulation index can be achieved in subsector 2, when considering zero current injection to the dc-link neutral point. This approach is applied to the other subsectors as well, and leads to the same conclusion. The full modulation index can be achieved in the full fundamental cycle when using the optimal zero-sequence component injection developed, in this paper.

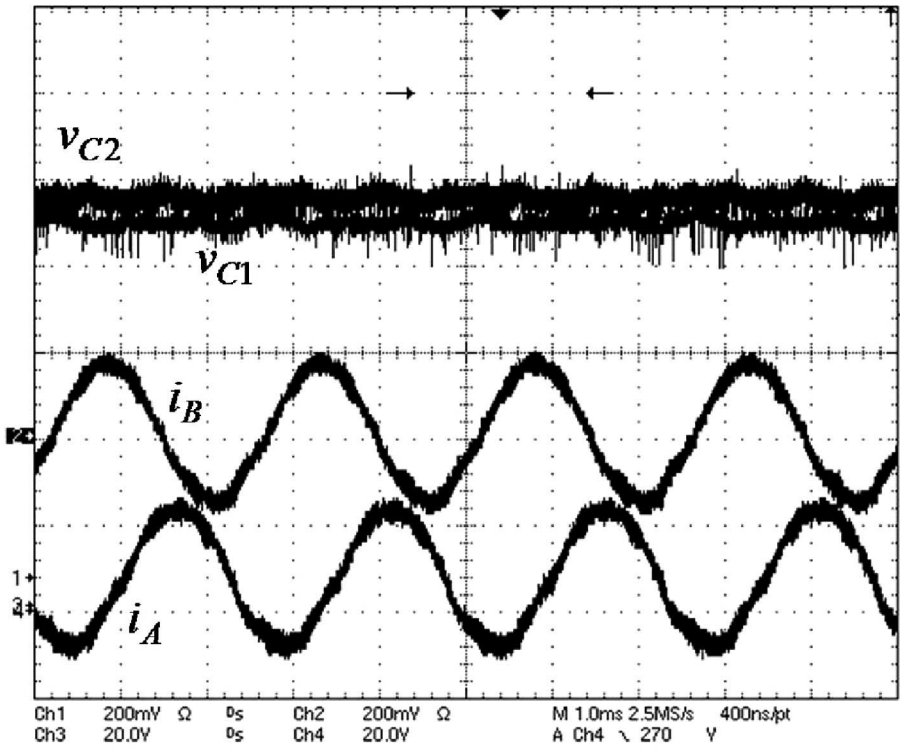

Fig. 22. Experimental results with P regulator. The top traces are the dc-link voltages. The bottom traces are the currents of phase A and phase B.

V. Simulation and Experimental Verification

A detailed Saber simulation has been built to verify the proposed model and control scheme. Table I shows the circuit parameters used in the small-scale simulation model. In the proposed model the ac input stage has the same feature as the two-level voltage source rectifier. Therefore, the conventional d–q small-signal model is applied for the input current and dc-link voltage control loop design [25]. Considering the switching frequency of 40 kHz and the system stability, the current control loop bandwidth and the dc-link voltage control loop bandwidth are selected to be 3.5 and 1 kHz, respectively. For the voltage unbalance control loop, a bandwidth of 400 Hz is chosen. Fig. 9 shows the steady-state waveforms of the dc-link voltages, ac phase A source voltage and current. Fig. 9 indicates that both the ac input currents and the dc-link voltages are well controlled. Fig. 10 shows the transient response for a load step-up case, in which the load resistance steps from 50 to 25 Ω. The simulation results indicate that the proposed control approach is stable under the load-step transient condition. Fig. 11 shows the voltage unbalance behavior under pulsating Δd_0 with the neutral-point voltage feedback loop open. Δv_1 is the voltage unbalance obtained from the proposed math model. Δv_2 is the Saber simulation result. The results show that the proposed model can predict the neutral-point voltage unbalance performance under small-signal perturbation. The simulation for unbalanced load condition is also carried out. A 15 Ω resistor is placed across capacitor C_1 and a 20 Ω resistor is across capacitor C_2. Fig. 12 shows the simulation results when using only a P regulator for the voltage unbalance control. The voltage unbalance is about 4 V. Fig. 13 shows the results for a PI regulator. The dc-link voltage is balanced after adding the integral regulator.

In order to further verify the proposed control approach, an experimental system is built at laboratory scale. The power stage consists of SiC Shottky diodes and Si MOSFETs, and the control system is implemented in a DSP and FPGA-based digital control board [24]. The voltage and current regulators are implemented in the floating point DSP (ADSP-21160), and modulator is implemented in FPGA (XILINX-XCV400). Fig. 14 shows the experimental system, with the configuration parameters in Table I. Fig. 15 shows the transient waveforms, when the converter changes from diode rectification mode to active control mode, and Fig. 16 shows the corresponding steady-state waveforms. Fig. 17 shows the dc-link voltage unbalance ($V_{C1} - V_{C2}$) in steady state. The maximum unbalance is about 4 V for the proposed approach. Fig. 18 shows the experimental result for the load step change, with the load increasing from 500 W to 1 kW within 100 μs. The test results indicate that the system is stable. The tests shown in Figs. 15–18 are using the carrier-based PWM. For comparison the corresponding steady-state experimental waveforms with the SVM-based controller are shown in Figs. 19 and 20. With the SVM, the maximum dc-link voltage unbalance is about 5 V, which is slightly higher than the proposed approach. The results indicate that the carrier-based control approach has similar performance to the SVM-based control scheme. The neutral-point voltages are well regulated by both methods, even though the dc-link capacitance is very

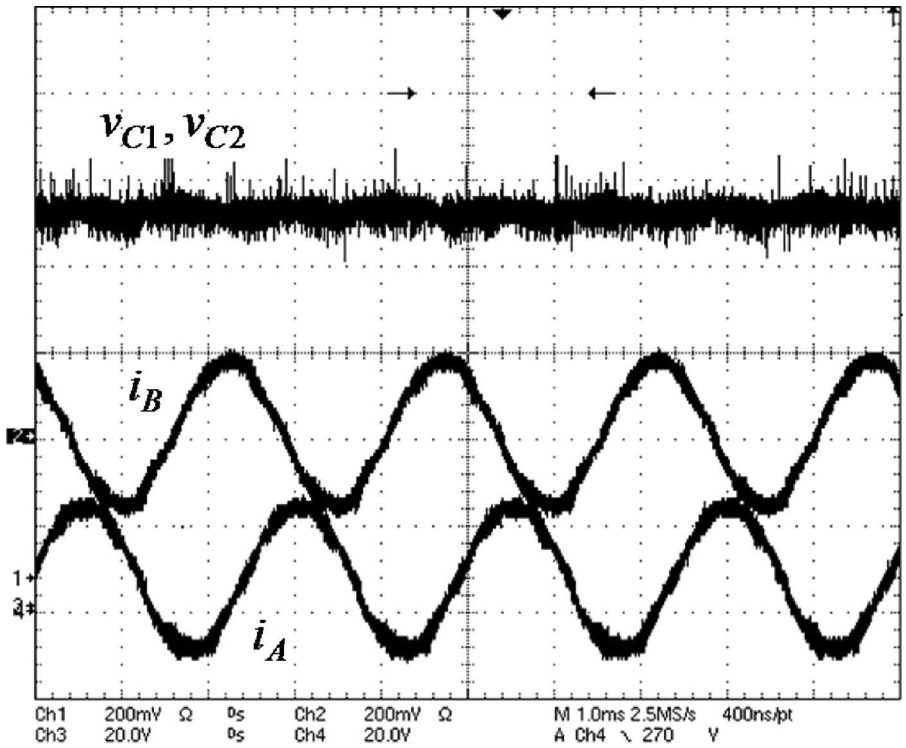

Fig. 23. Experimental results with PI regulator. The top traces are the dc-link voltages. The bottom traces are the currents of phase A and phase B.

small. Fig. 21 shows the experimental phase leg duty cycles (d_a, d_b, d_c) and zero-sequence components (d_0) for both control schemes. As shown in Fig. 21(a), the zero-sequence component of the proposed method exhibits the characteristics of the optimal neutral-point injection, which is a standard third-order harmonic. In Fig. 21(b), the zero component of the space vector control scheme shows different features, since its voltage balance regulation is achieved by only a feedback loop.

The performance of the proposed controller with unbalanced load condition is also investigated in the experiments. For this case, a 15.3 Ω resistor is paralleled with C_1 and a 20.9 Ω resistor is paralleled with C_2 as the unbalanced dc load. Fig. 22 shows the experimental results with the voltage unbalance regulator with only the P regulator. About 5 V steady-state unbalance is observed. The results with PI regulator are shown in Fig. 23. As can be seen, the dc-link voltage unbalance is minimized with the PI regulator even under unbalance load condition. The experimental results match the simulation results very well.

VI. Conclusion

This paper has presented a new average model for the non-regenerative three-level VIENNA-type boost rectifier using the concept of zero neutral-point current injection. The optimal zero-sequence duty cycle has been found to guarantee the dc-link voltage balance, based on which an equilibrium operating point can be determined, and the behavior of the neutral-point voltage deviation can be modeled as a simple first-order system. The proposed model features an extended frequency range of up to half of the switching frequency using conventional d–q representation; therefore, this model can be applied to high-performance controller design. Based on the proposed model, a carrier-based control approach was developed. The zero-sequence duty cycle, which contains both feed-forward and feedback components, is used to control the neutral-point voltage balance. The feed-forward component ensures zero current injection to the neutral point with simple calculation, and the feedback component compensates the non-idealities in the real system. The space vector analysis showed that the proposed control approach is mathematically equivalent to the space-vector-based control approach while the proposed approach achieves the zero-sequence component in a partially feed-forward way. Therefore, the proposed control method can significantly reduce the computation efforts. The analysis also proved that with the optimal zero-sequence component, the full modulation index can be still achieved. The proposed model and control scheme were verified in simulation and experiments.

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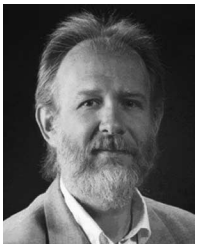

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