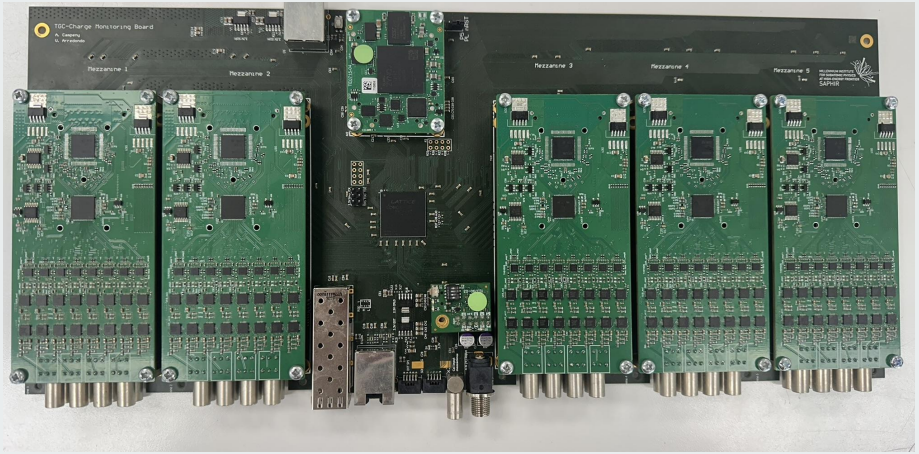
TGC-Charge Monitoring System Status

January 2025



MILLENNIUM INSTITUTE FOR SUBATOMIC PHYSICS AT HIGH-ENERGY FRONTIER SAPHIR

UNIVERSIDAD DE LA SERENA CHILE

Universidad Andrés Bello

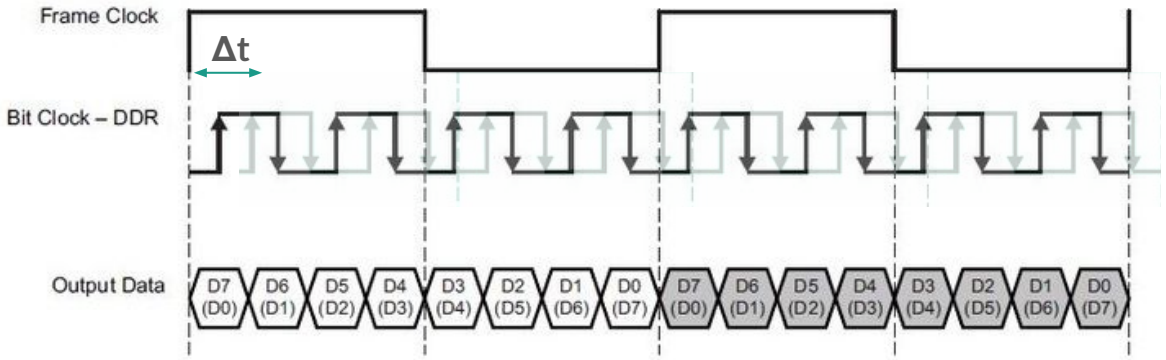
Team Change

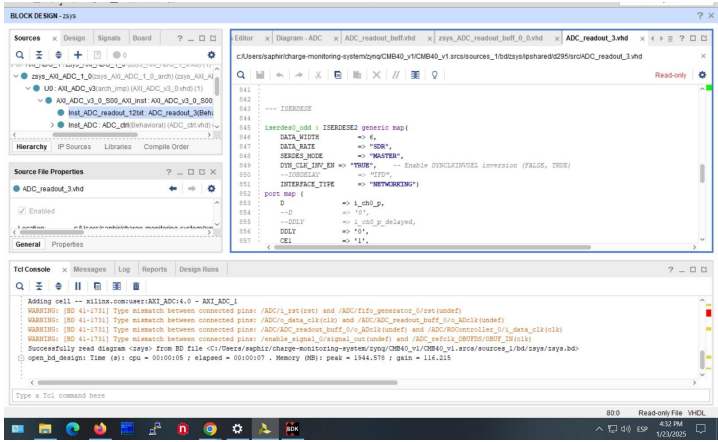
We are training the new engineer to help us with the development of the firmware we miss.
Current team is:

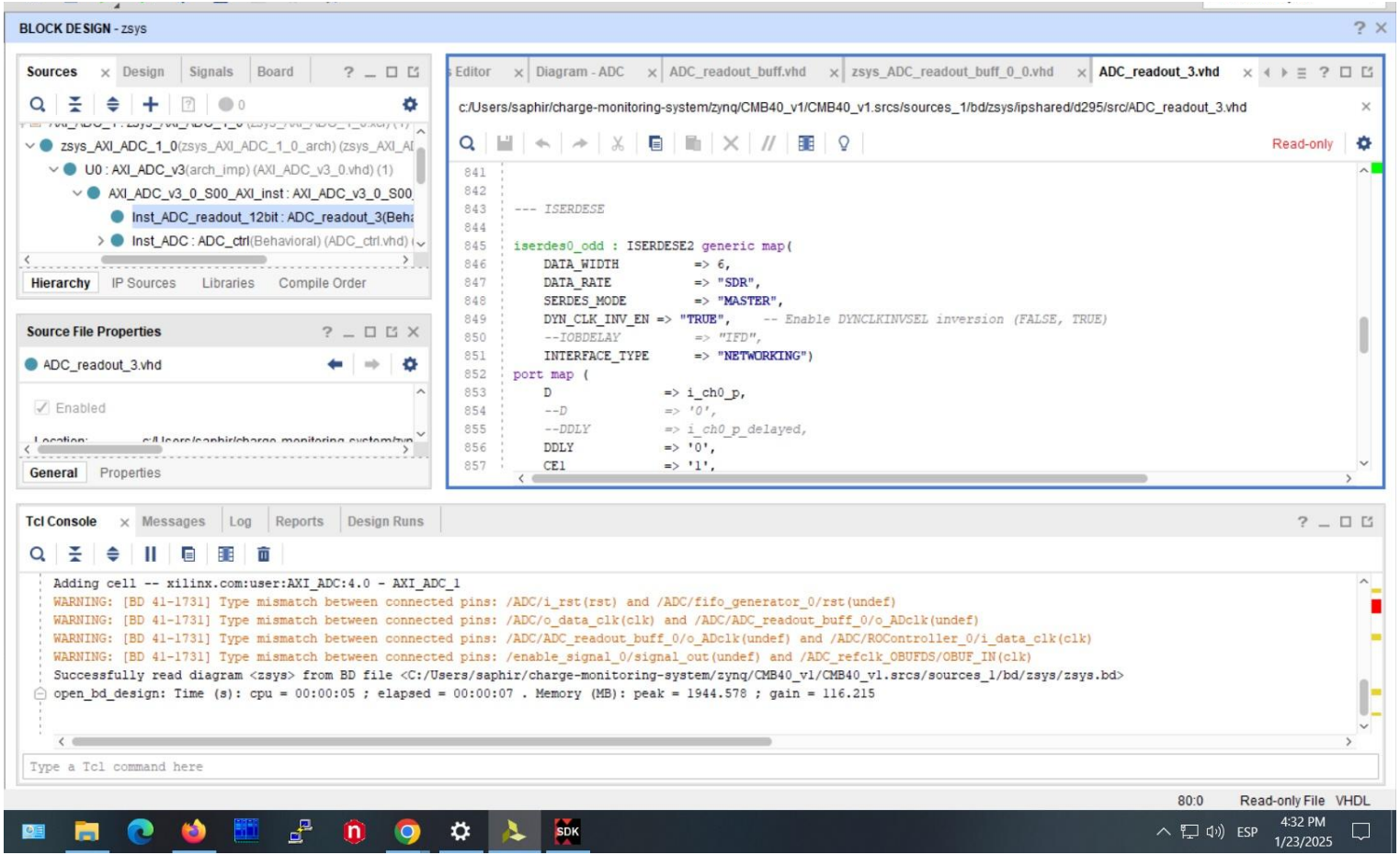
- Sergey Kuleshov (UNAB), procurement preparation
- Orlando Soto (ULS), firmware/hardware tests
- Felipe OIlivares (SAPHIR), procurement preparation
- Mauro Bonilla (SAPHIR), firmware / hardware development. New electronic engineer that is being trained
- Fabian Trigo (PhD Student), software (PS) and firmware (PL) development

TGC-Charge Monitoring system tests

- We identified a phase shift of clocks coming from the ADCs passing through de CPLD. We are using ISERDESE units of the zynq to synchronize the frame and bit clocks
  A manual shift will be applied in order to complete the hardware tests, then a routine to estimate the shift automatically will be developed



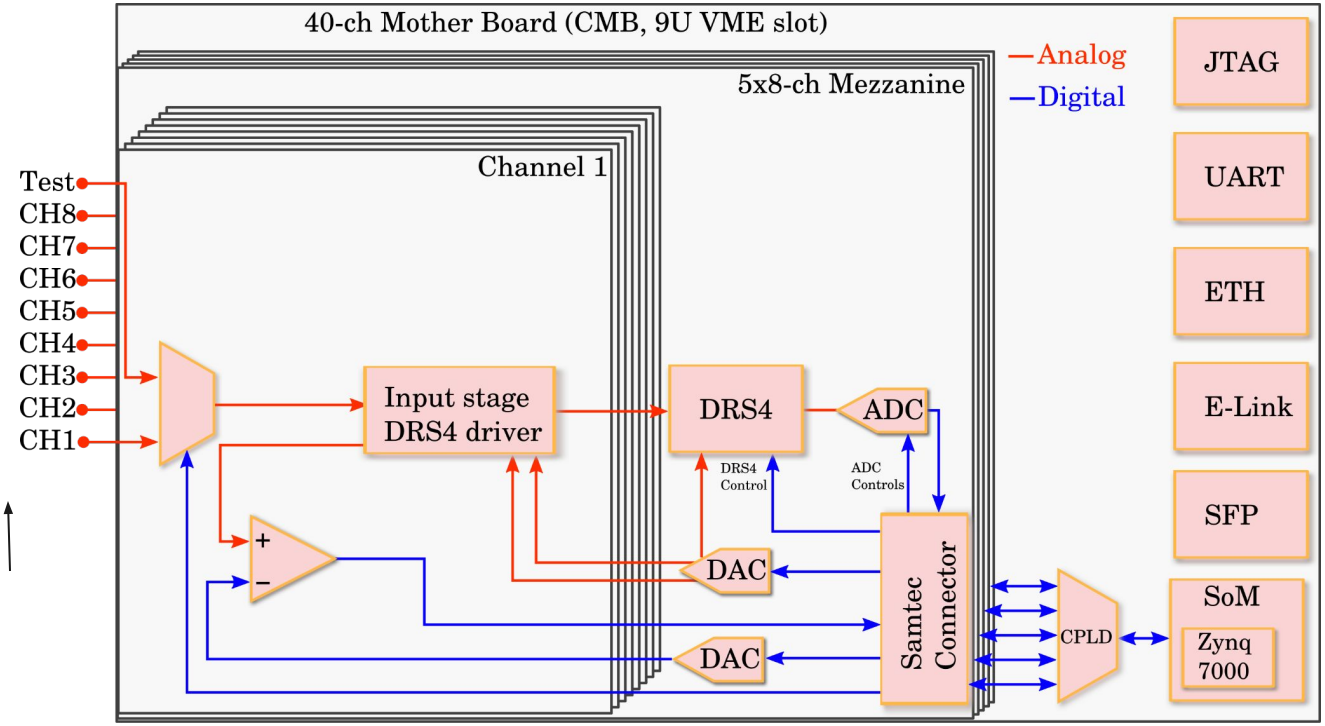



BLOCK DESIGN - zsys
Sources
Design
Signals
Board
zsys_AXI_ADC_1_0(zsys_AXI_ADC_1_0_arch) (zsys_AXI_AD
U0 : AXI_ADC_v3(arch_imp) (AXI_ADC_v3_0.vhd) (1)
AXI_ADC_v3_0_S00_AXI_inst : AXI_ADC_v3_0_S00_
Inst_ADC_readout_12bit : ADC_readout_3(Beha
Inst_ADC : ADC_ctrl(Behavioral) (ADC_ctrl.vhd)
Hierarchy
IP Sources
Libraries
Compile Order
Source File Properties
ADC_readout_3.vhd
Enabled
General
Properties
Editor
Diagram - ADC
ADC_readout_buff.vhd
zsys_ADC_readout_buff_0_0.vhd
ADC_readout_3.vhd
c:/Users/saphir/charge-monitoring-system/zynq/CMB40_v1/CMB40_v1.srcs/sources_1/bd/zsys/ipshared/d295/src/ADC_readout_3.vhd
Read-only
841
842
843 --- ISERDESE
844
845 iserdes0_odd : ISERDESE2 generic map(
846 DATA_WIDTH => 6,
847 DATA_RATE => "SDR",
848 SERDES_MODE => "MASTER",
849 DYN_CLK_INV_EN => "TRUE", -- Enable DYNCLKINVSEL inversion (FALSE, TRUE)
850 --IOBDELAY => "IFD",
851 INTERFACE_TYPE => "NETWORKING")
852 port map (
853 D => i_ch0_p,
854 --D => '0',
855 --DDLY => i_ch0_p_delayed,
856 DDLY => '0',
857 CE1 => '1',
Tcl Console
Messages
Log
Reports
Design Runs
Adding cell -- xilinx.com:user:AXI_ADC:4.0 - AXI_ADC_1
WARNING: [BD 41-1731] Type mismatch between connected pins: /ADC/i_rst(rst) and /ADC/fifo_generator_0/rst(undef)
WARNING: [BD 41-1731] Type mismatch between connected pins: /ADC/o_data_clk(clk) and /ADC/ADC_readout_buff_0/o_ADclk(undef)
WARNING: [BD 41-1731] Type mismatch between connected pins: /ADC/ADC_readout_buff_0/o_ADclk(undef) and /ADC/ROController_0/i_data_clk(clk)
WARNING: [BD 41-1731] Type mismatch between connected pins: /enable_signal_0/signal_out(undef) and /ADC_refclk_OBUFDS/OBUF_IN(clk)
Successfully read diagram <zsys> from BD file <C:/Users/saphir/charge-monitoring-system/zynq/CMB40_v1/CMB40_v1.srcs/sources_1/bd/zsys/zsys.bd>
open_bd_design: Time (s): cpu = 00:00:05 ; elapsed = 00:00:07 . Memory (MB): peak = 1944.578 ; gain = 116.215
Type a Tcl command here
80:0
Read-only File
VHDL
ESP
4:32 PM
1/23/2025

Workaround the bitslip problem

data stream analysis

DRS4 Transparent mode test



Firmware and software status

EMCI / EMP / DCS integration

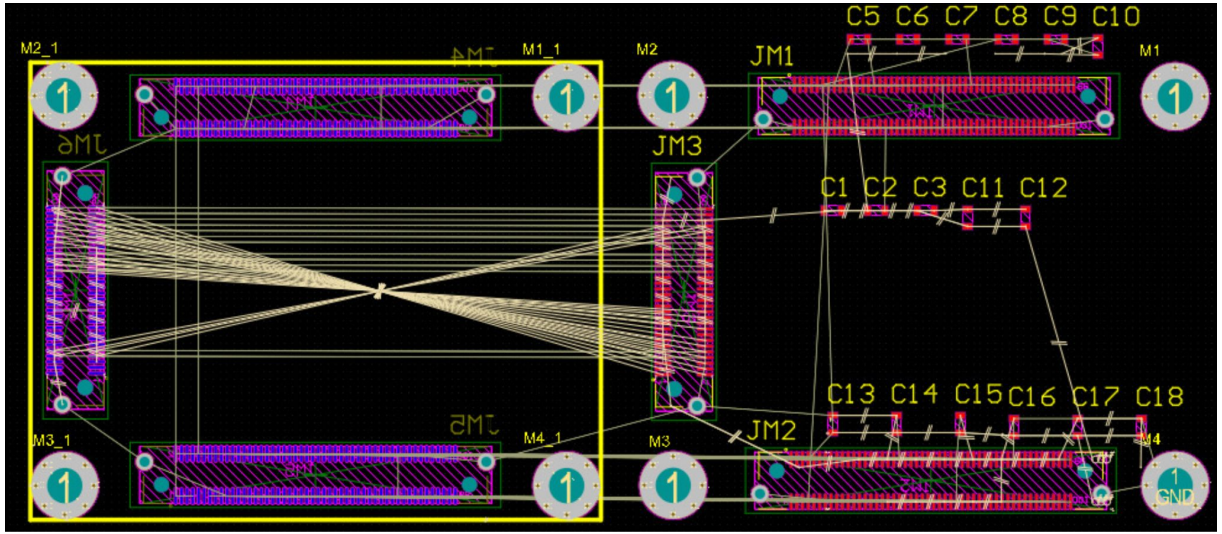
- Pruebas protocolo CLPS (protocolo)
- Cambio diseño carrier board EMCI
- Instalacion de software para integracion con DCS (WIN-OC) en servidor local (ULS)
- planes de desarrollo de firmware

Procurement preparation

QA and QC preliminary plans

Preparation for QC/QA tests

- We identified a possible problem with the samtec connector during the QC/QA tests. A safe board to address the possible problem of plug/unplug 100 boards is being designed



Procurement preparation

We have a successfully meeting with head of ANID (Chilean agency), they agree to purchase 700 DRS4 chips. we have the quote from radec, and felipe Olivares is preparing the paperwork for the purchasing