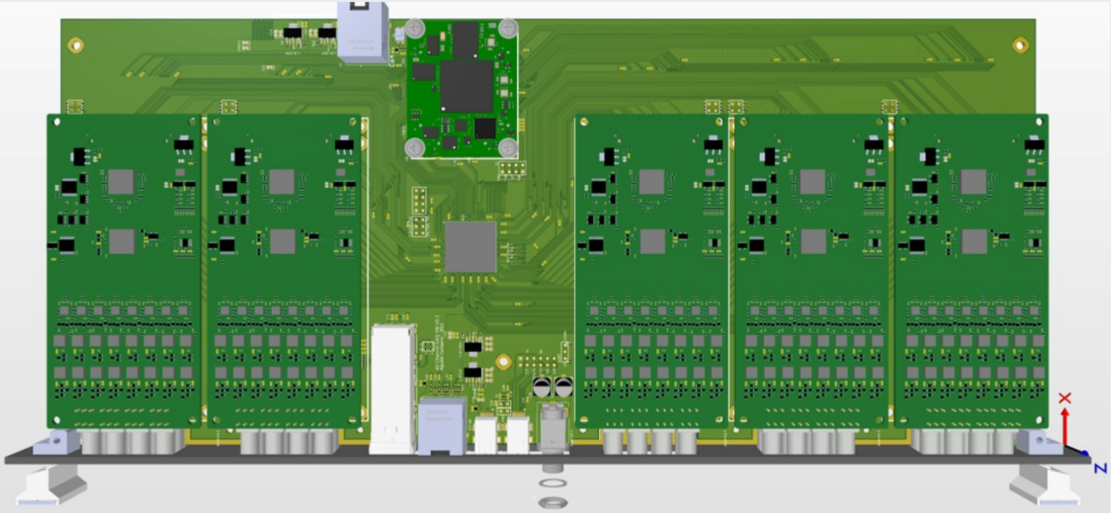
Estimation of EMP firmware for CMB

September 2024



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Methodology

1) Create a core design to transfer data from 1 emp-lpGBT block into Processing System
    1) Emulate data coming out of emp-lpGBT
    2) Implement an AXI4-Lite block to write data from PL to PS
    3) Multiplex data from emp-lpGBT to the AXI4-Lite block created
2) Replicate the design in EMP’s firmware, using the 12 available emp-lpGBT blocks

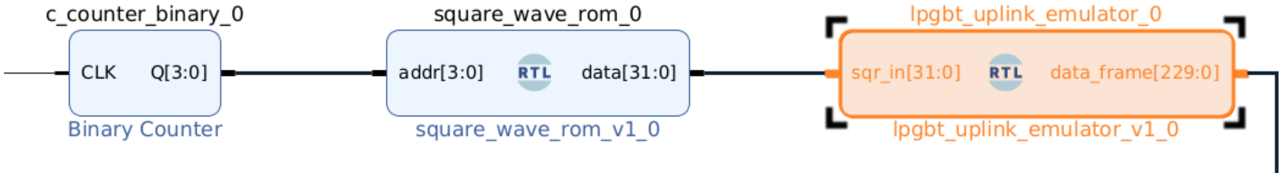
Caveats

- This estimation is done only considering the uplink data (data coming from Charge Monitoring Boards to the EMP)
  - This is a good proxy as out firmware is mainly uplink logic

Core Design

Emulate data from emp-lpGBT

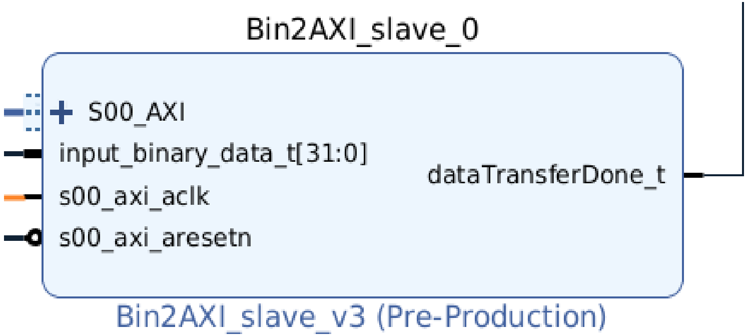
1) Binary Counter
2) Square wave generation
    1) This 32-bits square wave is the base signal that will be replicated in the 230-bits signal that will emulate the emp-lpGBT
3) lpgbt_uplink_emulator
    1) Copies the input square wave into a 230-bits signal; basically forking the input signal to expand its width



Core Design

AXI4-Lite block to connect PL to PS

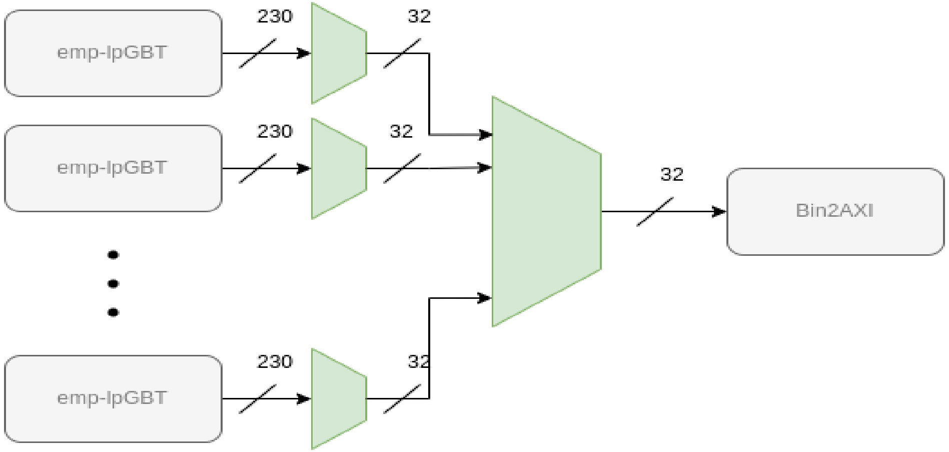
- Takes 32-bits input binary data
- Stores the emp-lpGBT data in internal registers and sends it to the PS
- Implementation based on Vivado tool “Create and Package New IP”



Implementation for 12 emp-lpGBT

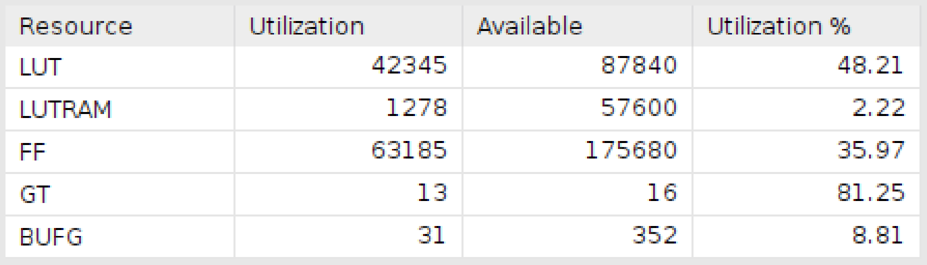
Data multiplexing from emp-lpGBT to AXI4-Lite Block

- The multiplexing phase allow to integrate the previous blocks to route the data from 12 emp-lpGBTs into the Processing System

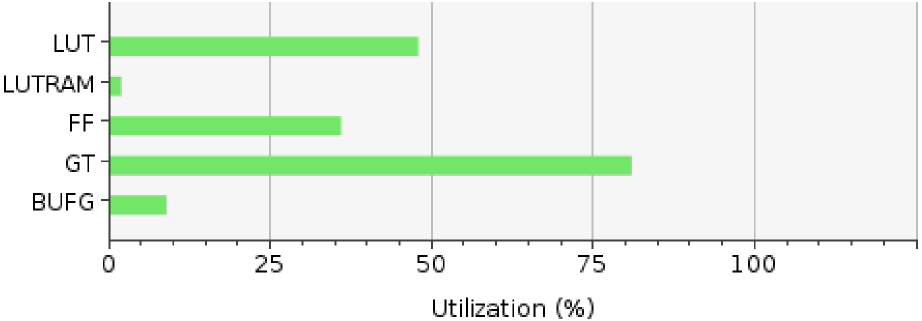


Utilization estimation for EMP’s Programmable Logic

From EMP firmware project



Resource	Utilization	Available	Utilization %
LUT	42345	87840	48.21
LUTRAM	1278	57600	2.22
FF	63185	175680	35.97
GT	13	16	81.25
BUFG	31	352	8.81


LUT
LUTRAM
FF
GT
BUFG
Utilization (%)