Final report

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Charge Monitoring Board status

Currently, the Charge Monitoring Board (CMB) motherboard is assembled, the CPLD is programmed and the communication between the Trenz board and the ADC is working. Additionally, the trigger circuit in the mezzanines is working; the trigger signal is received in the Trenz Board.

There are a couple of mezzanines under test with the Charge Monitoring Board's motherboard, and if the data acquisition with them works, the rest of the mezzanines will be soldered following the same instructions used for soldering the first ones.

Currently there is an issue with measuring the LVDS signal produced by the ADC and received by the Trenz Board. During our experiments, we generated a known pattern in the ADC, and we saw that it is received shifted by 1 bit. The guess is that the cause of that shift are the delays in the CPLD, which may causes the LVDS signals –the differential signals: frame clock, bits clock and data– to arrive out of their original phase into the Trenz board. As a result of that, a correction must be implemented yet to properly receive the data.

It was possible to see some signals coming from the DRS4, through the ADC, to the Trenz Board, but in order to judge if they are proper measurements, the LVDS phase shift in the signals must be repaired first.

The E-link communication with the EMCI board is not implemented yet in firmware. The main challenge there is that originally the Charge Monitoring Board design considered that the clocks for the E-link communication will come from the CMB itself, but according to the

EMCI and lpGBT teams, those clocks must come from the lpGBT. If we would like to implement the communication with the clocks being generated by the CMB, we should modify the EMCI/lpGBT itself, as clock crossing domains should be implemented in the EMCI for each communication with the each CMB. On the other hand, if the clock is generated in the lpGBT, a single clock crossing domain must be implemented in each CMB, which is a system that we already know.

Current design limitations

Firmware limitations

The trigger logic is the part of the firmware that receives the trigger signal from a mezzanine's channel and decides if the data capture must start. Currently, that module is not working properly. The root cause of that malfunctioning are not well studied, but probably it is due clock signals that instead of coming from a clock tree, comes from an input port, or from a combinational logic. To repair this module, I think it should be rewritten; this should not be so difficult, as it is a 172 VHDL lines module.

E-link communication is not implemented yet. As already said previously, the Charge Monitoring Board was originally designed to produce the clocks required in the E-link communication, but now we must receive those clock signals. As the Charge Monitoring Board motherboard is already designed, it is unlikely that the clock signals coming from the lpGBT will go into clock dedicated pins, which is not a catastrophic condition, but may add skew or tighter static timing constraints for the logic clocked by that signal.

Hardware limitations

Currently the E-link communication uses 6 cables (3 differential pairs): 2 for Rx, 2 for Tx and 2 for clock. However, the RJ-45 connector has 8 connections, and there are 2 extra cables that currently are not connected as differential pairs; even one of them

is connected to the enable pin of a voltage regulator, and the other to on CPLD pin and to one Trenz Board pin. The problem is that those 2 extra cables only may be useful if the CMB and EMCI share ground, because otherwise, their voltage may be undefined and even unexpected current can flow through them. Because of that, it must be checked if the CMB and the EMCI will share GND, and if not, those signals should be either: removed from the RJ-45 cable by removing their corresponding pins in the connector, or removed from the RJ-45 female connector in the motherboard.

Additionally, it was seen that plugging or unplugging the RJ-45 cable for the E-link communication may cause voltage oscillations in the power supply, which may reset the Trenz Board itself. Those voltage oscillations may be solved by soldering a TVS diode in where now there is the capacitor C27 or C26. However, a TVS diode with a footprint that fits the C27 or C26 capacitors mus be found.

General warnings when implementing the final design

1. To avoid over-voltage in the lpGBT chip, the communication protocol between the EMCI and the Trenz Board must be PPDS, not LVDS. To set this protocol, the designer must go to the Trenz's constraint file and set the proper communication protocol for the E-link communication pins.
2. The current prototype firmware for E-link communication in the EMP assumes that the CMB is constantly sending data. In this way, there is no need for memory instantiation in the EMP. If the designer decides to keep this design mindset, please he must remember to constantly send data from the CMB.

Version

Version	Date	Comment
1.0	2024/12/17	The report is created.