



6 June 2025

Technical Design Report

TGC-Charge Monitoring Board

ATLAS collaboration

Summary

For this style of document, the abstract has more the function of a summary.

ATLAS Doc:	xxx-yyy-zzzz	
EDMS Id:	123456	
Version:	0.1	
Last modified:	15:27 on 6 June 2025	
Prepared by: S. Kuleshov V. Agosin O. Soto V. Arredondo	Checked by: D. Person E. Person	Approved by: F. Person G. Person

Contents

1 Conventions and Glossary	5
2 Related Documents	5
3 Introduction (All)	5
4 Interfaces	7
4.1 Electrical Interfaces	7
4.1.1 CMB Front panel	7
4.1.2 CMB Back	8
4.2 EMCI carrier board	8
4.3 Mechanical Interfaces	11
5 Physical Description	13
5.1 Physical Location	15
6 Firmware (V. Arredondo)	15
6.1 ADC readout	16
6.2 DRS4 IC control firmware	18
6.3 CPLD communication	20
6.4 DAC control	23
6.5 Full waveform readout	24
7 Manufacturer	24
8 Power	26
9 Prototypes Development	27
9.1 Mezzanine board	27
9.2 Motherboard for two mezzanines, 16 channels	28
10 Testing, validation, and commissioning	28
10.1 Radiation Tests	29
10.1.1 Campaign 1	29
10.1.2 Campaign 2	35
10.1.3 Campaign 3	41
10.1.4 Conclusions	44
10.1.5 Future Radiation tests plan	45
11 Reliability Matters	46
11.1 Consequences of Failures	46
11.2 Prior Knowledge of Expected Reliability	46
11.3 Measures Proposed to Ensure Reliability of Component and/or System . .	46
11.4 Quality Assurance to Validate Reliability of Design and Construction or Manufacturing Techniques	46

11.5 Quality Control to Validate Reliability Specifications during Production . . .	46
12 Appendix	47

List of Figures

1 General connections block diagram	7
2 Front panel	7
3 Front panel	8
4 EMCI-VME board	9
5 Electrical signals for EMCI and CMB communication.	9
6 Vita 57.1 HPC pinout	11
7 Blue mini rack where the CMB will be installed. The CMBs will be inserted as VME cardboards. The slide is shown by the Japanese group at https://indico.cern.ch/event/977581	12
8 Mechanical dimensions of the board	13
9 Physical top	14
10 Physical description top view	14
11 Physical description front view	14
12 40 channels CMB connection diagram	15
13 Location of mini racks where CMB and VME-EMCI are placed in UX15.	15
14 Firmware: Digital signal diagram.	16
15 ADC schematic firmware block design in Vivado	17
16 Readout controller block design in Vivado	18
17 DRS4 initial sequence	20
18 DRS4 firmware block design in Vivado	20
19 Diagram of signal acquisition control logic	21
20 CPLD firmware schematic.	21
21 i2c block design to control the DAC at mezzanines.	23
22 Mezzanine board assembled.	27
23 New version mezzanine board, 3d model.	28
24 Prototype motherboard up to 2 Mezzanine connections.	28
25 Beam during the first campaign. The stars indicate non-recoverable failures.	30
26 Photos of the DUT and the control room setup	31
27 Connection diagram for the first irradiation campaign	31
28 Flow diagram of the Firmware used during the tests	32
29 Common failure observed. The top image shows a summary of one day of measurements. The bottom images show time slices before and after the failure.	32
30 Current consumption during the first week.	33
31 Current consumption seconds before DACs failures.	33
32 Time intervals between failures for the 16-ch CMB, during the first campaign	34
33 Current measurements during the weeks 2 and 3 (SoM + 16-channels motherboard).	34

34	Current measurements just before the non-recoverable failure.	35
35	Signals acquired with the mezzanine after the annealing process.	35
36	Beam during the second campaign. TID in Gy, HEH in part./cm ² , N1MeV in n/cm ²	36
37	Diagram of the firmware used. The LFSR and the comparators have TMR. .	37
38	Time interval between failures for the 16-ch CMB during the sec. campaign .	38
39	CMB 16-ch current consumption, the step indicates the moment of DACs failure during the sec. campaign	38
40	Cumulative fails during the sec. campaign for each B13 pair	39
41	Total cumulative B13 fails during the sec. campaign	39
42	Time interval between failures for the CPLD during the sec. campaign .	40
43	Beam during the second campaign. TID in Gy, HEH in part./cm ² , N1MeV in n/cm ²	41
44	Cumulative fails during the third campaign for each B13 pair	42
45	Total cumulative B13 fails during the third campaign	42
46	Time interval between failures for the CPLD during the third campaign .	43
47	Vivado block design of the project to read 1 mezzanine and send full wave- form readout using UART.	49

List of Tables

1	Front panel interfaces	8
2	EMCI-VME ADC pins	10
3	EMCI-VME I2C pins	11
4	Mux_sel IO pins from SoC to CPLD to select digital signals from the Mezzanine board.	22
5	Design Summary of CPLD firmware.	22
6	Resource utilization of full waveform readout using UART	24
7	Principal Components and manufacturers.	25
8	Power specifications	26
9	Power modules requirement.	26
10	Radiation levels required	29
11	CPLD firmware resources	36
12	Summary of radiation dose achieved	44
13	ADC alternatives	45
14	Mezzanine electrical signal pinout in LSHM-150 samtec connector.	48

1 Conventions and Glossary

BW: big wheels
CMB: charge monitoring board
TGC: Thin gap chamber
MDT: Monitoring Drift Tubes
ASD: Amplifier-Shaper-Discriminator
EMCI: Embedded Monitoring and Control Interface
EMP: Embedded Monitoring Processor
FE: Front-End
lpGBT: low power Giga Bit Transceiver
SoC: System on Chip
SoM: System on Module
COTS: Commercial off the shelf
MO: Monitoring Output
DCS: Detector Control System
MIP: Minimum Ionizing Particle
ToT: Time over threshold
CCHEN: Comisión Chilena de Energía Nuclear (Chilean Nuclear Energy Commission)
EIL4: End-cap Inner Layer Station 4
TBD: To be determined

2 Related Documents

- Embedded Monitoring and Control Interface technical specification.
- lpGBT – a User’s Perspective
- ATLAS phase-2 TDR
- ASD PRR
- Charge Monitoring Board SPR

3 Introduction (All)

The Muon Spectrometer of the ATLAS Experiment at CERN is composed of Thin Gap Chambers (TGC), Resistive Plate Chambers (RPC) and Monitoring Drift Tubes (MDT) technologies. TGCs are installed in 6 Big Wheels and in 2 Small Wheels. Gain stability and efficiency must be monitored during the Large Hadron Collider (LHC) operation (runs) using custom electronics. As the current TGC-Detector Control System (TGC-DCS) will be changed and the current Chamber Charge Monitoring Circuit (CCMC), which is part of it, will be replaced by the Charge Monitoring System (CMS). This system

represents a solution to monitor gain during runs for the forthcoming High Luminosity upgrade.

The Charge Monitoring System module is composed of one main board called Charge monitoring Board (CMB) and a data transfer system that will operate with the Embedded Monitoring and Control Interface (EMCI). The CMB will monitor the TGC output pulse shape for minimum ionizing particles (MIP). The analog pulses come from the analog output of the ASD boards (front-end board of TGC).

The data collected by a group of CMBs will be fed into the EMCI, which will pack the data and send it to an Embedded Monitoring Processor (EMP). This information will be available for the Detector Control System (DCS) for shifters.

The gain of each of the 3,408 detector chambers from the big wheels and the 126 detector chambers of the EIL4 TGCs can be monitored using the ASD board MO signals, with the TGC wires as inputs [9]. Only one such MO per chamber is enough to monitor the detector gain and serve as a diagnostic tool. The HL-LHC high luminosity will significantly increase the hit rate per channel. The ASD preamplifier baseline voltage will also be affected.

The CMB will trigger with individual MIPs, sample and digitize the MO pulse waveforms, register the peak and integrate the pulse to compute the input charge, pack the data and send it to a data concentrator. The concentrator will accumulate data and produce a histogram of measured charge for each of the 3,534 TGC detectors. The data concentrator will compute the mean, peak position, and RMS value from each histogram and transmit these values to the ATLAS Detector Control System (DCS) [11] on an hourly basis. Additionally, the CMB will be able to register and produce a raw, scope-like picture of a selected channel upon request. This sampled and digitized waveform can be packed and transmitted to the data concentrator, thus providing more information for diagnostics purposes.

The CMB uses the DRS4 chip, which is a switched-capacitor array working as a Domino Ring Sampler. The domino principle allows for sampling the triggered pulse shape in a 1[μ s] time window with a 1[ns] time slice (sampling period). The triggered pulse occurs in the middle of the time window. The pulse samples can be processed using the best-suited algorithm. One possibility is to filter the baseline during 100-400 [ns] before the pulse and use it for a pedestal (offset) subtraction to compute the signal using correlated double sampling. The pulse position could be calculated with a precision better than 1 [ns] and the pulse charge could be calculated in the 100-200[ns] time window by an integration of the pulse shape with the pedestal subtraction. This procedure's result is not affected by the time distribution of clusters [5] considering the integration time of the pre-amplifier shown in Fig. 3a. Another possibility is to use the digital correlated double sampling (DCDS) technique [6] to determine the optimal filter coefficients from the measured noise spectrum, and implement the filter algorithm in the FPGA. This novel technique deals with the baseline restoration and any other low-frequency noise component if the front end does not saturate. Background rejection is mandatory in a TGC monitoring system. The main background radiation components in the ATLAS muon spectrometer are neutrons and low-energy gammas. A coincidence scheme will be used to detect MIPs and veto other radiation components, as explained in section 9.3.1. of the TGC-CMS SPR.

4 Interfaces

The CMB interacts with the ASD-based circuit, through the ASD's monitoring output (MO) and with the EMCI through the E-Link. A diagram of these interactions can be seen in Fig. 1:

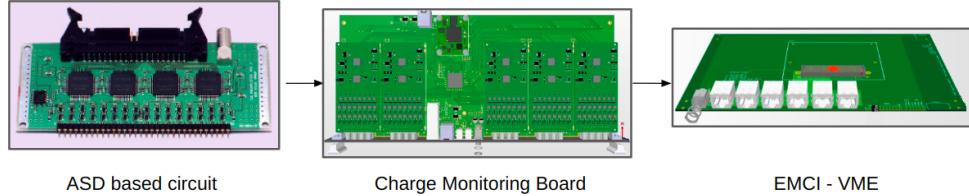


Figure 1: General connections block diagram

The CMB has 5 replaceable mezzanines that attach to the motherboard (each mezzanine can interact with up to 40 MO's from ASD's), a replaceable SoM, power connector, a communication interface to communicate with the EMCI board, SPI interface, JTAG interface and also 2 debugging purpose connector. The EMCI is attached to an EMCI carrier board (EMCI-VME). The charge monitoring board as well as the EMCI carrier board, are located in a mini rack as VME cardboards.

4.1 Electrical Interfaces

The connections between the ASD boards and the CMBs in the big wheels is done using coaxial cable with Lemo connectors arranged in bundles and routed to the mini rack where the CMBs are located. The connection of the coaxial cables to the CMB is done using double-channel Lemo sockets, which have an impedance of 50 Ohms suitable for this application. The connection between CMBs and EMCI boards is done through the so-called E-Link, enabled by the lpGBT ASIC [6], using the Cern Low Power Signaling (CLPS) standard.

4.1.1 CMB Front panel

The charge monitoring board front panel has 40 Lemo connectors, 1 SFP+ connector, 1 RJ45 connector, 2 MiniI/O connectors, and 1 barrel power connector. The description is shown in table 1.

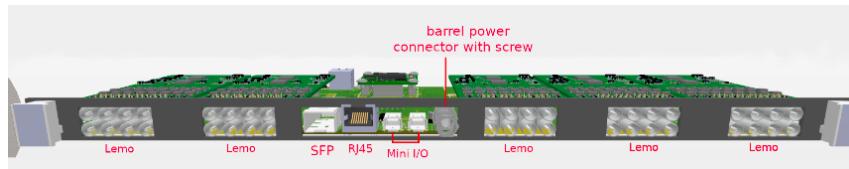


Figure 2: Front panel

Component name	Component specification	Connections to/from CMB
Double Lemo socket	LEMO connectors. (50 [ohm]) from ASD to Mezzanine board	TGC Front-end
RJ45 socket	RJ45 socket CAT5e 8p8c	EMCI-VME to CMB interface: UTP.
Power connector	Barrel with screw 11 [A]. Internal pin diameter of 2 [mm]. Barrel outer diameter 6.4 [mm]	From Crate power supply to CMB
SFP+	SFP connector	Can transmit using a optical transceiver
Mini I/O socket	8 pin socket TBD industrial Mini I/O F 8 POS 0.635mm Solder RA SMD 8 Terminal	Connection to satellite board to read the temperature of BW TGC via SPI protocol
Mini I/O socket	8 pin socket Mini I/O Mini I/O F 8 POS 0.635mm Solder RA SMD 8 Terminal	Connection to JTAG in CMB to program the firmware if necessary

Table 1: Front panel interfaces

4.1.2 CMB Back

The back of the CMB has an RJ45 socket for Ethernet connection which is used for debugging purposes. It is connected to the Processing System of the SoM to enable the transfer of data using TCP/UDP protocol.

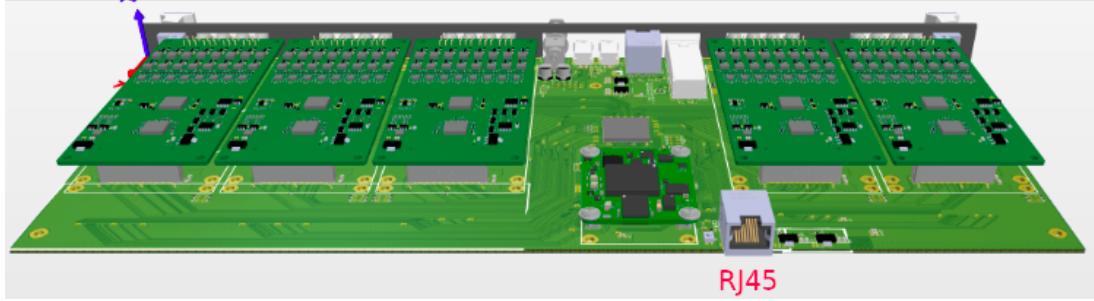


Figure 3: Front panel

4.2 EMCI carrier board

The EMCI [1] is installed as a mezzanine board in a different VME motherboard (EMCI-VME) as shown in figure 4. The EMCI is plugged into the EMCI-VME via an FMC connector. This EMCI-VME board is placed in the same crate as the CMB.

The EMCI-VME routes the E-Link signals from an FMC connector to six RJ-45 sockets located at the front panel. The front panel includes an MTP to MPO connector for the VTRx+ [13], DAC, ADC, and I2C connection interfaces. The connection between the EMCI-VME and the CMB will be implemented using standard UTP cable and RJ-45. Figure 4 shows the EMCI-VME board:

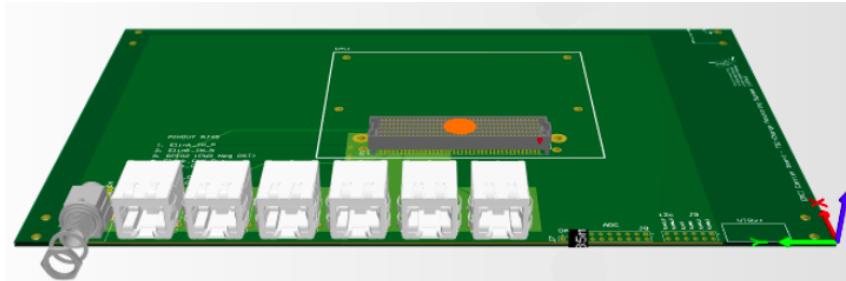


Figure 4: EMCI-VME board

The electrical signal for each of the RJ45 (using the T-568B standard) can be seen in figure 5:

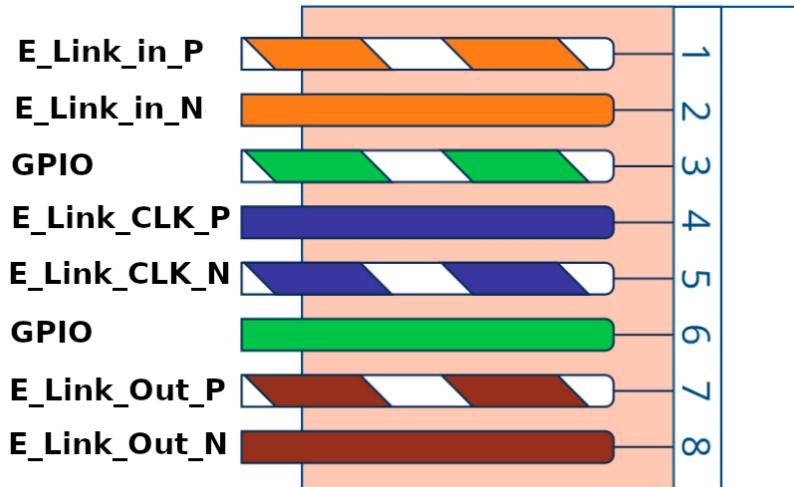


Figure 5: Electrical signals for EMCI and CMB communication.

As it can be seen from figure 5, each of the 6 RJ45 connectors is implemented having 3 pairs of differential signals for differential communication: E_link_out_P E_link_out_N, E_link_in_P E_link_in_N, and E_link_clk_P E_link_clk_N. Each pair of differential traces have a differential impedance of 100 [ohms]. There is also an indication of this pin assignment at the top of the board.

The connection for DAC interface has 2 pin header places: 1 signal pin, and a ground pin; The ADC connection has 16 pins, The signals are single-ended, and correspond to the ones shown in table 2.

pin	function
1	ADC_0
2	GND
3	ADC_1
4	GND
5	ADC_2
6	GND
7	ADC_3
8	GND
9	ADC_4
10	GND
11	ADC_5
12	GND
13	ADC_6
14	GND
15	ADC_7
16	GND

Table 2: EMCI-VME ADC pins

The I2C interface has 12 single-ended pins. The signals correspond to the ones shown in table 3.

pin	function
1	I2C Master SDA 1
2	GND
3	2C Master SCL 1
4	GND
5	I2C Slave SDA
6	GND
7	I2C Slave SCL
8	GND
9	I2C Master SDA 0
10	GND
11	I2C Master SCL 0
12	GND

Table 3: EMCI-VME I2C pins

All of these interfaces arrive at a High Pin Count (Vita 57.1 HPC) connector. This HPC connector has 400 pins and realizes the connection between the input/output of the EMCI-VME board and the EMCI. The pinnout of this connection can be seen in figure 6

	K	J	H	G	F	E	D	C	B	A
1	GND		GND		GND	GND	GND	GND	GND	GND
2	GND		GND		GND	GND	GND	GND	GND	GND
3			GND		GND		GND	GND	GND	GND
4			GND		GND		GND	GND	GND	GND
5			GND		GND		GND	GND	GND	GND
6	GND		GND		GND		GND	GND	GND	GND
7			GND		GND		GND	GND	GND	GND
8	GND		GND		GND	i2c slave SCL	GND	GND	GND	GND
9			GND		GND	i2c slave SDA	GND	GND	GND	GND
10			GND		GND		ADC 0	GND		
11			GND		GND		ADC 1	GND		
12	GND		GND		Gpio 7		GND	GND	GND	GND
13			GND			GND	GND			
14	GND		GND		Gpio 8	GND	i2c master SCL 0	ADC 2	GND	
15			GND		GND		i2c master SDA 0	ADC 3	GND	
16	GND		GND		Gpio 9		GND	GND		GND
17			GND		Gpio 10	GND	i2c master SCL 1	ADC 4	GND	
18	GND		GND		GND		i2c master SDA 1	ADC 5	GND	
19			GND		GND		GND			
20	GND		GND		GND		Gpio 1	GND		GND
21			GND		GND		Gpio 2	GND		
22	GND		GND		GND		GND	ADC 6	GND	
23			GND		GND		Gpio 3	ADC 7	GND	
24	GND		GND		E link CLK P5	GND	E link CLK P6	GND		GND
25			GND		E link CLK N5		E link CLK N6	GND		GND
26	GND		GND				GND	GND		
27			GND				Gpio 5	DAC		
28			E link IN P5		GND		Gpio 6	GND		
29	GND		E link IN N5		GND		GND	GND		
30	GND		E link CLK P2		E link OUT P1	GND			GND	
31	E link OUT P2	E link CLK N2	E link OUT P5	E link OUT N1	E link OUT P6				GND	
32	E link OUT N2	GND	E link OUT N5	GND	E link OUT N6	GND			GND	
33	GND	E link OUT P4	GND		GND		GND	GND		
34	E link OUT P3	E link OUT N4	E link IN P1	Gpio 11					E Link In P6	
35	E link OUT N3	GND	E link IN N1	GND	Gpio 12	GND			E Link In N6	
36	GND	E link CLK P3	GND		GND		5 [V]	GND	E Link In P3	GND
37	E link CLK P1	E link CLK N3	E link CLK P4	E link IN P4		GND		5 [V]	E Link In N3	GND
38	E Link CLK N1	GND	E link CLK N4	GND	E link IN N4	GND		GND	E Link In P2	
39	GND		GND		GND		GND	GND	E Link In N2	GND
40		GND		GND		GND		GND		

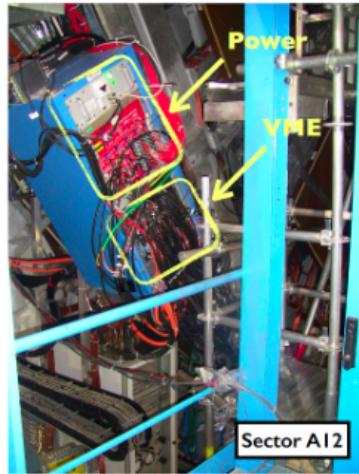
Figure 6: Vita 57.1 HPC pinout

4.3 Mechanical Interfaces

The CMB will mechanically comply with the VME standard. The board is a 9U short version of 160mm. Figure 7 shows the VME crate inside the blue mini rack.

Minirack

24 miniracks in the full TGC system 3/10



Power modules will be replaced
at the Phase II upgrade, but
exactly same space will be needed.

The VME crate will remain.
The boards in the VME crates
will be replaced. The number of boards
for Phase II is smaller than Run 1-3,
and 5 slots could be used for Ch Mon.
Note: the crate is special (see next page).

Figure 7: Blue mini rack where the CMB will be installed. The CMBs will be inserted as VME cardboards. The slide is shown by the Japanese group at <https://indico.cern.ch/event/977581>

For the EIL4 TGC case, the rack mentioned above will have the same characteristics as those present in the mini rack.

The board has 37 x 3,2 [mm] size holes for screw placement. 30 of these are for placing the mezzanines, 4 for the SOM, and 30 for the general board. In figure 8 the dimensions and hole location of the board can be seen:

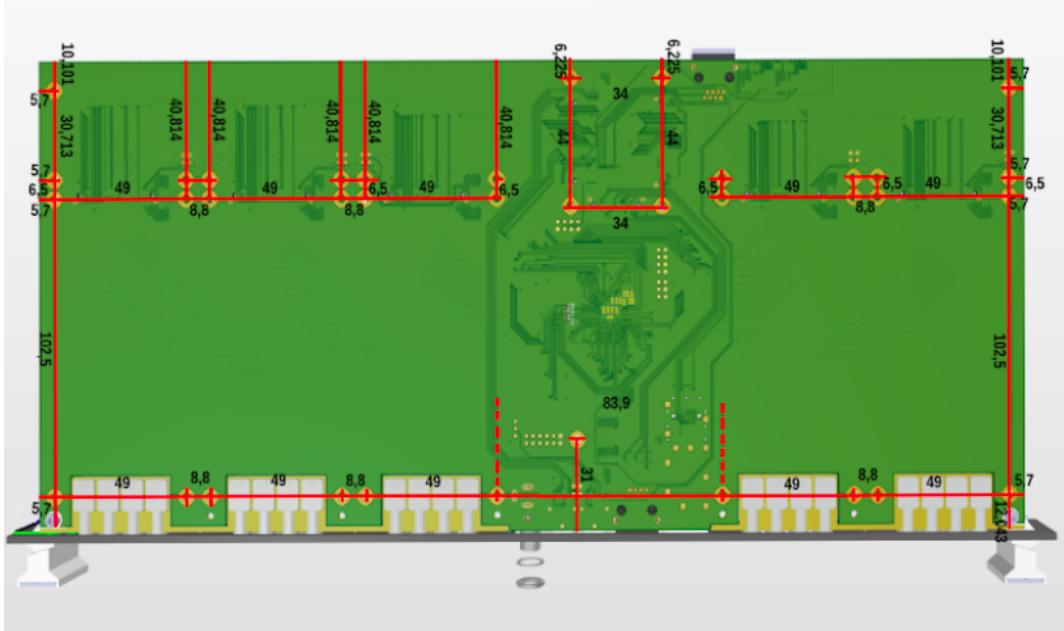


Figure 8: Mechanical dimensions of the board

5 Physical Description

The CMB corresponds to a 160,0 [mm] x 366,7 [mm] PCB board. It is composed of 5 mezzanine boards, one SOM a CPLD, and input and output connectors. Each mezzanine corresponds to a 115 [mm] x 55[mm] board, the SOM corresponds to a 50[mm]x40[mm] PCB board.

The CMB assembly is composed of 7 PCBs: One main board (CMB Motherboard) to which five DRS4-based boards (8-channel mezzanine boards) and one commercial SoM Zynq system are connected. Therefore, each CMB has a maximum of 40 analog inputs to be monitored. A connection diagram can be seen in Figure 35. The DRS4 sampling and digitizer board, and the SoM Zynq board will be connected to the main board using Samtec Razor Beam connectors.

Considering the available space, one CMB can be placed in a single VME slot. Thus the maximum board assembly thickness is restricted to 20 mm and the board thickness is limited to 1.6mm. The width corresponds to a standard 9U, and the length is 160mm. Figure 9 and 10 shows a model of the board:

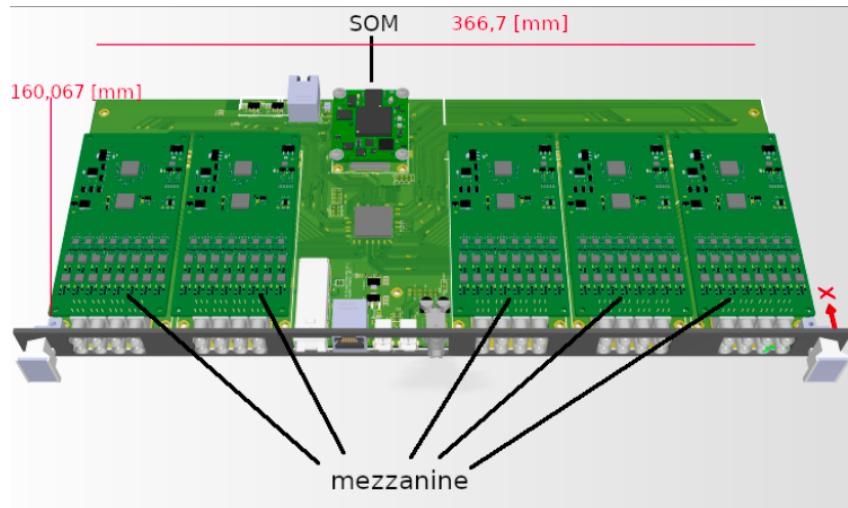


Figure 9: Physical top

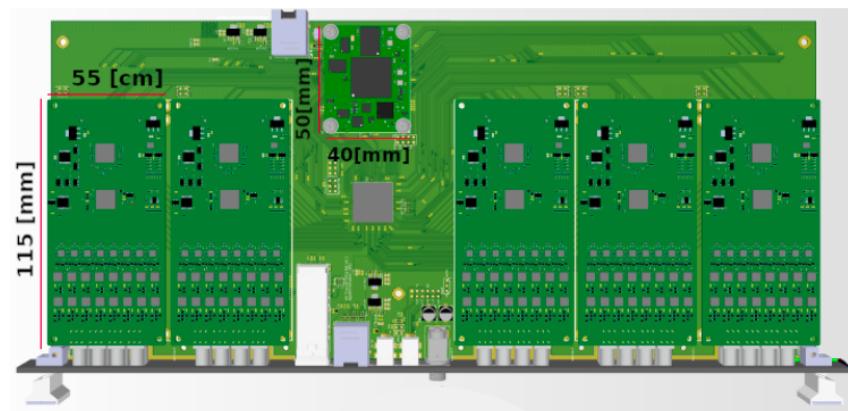


Figure 10: Physical description top view

The front panel corresponds to a 418[mm]x 20 [mm] aluminum panel, with 2 plastic pins at each side to dismount or move the panel:

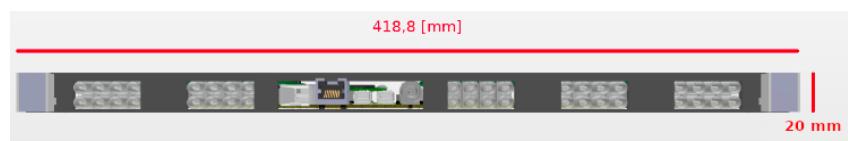


Figure 11: Physical description front view

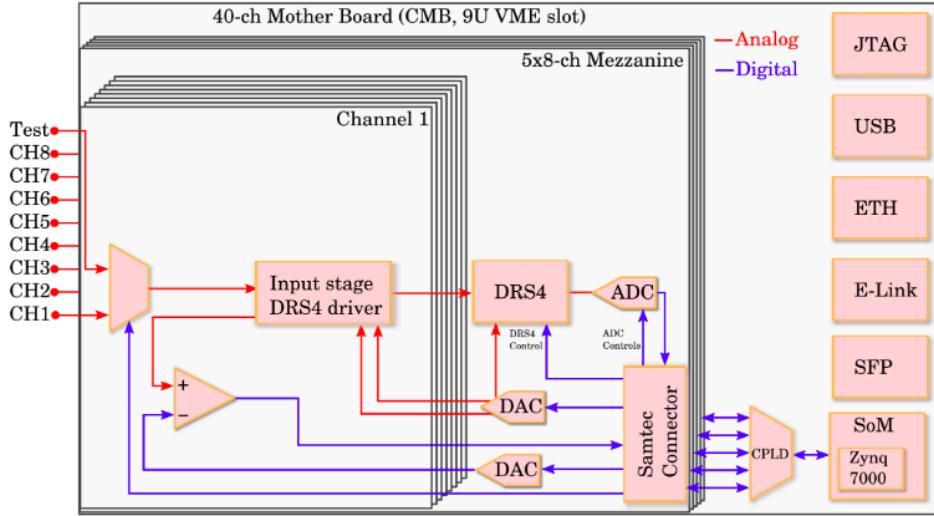


Figure 12: 40 channels CMB connection diagram

5.1 Physical Location

The physical location where the CMB will be placed corresponds to the big wheel miniracks, and also EIL 4 miniracks, this can be seen in the SPR document [2]. For reference, in figure 13 the mini racks where the CMB and VME are placed can be seen.

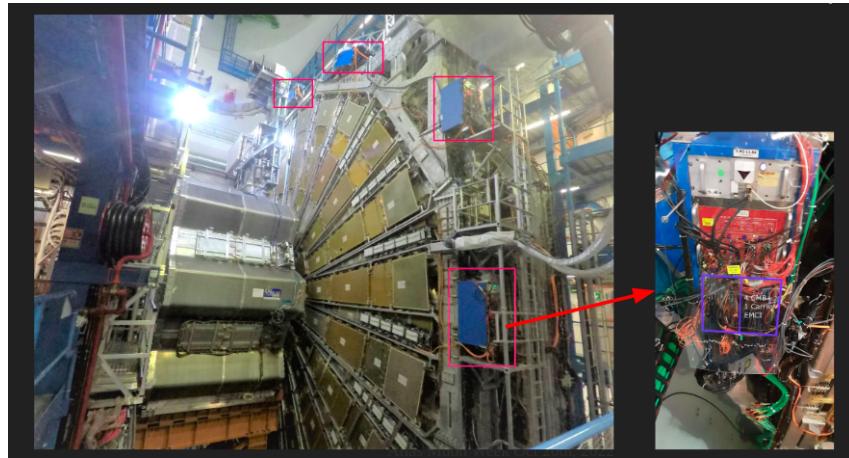


Figure 13: Location of mini racks where CMB and VME-EMCI are placed in UX15.

6 Firmware (V. Arredondo)

Charge Monitoring Board will use Xilinx *Vivado* as IDE for developing the firmware to use the SoM Trenz Te0715 and its peripherals, and *Lattice Diamond* for the program the CPLD. The language that will be used is VHDL. The CPLD will be used as a multiplexer, where 39 digital signals from each mezzanine will be selected from SoM using 3 pins called

Mux_sel. Other signals that cannot be multiplexed, the trigger and the digital signal to stop the acquisition on the DRS4, will be directly connected to the SoM where the main firmware is programmed. The communication with other systems will be via a differential signal with an RJ45 socket for the Elinks located in the Programmable Logic.

The description of the electrical signals is shown in Fig. 14. Other peripherals such as SFP+, RJ45 rear connector, and USB are not taken into account in the main firmware as they will only be used for debugging purposes.

The following subsection describes in general the main blocks of the firmware.

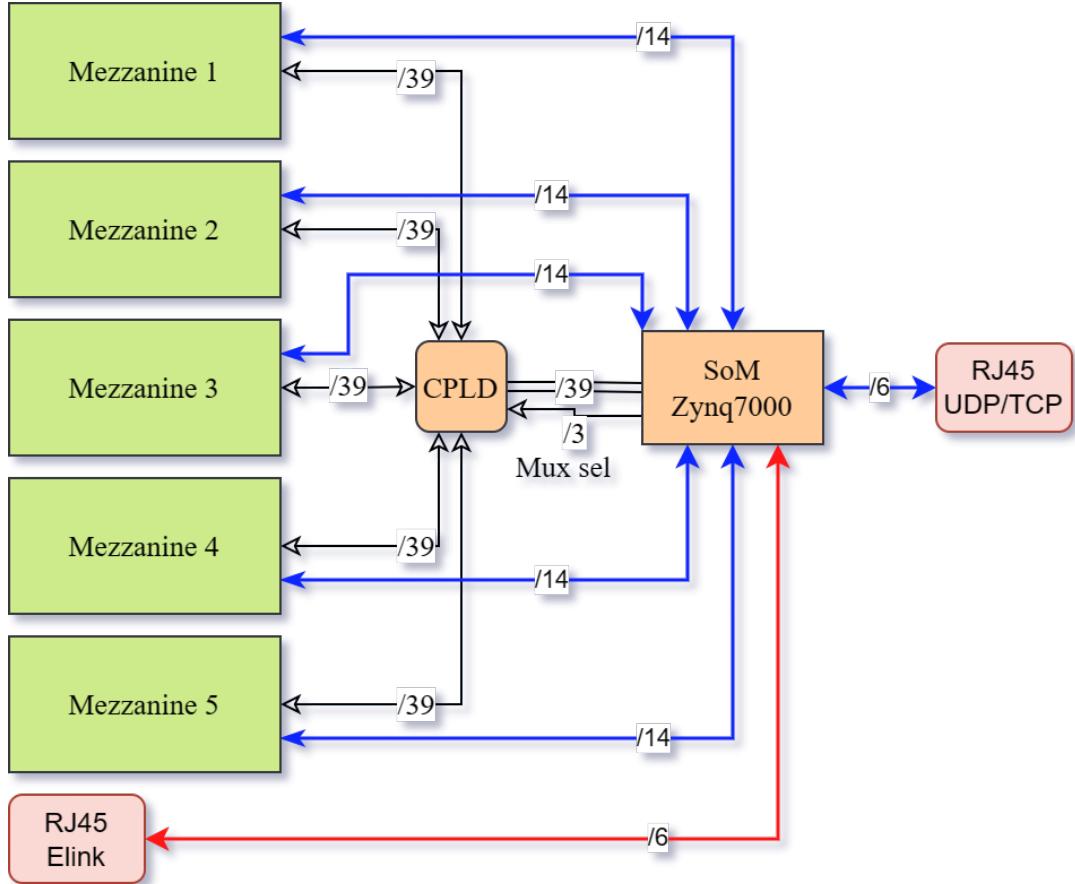


Figure 14: Firmware: Digital signal diagram.

6.1 ADC readout

The ADC used is soldered on the mezzanine board. The ADC is controlled by SPI protocol communication, which is programmed by the SoC, the SPI bus is connected to all mezzanines. The current model of the ADC is Texas Instrument ADS5296.

The ADC outputs are differentials standard LVDS18. The SoC IO pins for all the banks are 2.5 [V] which is compatible with the differential signal output of the ADC. Figure 15 shows the block design of the firmware of ADC. There are 3 main blocks.

- ADC input buffer: This block instantiates LVDS input buffers for all the input pins from SoC connected to the LVDS digital outputs of the ADC.
- ADC serdes and readout: This block readout the LVDS signal and convert it to the 16-bit digital output of each channel. Also, control the ADC modes with the SPI bus.
- Mapper: Convert the 16-bit signal to 12-bit digital signal that is the actual bit length of ADC.

The clocks inputs of the ADC readout firmware are the following:

- LCLK :Bit clock from ADC. 6 times the input clock frequency of the ADC that is the same as the DRS4 readout clock (SRCLK).
- ADCLK:Frame clock of ADC. Same frequency as the DRS4 readout clock (SRCLK).
- PSCLK: Internal clock of the SoC, generated by a controlled oscillator at the TRENZ board. The frequency is 100 Mhz.

The output of the Mapper block is connected to the RO_Controller block. This RTL block will control when to store the data in the ADC FIFO based on the trigger logic. The diagram of this process is shown in figure 16. The data stored in the FIFO will be analyzed and sent to the communication protocol. In the diagram is implemented UART communication protocol that sends the full waveform acquired by the DRS4.

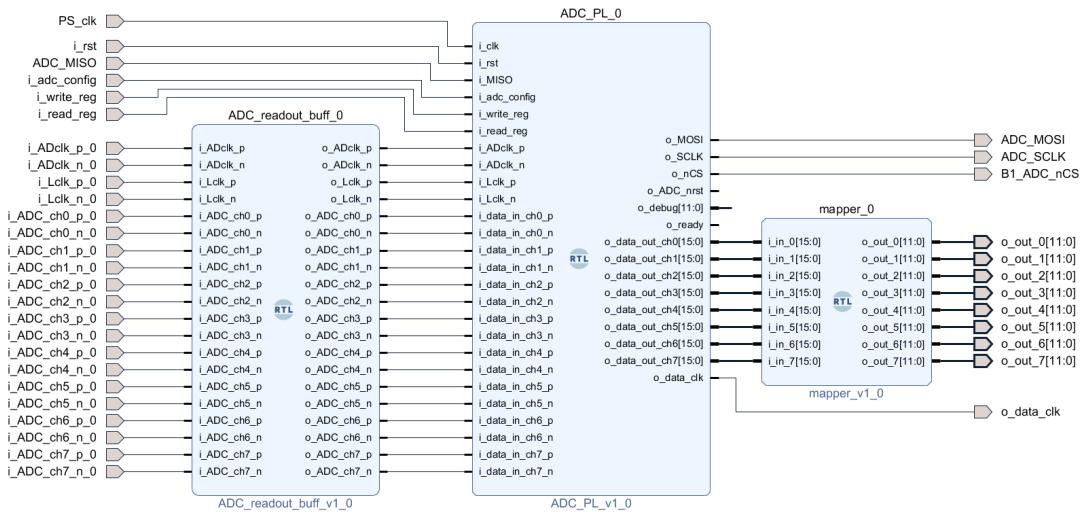


Figure 15: ADC schematic firmware block design in Vivado

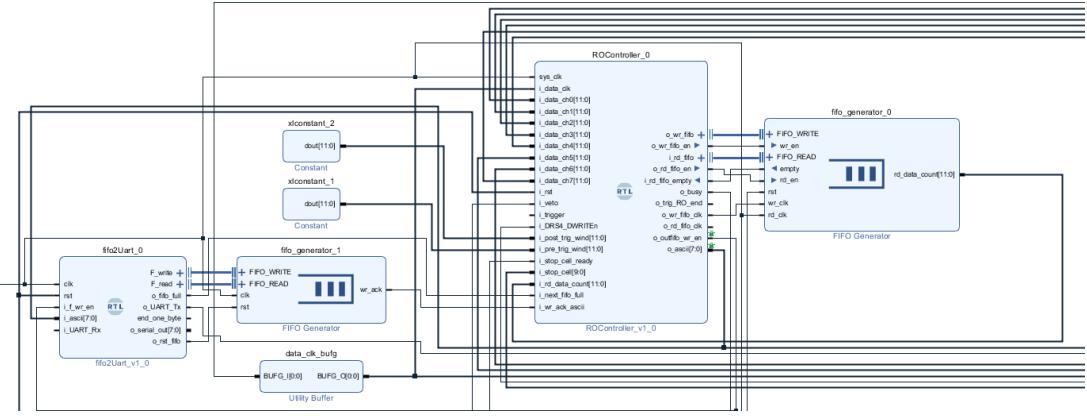


Figure 16: Readout controller block design in Vivado

6.2 DRS4 IC control firmware

The firmware of the DRS4 will control the IC readout to start or stop the Domino ring sampling cells, change the sampling frequency, change the readout frequency, choose how many cells will be read and the operation modes of the DRS4 that can be accessed with the control signals.

The input signals of the RTL block are described below:

- clk: Input clock for the logic of the block design. The actual is 50 MHz.
- read shift reg init: Bit to initiate the shift register load at the DRS4.
- conf register init: Bit to initiate the register initialization of the DRS4.
- start ROI : Bit to enable the region-of-interest mode of DRS4, the actual mode that is used in the readout.
- full readout start: Bit to enable full readout of DRS4.
- refclk counter: 7-bit signal counter to choose the sampling frequency of the DRS4. The function is

$$refclk = \frac{clk * 1024}{F_{sampled}}$$

For example, with 50 MHz clk and to sampled 2 GSPS, the refclk counter will be 25.

- cell counts: 12-bit input to determine the number of cells to be read in the ROI mode. From 0 to 1023.
- config states: 3-bit input of the config states that are sent to the DRS4 in the conf register init.

- trigger delay count: 8-bit input to choose the delay since the input trigger arrives. Each count is 2 ns approx.
- SROUT: Signal from DRS4 that represents the cell number when the sampling ring stop.
- PLLKC : Digital signal, when high the internal PLL of DRS4 is locked. Actually is not very representative since can be high even if the DRS4 is not locked.

The output signal description is described below:

- o_A3_0 : 4-bit control signal that enables different modes at DRS4.
- o_sclk : Readout clock of DRS4. The main use is when is enable the differential analog output of DRS4 to be read by the ADC.
- o_srin : Shift register input that determine initial configuration of the DRS4 based on 3 bit the input i_config_states.
- o_rsrload : Read Shift Register Load Input, signal that it is loaded one time to indicate where is the cell number 0.
- o_nReset: Negedge reset for DRS4.
- o_denable: Enable signal for DRS4 chip.
- o_dwrite: Stop adquisition on DRS4 when is low.
- o_refclk: Reference clock of DRS4 chip, indicates the sampling frequency using the relation : $F_s = 2048 * refclk$
- o_drs4_states_vector: For debugging purposes, indicates the states of the SM of the RTL.
- o_stop_cell: Indicate the number of the cell when the DRS4 stops sampling and starts the readout. This allows identifying each cell to apply common mode voltage correction.
- o_stop_cell_ready: Flag that indicates when to read the o_stop_cell.
- o_srclk_test: Clock with the same frequency of SRCLK but it is always running. The use is for the reference clock of the ADC.
- o_dwrite_for_trigger: Signal dwrite to the readout logic of the ADC.

An example of the DRS4 initialization sequence is shown in figure 17. The initial configuration shows that BIT 0,1 and 2 of SRIN is high. This means that the Domino ring will run in continuous cycling, enable the pin of PLLCLK and enable the loop of WSROUT to WSRIN.

A description of how the block of DRS4 and ADC should be used is described on figure 19.

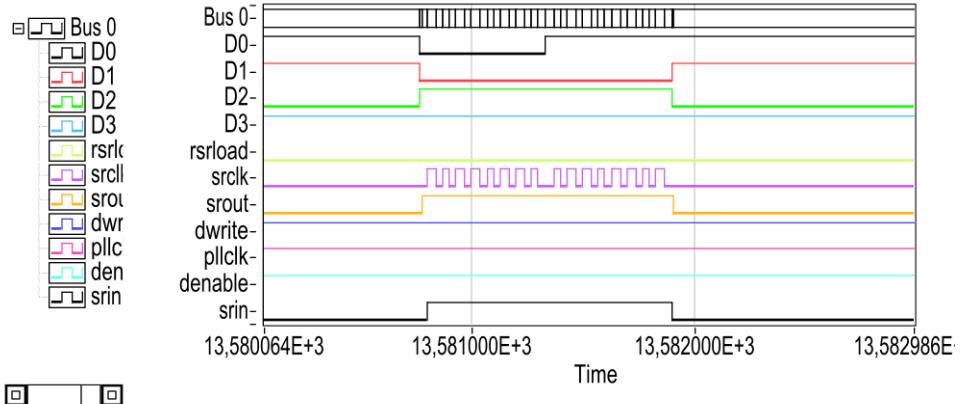


Figure 17: DRS4 initial sequence

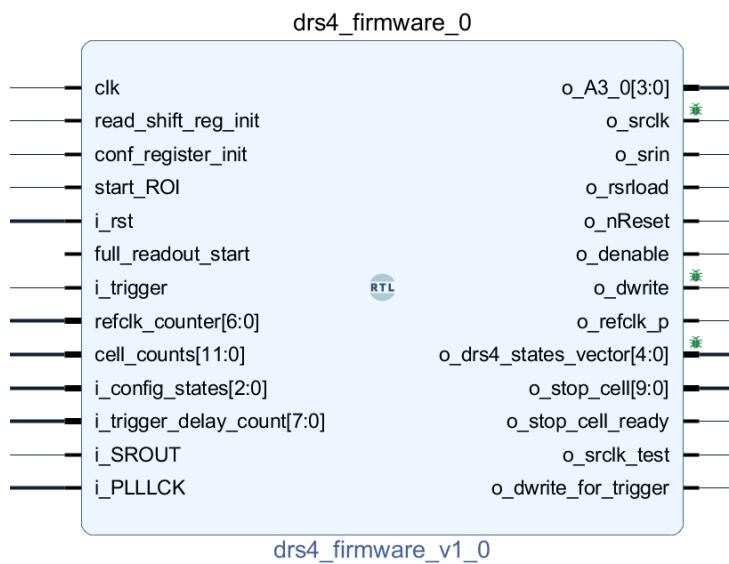


Figure 18: DRS4 firmware block design in Vivado

6.3 CPLD communication

The CPLD will be mounted in the motherboard and work as a digital multiplexer between the signal from each mezzanine to the SoM. Each motherboard can manage up to 5 mezzanines, and each one has 46 digital signals, of which 39 can not be shared between mezzanines.

The communication between the SoM and CPLD will be using 3 IO pins from SoM to the CPLD called *Mux_sel*. In the CPLD the ball pin is C13, E13, and D13. These pins will represent which signals from a mezzanine board will be connected to the SoM. The connection is shown in table 4 and a schematic representative of the CPLD firmware is shown in figure 20.

The CPLD model *LCMXO3D-9400HC-6BG484I* will be flash programmed using Lattice Diamond software. The preliminary amount of resources is shown in table 10.1.2

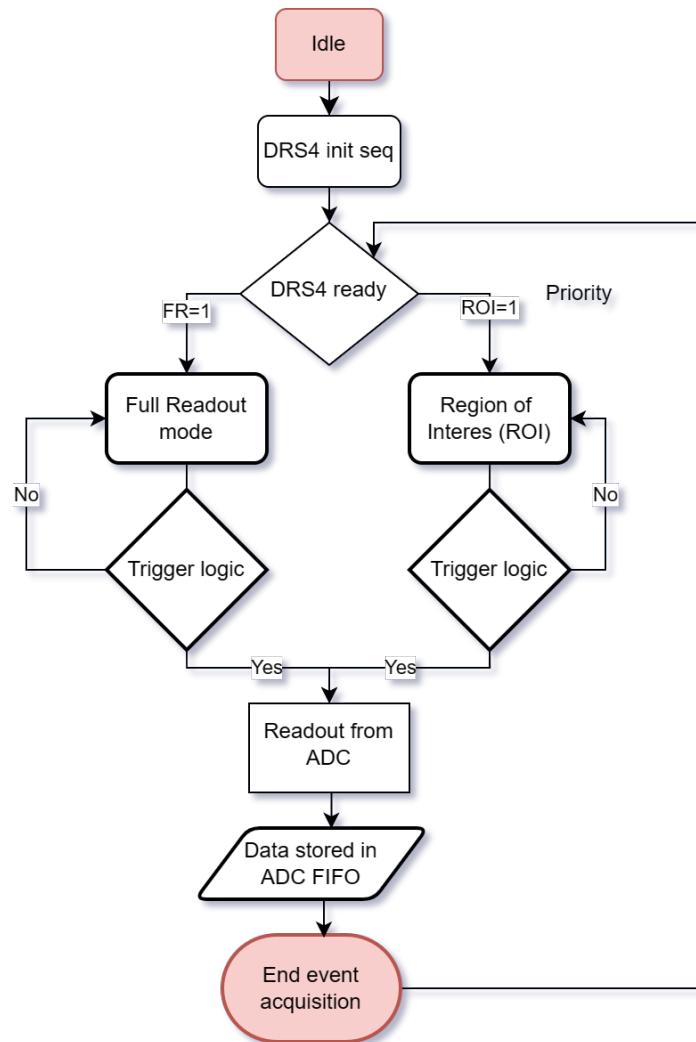


Figure 19: Diagram of signal acquisition control logic

without TMR at the logic.

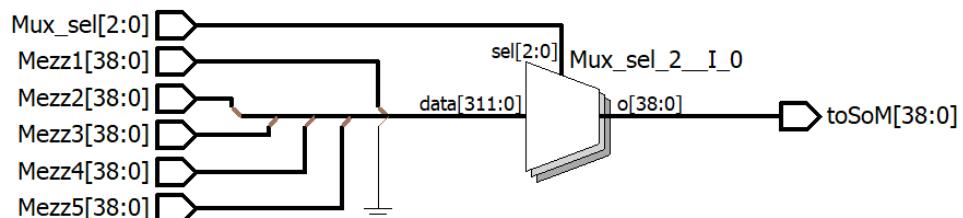


Figure 20: CPLD firmware schematic.

Mux_sel[2:0]	Mezzanine active
000	none
001	Mezz 1
010	Mezz 2
011	Mezz 3
100	Mezz 4
101	Mezz 5

Table 4: Mux_sel IO pins from SoC to CPLD to select digital signals from the Mezzanine board.

Number of registers:	0 out of 10552 (0%)
PFU registers:	0 out of 9400 (0%)
PIO registers:	0 out of 1152 (0%)
Number of SLICEs:	59 out of 4700 (1%)
SLICEs as Logic/ROM:	59 out of 4700 (1%)
SLICEs as RAM:	0 out of 3525 (0%)
SLICEs as Carry:	0 out of 4700 (0%)
Number of LUT4s:	118 out of 9400 (1%)
Number used as logic LUTs:	118
Number used as distributed RAM:	0
Number used as ripple logic:	0
Number used as shift registers:	0
Number of PIO sites used:	237 + 4(JTAG) out of 384 (63%)
Number of block RAMs:	0 out of 48 (0%)
Number of GSRs:	0 out of 1 (0%)

Table 5: Design Summary of CPLD firmware.

6.4 DAC control

Each mezzanine will use two DAC model 7678 from texas instruments. This IC uses an i2C communication protocol and is shared between all the mezzanines, using a CS (chip select) to enable or disable which the communication data flow.

The first DAC will control the voltage of the comparators mounted in the mezzanines, which select the voltage level for a trigger connected to the analog signal. The second DAC will control the voltage reference control for the ADC and the DRS4, some signal determines the common mode voltage.

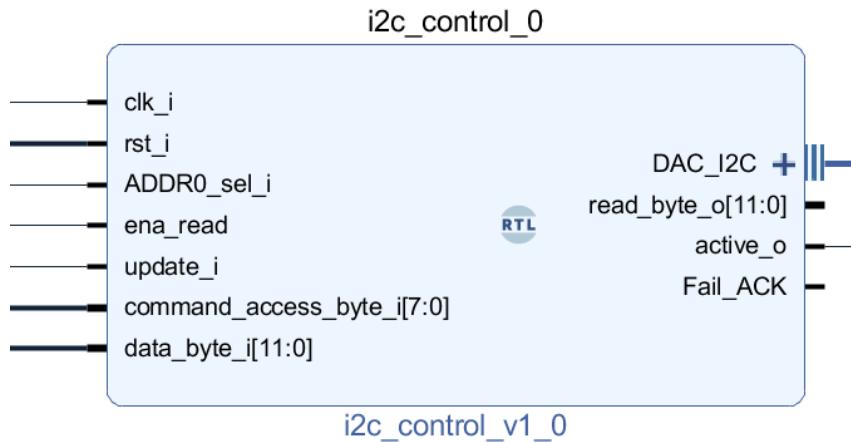


Figure 21: i2c block design to control the DAC at mezzanines.

The description of signals of the block are described below:

- clk_i Clock from the Processing system, 100 MHz
- rst_i: rst signal
- ADDR0_sel_i: Bit to select the address bit register of the DAC 7678.
- ena_read: Enables the read from SDA IO pin
- update_i: Indicate when to send data using i2c.
- command_access_byte: 8-bit word that indicates operations based on the documentation of DAC7678
- data_byte_i: 12-bit input that indicates the level of voltage of the DAC.
- DAC_I2C : Bidirectional signal of i2c standar.
- read_byte_o : Read a byte from the DAC 7678.

6.5 Full waveform readout

The full waveform readout will send the data taken from 1147 samples of every channel from the ADC. The main communication protocol will be the Elink interface for the lpGBT. The current implementation can use TCP/UDP protocol on the Processing System (PS) or UART transmission on the Programmable Logic (PL).

The implementation configures the sample rate of DRS4 and ADC and the trigger logic can be implemented in different forms.

The block design can be seen in Fig. 47, where the design is using UART to send the full waveform of 8 channels from a mezzanine. The resource utilization is shown in table 6. It must be considered that Triple Memory Redundancy (TMR) will be applied to the next firmware version, which will increase the total resources.

Resource	Utilization	Available	Utilization %
LUT	5356	46200	11.59%
LUTRAM	261	14400	18.1%
FF	5234	92400	5.66%
BRAM	13	95	13.68%
IO	50	150	33.33%

Table 6: Resource utilization of full waveform readout using UART

7 Manufacturer

All components will operate in a radiation environment; thus, all COTS must be certified to be radiation-tolerant at the level specified in section 10. The main COTS components in the boards are described in Tab. 7. The CMB prototype PCBs were fabricated by a trustworthy company and then the components were soldered in Chile

Component	Manufacturer	Comments
DRS4	RADEC.ch	According to the manufacturer, the IC has been tested for radiation tolerance by our group.
ADC	Texas Instrument	ADC speed must be at least 30MSPs to match the readout speed of DRS4, 8 channel differential input, common mode voltage of 0.95 [V], and with a 10-bit resolution.
Differential Op Amps	Texas Instrument	An analog bandwidth of 200 MHz is enough to sample the ASD pulses, THS4509RGTR has been tested at CHARM. .
SoM	Trenz	The SoC inside SoM is a Zynq-7000 from Xilinx, well known for being radiation tolerant. Other components on the SoM board will be tested for radiation tolerance.
Voltage regulators	Texas Instruments and Microchip Technology	Several COTS ICs have been tested under radiation and reported in the literature. The CMB will use qualified components.

Table 7: Principal Components and manufacturers.

8 Power

The CMB operates with 5 V. The CMB will include LDOs to generate the operating voltages from the 5 V input, which were properly chosen to be radiation tolerant [7, 5]. The power for the CMB will be provided, for each Minirack or EIL4 rack, by one channel of the existing power supply modules during the run. The module should be renewed during the run-4/run-5 shutdown and the corresponding module will be purchased for the CMB. This interconnection was reviewed in a dedicated meeting [3]. The 5V value was chosen for compatibility between CMB, EMCI, and other components. Tab. 8 shows the expected power requirement for a single CMB and the expected power requirement from the power supply in both the mini rack for the BWs and the rack of EIL4. It's worth noticing that the chosen CMB topology uses a multiplexer to select one of the five mezzanines in the CMB to be read at a time. It means that the power requirement can be significantly reduced if only one mezzanine board is powered on and read out at a time. The available GPIO signals from the EMCI board will be used to reset the board power, see Fig. 5. The power modules installed for run 4 already meet the requirements

Name	Max/Nom/Min V Supplied (V)	Nom/Max I for Voltage Source (A)	Power Requirements (W)
CMB	6/5.0/4.0	6/7	35
Minirack BW (4 CMBs + 1 EMCI)	6/5.0/4.0	25/29	145
Rack EIL4 (2 CMB + 1 EMCI)	6/5.0/4.0	14/16	80

Table 8: Power specifications

of Tab. 9 and the ones that will be installed for run 5 should also meet these minimum requirements which include a 35% tolerance for the minimum current and thus the power.

Name	Min V Supplied (V)	Min I for Voltage Source (A)	Min Power Requirements (W)
One channel per minirack in BW	5	30	150
One channel per EIL4 Rack	5	15	75

Table 9: Power modules requirement.

9 Prototypes Development

9.1 Mezzanine board

For the mezzanine board, a PCB was already designed and manufactured by PCBCart company. This board was tested and worked properly according to the requirement of the system. Figure 22 shows the PCB already tested at CHARM successfully.

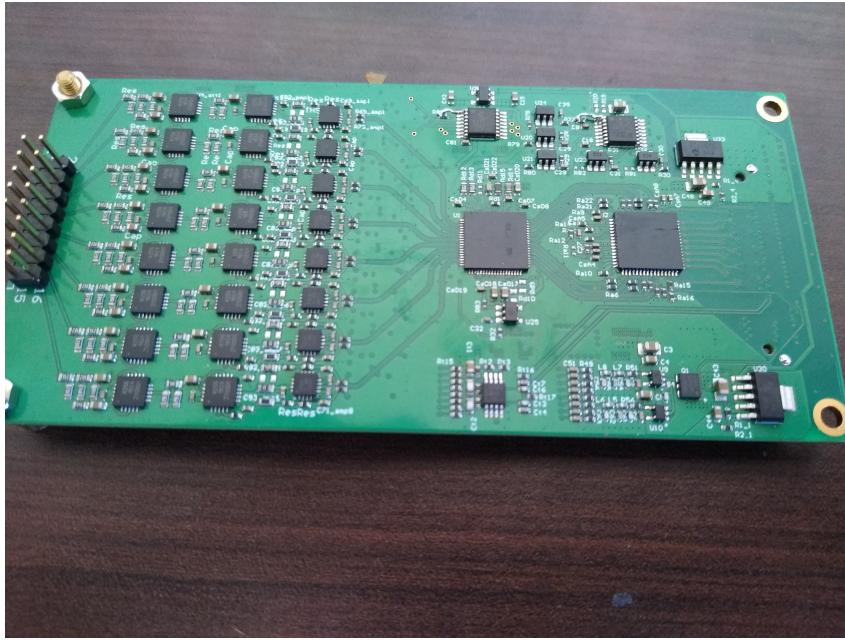


Figure 22: Mezzanine board assembled.

The new design of the mezzanine will include compatibility with other components, such as LDO and ADC that are currently out of stock a global level. This will be done by merging the footprint of some devices.

Also, the new model will include holes to add a test socket. This way we can test DRS4 and ADC IC before solder to be sure that the Mezzanine works properly and this way takes care of the low availability of these IC. Figure 23 shows the design of the board.

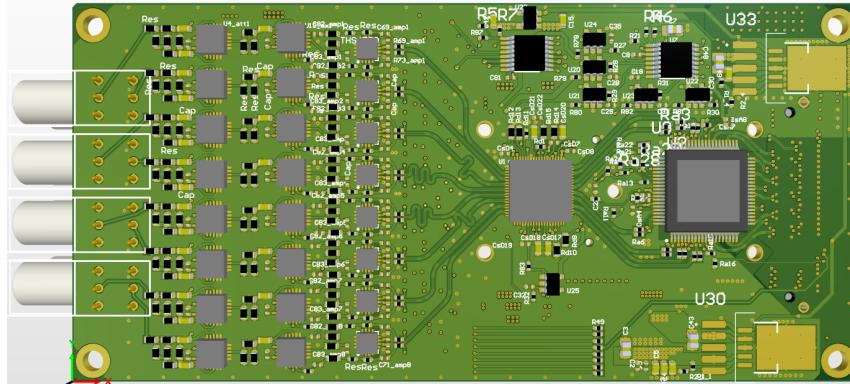


Figure 23: New version mezzanine board, 3d model.

9.2 Motherboard for two mezzanines, 16 channels

The first prototype with the capability to control two Mezzanine boards was produced and tested already. This prototype was also tested with mezzanines in a radiation environment at GIF++, CCHEN (Chili), and CHARM. Figure 24 shows the PCB assembled with one mezzanine and the SoM mounted on it.

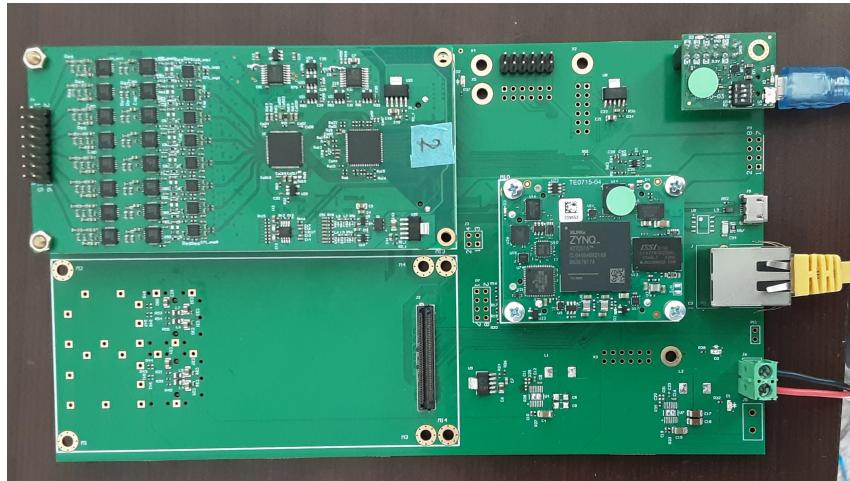


Figure 24: Prototype motherboard up to 2 Mezzanine connections.

10 Testing, validation, and commissioning

- The PCB design validation, including temperature, power supply levels, switching, and signal timing, will be carried out at CERN as well as in Chile.
- The PCBs will go through a quality control process carried out by the manufacturing company.
- Radiation tests were done in the CHARM facility and are described in the subsection 10.1.

	TID Gy	NIEL	SEE (T>20MeV)
<i>SRL</i>	4.1	1.1E+11	1.6E+10
<i>SF_{sim}</i>	1.5	2	2
<i>SF_{ldr}</i>	5	1	1
<i>SF_{lot}</i>	4	4	4
RTC	123	8.8E+11	1.3E+11

Table 10: Radiation levels required

- The final CMB functionality test will be done by us using an ASD circuit and an analog signal generator.
- Validation of the communication with the EMCI card will be performed by the Chilean cluster using the open-source IP CORE of lpGBT for Elinks down and upstream, and an EMCI board provided by the EMCI-EMP team at CERN. The optical link from EMCI will be connected to a board with an optical transceiver with an FPGA that will control the reception and transmission.
- The LEMO cable extensions to the mini rack must be installed at the beginning of the LS3 and should be done coherently with the other TGC front electronics replacement.
- There are power supply channels available for the Charge Monitoring systems during run 4 reviewed in section 7.
- For run 5 the power supply modules will be replaced by new modules and the new modules should meet the given requirements given in Table 7.2.

10.1 Radiation Tests

The main tests were done in the CHARM facility at CERN [12]. This facility has a radiation environment that includes a mixture of particles similar to the ones that ATLAS will produce, this allows us to make a comprehensive test. We carried out three different irradiation campaigns, with the aim of reaching the radiation levels required in Tab. 10.1 and beyond. No isolated component testing was performed except for the CPLD.

The critical components of the system are DRS4, ADCs, and DACs for the Mezzanine; the CPLD for the Mother Boards; the ARM and Artix-7 FPGA inside the Zynq Z-7015 of the SoM.

10.1.1 Campaign 1

The DUT was the 16 channels CMB which includes one Mezzanine (8 channels), and one SoM TE0715-05-52I33-A. During the runs, we tested the DRS4, ADCs, DACs, and the SoC Zynq Z-7015 within the SoM TE0715-05-52I33-A, besides the LDO

regulators and other components that are in the CMB. The DUT was positioned in the CHARM facility's overhead conveyor, and the tests were done from May 25th to June 6th, the complete beam time during the test is shown in Fig. 25.

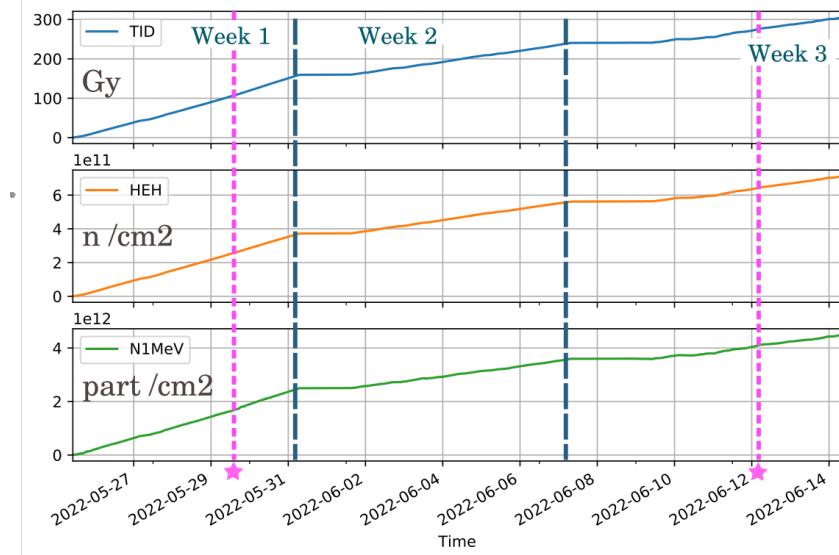


Figure 25: Beam during the first campaign. The stars indicate non-recoverable failures.

Experimental setup

We injected 5MHz sinusoidal signals from the signal generator into the DUT, then the DUT digitalized them and sent them back through an RS485 bus to the control room PC. In parallel, we measured the total current consumption and the ability to power cycle the entire system in case of failure. Photos of the DUT and the control room are shown in Fig. 26, and the connection diagram is shown in Fig. 27. Due to the limitation of the communication bus (UART over RS485), we performed acquisitions every 10s.

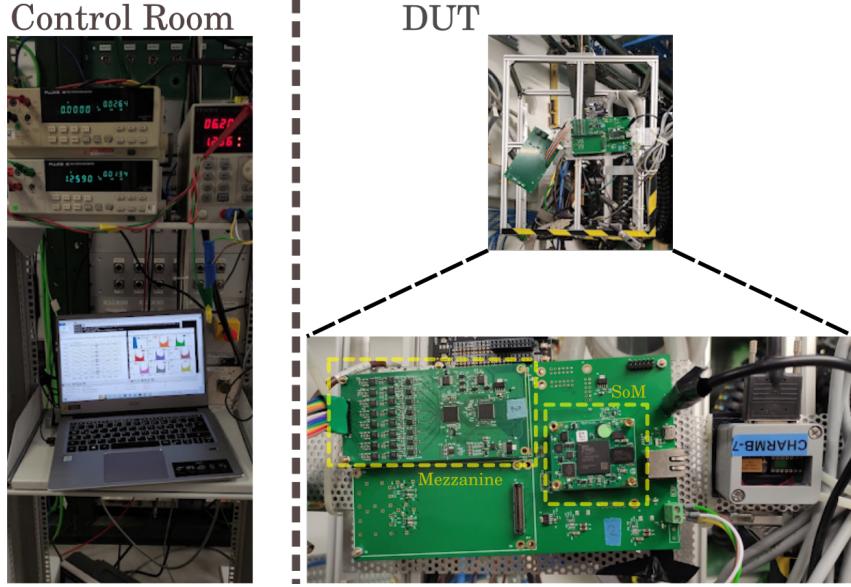


Figure 26: Photos of the DUT and the control room setup

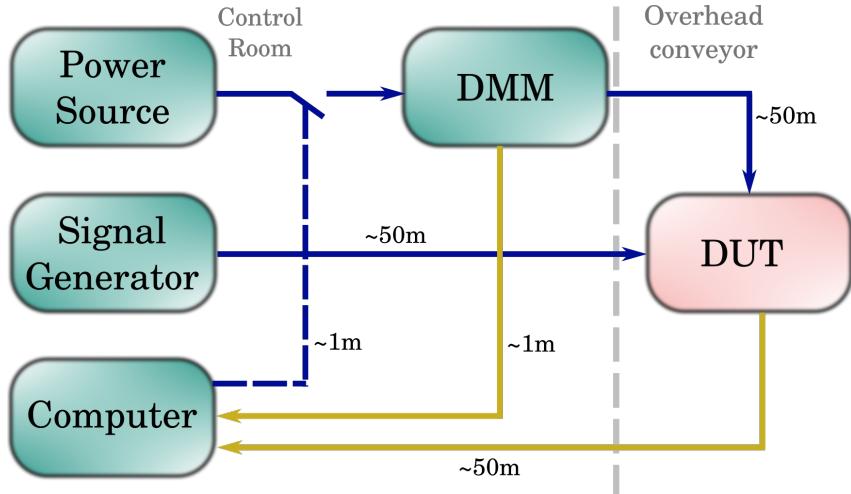


Figure 27: Connection diagram for the first irradiation campaign

Firmware used

The firmware for the test was designed using the main components of the final application, these are the digitalization of the input signal at the highest rate possible and the use of a FIFO queue for the data transmission. The communication was done using UART, which will not be part of the production firmware. The diagram of the firmware is shown in Fig. 28. We used the multiboot feature of the Zynq SoC, allowing us to store up to 8 images in flash memory. When the ZYNQ SoC is powered on, the ARM processor uses an algorithm to search for a flawless image, once the image is found, it is loaded and the firmware starts. The ARM processor in the firmware is only used to set up clocks and make initialization routines, then the

FPGA takes the control of the system. The final firmware will not use the processor for the initialization routines, making the system even more robust.

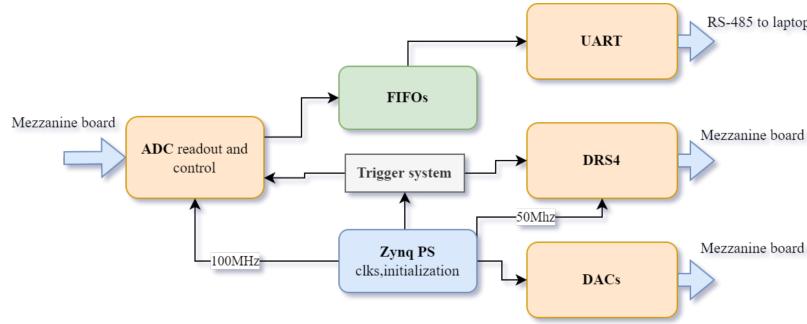


Figure 28: Flow diagram of the Firmware used during the tests

Measurements and results

During the data taking, the failures were registered after a communication time-out was reached. We also observed a few occasions with data corrupted. Fig. 29 shows the common failure observed during the runs. Is worth mentioning that channels 3 and 6 are not digitalizing well due to an identified firmware bug. The nominal

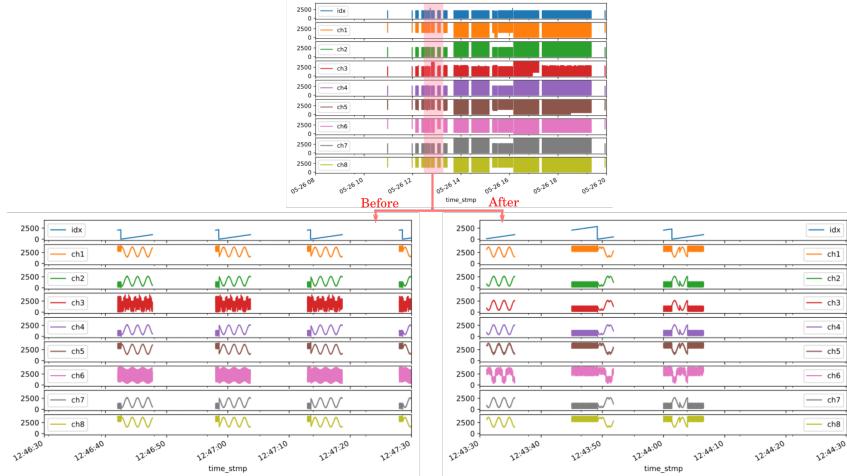


Figure 29: Common failure observed. The top image shows a summary of one day of measurements. The bottom images show time slices before and after the failure.

current consumption was $\tilde{1.25}$ A having small fluctuations, besides the spikes of up to 25% (250mA increase) related to latch-up events, see Fig. 30. The system was working stable until 05-29 13:40:00, then it couldn't recover (left star in Fig. 25). The system accumulated TID: 106 Gy, SEE: $2.56E+11$ part./cm², and N1MeV: $1.67E+12$ n/cm². The current consumption just before the incident is shown in Fig. 31 and the Mean time between failures is shown in Fig. 32. After inspection,

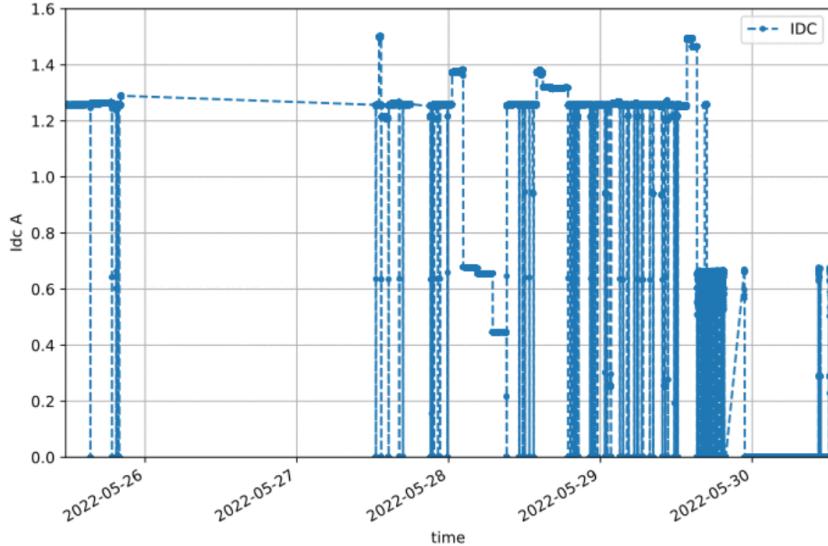


Figure 30: Current consumption during the first week.

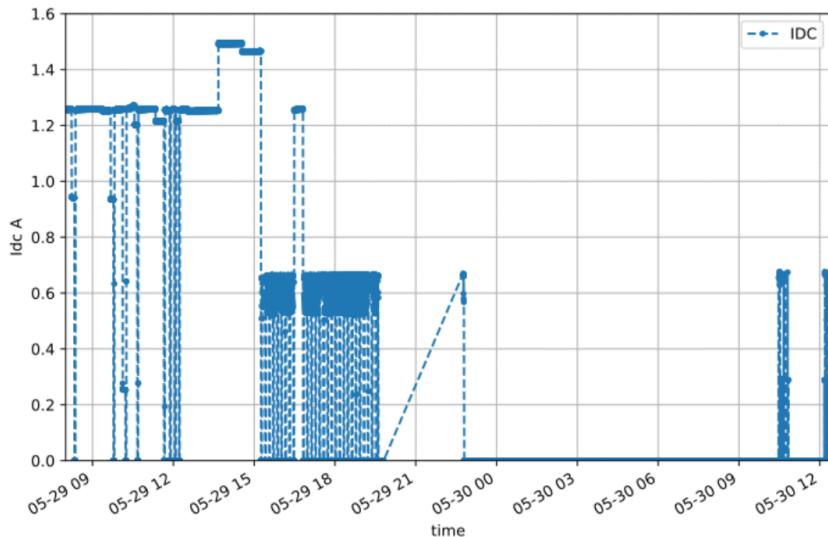


Figure 31: Current consumption seconds before DACs failures.

we determined the mezzanine was not working and decided to take it out to follow up the test with the motherboard and the SoM. Here the firmware shown in Fig. 28 was slightly modified to emulate the signals from the signal generator. The system worked for 11 days more until it failed and couldn't recover (right star in Fig. 25), reaching the levels **TID: 271 Gy, SEE: 6.34E+11 part./cm² and N1MeV: 4.03E+12 n/cm²**. The average current consumption was 0.62 A having a few spikes up to 15%(90mA), and can be seen in Fig. 33. On Jun. 28th, we recovered our modules and were able to test them in a laboratory, we found that the SoM was completely destroyed, not even able to be identified by the JTAG. Nevertheless, inserting the Mezzanine in a new 16-channel CMB we found that it was operative,

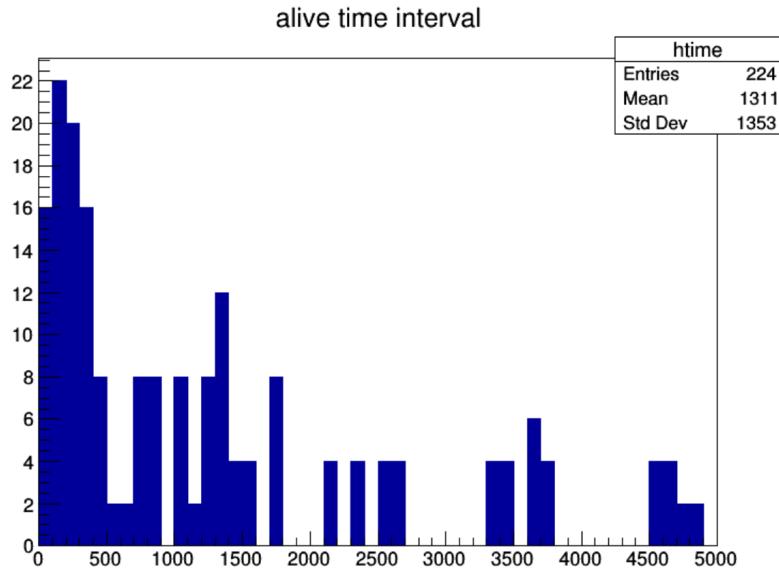


Figure 32: Time intervals between failures for the 16-ch CMB, during the first campaign

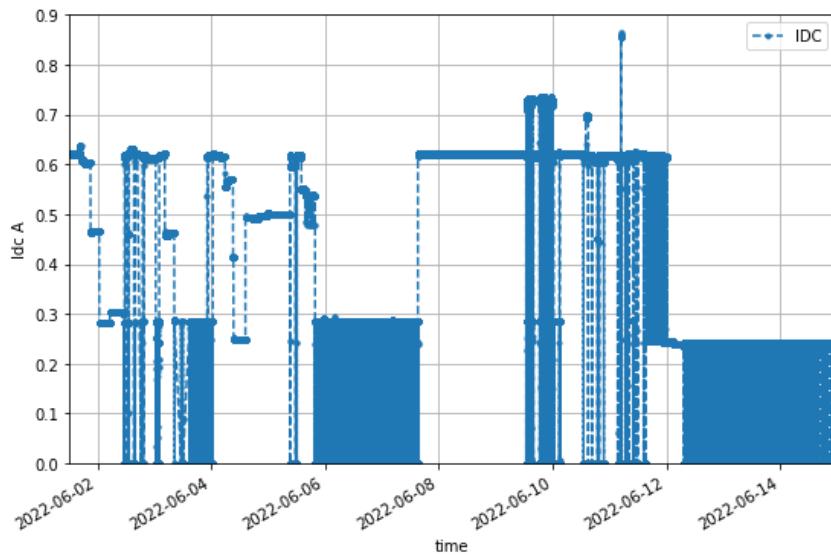


Figure 33: Current measurements during the weeks 2 and 3 (SoM + 16-channels mother-board).

see Fig. 35. We keep the Mezzanine to be used in the next radiation campaign.

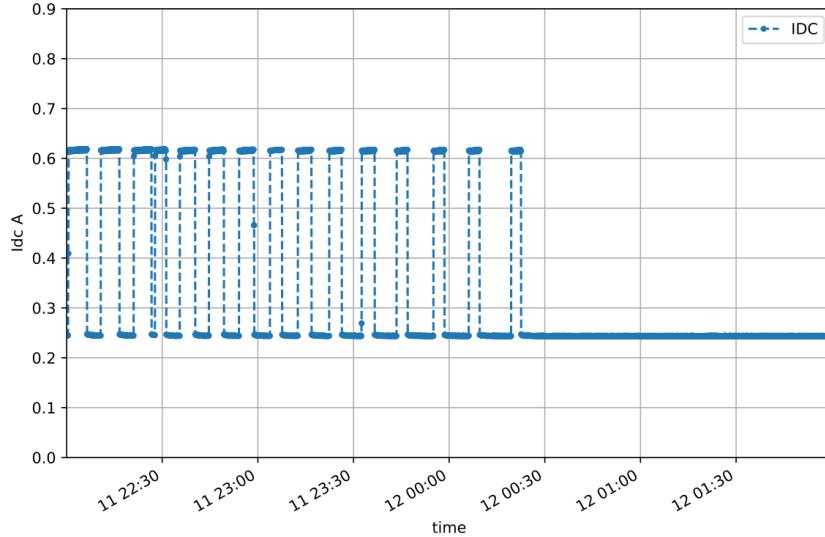


Figure 34: Current measurements just before the non-recoverable failure.

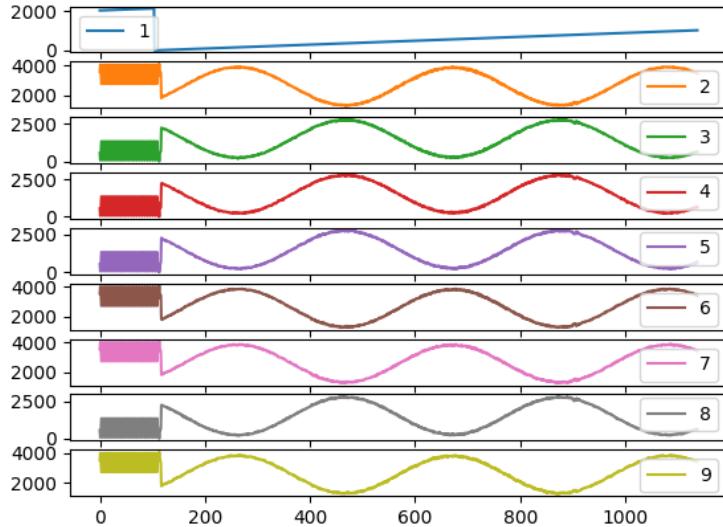


Figure 35: Signals acquired with the mezzanine after the annealing process.

10.1.2 Campaign 2

This campaign was focused on the CPLD that will serve as a multiplexer for the ADCs differential signals. Here we used benchmark firmware as in [8, 10, 4] which makes exhaustive use of different CPLD resources. Also, the Mezzanine from the Campaign 1 was tested using a new 16-channel CMB, in order to accomplish the radiation levels required.

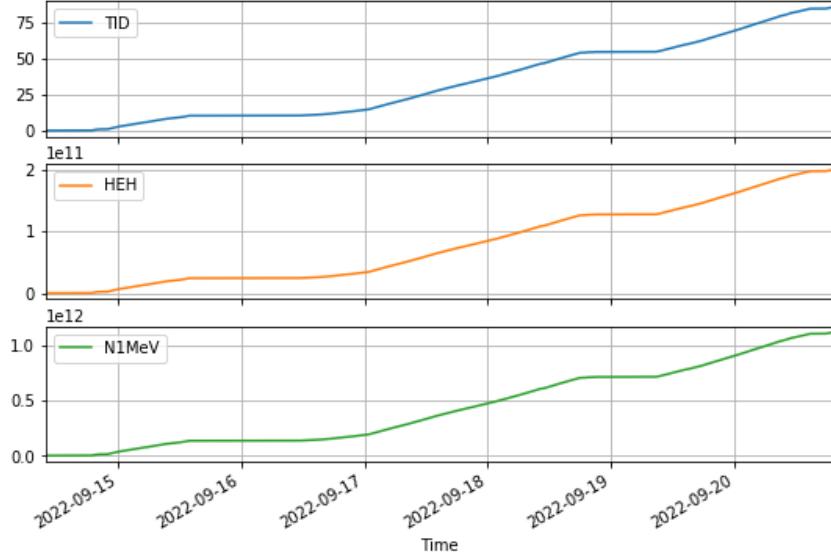


Figure 36: Beam during the second campaign. TID in Gy, HEH in part./cm², N1MeV in n/cm²

Registers	4665 / 10552	44%
Slices	3271 / 4700	70%
LUT4s	5698 / 9400	61%

Table 11: CPLD firmware resources

Experimental setup

The setup for the CMB was the same as the one for the first campaign. In the case of the CPLD, the setup did not require any external input, since the test consisted of a built-in self-test (BIST) strategy. The monitoring output of the CPLD was stored for later analysis.

Firmware used

The CPLD was populated by benchmark circuits, B13 [8], each circuit was fed by a unique Linear Feedback Shift Register (LSFR), which was implemented using Triple Modular Redundancy (TMR), the B13 were grouped in pairs, and the output of each pair was sent to a comparator, also implemented with TMR. The comparator shows whether the output of the B13s are identical, which in absence of radiation must be, hence any discrepancy can be accounted for an SEU in one of the B13. The flow diagram of the firmware is shown in Fig. 37 and the total resources used are shown in Tab. 10.1.2.

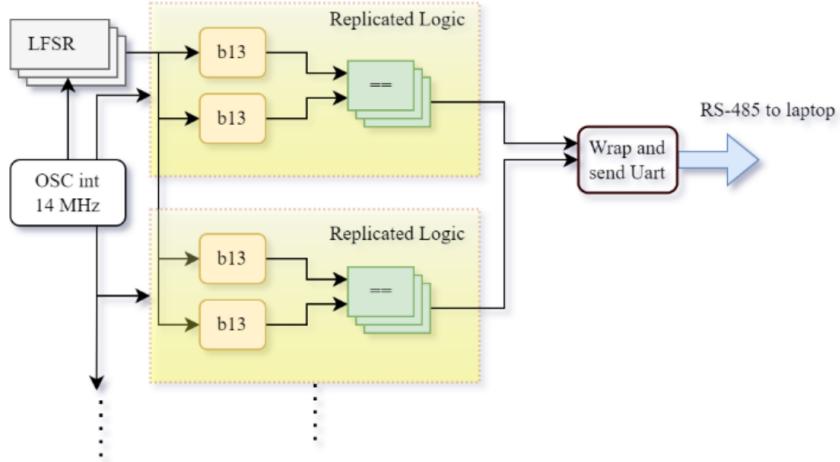


Figure 37: Diagram of the firmware used. The LFSR and the comparators have TMR.

Measurements and results

The CPLD survived the irradiation period as well as the CMB 16-ch with the exception of the mezzanine's DACs, which only survived 3.5 days, see Fig. 39. The MTBF of the CMB 16-ch was about 18 min, see Fig. 38.

The CPLD cumulative errors per B13 pair are shown in Fig. 40, and the total errors are in Fig. 41. We measured the number of failures on a given fixed interval and got the MTBF of about 2 min, see Fig. 42.

The mezzanine (except DACs) and the CPLD accumulated **TID: 85Gy, SEE: 1.99E+11 part./cm²**, and **N1MeV: 1.12E+12 n/cm²**. The DACs accumulated **TID: 31 Gy, SEE: 0.72E+11 part./cm²**, and **N1MeV: 0.40E+12 n/cm²**.

In order to reach the required dose for the CPLD, a new campaign was needed.

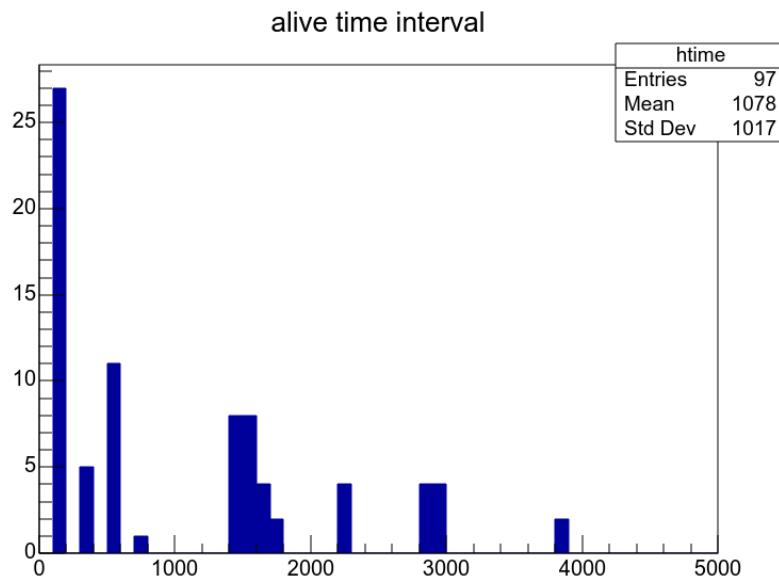


Figure 38: Time interval between failures for the 16-ch CMB during the sec. campaign

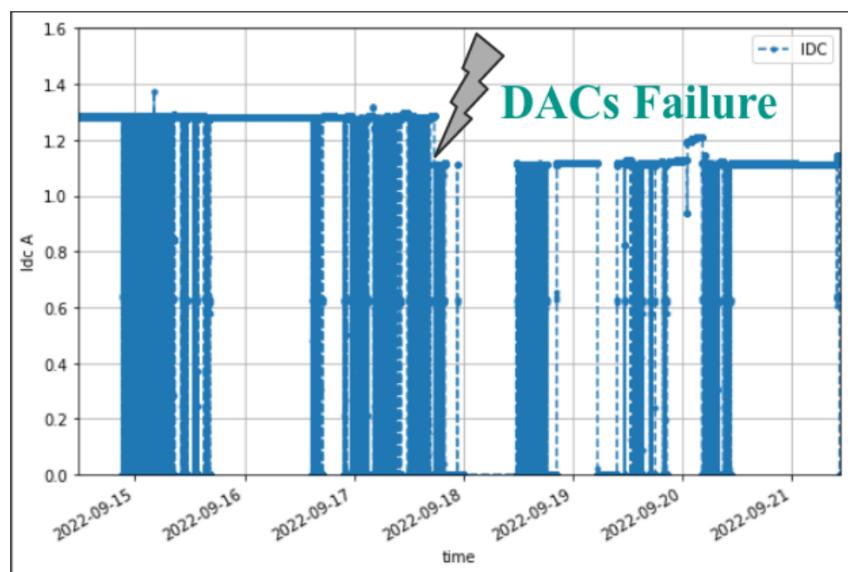


Figure 39: CMB 16-ch current consumption, the step indicates the moment of DACs failure during the sec. campaign

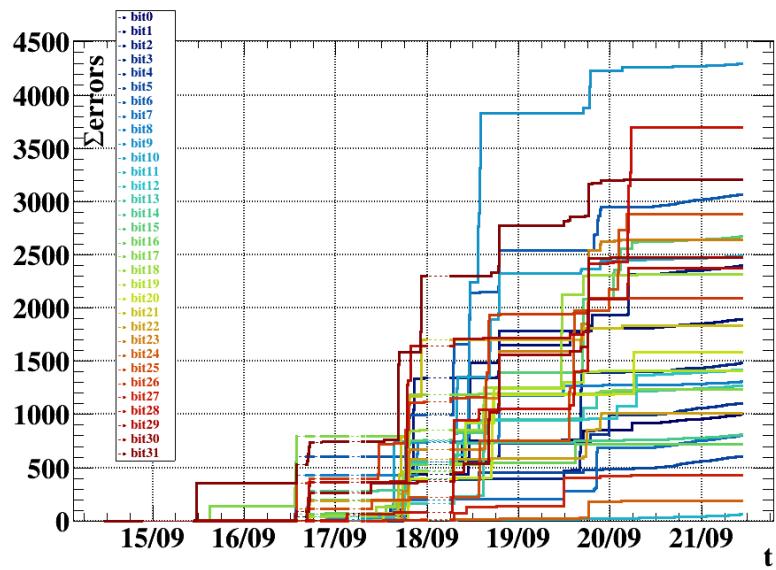


Figure 40: Cumulative fails during the sec. campaign for each B13 pair

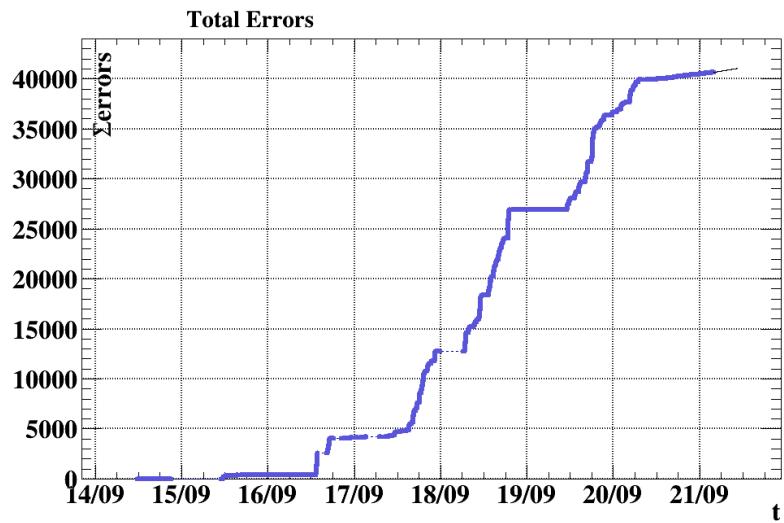


Figure 41: Total cumulative B13 fails during the sec. campaign

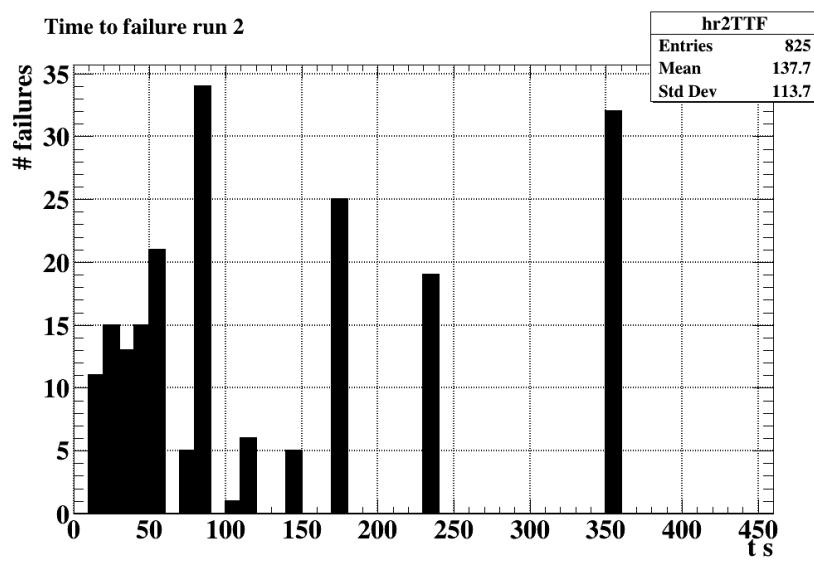


Figure 42: Time interval between failures for the CPLD during the sec. campaign

10.1.3 Campaign 3

This campaign was centered around the CPLD, the strategy used was the same as the previous campaign.

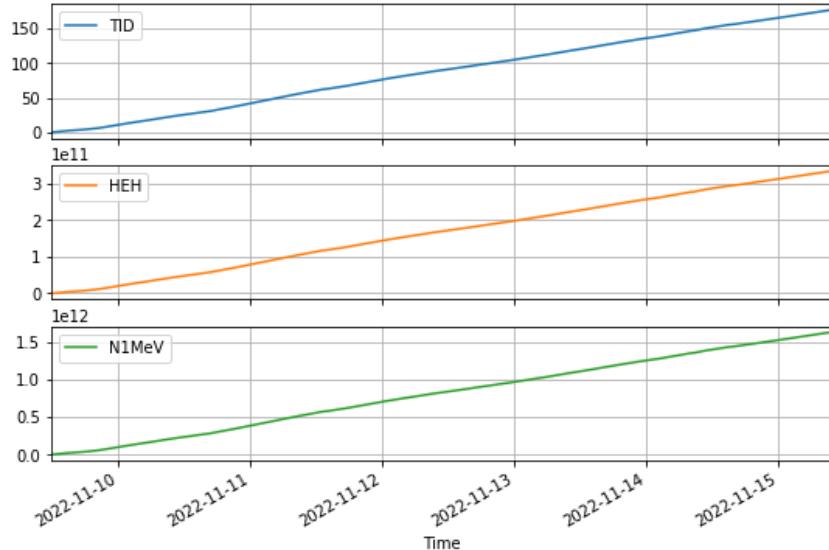


Figure 43: Beam during the second campaign. TID in Gy, HEH in part./cm², N1MeV in n/cm²

Experimental setup

The setup was the same as the previous campaign.

Firmware used

The firmware was similar to the previous campaign.

Measurements and results

The CPLD survived the irradiation period and the cumulative errors per B13 pair are shown in Fig. 44, and the total errors are in Fig. 45. We measured the number of failures on a given fixed interval and got the MTBF of about 1.25 min, see Fig. 46.

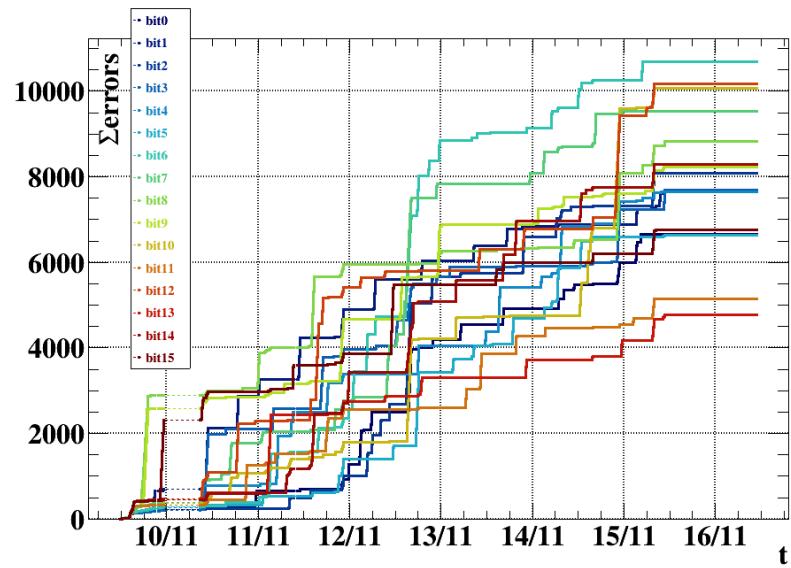


Figure 44: Cumulative fails during the third campaign for each B13 pair

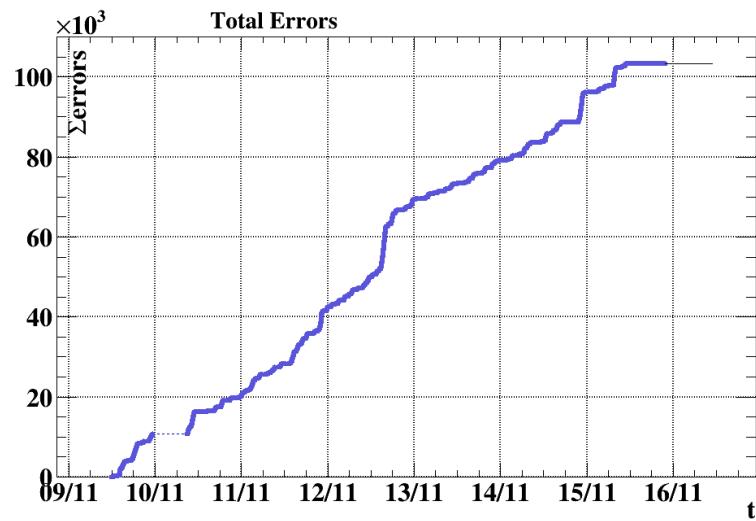


Figure 45: Total cumulative B13 fails during the third campaign

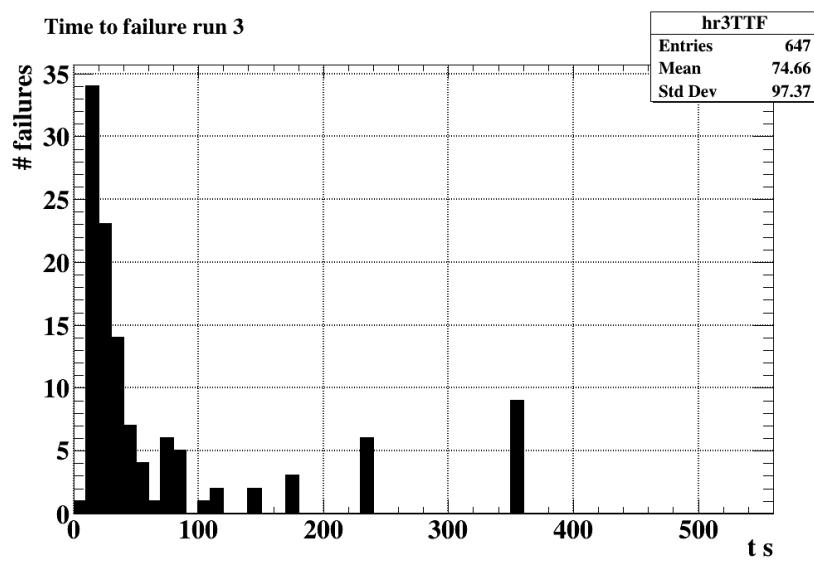


Figure 46: Time interval between failures for the CPLD during the third campaign

10.1.4 Conclusions

The whole system overcomes the radiation levels required for the final system location, the weakest part are the DACs. The compilation of the results obtained is shown in Tab. 10.1.4. The intensity of the beam in the CHARM facility is pretty big compared to the LHC operation conditions, the module with the bigger failure rate is the CPLD, with 1.25 min of MTBF, which happened during the third campaign. The beam intensity during this campaign corresponds to getting a TID dose of 176.32 Gy in 6 days, according to the ATLAS simulations in the ATLAS TDR, the TID over the 10 years of operation will be 4.1 Gy in the final location of the system, using the safety factors we get the time equivalence:

$$\Delta T_{LHC} / \Delta T_{CHARM} = \frac{176.32/6}{4.1 \cdot 1.5 \cdot 5 \cdot 4 / 3650} = 872.04 \quad (1)$$

In the worst-case scenario, we get about **one failure per day**. The final firmware that will run in the CPLD, will use quite fewer resources than the one used during the test (approx 1/3), allowing higher reliability for the system.

	Target Dose	Reached Dose Trenz board TE0715	Reached Dose Mezzanine	Reached Dose Mezzanine (DACs)	Reached Dose CPLD
TID Gy	123	271 (220%)	191 (155%)	137 (111%)	261 (212%)
HEH part./cm²	1.3E+11	6.34E+11 (488%)	4.55E+11 (350%)	3.28E+11 (252%)	5.3E+11 (408%)
N1MeV n/cm²	8.8E+11	4.03E+12 (457%)	2.79E+12 (317%)	2.07E+12 (235%)	2.75E+12 (312%)

Table 12: Summary of radiation dose achieved

10.1.5 Future Radiation tests plan

Even though we know the system overcomes the radiation levels required, the IC shortage problem can cause the changing of the ADC model (current ADC: ADS529). Other alternatives will be irradiated to work around the IC shortage problem. The ADCs features are summarized in Tab. 10.1.5.

IC	resolution	package	max samp. freq
ADS5296	12 bit	QFN64	80MSPS
ADS5294	12 bit	QFP80	80MSPS
ADS5287	10 bit	QFN64	50MSPS

Table 13: ADC alternatives

11 Reliability Matters

11.1 Consequences of Failures

If the CMB fails, the detector will still be functional. Since the CMBs' main objective is monitoring the TGC status, a malfunctioning CMB will result in missing monitoring data. Nevertheless, software backup and safe booting will be incorporated into the CMBs' firmware.

11.2 Prior Knowledge of Expected Reliability

The radiation hardness is the main reliability test for the CMBs. Nevertheless, radiation-induced upsets are expected to happen so logic redundancy will be implemented in firmware design to prevent soft errors.

11.3 Measures Proposed to Ensure Reliability of Component and/or System

To ensure reliability, all components must be selected and tested to be radiation-hard whenever possible, or at least tolerant to the required level. On the other hand, logic redundancy will help to prevent soft errors. In case a board is malfunctioning, a power cycle can be performed by shutting down specific boards. Since the design is modular, if one board fails, individual components can be replaced if damaged. Ensuring the integrity of the whole system. The system doesn't crash if one or more boards are disconnected.

11.4 Quality Assurance to Validate Reliability of Design and Construction or Manufacturing Techniques

To test the electronics mounted in PCBs, burn-in tests and accelerated aging through high-temperature tests will be carried out. Mechanical stress tests do not apply in this design. Also, tests on a high-radiation environment have been done at different facilities: GIF++, CCHEN Chile, and the mixed field of the CHARM facility, which is the most thorough test.

11.5 Quality Control to Validate Reliability Specifications during Production

Since the design will be modular, all the digitizer modules can be easily tested on any working motherboard. In this part of the production, the CMB will be configured with a debugging functionality and every channel of the CMB will be tested to ensure correct operation. No radiation tests will be carried out during this stage since the radiation hardness should be checked before the design. Also, an additional SoC will be needed to simulate the communication with the EMCI system, this can be achieved by using an IGBT IPCORE-compatible module to load the firmware in the SoC, which will simulate the EMCI system.

12 Appendix

List of the signals of each mezzanine

The digital signals of a mezzanine board connected to the motherboard using SAMTEC connector LSHM-150 are listed below :

Vivado block design 8 channel project

pin num- ber	signal	pin num- ber	signal	pin num- ber	signal
1	5[V]	35	OUT5 N	69	GND
2	5[V]	36	dwrite	70	GND
3	5[V]	37	OUT6 P	71	trigger ch 0
4	5[V]	38	denable	72	nSHDN
5	5[V]	39	ADC LCLK N	73	trigger ch 1
6	5[V]	40	GND	74	x
7	5[V]	41	ADC LCLK P	75	trigger ch 2
8	Mux1[0]	42	GND	76	x
9	5[V]	43	GND	77	trigger ch 3
10	Mux1[1]	44	DRS4 WSRIN	78	GND
11	5[V]	45	ADCLK N	79	trigger ch 4
12	Mux2[0]	46	nReset	80	Test signal
13	GND	47	ADCLK P	81	trigger ch 5
14	Mux2[1]	48	DRS4 A1	82	ADC interleave
15	ADC ref CLK P	49	OUT4 N	83	trigger ch 6
16	GND	50	GND	84	ADC PDN
17	ADC ref CLK N	51	OUT4 P	85	trigger ch 7
18	DRS4 ref clk P	52	GND	86	ADC Sync
19	OUT8 N	53	GND	87	GND
20	DRS4 ref clk N	54	DRS4 A0	88	GND
21	OUT8 P	55	OUT3 N	89	DAC SEL1
22	GND	56	RSRLOAD	90	SDOUT
23	GND	57	OUT3 P	91	DAC SCLK
24	PLLCK	58	SRCLK	92	ADC nCS
25	OUT7 N	59	OUT2 N	93	DAC SDA
26	DRS4 A2	60	GND	94	ADC sDATA
27	OUT7 P	61	OUT2 P	95	DAC nCLR
28	DRS4 A3	62	GND	96	ADC SCLK
29	OUT6 N	63	GND	97	DAC SEL0
30	GND	64	SRIN	98	ADC nReset
31	OUT6 P	65	OUT1 N	99	DAC nReset
32	GND	66	SROUT	100	GND
33	GND	67	OUT1 P		
34	DTAP	68	WSROUT		

Table 14: Mezzanine electrical signal pinout in LSHM-150 samtec connector.

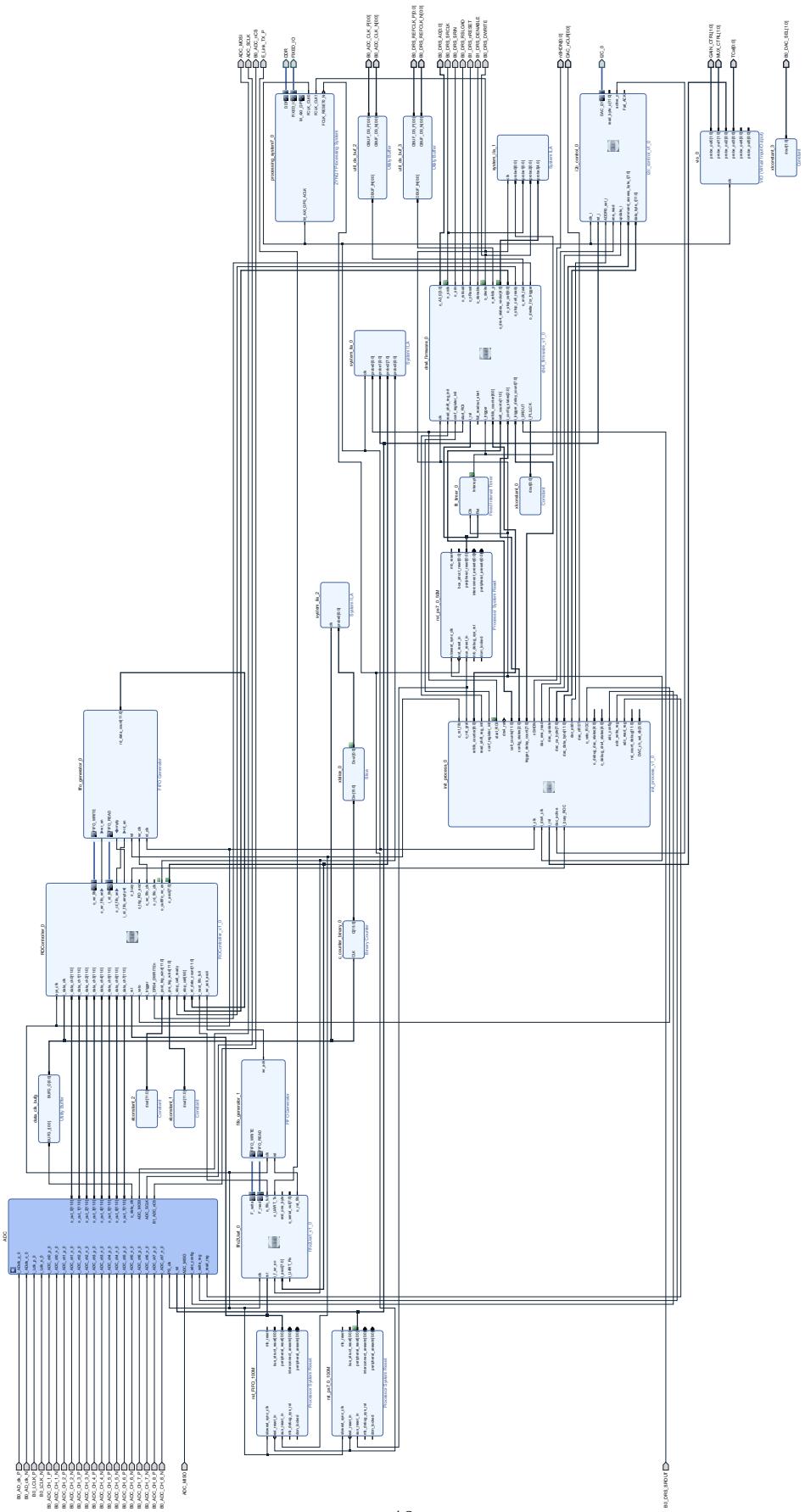


Figure 47: Vivado block design of the project to read 1 mezzanine and send full waveform readout using UART.

References

- [1]
- [2] .
- [3] M. Aoki. Tgc chmon power requirement. <https://indico.cern.ch/event/1020764/>.
- [4] S. Davidson. ITC99' official site. <https://www.cerc.utexas.edu/itc99-benchmarks/bench.html>.
- [5] L. L. Foro. Tid irradiation test campaign. https://edms.cern.ch/ui/file/1582526/1/R2E-Study_TID_Campaign_Test_Report_MCP1826_DC1448.pdf.
- [6] P. Moreira. lpgbt-a user's perspective. 2018.
- [7] J. M. G. S. Pascal Oser. Voltage regulators (lp3990 - lp2980 - lm340) and voltage reference (max6350). https://edms.cern.ch/ui/file/1231452/1/PSI_VoltageRegulator_Report_LP3990_LP2980_LM340_MAX6350.pdf.
- [8] R. Ferraro S. Danzeca, A. Scialdone. Ng-medium fpga radiation test report at psi. *EDMS: 2261505*, Oct. 2019.
- [9] O. Sasaki and M. Yoshida. Asd ic for the thin gap chambers in the lhc atlas experiment. *IEEE Transactions on Nuclear Science*, 46(6):1871–1875, 1999.
- [10] G. Squillero. github repository. <https://github.com/squillero/itc99-poli>.
- [11] S. Tarem, S. Bressler, A. Harel, E. Hadash, R. Lifshitz, N. Lupu, and L.J. Levinson. Detector-control system for the atlas muon endcap trigger. *IEEE Transactions on Nuclear Science*, 52(4):1207–1211, 2005.
- [12] A. Thornton. Charm facility test area radiation field description. *Annalen der Physik*, 2019.
- [13] C.S.L.O.J. Troska. The versatile link+ application notee.