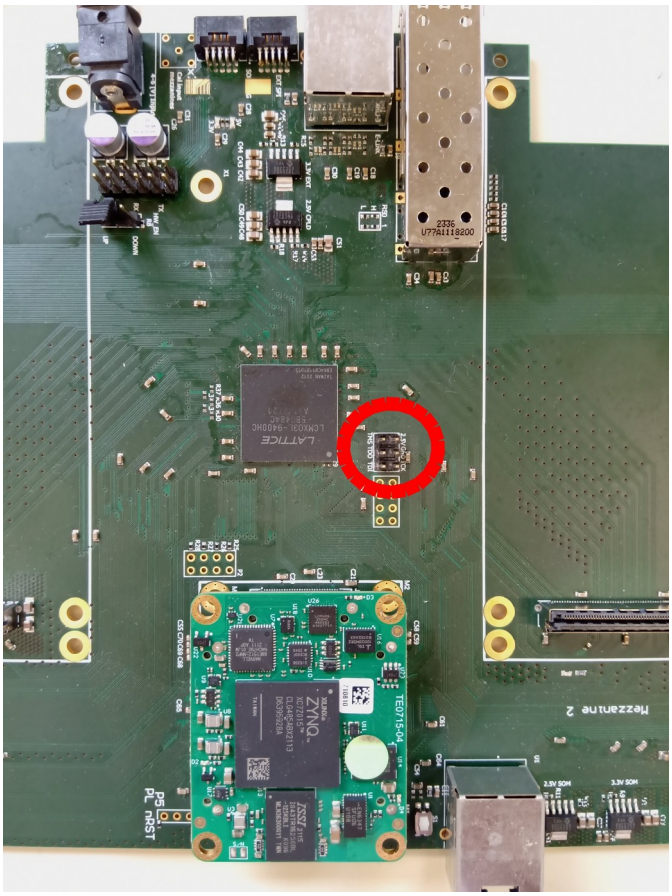
How to load CPLD’s firmware into Charge Monitoring Board motherboard

Renzo Barraza – 2024/09/16

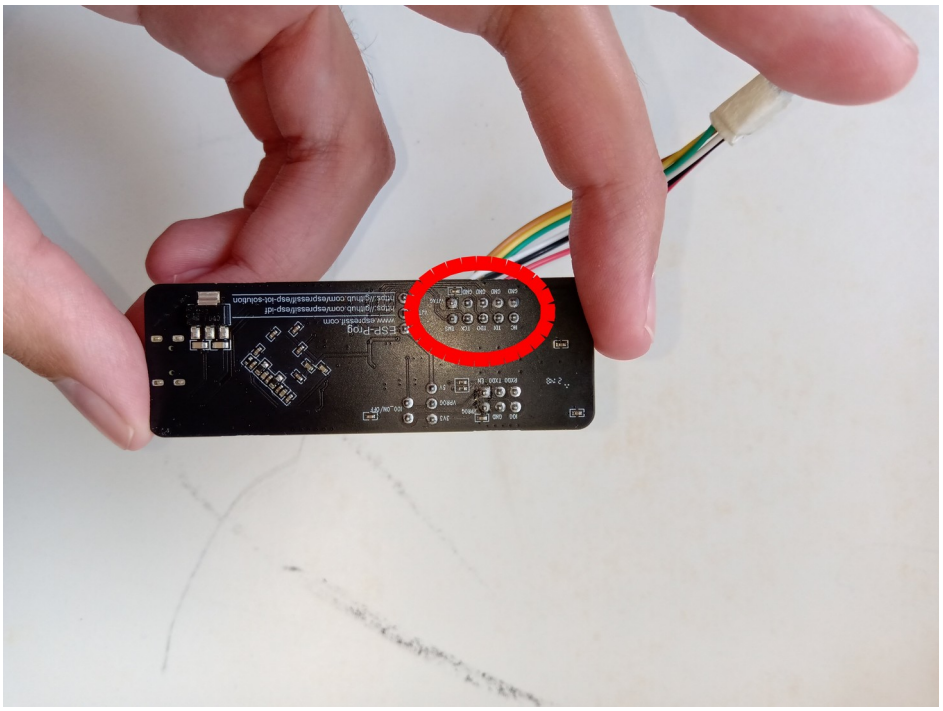
Step 1: Connect the programmer with the Charge Monitoring Board motherboard

To program the CPLD you must use a programmer that transforms the serial communication from your computer into JTAG communication; which is understood by CPLD. In order to make that we have available the programmar “ESP-Prog” from espressif.

To connect the ESP-Prog to the Charge Monitoring Board motherboard, you must use the pins sorounded by a circle in the following image



Those pins must be connected to the ESP-Prog programmer by matching their names with the ones at ESP-Prog. You can find the ESP-Prog names at this part of the programmer:



After connecting the both boards (the CMB motherboard and the programmer) by matching the pin's names, you can connect the programmer to your computer with a USB cable.

WATCH OUT: When you are programming the CPLD, the **Trenz SoM module must not be mounted in their Samtech socket**, and the **CMB motherboard must be disconnected from the power source**. The reason for this is that the ESP-Prog has a Vdd pin that will power the CPLD with 3.3V when it is programming it, but the Charge Monitoring Board's motherboard has its own voltage regulator to power the CPLD during normal operation, and it will deliver 2.5V to the CPLD; if you connect the ESP-Prog and power the CMB motherboard with an external source at the same time, you may end with 2 power sources without a common reference supplying the same node. Additionally, if you program the CPLD with the Trenz board mounted on the motherboard, it is probable that the SoM will consume current, that current will come from the ESP-Prog board, and it won't be able to supply it, so the voltages will drop and the programming may fail.

Step 2: Setting your Lattice Diamond session

Before continue with any work on your firmware, you must correctly set the device that you will program. For that first open the software Lattice Diamond, and by clicking at File → Open → Project, open the file called “CMS_MUX_IO.ldf”. This will open the CPLD’s firmware project.

After that, in the menu in the left column, select the tab “File List”, and at its header, after the name of the project, you will see your hardware’s part model; check that it is the same that you want to program. At today’s date[1], the CPLD used in the Charge Monitoring Board motherboard is: **LCMXO3L-9400C-5BG484C**. WATCHOUT, even a change of one letter may mean a change in the model you are programming.

If you want to change your hardware’s model, right click in the hardware’s part model and press “Edit”. This will open a new window where you can select the your correct hardware; the correct CPLD in our case.

Step 3: Process your design (synthesis, place and route, atc.)

If you want to update some part of the firmware, you can choose the tab “File List” (at the left column) and open the VHDL file you want to update.

After you have donne your updates, go to the tab called “Process” and enable all the processes you want Lattice to make with your firmware. Then, in the upper options go to: Tools → Run Manager, and in the Run Manager select the design you want to process. After selecting it, right click on it and select “Run” or “Rerun”. This should launch all the processes selected by you in the “Process” tab

Step 4: Program your devide

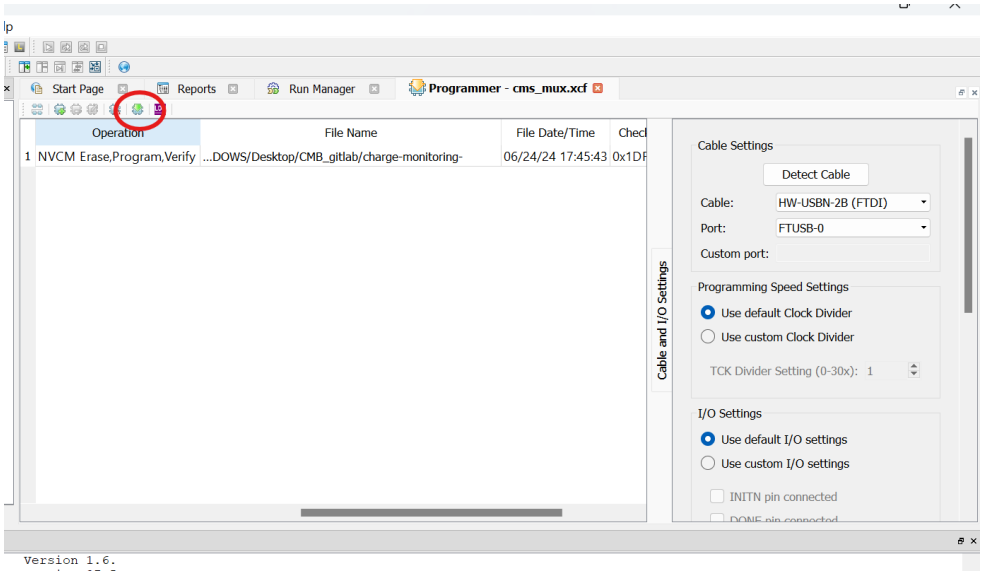
Once the Exported files are generated in the previous step, you can program them into your CPLD by clicking in the upper menu bar: Tools → Programmer. There you must select the

1 2024/09/16

hardware you are using, the file you want to load and the actions you want to make by setting the fields “Devide Family”, “Device”, “Operation” and “File Name”.

Assuming you already connected the programmer to your computer, in the same “Programmer” view, in the right menu, push button “Detect Cable”. This should detect the devide you want to program. Let the options “Programming Speed Settings” and “I/O Settings” in the values marked as default; for example, select “Use default clock divider”.

After your hardware have been detected, look for the icon “Program” in the options’ bar; at leas in Lattice Diamond 3.13.0.56.2, that icon is in the position marked by the red circle in the following image:



If programming fail, try the other port detected in the Cable Settings menu, as it is not always clear which port is the one you must program. Additionally, if you first selected the wrong port, a blue light may turn on in the ESP-Prog programmer, that may block you to program the CPLD again. To repair that, just disconnect and reconnect the ESP-Prog to your computer; that should get the blue light to turn off.

WATCH OUT: if the Trenz SoM is connected to your motherboard when you programm the CPLD, make sure the motherboard is powered with 5V through the power jack; otherwise the CPLD programming may fail.