E-link communication between Charge Monitoring Board (CMB) and EMCI

2024/10/21 – Renzo Barraza

General context about communication between CMB and EMCI

The EMCI board is a middle step between the communication that starts in the Charge Monitoring Board (CMB), passes through the EMP board, and ends in the Detector Control System; the EMCI board acts as a concentration board, that collects data from 4 Charge Monitoring Boards.

In the physical layer, the communication is done through a RJ-45 cable, where one differential pair carries data from the Charge Monitoring Board; other differential pair carries data from the EMP to the Charge Monitoring Board; a third differential pair carries the clock signal, needed for the communication protocol, from the EMP to the CMB; and finally, there are 2 other GPIO wires for communication, which are not differential pairs between them.

It must be noticed that the clock signal for the communication comes from the EMCI and it is received by the Charge Monitoring Board. This design decision was made by recommendation fo the lgGBT team; the exact recommendation from the lpGBT team was:

> If the Front-end [front-end from the EMCI, i.e., the Charge Monitoring Board] does not have a CDR circuit (this is a circuit that generates a clock from the incoming data), it is hard that the Front-end itself could be able to generate the necessary clocks for the communication.

Caveats

1. The 2 GPIO cables that are inside the RJ-45 cable in the E-link communication, are not set as differential pairs; they does not reach a differential pair input in the CMB. Additionally, the ground node is not shared between the Charge Monitoring Board and

the EMCI, so these GPIO cables must be disconnected of properly referred to some ground in the final design.

Communication protocol used by the EMCI board

According to the EMCI[1] and lgGBT[2] documentation, the protocol used by EMCI (and the lpGBT inside of it) uses the protocol CERN Low Power signaling (CLPS). The characteristics of this protocol are:

- Link types:
  - Point-to-point;
  - Multi-drop transmitter.
- Maximum data rate:
  - 1.28 Gbps (NRZ signalling).
- Maximum clock frequency:
  - 1.28 Ghz.
- Programmable signalling level:
  - 100 mV to 400 mV (single-ended amplitude);
  - 200 mV to 800 mV (differential amplitude).
- Common mode voltage:
  - 600 mV (nominal, for 1.2 V supply voltage).
- Load impedance:
  - 100 Ohm differential.

The previous specifications means that, if in this protocol we have 2 differential signals, called Tx_p and Tx_n, those digital signals will have a common mode voltage of 600 mV and will have a peak to peak amplitude that can be between 100 mV and 400 mV. To make it clear, below there is a diagram of how one of the previous signals (Tx_p in this case) will look in amplitude.

1 https://edms.cern.ch/ui/file/2332346/2/EMCI_electronic_specifications_v1.2_docx_cpdf.pdf
2 https://lpgbt.web.cern.ch/lpgbt/v1/ePorts.html#cern-low-power-signalling-clps

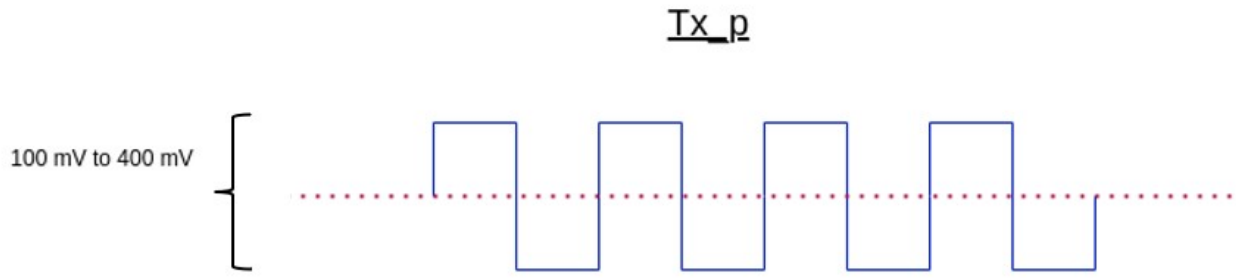

Figure 1: CLPS single ended signal amplitude

Additionally, according to the lgGBT team, these margins must be strictly observed, as “if Tx_p plus the common mode voltage surpass the 1.2V, there exist the risk to damage the link [i.e. the lpGBT]”.

Communication protocol used by the Charge Monitoring Board (CMB)

The communication between the Charge Monitoring Board and the EMCI is manged by the Trenz board inside the CMB; the Trenz board model is Trenz TE0715. However, the Trenz board does not produce or read natively the CLPS protocol, so a proxy must be found.

The hardware of the Charge Monitoring Board already shifts the common mode voltage of the signal coming out of the Trenz board to the 600 mV required by the CLPS standard. Because of that, the main criteria to choose an alternative communication protocol is that it must comply with the maximum differential voltages set by the CLPS standard.

The available differential protocols supported by the Trenz TE0715 are[3] [4] in the following table; there the voltages mean the peak-to-peak voltage of the single ended signals, i.e. an amplitude measured similar to the one seen in Figure 1.

3 Zynq-7000 All Programmable SoC (Z-7007S, Z-7012S, Z-7014S, Z-7010, Z-7015, and Z-7020): DC and AC Switching Characteristics
4 7 Series FPGAs SelectIO Resources User Guide

I/O Standard	VID			VOD		
	V,min	V,typ	V,max	V,min	V,typ	V,max
BLVDS	0.1	--	--	[5]	[6]	[7]
MIN_LVDS	0.200	0.400	0.600	0.300	0.450	0.600
PPDS	0.100	0.250	0.400	0.100	0.250	0.400
RSDS	0.100	0.350	0.600	0.100	0.350	0.600
TMDS	0.150	0.675	1.200	0.400	0.600	0.800
LVDS	0.100	0.350	0.600	0.247	0.350	0.600

Based on this information, the only standard that fits the limits of the CLPS standard is the PPDS. Because of that, the PPDS is the standard used to implement, from the Charge Monitoring Board side, the communication with the EMCI board.

5 VOD for BLVDS will vary significantly depending on topology and loading.
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7 VOD for BLVDS will vary significantly depending on topology and loading.

Versions

Date	Version	Comment
2024/10/21	1	Original version