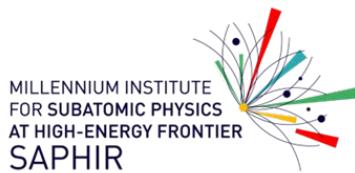


TGC-Charge Monitoring System

Preliminary Design Review

Sergey Kuleshov, Orlando Soto, Victor Arredondo, Vicente Agosin

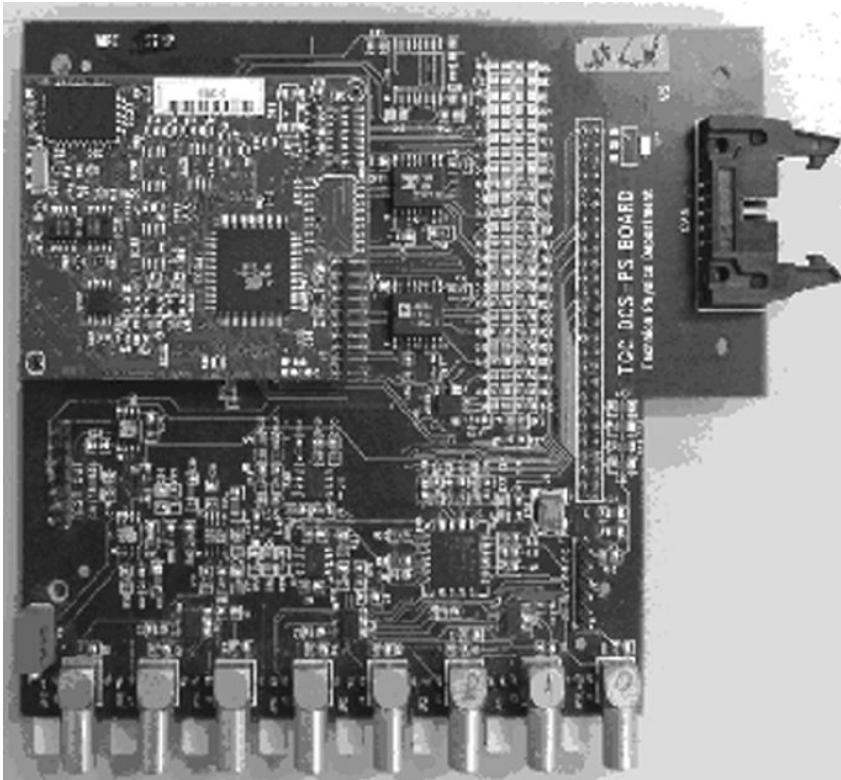


Outline

- Context
- Requirements
- Electrical Interfaces
- Physical Description
- Firmware
- Prototypes development
- Testing, validation, commissioning
- Radiation tests
- *SPR recommendation answers.*

Context: Actual monitoring system

The actual DCS-PS boards is responsible, among other task, to measure the TGC gain stability with the Chamber Charge Measurement Circuit (CCMC) [1]. The PS board will be upgraded and the function of the CCMS will be done by the TGC-Charge Monitoring board.



[1] S. Tarem *et al.*, "Detector-control system for the ATLAS muon endcap trigger," in *IEEE Transactions on Nuclear Science*, vol. 52, no. 4, pp. 1207-1211, Aug. 2005, doi: 10.1109/TNS.2005.852633.

Context: System capacity

The system consist of Charge Monitoring Board (CMB), which holds 5 mezzanines that serve 8 channels each, adding up to 40 channels per CMB.

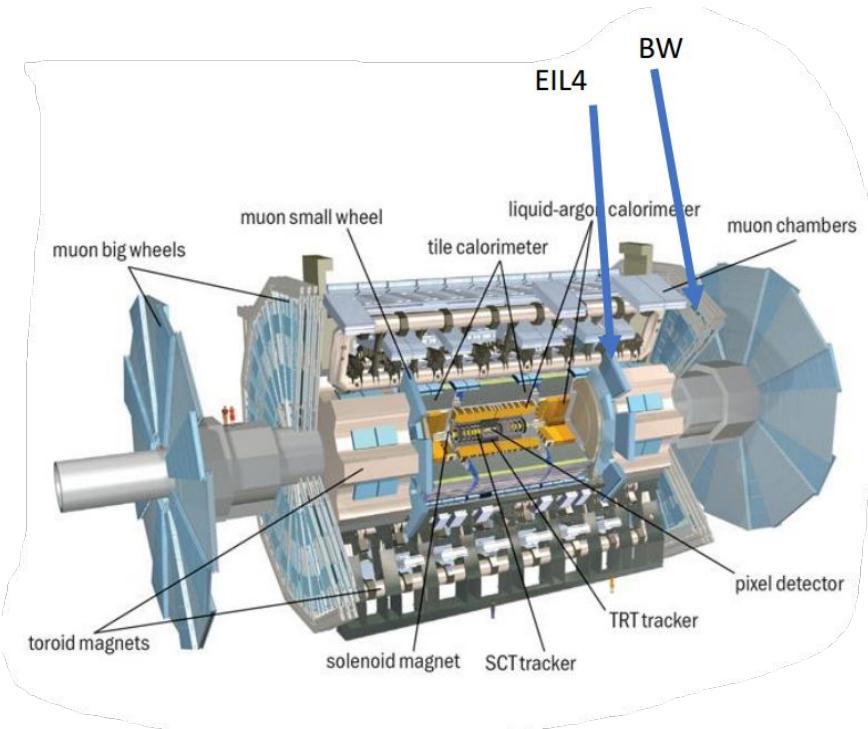
3408 ch. on BW and 126 ch. on EIL4, which lead to 96 CMB on BW and 4 CMB on EIL 4 (100 Total).

2 mV to 500 uV voltage resolution depending on ADC available

	# of endcaps	# Racks per endcap	# CMB per rack	Input channel capacity	Input channel used
BWs	2	12	4	$2 \times 12 \times 4 \times 40 = 3840$	3408
EIL4	2	1	2	$2 \times 1 \times 2 \times 40 = 160$	126
Total				4000	3534

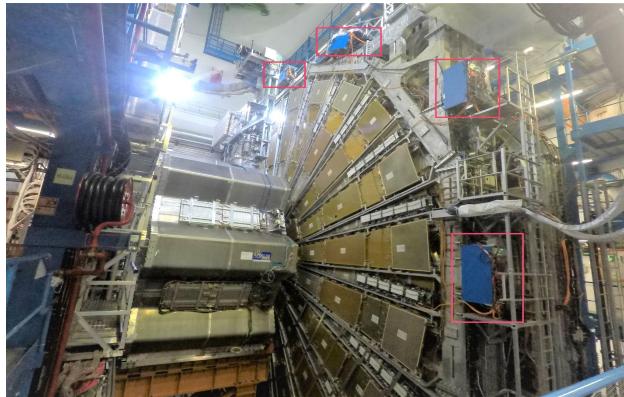
Context

- ATLAS muon spectrometer
 - Big wheels
 - TGCs wheels
- Purposes:
 - Monitor TGC detector gain stability
 - Measure detector efficiency
- Mechanism:
 - Monitor pulse shape for MIPs
 - Can measure temperature of TGCs with external board (SPI connection).
 - Data collected to be sent through EMCI to EMP
 - DCS will have access to this data.

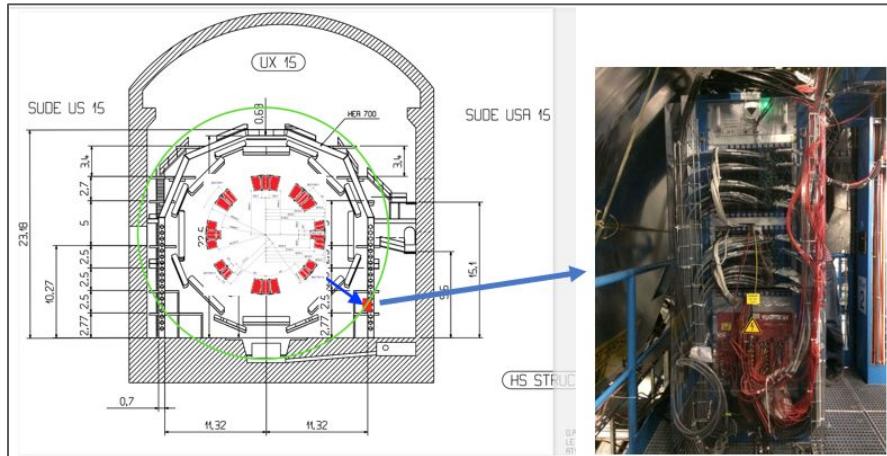


Context: System capacity

- TGC's ASD's (MO) from EIL4 and Big wheels are monitored by CMB.
- 4 CMB will be placed in miniracks for EIL4 TGC's
- 96 CMB will be placed in M1 miniracks for Big wheel TGC's

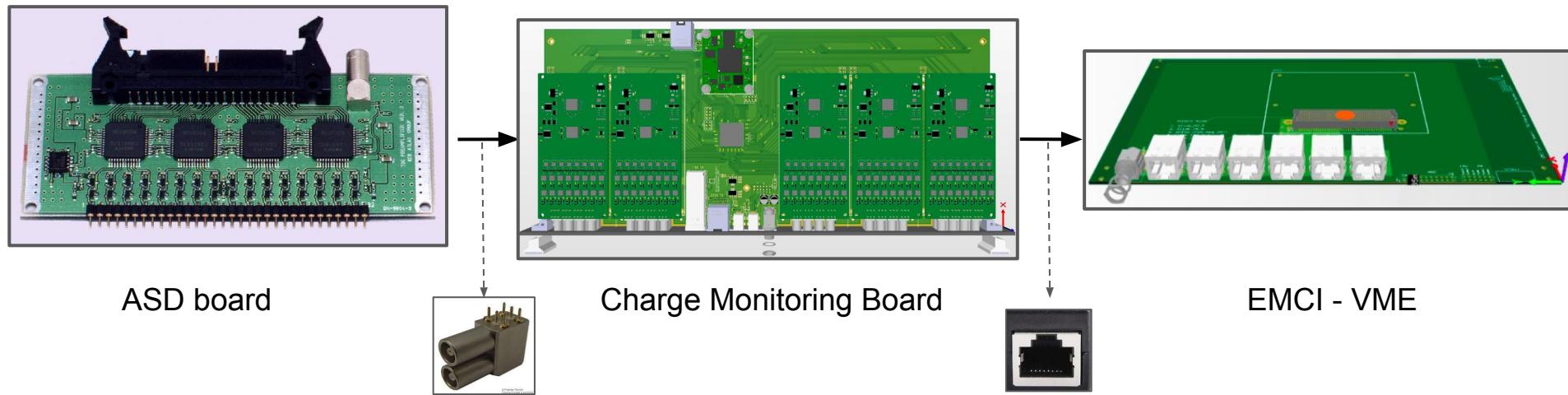


Big wheel miniracks



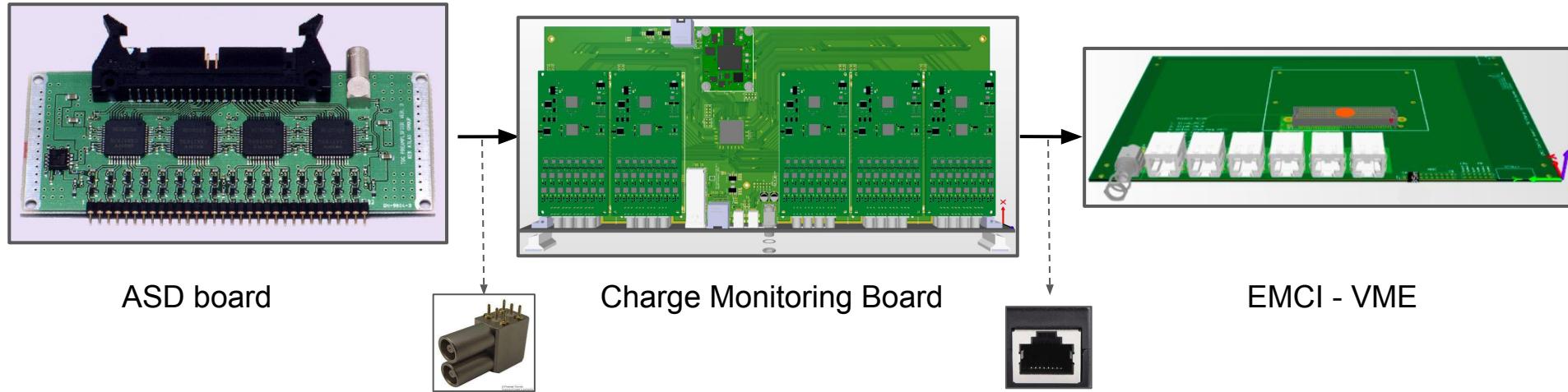
EIL 4 miniracks

Electrical interfaces: Overview



The CMB receives its inputs from the ASD board (**ASD's monitoring output**) using Lemo 00 double channel socket mounting on the mezzanine board. Will send the collected data to the EMCI-VME board (corresponding to a **EMCI carrier board**) using UTP cable with RJ45 socket.

Electrical interfaces: Overview



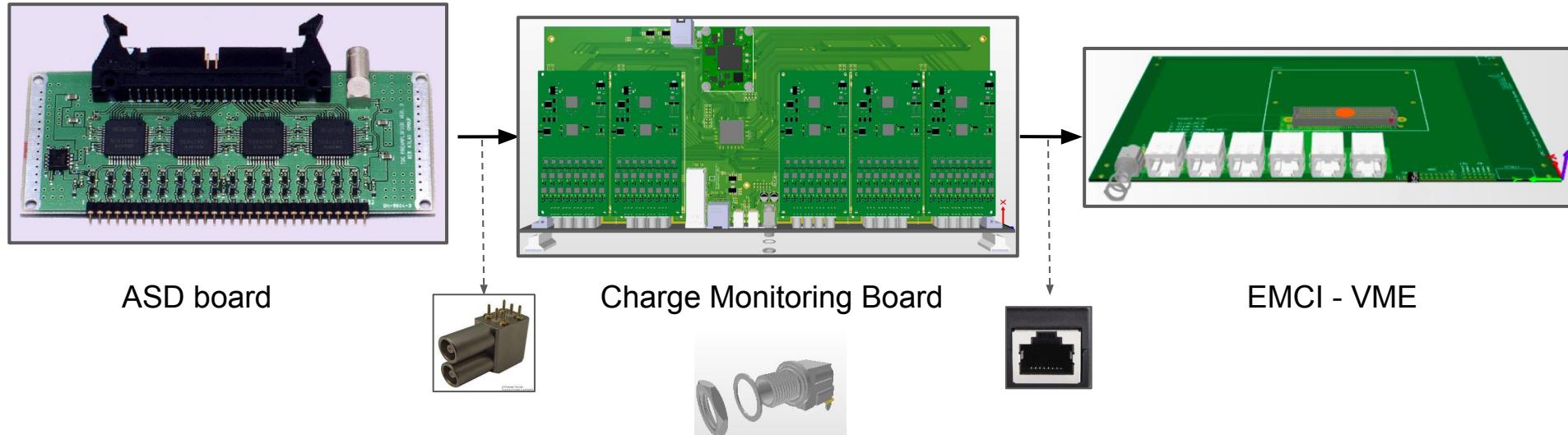
ASD board

Charge Monitoring Board

EMCI - VME

Lemo cables will be recycled from the current ASD to CCMC connections. To achieve the total length, lemo extension (LEMO "I") and lemo cables will be used.

Electrical interfaces: Overview



ASD board

Charge Monitoring Board

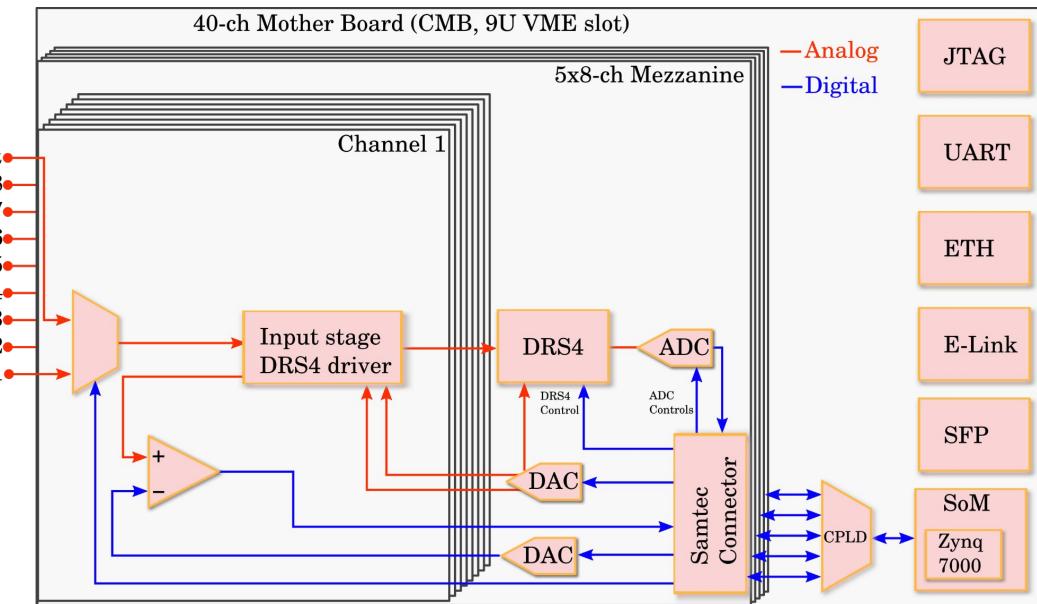
EMCI - VME

Power connection of the Charge monitoring board and EMCI-VME will use a barrel connector with center pin diameter of 2 mm, outer diameter of 6.4 mm and internal depth of 18 mm. Both boards will use a supply channel from the **power supply available on the VME-crate**.

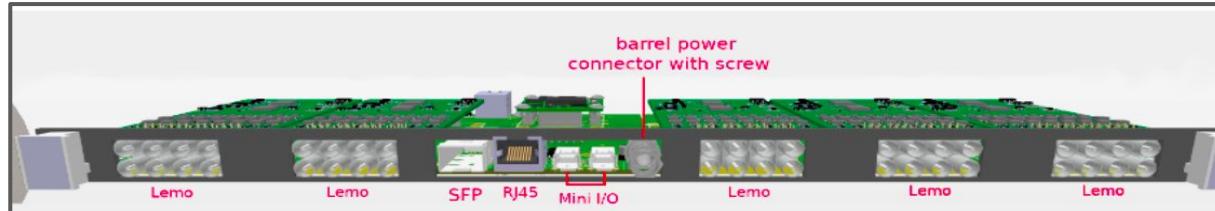
Electrical interfaces: Analog and digital schematics

System connection diagram

- 1 motherboard, 5 mezzanines
- 8 inputs per mezzanine
- 50 Ohms analog inputs Lemo 00
- Conditioning and multiplexing stages
- Analysis stage
- Optical output signals
- Electrical output signals

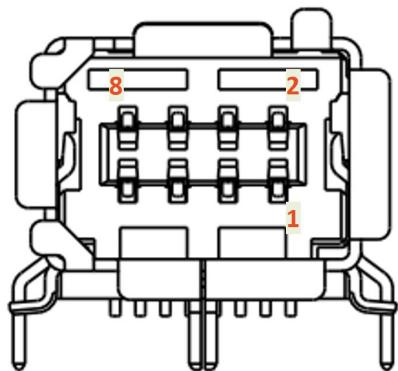


Electrical interfaces: CMB front view



Component	Specification	Connection to/from CMB
Double Lemmo socket	LEMO 00 connectors. (50 [ohm]) from ASD to Mezzanine board	TGC front end
RJ45 socket	RJ45 socket CAT5e 8p8c	EMCI-VME to CMB (UTP)
Power connector	Barrel with screw 11 [A]. Internal pin diameter of 2 [mm]. Barrel outer diameter 6.4 [mm] inner length 18 [mm]	From Crate power supply to CMB
SFP+	SFP connector	optical transceiver
Mini I/O socket left	8 pin socket TBD industrial Mini I/O F 8 POS 0.635mm Solder RA SMD 8 Terminal	Connection to satellite board to read the temperature of BW TGC via SPI protocol
Mini I/O socket right	8 pin socket Mini I/O Mini I/O F 8 POS 0.635mm Solder RA SMD 8 Terminal	JTAG in CMB to reprogram the firmware
Lemo 00 socket	LEMO 00 connectors. (50 [ohm]) for calibration purposes.	Front panel

Electrical interfaces: MINI IO pinout



MINI IO left: SPI communication

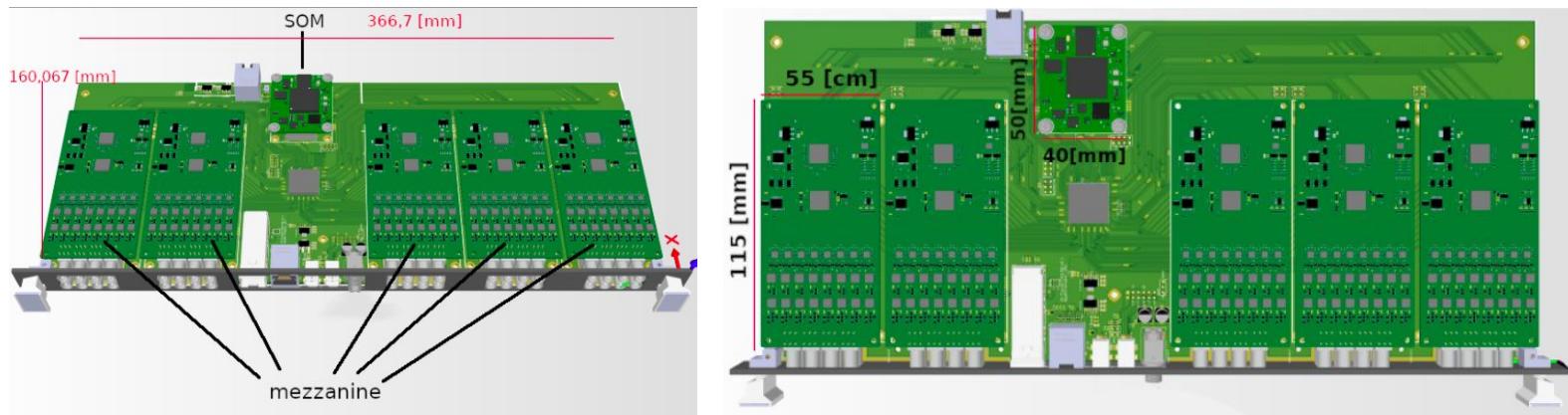
8: 3.3 [V] ext	6:	4: M_MISO	2: M_MOSI
7: GND	5:	3: M_SCLK	1: M_nCS

MINI IO right: JTAG signals

8: MIO15	6:TCK	4: TDO	2: TMS
7: GND	5:MIO0	3: VCCJTAG	1: TDI

CMB Physical description

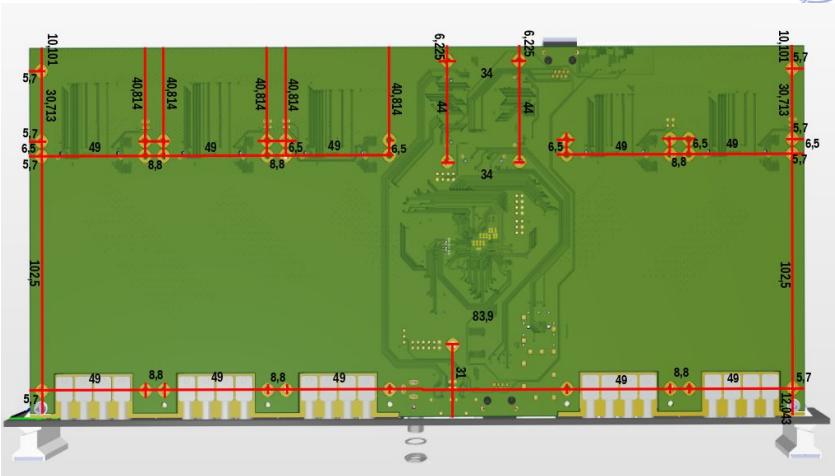
- The CMB motherboard corresponds to a **160,0 [mm] x 366,7 [mm]** PCB board
- Composed of **7 boards**: 1 main board (CMB Motherboard), 5 mezzanines (8 channel DRS4-based boards) and 1 commercial SoM Trenz TE0715 (Also can be used TE0712 or TE0720)
- Front panel corresponds to a **418,8[mm] x 19,4 [mm]** aluminum panel, with 2 plastic pins at each side



CMB: Physical description

- Complies with the **VME standard**
- 37 x 3,2 [mm] size hole for screws placement

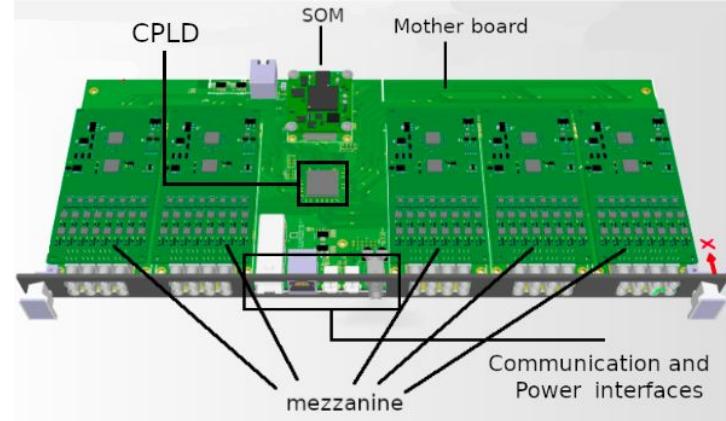
- Front holes for attachment of the front panel on the racks.



Motherboard: electrical interfaces

Motherboard features

- CPLD for multiplexing signals from mezzanines
- Connections for interchangeable mezzanines and SoM
- Communication and power interfaces



Component	Specification	Connection to/from CMB Motherboard
Mezzanines	Each mezzanine has 4 double Lemo connectors (total of 8 Lemo input channels)	100 pin Samtec Razor beam connector
SoM	TE0715-04-52I33-A or similar	Samtec Razor beam connector
Communication and power interfaces	Specified in CMB front view	Part of CMB motherboard
CPLD	Lattice MachXO3D Family CPLD LCMXO3L-9400C-5BG484C	Part of CMB motherboard

Motherboard: Power scheme

4 to 6 V input from power supply.

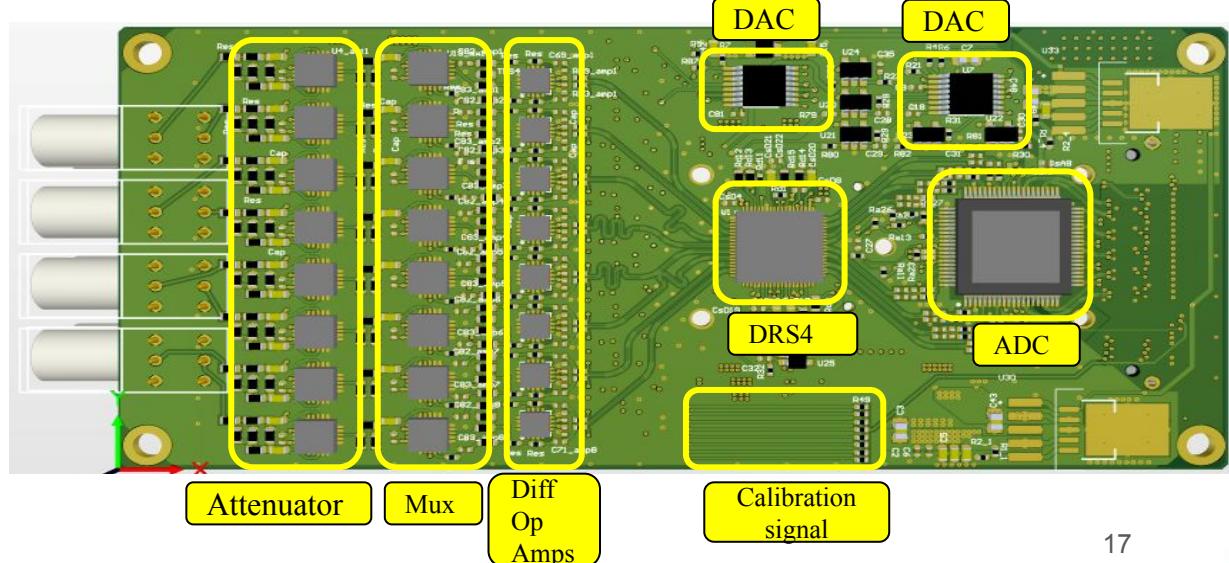
LDO voltage adj regulator rad tolerant will be used to supply Xilinx SoM, IO banks, CPLD and for external device connection with SPI protocol available in Mini IO socket.

Regulator	Voltage	Current consumption
MCP1826	3.3 [V] SoM core supply	550 [mA]
MCP1826	2.5 [V] SoM IO Banks	300 [mA]
MCP1826	2.5 [V] CPLD	150 [mA]
MCP1826	3.3[V] external	800 [mA]
	Total	1.9 [A]

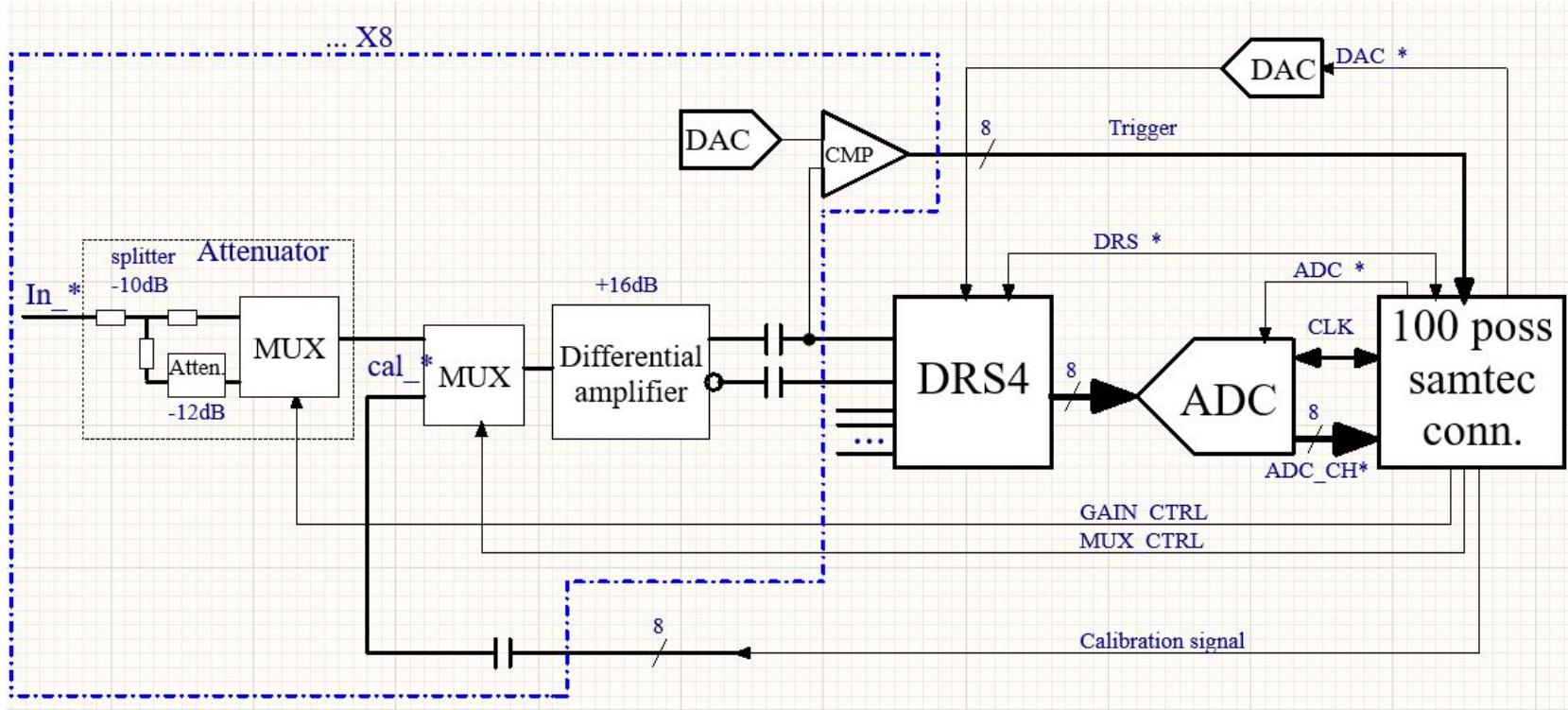
Mezzanine: Overview

Mezzanine features

- **DRS4 based** signal acquisition
- **8 lemo 00 inputs** + external calibration.
- Signal conditioning stage
- Controlled by SoM in motherboard
- 115 [mm] x 55 [mm]



Mezzanine: Schematic diagram



* Detailed information of each block in SPR

Mezzanine: power scheme

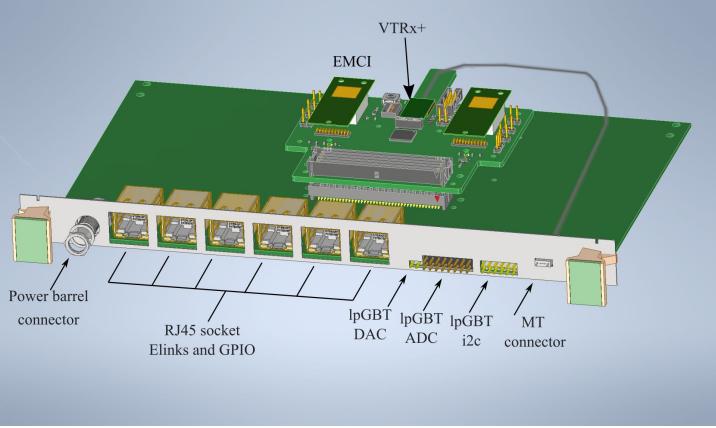
4 to 6 [V] input from the 100 poss connector samtec. LDO rad tolerant will be used, some are adjustable and other fixed (LP3990)

Regulator	Voltage	Current consumption
LP3990-3.3	3.3 [V] V_A Mux	0.008 [mA]
LP3990-3.3	3.3 [V] V_B DAC and op amp	5 [mA]
LP3990-2.5	2.5 [V] V_A DRS4	10 [mA]
LP3990-2.5	2.5 [V] D_A op amp trigger	30 [mA]
MCP1826	2.5 [V] D_B DRS4	150[mA]
MCP1826	1.8 [V] ADC AVDD	230 [mA]
MCP1826	3.3 [V] V_C diff op amp	320 [mA]
MCP1826	1.8 [V] ADC DVDD	150 [mA]
	Total	746[mA]

EMCI Carrier board: Electrical interfaces

EMCI carrier board features

- EMCI Installed as a **mezzanine**.
- Located in same crates as the CMB.
- **Up to 6 CMB's** connection though Elinks and GPIO

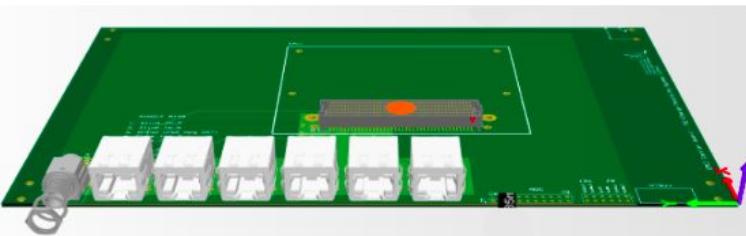


Component	Specification	Connection to/from CMB
RJ45	6 RJ45 T568B standard CAT5e MFG: SS-7188S-A-PG4-1-BA	Up to 6 CMB motherboard front end
FMC Connector	FMC HPC connector (10mm height version). Connection to EMCI	Not connected directly to CMB.
MTP adapter	MT to MT front panel adapter	Fiber optics to interface with EMP or FPGA based board with capability to connect with optical fiber.
DAC pin header	2 pin for pin header with DAC interface	Not connected to CMB
ADC pin header	16 pin pin header for ADC interface	Not connected to CMB
i2c pin header	12 pin pin header for i2c communication	Not connected to CMB
Power barrel connector	Barrel with screw 11 [A]. Internal pin diameter of 2 [mm]. Barrel outer diameter 6.4 [mm]	20

EMCI Carrier board: Electrical interfaces

EMCI carrier board features

- EMCI Installed as a **mezzanine**.
- Located in same crates as the CMB.
- **Up to 6 CMB's** connection though Elinks and GPIO

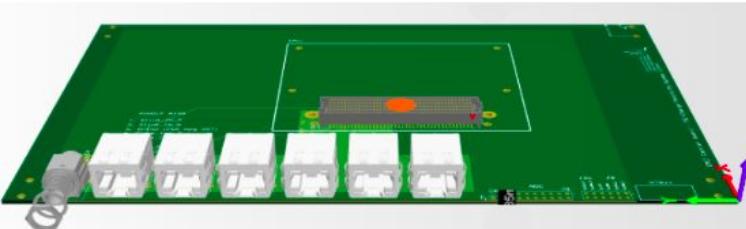


EMCI Carrier board: Electrical interfaces

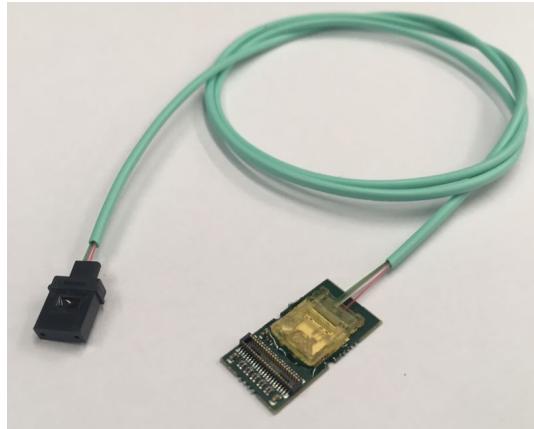
Two optical channels from MT in VTRx+ will be used (TX1 and RX1).

- For interface MT connector, a MT-MPO adapter will be used in test setup.
- For final setup, a MT-MT connection will be used as recommended in
<https://edms.cern.ch/ui/file/2149674/1/VTRxPlusApplicationNote.pdf>

To connect with optical fibers available in the Miniracks, different option will be studied depending of the investment. MT to 12 LC connector and one duplex LC-LC clamp.



VTRx+ connector from EMCI board

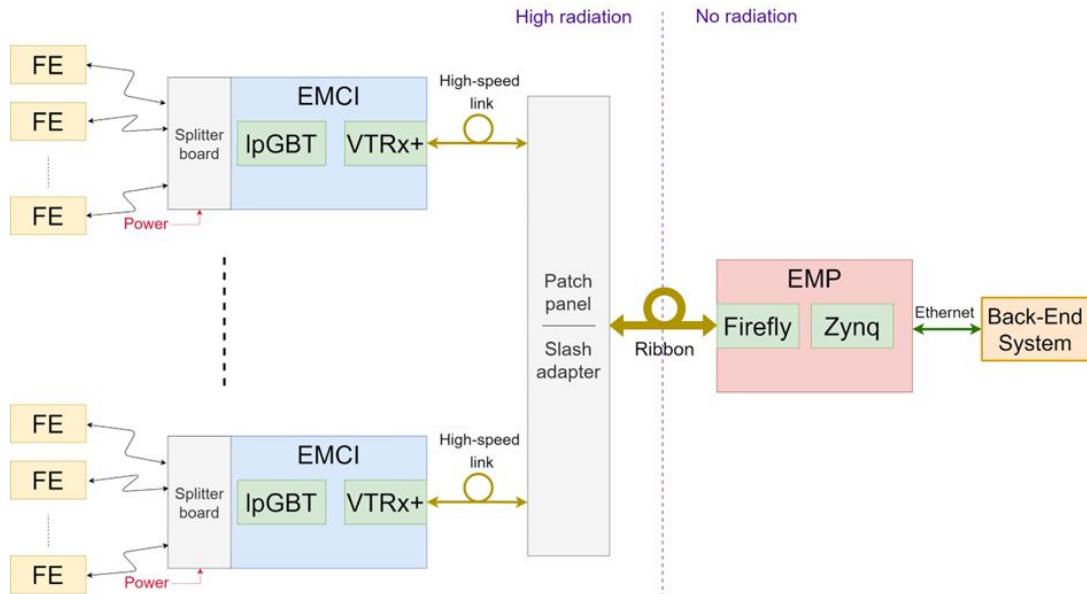


MT to MPO adapter



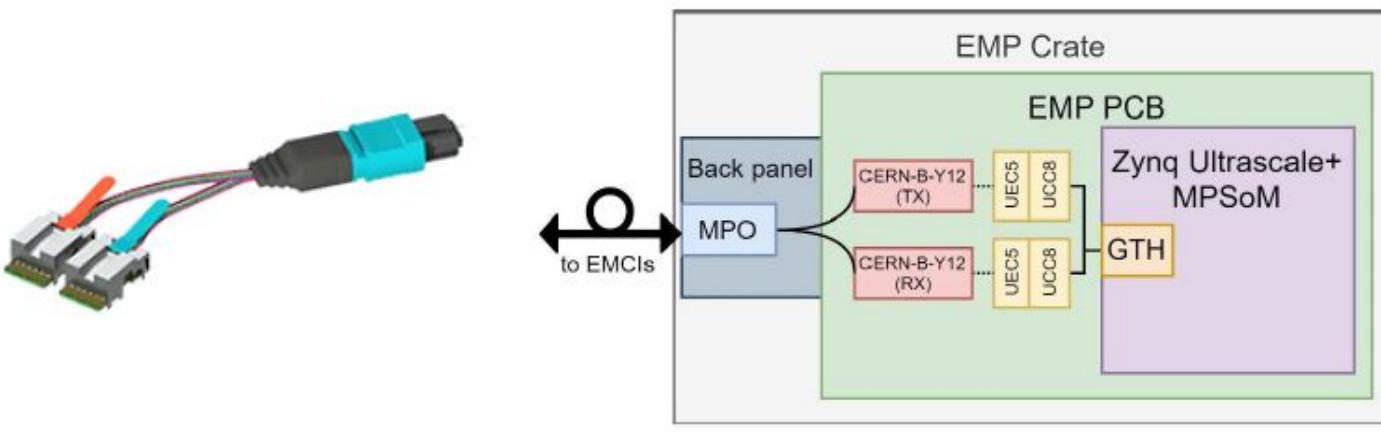
EMP-EMCI interface

Two LC fiber optics will be available from miniracks where EMCI will be placed to a patch panel tbd. 24 LC, from 12 EMCI board will be faced one MPO 24 channels from the patch panel.



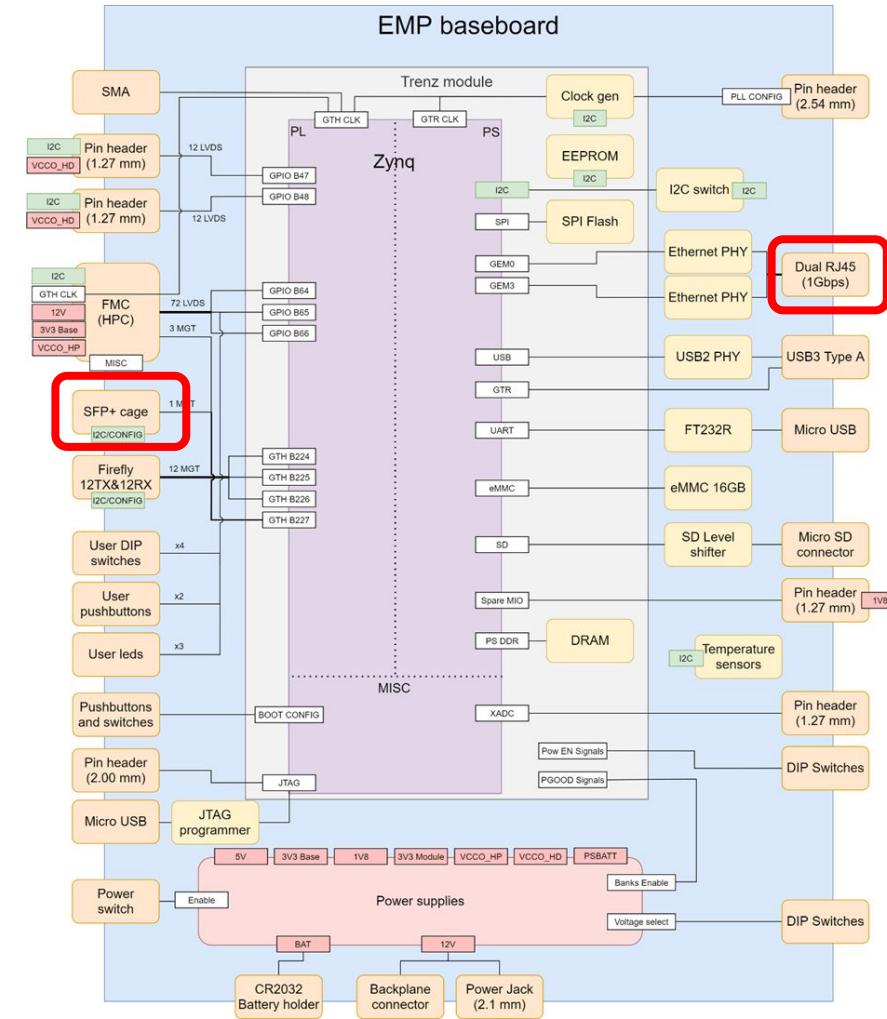
EMP-EMCI interface

Two LC fiber optics will be available from miniracks where EMCI will be placed to a patch panel tbd. 24 LC, from 12 EMCI board will be faced one MPO 24 channels from the patch panel.



EMP-Server-DCS

For Atlas DCS to control charge monitoring boards and access the data, a server connected to EMP will be used. The server will be connected to EMP board using the dual RJ45 socket or the SFP+ connector available.



Firmware

Main Targets:

- Capture analog pulse from ASD board controlling ICs in the CMB mezzanine board.
- Get pulse shape and integrate charge of pulses using data collected.
- Send data using standard communication protocols available.
- Calibration DRS4 cells.
- Firmware update.

Firmware

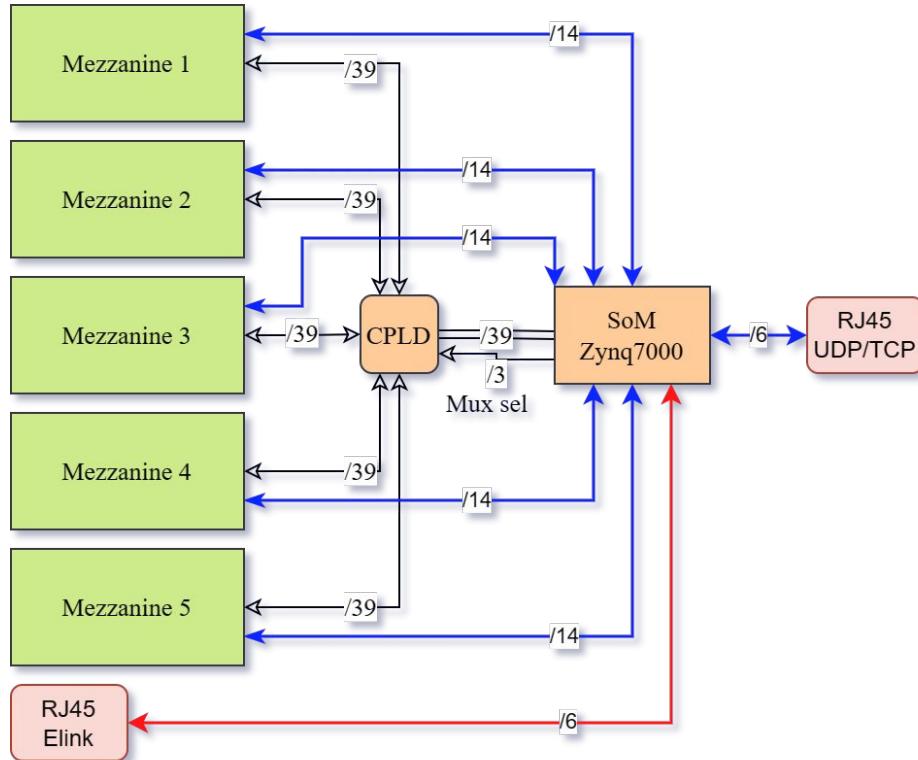
Two main programmable logic devices:

- CPLD, works as a multiplexer
- SoM, Zynq7000

Total of **46 digital signal** per mezzanine.
 Some are shared from SoM
 (SPI,i2c,reference clocks,...).

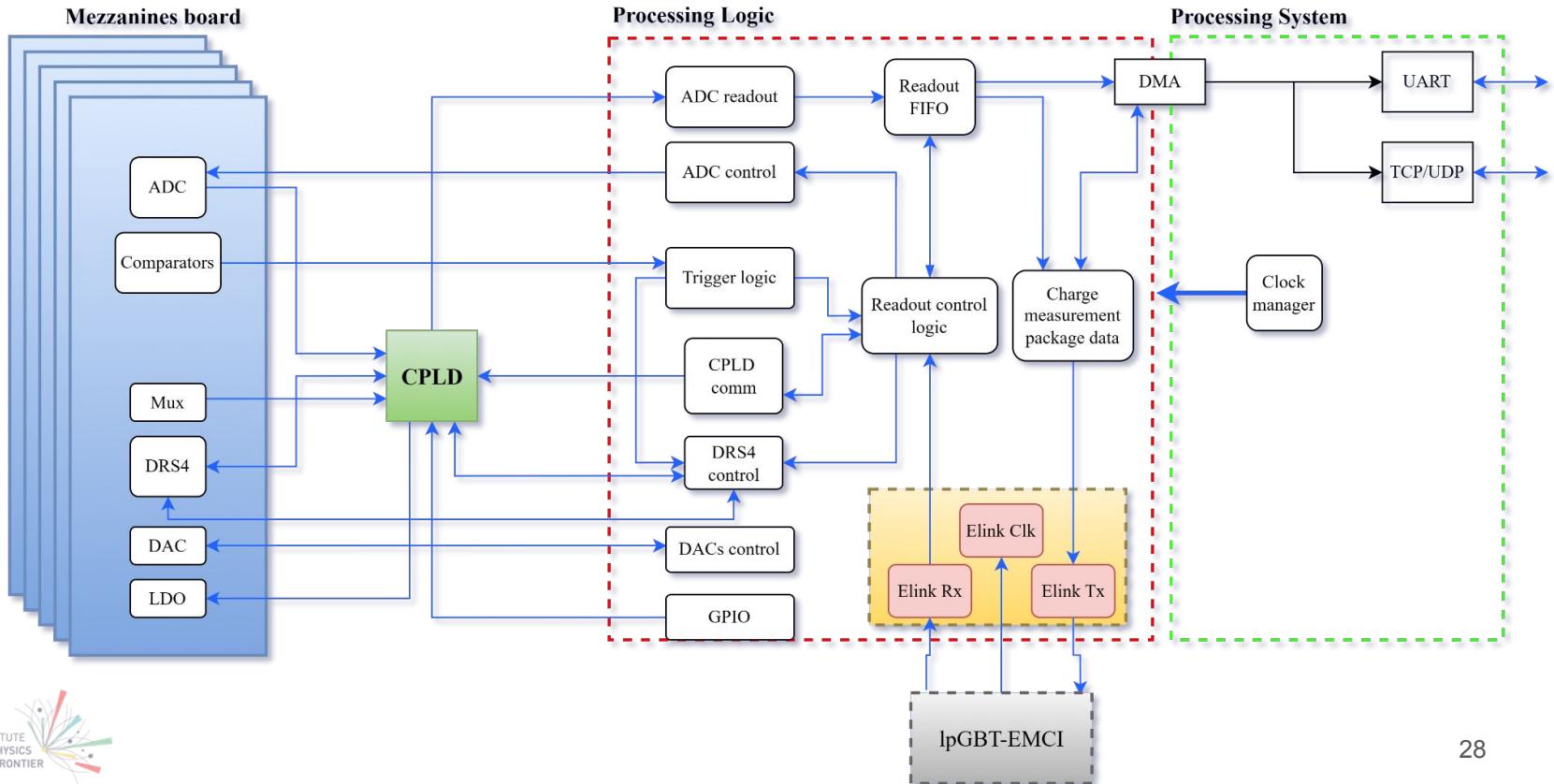
351 digital signal in total.

Mux_sel of 3 bits allows the selection of mezzanines signals that will be read and write by the SoM.



Digital signals to CPLD and Zynq7000

Firmware: SoM diagram



Firmware: Resources estimate

SoM Trenz TE0715

Resource	Utilization	Available	Utilization %
LUT	9568	46200	20.7
LUTRAM	322	14400	2.24
FF	8920	92400	9.8
BRAM	20	95	21.05
IO	146	150	97.3
DSP	48	160	30

CPLD Lattice
LCMXO3L-9400C-5BG484C

Resource	Utilization	Available	Utilization %
LUT	264	9400	4
Registers	332	10552	4
Slices	224	4700	4
BRAM	0	0	0
IO	205	384	54

The resource estimate was with use of Triple memory redundancy.

Firmware: Resources estimate

Payload per event per elink, using 12 bit adc

- Normal operation: 32 Bytes per event (trigger in the 8 channels of 1 mezzanine)
- Full readout mode: 13.2 KB per event (sent of 8 channels from 1 mezzanine)

Expecting 10 to 15 KHz between events:

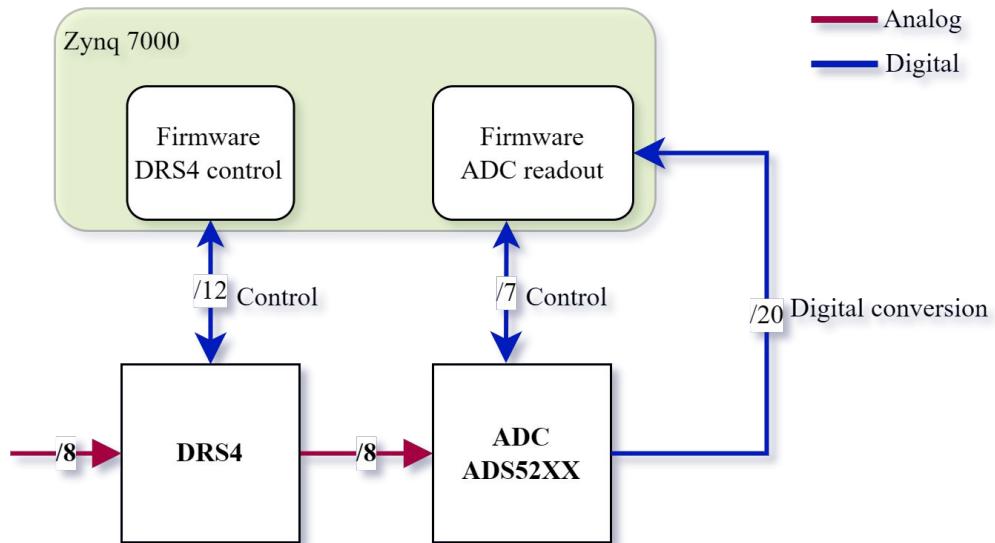
- Normal operation: 480KBps
- Full readout mode of 8 channels mezzanine: 198000 KBps

Readout of an event on TGC-CMB will take up to **50 us.**

Firmware: Analog readout

DRS4 will use 12 control signal, some will be multiplexed using CPLD (A[3:0],SRIN,...).

The digital signal of each channel of ADC will be read using the CPLD depending on which mezzanine the trigger occurs.

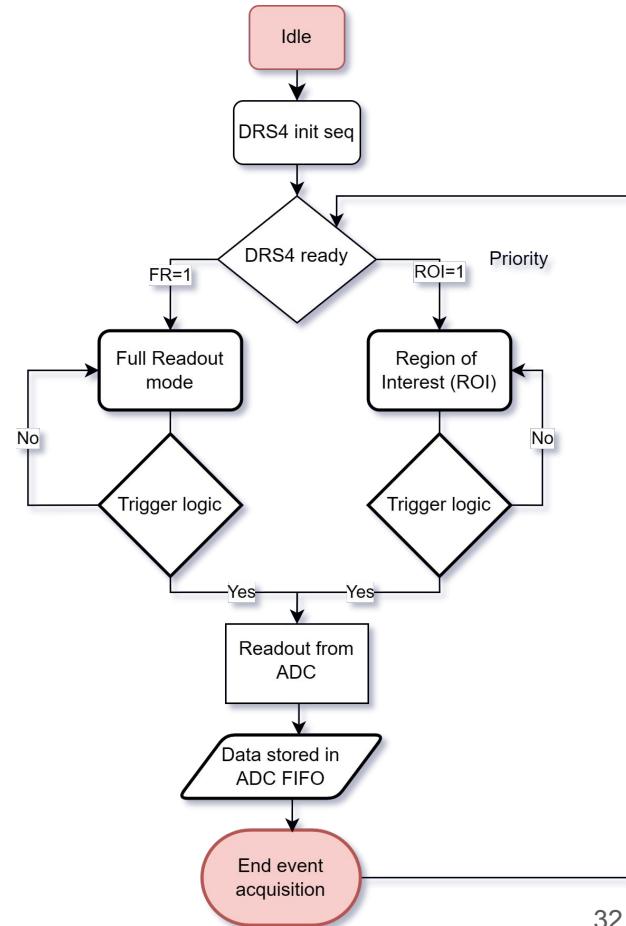


Firmware: Analog readout flow

The control of Mezzanine will follow the diagram described.

- First the initialization of the IC will be done.
- Wait for a triggers occurs.
- Read data from ADC and store on a FIFO.

DRS4 have two operation modes that will be used. **Full readout mode** always start acquisition from cell 0 to 1023. **ROI** allow to shorten the acquisition window and start from the cell when the trigger occurs.



Firmware: Calibration

Using the mux on the mezzanine, a calibration signal will be used for the following calibration tasks:

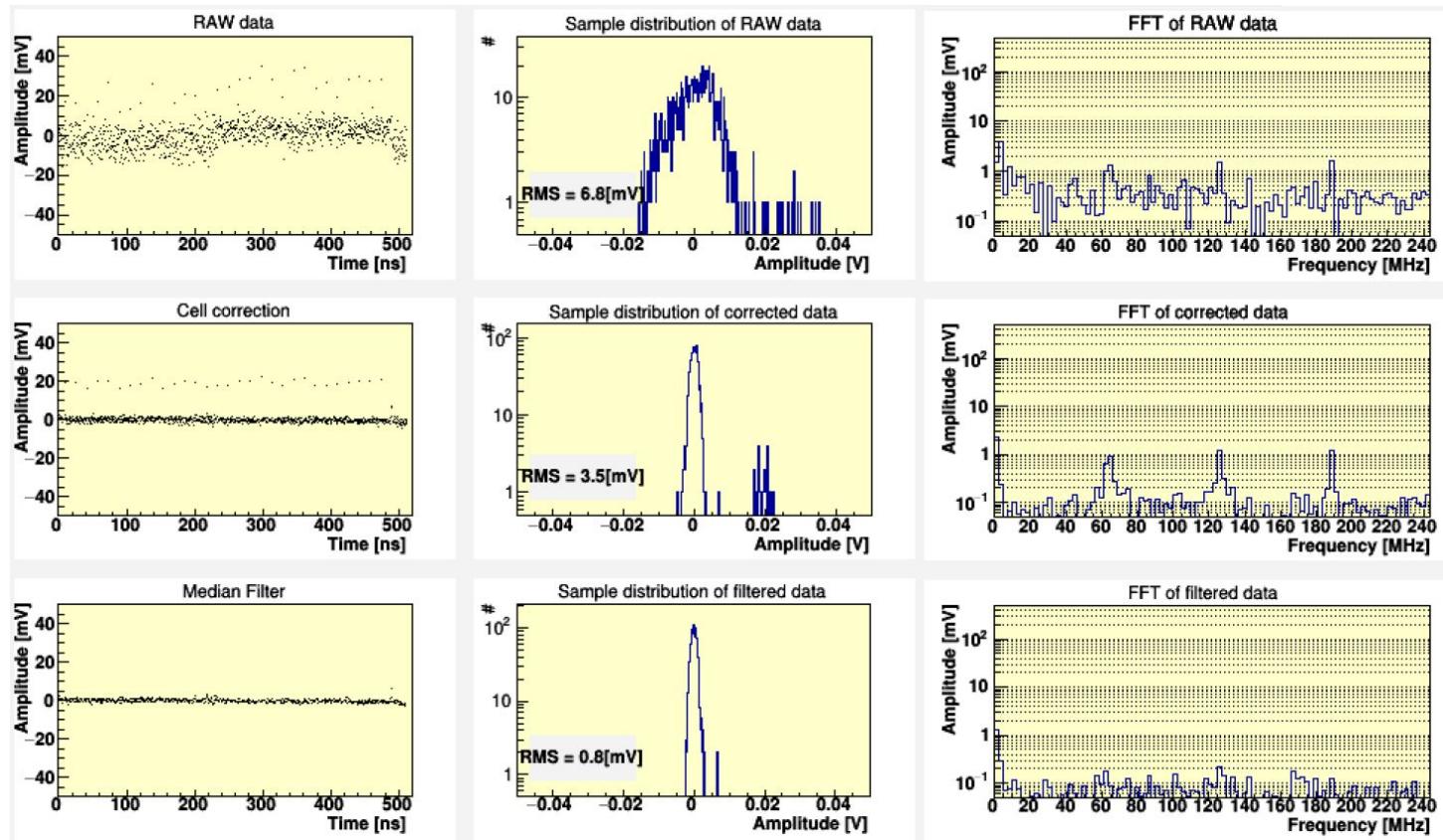
1. Cell offset voltage correction of the **1024** capacitor array of DRS4.

Fixed or ground voltage can be connected to 8 analog input of DRS4 using the mux and the TCal analog signal. The sampling data will be analyzed and stored on memory (Server, SoM, EMP) that will be used in normal operation to correct this values.

2. Timing and amplitude calibration using the external analog signal

Similar procedure, injecting a well defined frequency signal and low noise on TCal can be used to measure the different timing delay of the 8 channels of DRS4. The data will preferably be stored in an external memory (Server, SoM, EMP). The jitter of DRS4 should be less than 50 [ps] Even though **this is not considered an issue** for the selected bandwidth, the temporal correction would be particularly desired for precise timing applications.

Firmware: Calibration of DRS4 cells voltages



Firmware: Update

Two options can be used to update the firmware on SoM (CPLD will not be updated since it will operate as a mux).

1. Use the elinks connection to write on golden region of Trenz memory.
2. Use Jtag signals of the motherboard to update the SoM.

Firmware: Communication.

There are four ways to communicate with other boards, in priority order these are:

1. Main: **Elinks** with RJ45 socket (1 elink clock, 1 elink rx, 1 elink tx) **(1)**
2. Debug: **SFP+**
3. Debug:**TCP/UDP** using RJ45 socket **(Results presented later in prototypes section)**
4. Debug:**UART** using MIO on the SoM and and IO in PL **(Used in radiation tests at CHARM in 2022)**

Elink communication test will be performed using EMCI board connected to a TGC-CMB and a EMP board this year

Firmware: Communication.

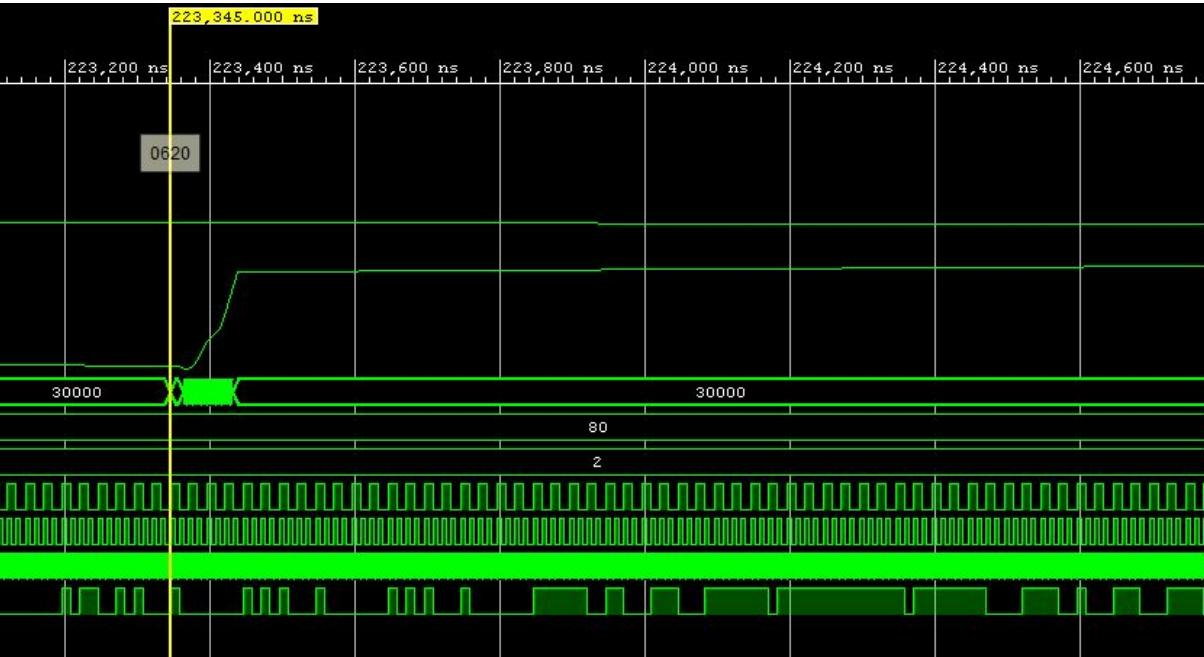
There are four ways to communicate with other boards, in priority order these are:

1. Elinks with RJ45 socket (1 elink clock, 1 elink rx, 1 elink tx)

Data received



Name	Value
> eedata[15:0]	0620
> elinkin16bit[15:0]	1301
> efifoDin[17:0]	01301
OutputDataRate	80
> elinkEncoding[1:0]	2
clk40	1
clk80	1
clk160	1
DATA1bitIN	1



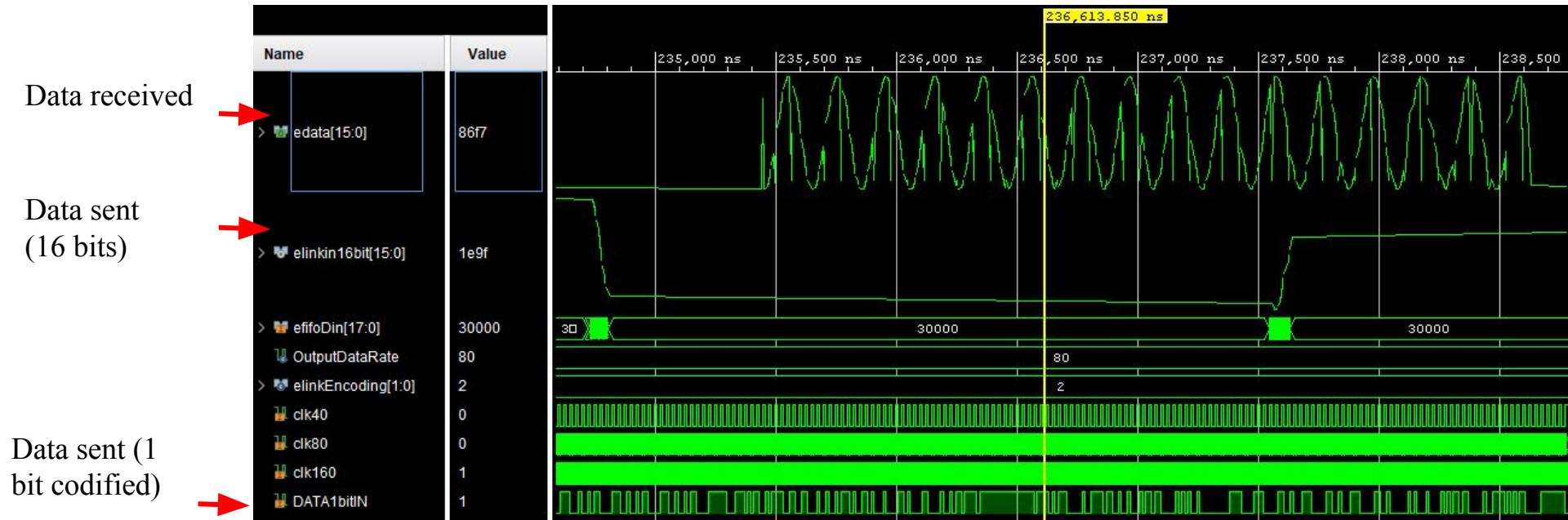
Data sent (1 bit codified)



Firmware: Communication.

There are four ways to communicate with other boards, in priority order these are:

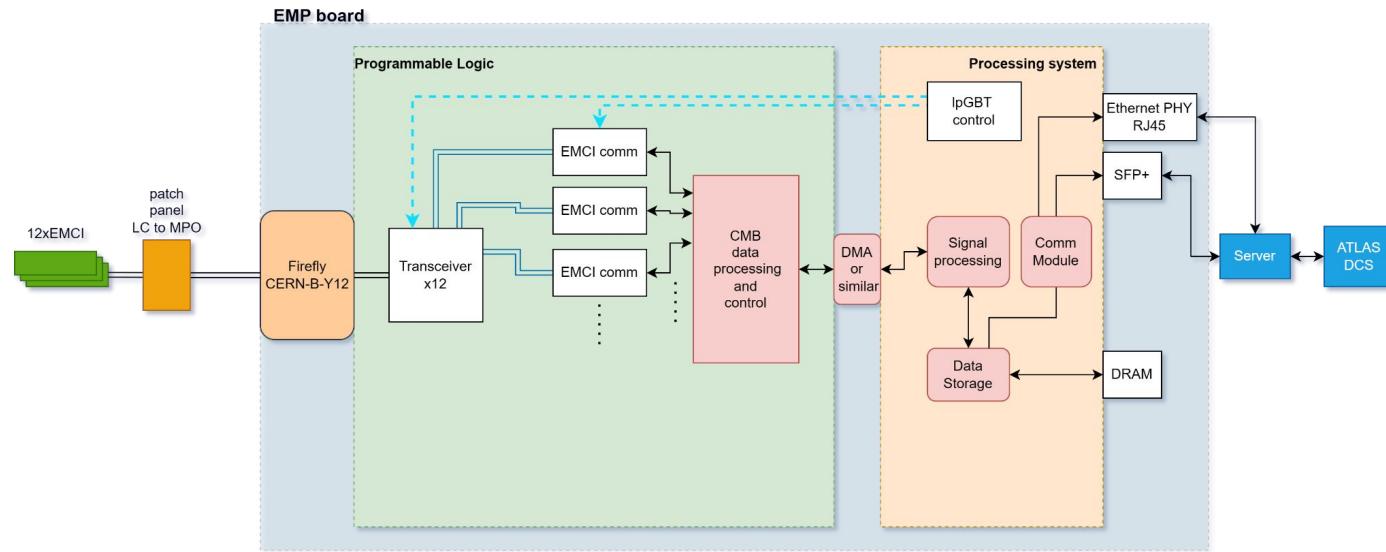
1. Elinks with RJ45 socket (1 elink clock, 1 elink rx, 1 elink tx)



Firmware: EMP-EMCI communication

In order to read the data from TGC-CMBs, we will use the IpCores development by EMP-EMCI team and develop RTL modules to recover the data from each TGC-CMB that EMP can handle ($12 \times 4 = 48$).

We will split each TGC-CMB data and using DMA or similar module available on EMP board MPSoC TE0807 we will send the data to the processing system in which we will do a signal processing to each TGC signals before sending to the Server.



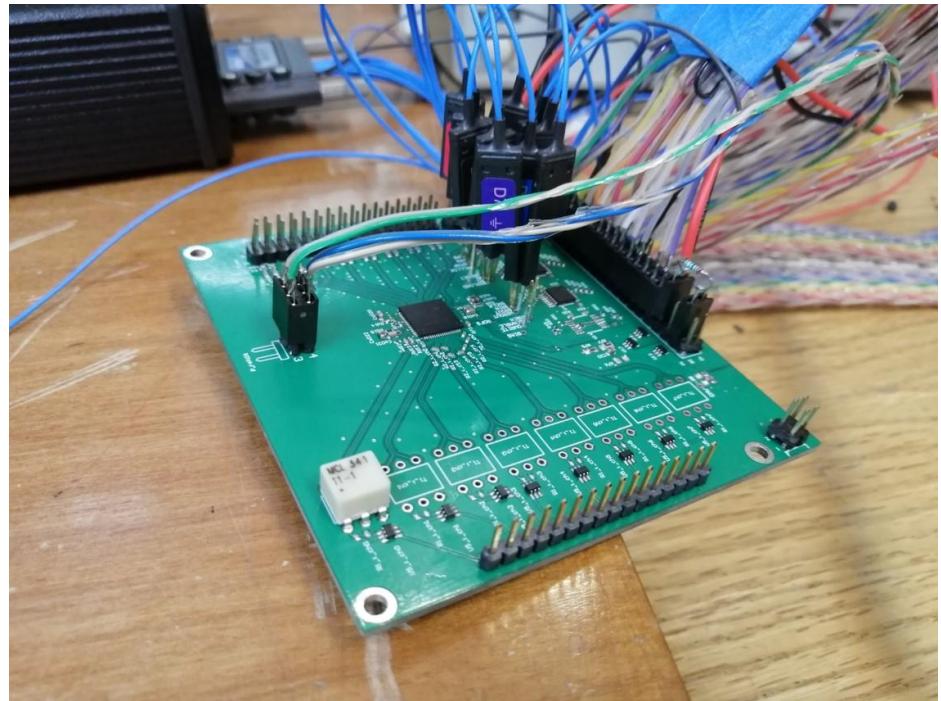
Prototypes development

6 prototypes boards were developed:

1. DRS4 breakout board
2. CPLD breakout board
3. 4 channels mezzanine with Vita 57.1 standard connector.
4. 8 channels mezzanine board.
5. 2 mezzanine motherboard.
6. Full prototype motherboard up to 5 mezzanine connections.

Prototypes development: DRS4 breakout board

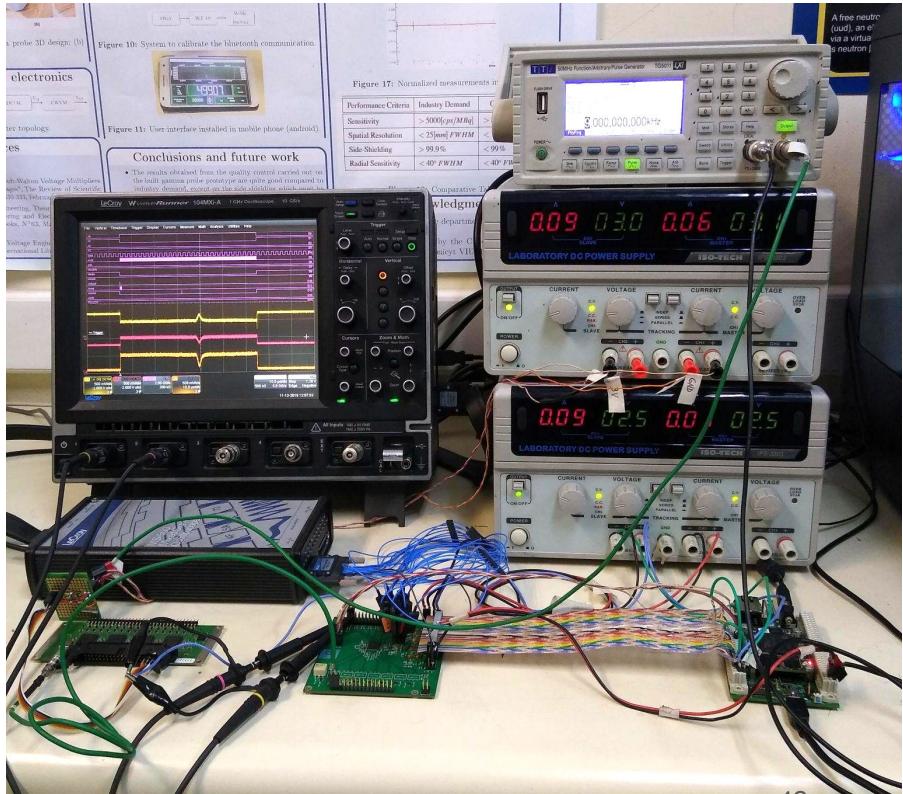
Purpose: Control DRS4 using one channel for test acquisition, measurement control signals and differential analog output of the chips



Prototypes development: DRS4 breakout board

The setup consists on:

- DRS4 baseboard.
- Trenz Artix7 with carrier board TE0703 to control DRS4.
- ASD board, connected to DRS4 baseboard and signal generator.
- Signal generator, pulses of 500 mV amp, 5 ns rise time, 20 ns on time, 15 ns fall time.
- Two power supplies.
- Oscilloscope with digital probes.



Prototypes development: DRS4 breakout board

Pulse generated by ASD was captured by DRS4 and measured on the oscilloscope.

Ch1: out1_n of DRS4

Ch2: out_p of DRS4

digital signals measurement the DRS4 inputs and output control signals.

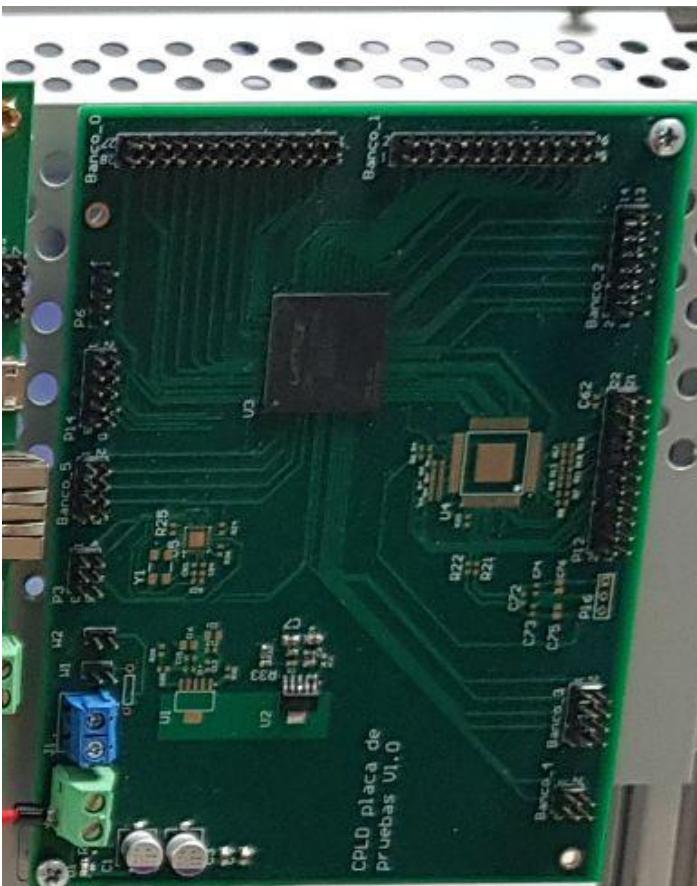


Prototypes development: CPLD breakout board

Development to test the CPLD that will be used in the 5 mezzanines motherboard as a multiplexer.

The model is **LCMXO3L-9400C-5BG484C**

Used in radiation test at CHARM and basic programming test.

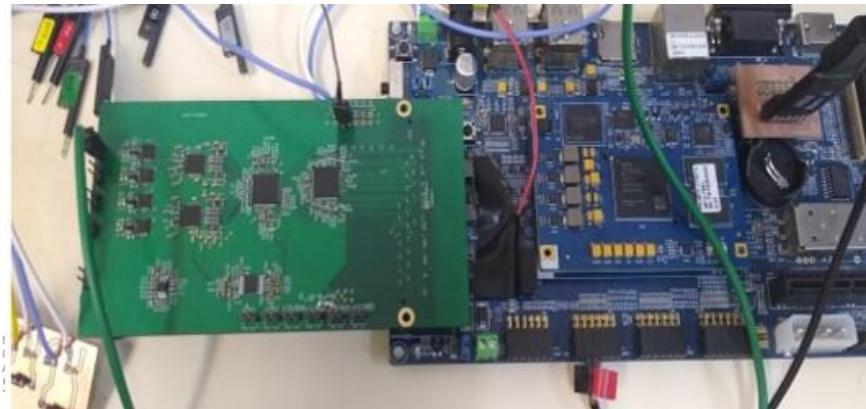


Prototypes development: 4 chann. mezzanine

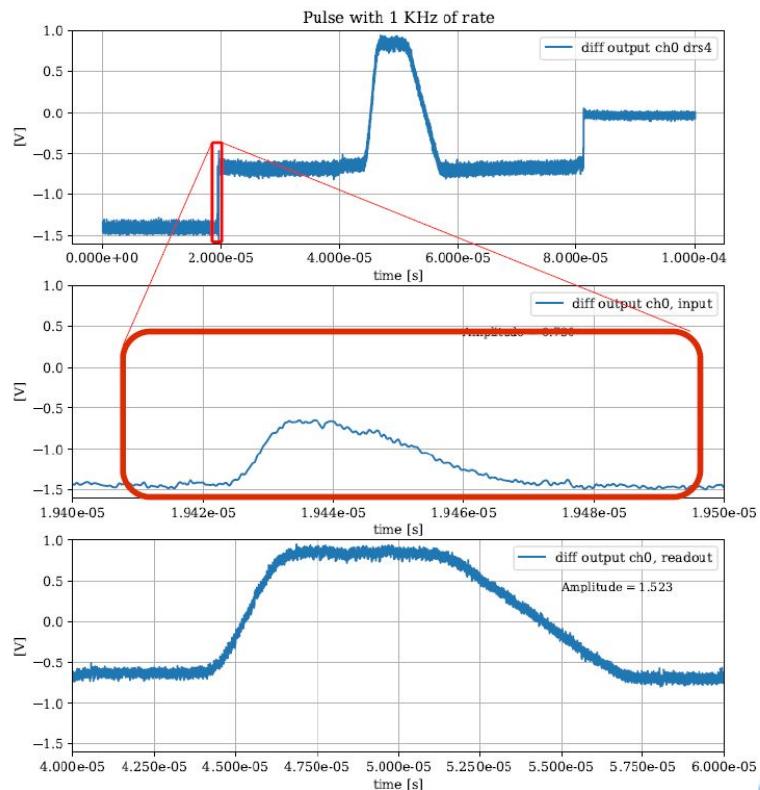
Input stage with diff op amp and mux

ADC ads5296 12 bit resolution and DRS4 chip.

Development board MYD-C7Z015 with xilinx XC7Z015



45



Prototypes development: 8 ch Mezzanine

Based on the design
presented in previous slides.

This version comes with sine
wave and pulse generator for
initial tests. Standard pin
header input connector for
tests.



Prototypes development: 2 mezzanine motherboard

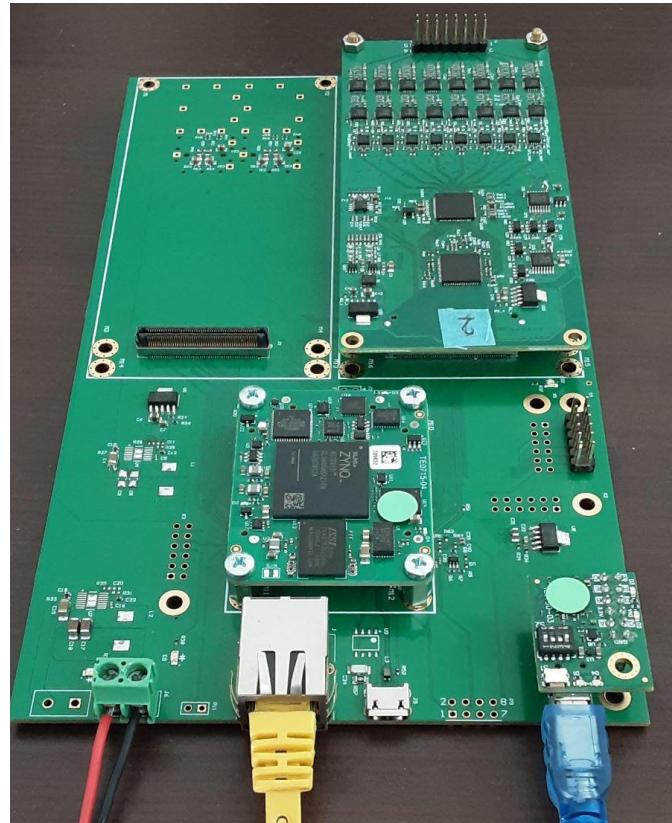
Capability for 2 mezzanine of 8 channel each.

Compatible with trenz board

TE0712,TE0715 and TE0720 depending on the requirement.

Interfaces available:

- SFP+, SPI pin headers, SD card headers, mini USB master, Xilinx Jtag and RJ45 connected to Processing system.



Prototypes development: 2 mezzanine motherboard

The physical connection is an Unshielded-Twisted-Pair (UTP) cable connected to the Gigabit Ethernet interface. Our tests show that the the Zynq system takes about 650µs to transmit a payload of 40 kB for a single event split in multiple Ethernet frames of 1500 bytes

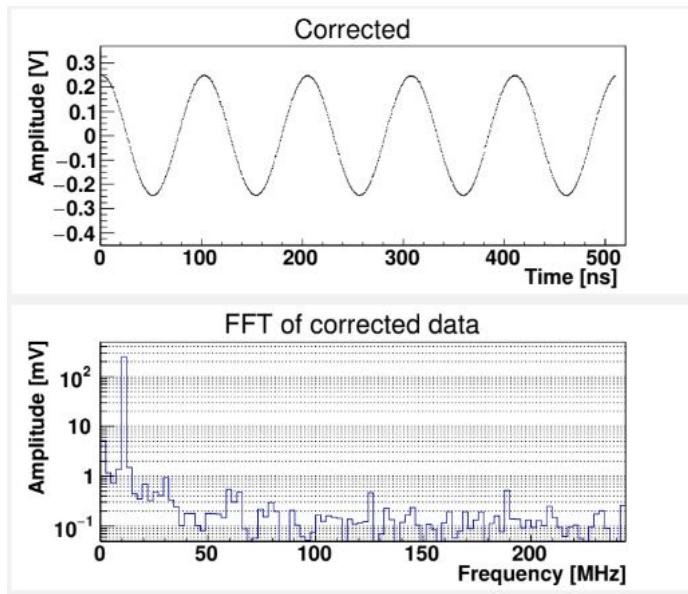
No.	Time	Source	Destination	Protocol	Length	Info
6	0.191152	192.168.1.10	192.168.1.5	TCP	1500	6543 → 61791 [ACK] Seq=1447 Ack=11 Win=49990 Len=1446
7	0.191152	192.168.1.10	192.168.1.5	TCP	1500	6543 → 61791 [ACK] Seq=2893 Ack=11 Win=49990 Len=1446
8	0.191265	192.168.1.5	192.168.1.10	TCP	54	61791 → 6543 [ACK] Seq=11 Ack=4339 Win=65070 Len=0
9	0.191748	192.168.1.10	192.168.1.5	TCP	1500	6543 → 61791 [ACK] Seq=4339 Ack=11 Win=49990 Len=1446
10	0.191765	192.168.1.5	192.168.1.10	TCP	54	61791 → 6543 [ACK] Seq=11 Ack=5785 Win=65070 Len=0
11	0.191786	192.168.1.10	192.168.1.5	TCP	1500	6543 → 61791 [ACK] Seq=5785 Ack=11 Win=49990 Len=1446
12	0.191786	192.168.1.10	192.168.1.5	TCP	1500	6543 → 61791 [ACK] Seq=7231 Ack=11 Win=49990 Len=1446
13	0.191786	192.168.1.10	192.168.1.5	TCP	1500	6543 → 61791 [ACK] Seq=8677 Ack=11 Win=49990 Len=1446
14	0.191811	192.168.1.5	192.168.1.10	TCP	54	61791 → 6543 [ACK] Seq=11 Ack=10123 Win=65070 Len=0
15	0.191843	192.168.1.10	192.168.1.5	TCP	1500	6543 → 61791 [ACK] Seq=10123 Ack=11 Win=49990 Len=1446
16	0.191843	192.168.1.10	192.168.1.5	TCP	1500	6543 → 61791 [ACK] Seq=11569 Ack=11 Win=49990 Len=1446
17	0.191865	192.168.1.5	192.168.1.10	TCP	54	61791 → 6543 [ACK] Seq=11 Ack=13015 Win=65070 Len=0
18	0.191891	192.168.1.10	192.168.1.5	TCP	1500	6543 → 61791 [ACK] Seq=13015 Ack=11 Win=49990 Len=1446
19	0.191905	192.168.1.5	192.168.1.10	TCP	54	61791 → 6543 [ACK] Seq=11 Ack=14461 Win=65070 Len=0
20	0.191924	192.168.1.10	192.168.1.5	TCP	1500	6543 → 61791 [ACK] Seq=14461 Ack=11 Win=49990 Len=1446
21	0.191924	192.168.1.10	192.168.1.5	TCP	1500	6543 → 61791 [ACK] Seq=15907 Ack=11 Win=49990 Len=1446
22	0.191924	192.168.1.10	192.168.1.5	TCP	1500	6543 → 61791 [ACK] Seq=17353 Ack=11 Win=49990 Len=1446
23	0.191950	192.168.1.5	192.168.1.10	TCP	54	61791 → 6543 [ACK] Seq=11 Ack=18799 Win=65070 Len=0
24	0.191972	192.168.1.10	192.168.1.5	TCP	1500	6543 → 61791 [ACK] Seq=18799 Ack=11 Win=49990 Len=1446
25	0.191972	192.168.1.10	192.168.1.5	TCP	1500	6543 → 61791 [ACK] Seq=20245 Ack=11 Win=49990 Len=1446
26	0.191972	192.168.1.10	192.168.1.5	TCP	1500	6543 → 61791 [ACK] Seq=21691 Ack=11 Win=49990 Len=1446
27	0.191972	192.168.1.10	192.168.1.5	TCP	1500	6543 → 61791 [ACK] Seq=23137 Ack=11 Win=49990 Len=1446
28	0.192004	192.168.1.5	192.168.1.10	TCP	54	61791 → 6543 [ACK] Seq=11 Ack=24583 Win=65070 Len=0

Successful received data packets

Prototypes development: 2 mezzanine motherboard

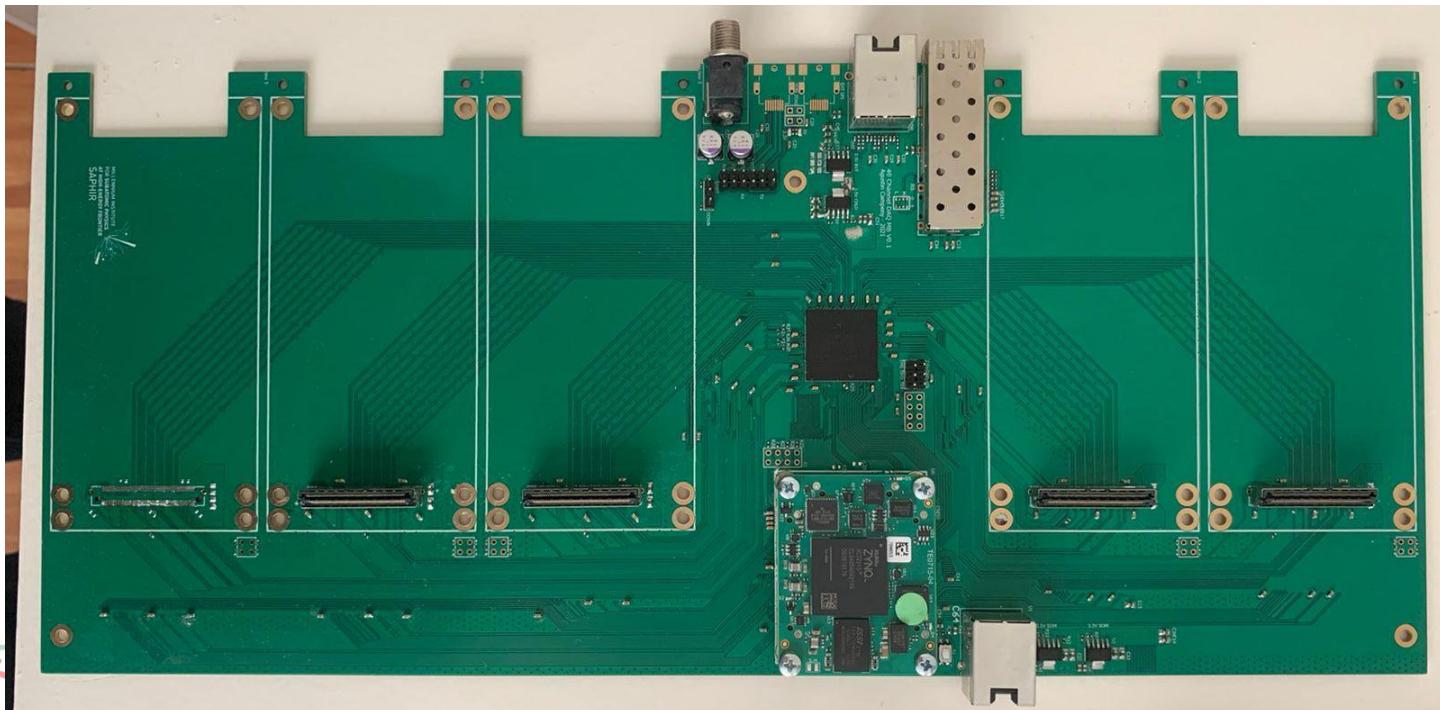
The physical connection is an Unshielded-Twisted-Pair (UTP) cable connected to the Gigabit Ethernet interface. Our tests show that the the Zynq system takes about $650\mu\text{s}$ to transmit a payload of 40 kB for a single event split in multiple Ethernet frames of 1500 bytes

Successful received data packets



Prototypes development: Full prototype CMB-5mezz

Full prototype assembled and under tests.

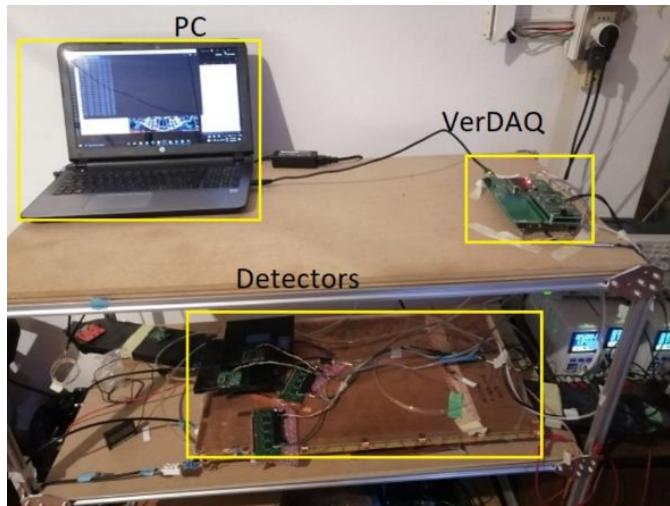


Prototypes development: 2 mezzanine motherboard

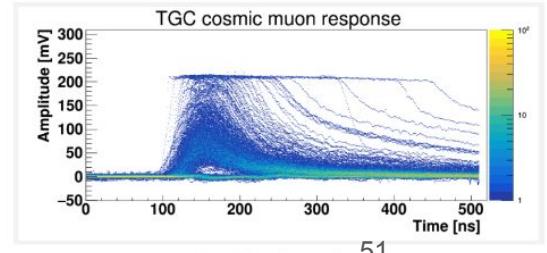
Prototype setup to test CMB-2mezz motherboard with one CMB-mezz board connected to TGC detector.

Ref article:

<https://iopscience.iop.org/article/10.1088/1748-0221/17/01/P01023>



(a) Experimental Setup



Data monitoring

The output data from CMB will be sent to the ATLAS DCS through the EMCI using Elinks or IpGBT, and the EMP that collect the data of EMCIs.

EMP will send the data to a server, probably location on USA15.

From the DCS we will be able to access to the data and operate the CMB under different operation modes as described in SPR document:

1. Charge delivering
2. Full waveform
3. Debug
4. Calibration mode
5. Firmware Update

Radiation tests

We will perform radiation tests on an entire mezzanine board connected to a TGC-CMB of 16 channels prototype motherboard and a breakout board for CPLD. IC shortage unable us to do test on each component.

The tests carried out consist in the following:

- Monitor the data generated by the DUT (CPLD breakout board and TGC-CMB prototype).
- Monitor the current of the system using desktop digital multimeter (DMM) for each board.
- Power reboot if data are corrupted or the current change from normal operation.

If more IC are available, we will perform radiation test on each component designed special board for it.

Radiation tests

TGC-CMB will use LDO of the same family of the already tested under radiation environment:

- MCP1826T (<https://edms.cern.ch/document/1583269/1>) TID test
- LP3990-1.8 (<https://edms.cern.ch/document/1231452/1>) .

TGC-CMB will use voltage regulators MCP1826ADJ, LP3990-2.5 and LP3990-1.8

Flash memory from the same family that uses the SoM (S25FL256S) was tested by PSI
<https://edms.cern.ch/document/2015835/1>. The flash S25FL256L, could not complete erase memory operation over **300 Gy**.

Radiation tests

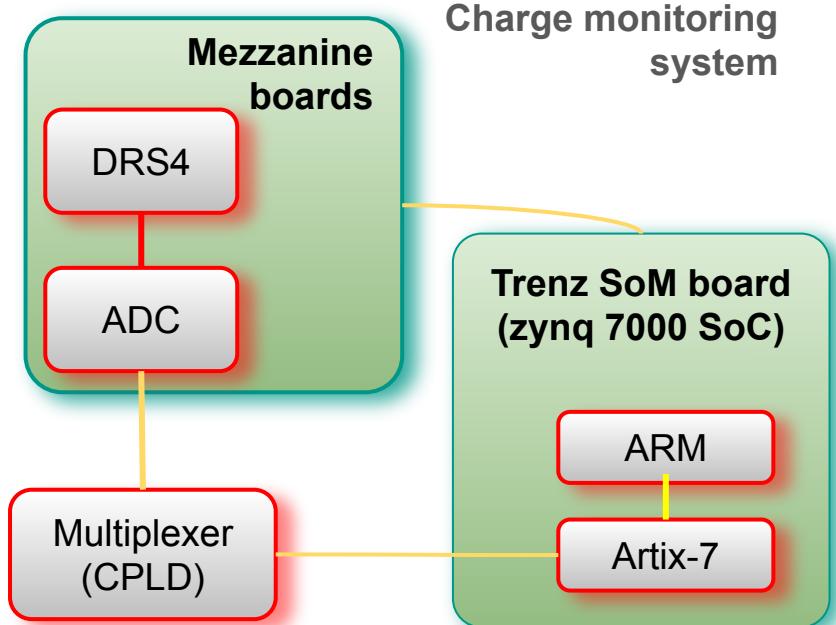
The critical components of the system are:

- DRS4, ADCs and DACs for the Mezzanine;
- CPLD for the motherboard
- The ARM processor and the Artix-7 FPGA in the Zynq SoC within the commercial SoM Trenz TE0715

The target radiation tolerant criteria (RTC) is estimated according to the location : TGC M1 mini rack (R~12m and Z = 11m) considering luminosity of 3000 fb^{-1}

We carried out 3 irradiation campaigns in the CHARM facility at CERN, using 2 configurations:

1. The whole system (CMB-16ch) without CPLD,
2. The CPLD.



	TID (Gy)	NIEL n/cm ²	SEE part./cm ²
SRL	4.1	1.1E+11	1.6E+10
SF _{sim}	1.5	2	2
SF _{ldr}	5	1	1
SF _{lot}	4	4	4
RTC	123	8.8E+11	1.3E+11

Radiation test: Component tested

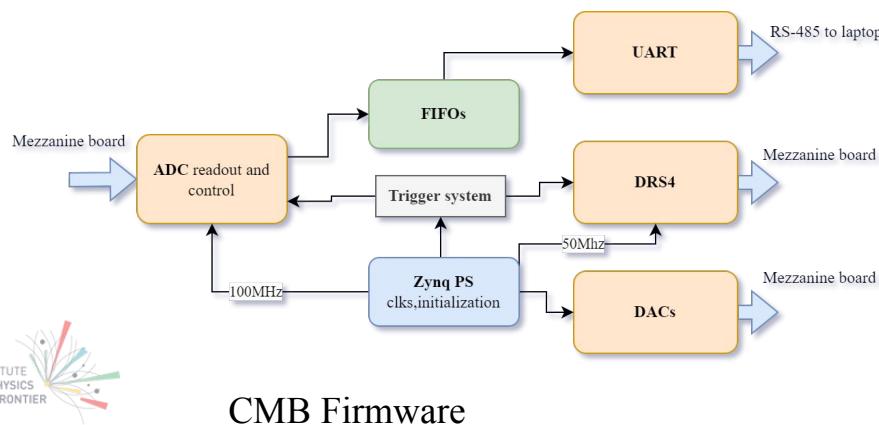
Component	Model	Qty
Multiplexer	4257-52	8
Op amp	THS4509	8
Op amp	TSH341ILT	1
Op amp	AD8605ARTZ-REEL7	5
Op amp	ADCMP600BKSZ-REEL7	8
DAC	DAC7678	2

Component	Model	Qty
Voltage regulator	LP3990-2.5	2
Voltage regulator	LP3990-3.3	2
Voltage regulator	MCP1826ADJ	7
SoM	TE0715-04-52I33	1
CPLD	LCMxo3L-9400C-5BG484C	1
Comparators	ADCMP600BKSZ-REEL7	8

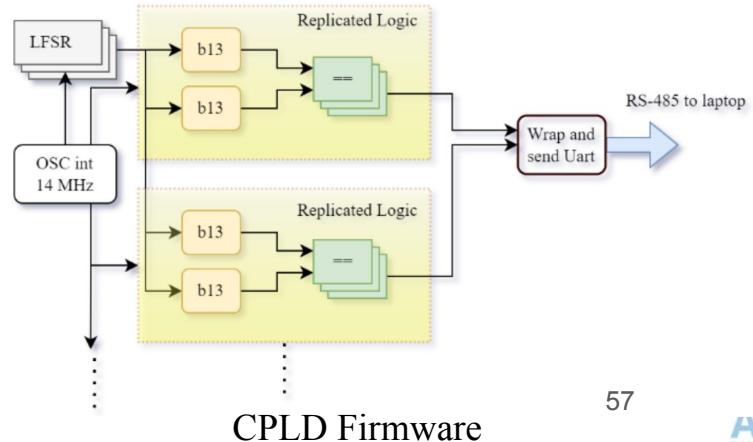
Radiation tests: Firmware used

For the **CMB test**, a **full readout waveform** was done using an UART on the processing logic for the communication. The RS485 protocol was implemented to send data over long distance (~100m).

For **CPLD testing**, no external input was used, a **build-in self test** (BIST) firmware was used instead. Benchmark circuits taken from CAD group of Politecnico di Torino (**B13: ITC'99 benchmark**, <https://github.com/squillero/itc99-pol>) were feed by a common random input, then, their outputs were passed through a comparator and the result registered, following the work from A. Scialdone et al. <https://doi.org/10.1109/TNS.2022.3162037>



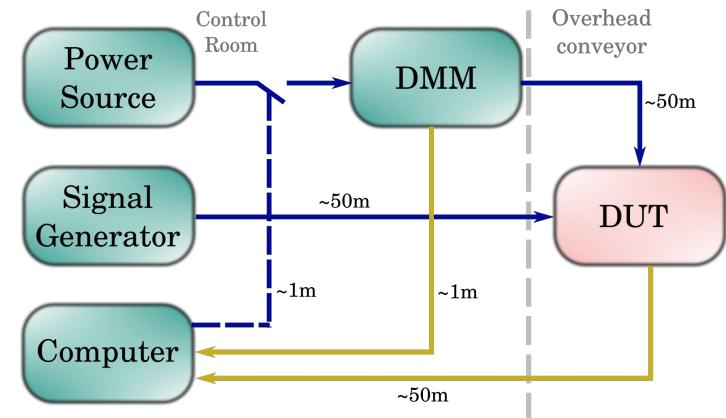
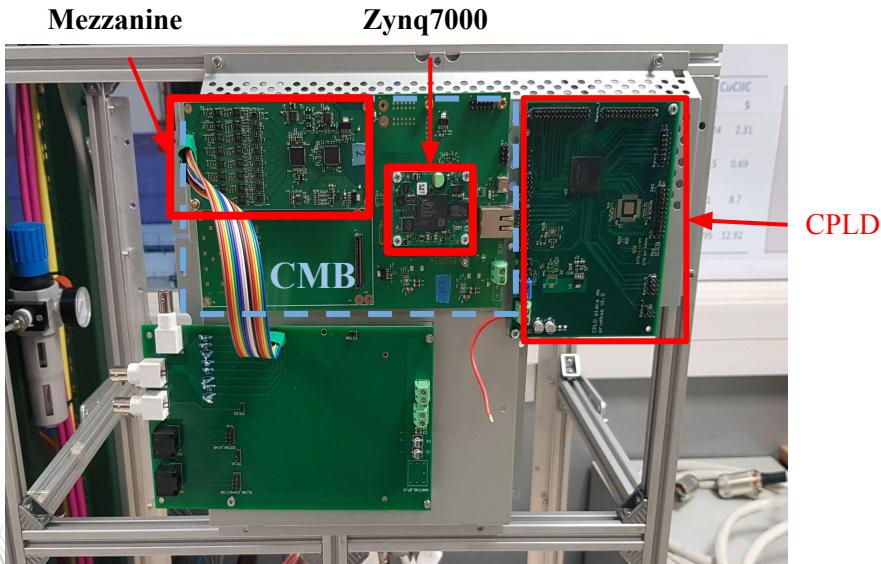
CMB Firmware



CPLD Firmware

Radiation tests: Common configuration for the DUT

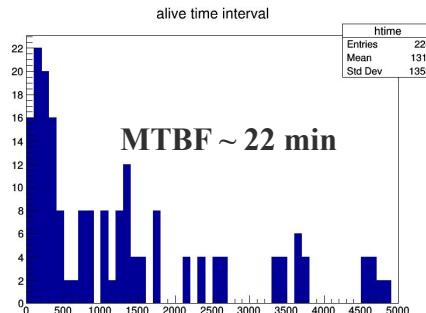
The DUTs current consumption was monitored together with their respective outputs. For the CMB the tests includes the input from a signal generator, while for the CPLD a self contained tests was carried out.



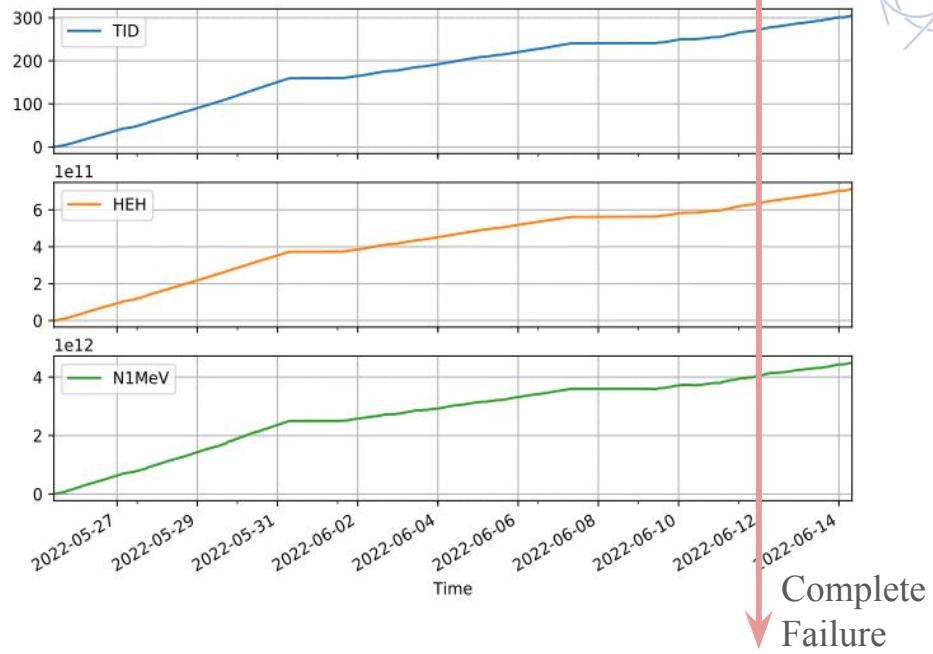
SoM Trenz TE0715 Tests

The CMB together with the SoM surpass the RTC level during the first campaign. During this campaign, the first 106 Gy included the mezzanine, after that point, the test continues up to 271 Gy where the SoM suffered a complete failure.

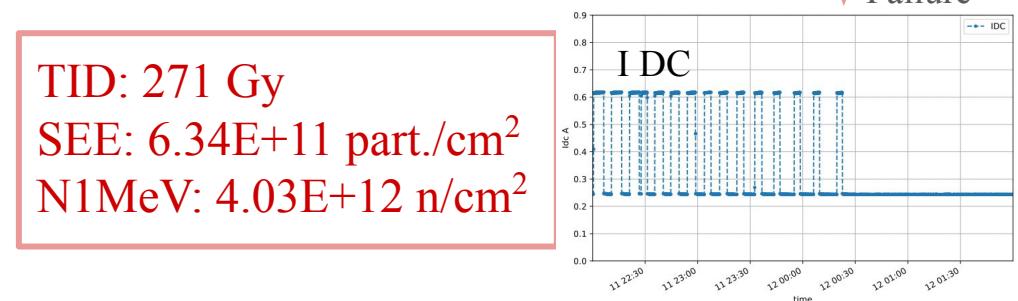
The MTBF was about 22min which is equivalent to 27 days of HL-LHC operation



Beam first campaign



TID: 271 Gy
SEE: $6.34E+11$ part./cm 2
N1MeV: $4.03E+12$ n/cm 2



Mezzanine Tests

The Mezzanine was tested during the **first and second campaign**. During the first campaign, it stopped working when it reached 106 Gy. Then, after \sim 2 week, continued working and was ready for second campaign. Here it reached 31Gy more, when one of the DAC crashed. The rest of the system continued working for 85Gy more.

Mezzanine except DAC:

TID: 191Gy

SEE: $4.55E+11$ part./cm²

N1MeV: $2.79E+12$ n/cm²

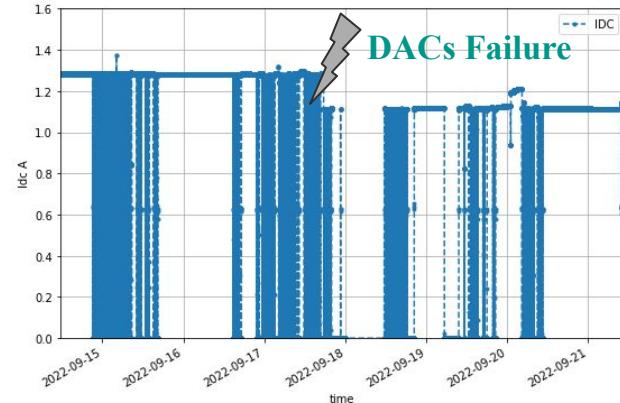
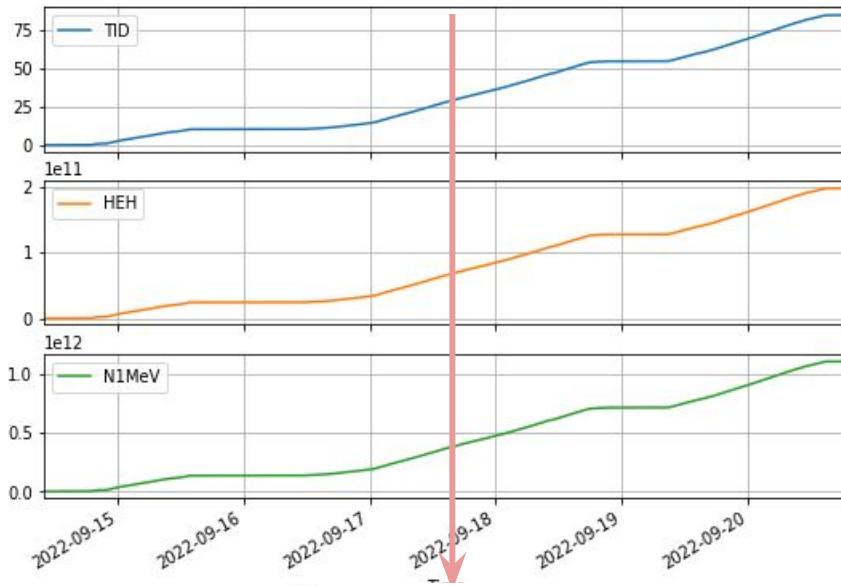
Mezzanine DAC:

TID: 137Gy

SEE: $3.28E+11$ part./cm²

N1MeV: $2.07E+12$ n/cm²

Beam second campaign



CPLD tests

The **CPLD** was tested during the second and third campaign. The CPLD survived the entire period and a consistent rate of circuits failures was detected during beam operation as it was expected.

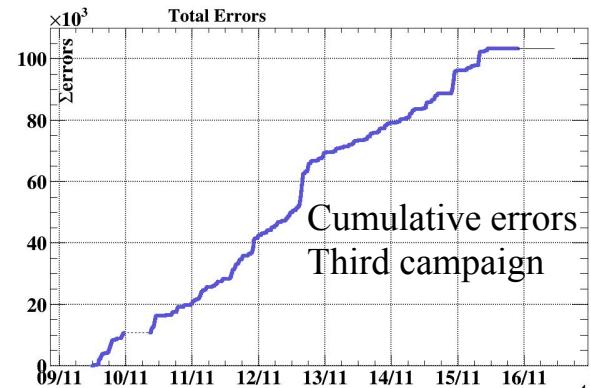
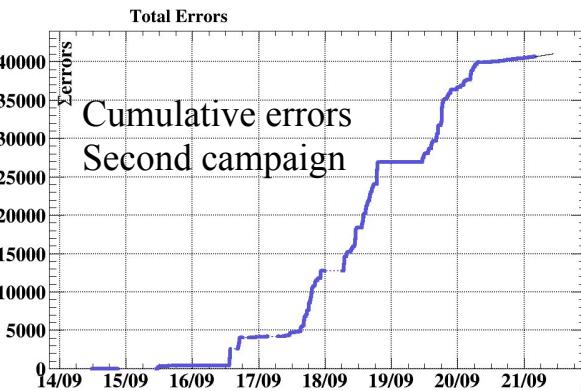
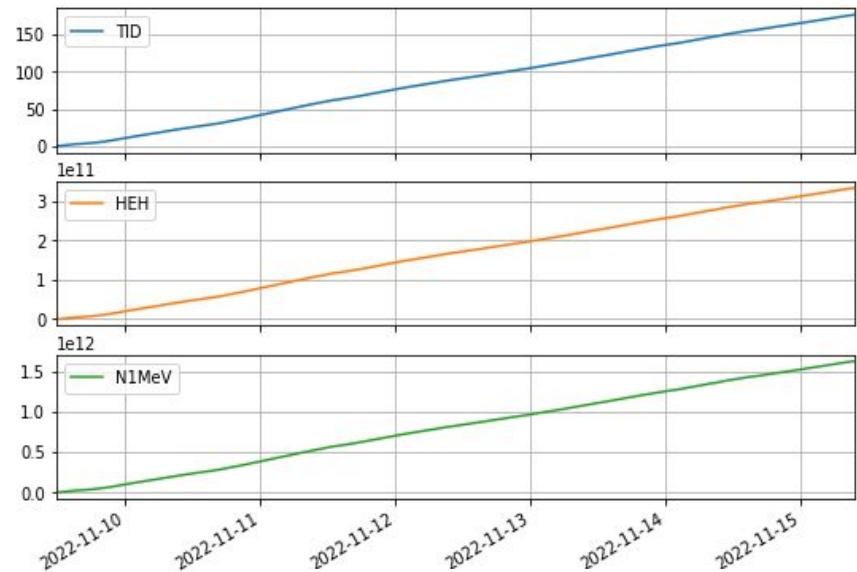
The **MTBF** was ~ 1.25 min equivalent to ~ 1 days in HL-LHC, with the CPLD at full capacity, this number will get reduced in the final firmware.

TID: 261 Gy

SEE: $5.31E+11$ part./ cm^2

N1MeV: $2.75E+12$ n/ cm^2

Beam Third campaign



Radiation Tests: Summary

	Target Dose	Reached Dose Trenz board TE0715	Reached Dose Mezzanine	Reached Dose Mezzanine (DACs)	Reached Dose CPLD
TID [Gy]	123	271 (220%)	191 (155%)	137 (111%)	261 (212%)
HEH	1.3E+11	6.34E+11 (488%)	4.55E+11 (350%)	3.28E+11(252%)	5.3e+11 (408%)
N1MeV	8.8E+11	4.03E+12 (457%)	2.79E+12 (317%)	2.07E+12(235%)	2.75e+12 (312%)

The whole system overcomes the radiation levels required for the final system location, the weakest part are the DACs. To go around the problems of the IC shortage, new test will be needed to ensure the production.

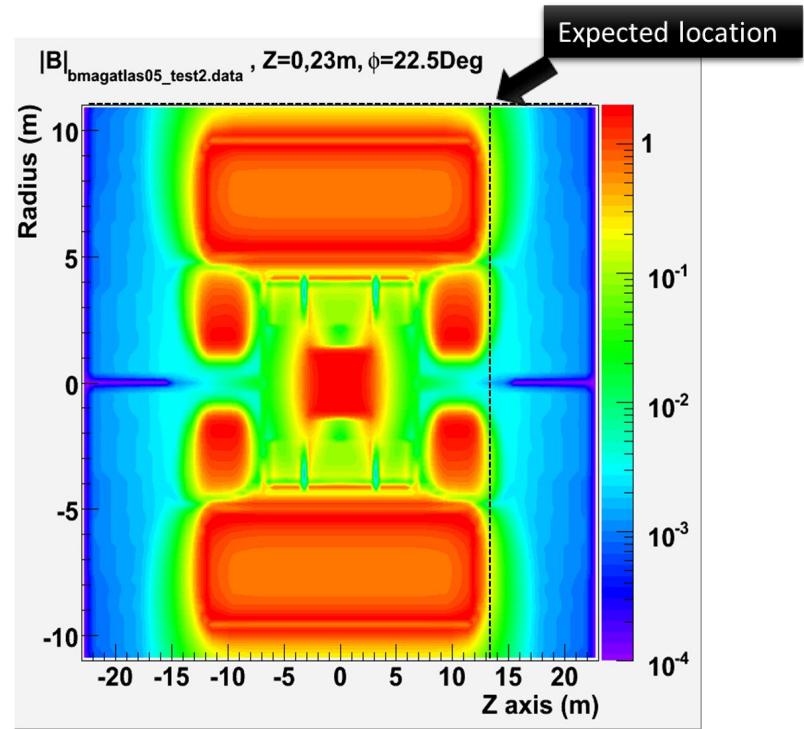
Magnetic field tolerance

Considering an expected location of 12 meters from collision point and 11 meters of radius and using the magnetic field map of 22,5Deg from semi-analytical calculation from ATLM, the expected intensity of the magnetic field is from **0.01 to 0.1 Tesla**.

TGC-CMB won't have components susceptible to magnetic field.

Reference Field Map:

<http://atlas.web.cern.ch/Atlas/GROUPS/MUON/magfield/14.2.0-bmagatlas05/bfullb05test2.png>



SEE Mitigation

The following techniques will be used to mitigate SEE:

- Triple memory redundancy on programmable logic. TMRgen*, TMR tools by xilinx, and custom logic will be implemented.
- Multi-boot process: Update Image and Golden Image on NVM (flash memory) with ECC when start the SoC.
- Checksum of the boot image.
- ECC on the FIFOs.

Testing, validation, and commissioning

- The PCBs will go through a quality control process carried out by the manufacturing company.
- Radiation tests were done in CHARM
- Communication tests will be performed using EMCI board, optical links for VTRx+, Raspberry Pi for IpGBT configuration, EMCI Carrier board, a board with capability for optical communication, and the Charge Monitoring board.
- Available communication interfaces of CMB will be used to validate the capabilities of our board independently of EMCI communication tests.
- The LEMO cable extensions to the mini rack must be installed at the beginning of the LS3 and should be done coherently with the other TGC front electronics replacement.
- Power supply channels will be provided using CAEN A3050D placed by the Japanese group on RUN4 (<https://indico.cern.ch/event/1020764/>)

Summary

- Radiation test on critical components were performed in 2022 and all component passed. More radiation test will be done this year using differents ADC (ADS5287, ADS5294) compatible with the mezzanine board.
- Due to shortage of IC, mezzanine will be updated to be capable to work with more ADC and LDO from the same family of those already tested in a radiation environment.
- Full functional test using CMB-2mezzanine board and one mezzanine were done and published “*VerDAQ: a Versatile Data AcQuisition system for high energy physics experiments*”
- First full prototype that will use 5 mezzanines boards was designed and assembled and is under tests.
- Communication test with EMCI and EMP board will begin first semester of this year.

THANKS

SPR report recommendation

R: The CMB will support charge readout mode and full waveform readout mode, with auto-trigger function. The charge monitoring data volume in the different readout modes to EMP should be worked out with details.

A: Payload per event per elink, using 12 bit adc

- Normal operation: 32 Bytes per event (trigger in the 8 channels of 1 mezzanine)
- Full readout mode: 13.2 KB per event (sent of 8 channels from 1 mezzanine)

Expecting 10 to 15 KHz between events:

- Normal operation: 480KBps
- Full readout mode of 8 channels mezzanine: 198000 KBps

Readout of an event on TGC-CMB will take up to **50 us.**

SPR report recommendation

R: MT ferrule from the VTRx+ module on EMCI is miniature and should be handled with care. It is recommended to identify a proper coupler to convert MT connector to a more robust connector, e.g. MTP-12 or LC-2, to allow easy handling of trunk cables from minirack to USA15.

A: Slide 22 answer this recommendation.

SPR report recommendation

R: The team is testing an early prototype CMB mezzanine and developing FPGA firmware. The team should contact the EMCI team to obtain an EMCI board to facilitate the prototype development

A: We get an EMCI board. backup slides show our setup to test them. We will change the board to emulate EMP by the one that EMP team lend to us.

SPR report recommendation

R : Radiation tolerant voltage regulators of LP3990 and MCP1826 are planned to be used on the CMB design. The radiation tolerance of COTS components should be documented by PDR, to prepare for the radiation tests required by FDR and PRR.

A: There is some documentation of radiation studies on voltage regulators of the same family and model on slide 54. We do radiation test using this regulator and the board working fine in level of voltage.

SPR report recommendation

R: A Trenz SoM with Zynq-7000 SoC is planned to be used on the CMB, the radiation tolerance of Zynq-7000 SoC should be carefully considered, particularly the PS part with operating system. In addition, the peripheral components on SoM will need to be radiation qualified. A simpler scheme should be considered for the prototype design, e.g. an Artix-7 FPGA on board

A: Zynq-7000 was tested in radiation environment at CHARM showing a good behavior up to 271 Gy. Also the SoM can be replaced easily using the samtec connector availables. We will study the design of a simpler FPGA.

SPR report recommendation

R: The FPGA configuration through a remote JTAG interface with GPIOs of IpGBT besides the onboard Flash memory should be considered. This will provide a redundant design in case the FPGA can't be programmed through the on-board Flash memory and also provide the option to update the firmware remotely.

A: Slide 11 and 12 present an external FPGA connector. EMCI has 14 GPIO availables. For program 4 CMB. We will use two GPIO per CMB left 6 GPIO available to emulate signals TMS,TCK, TDI and TDO. We will do test using daisy chain JTAG configuration using the available external connector on the CMB.

SPR report recommendation

R: The SEU mitigation of FPGA should be further developed by PDR, including the SEM (Soft Error Mitigation), triple module redundancy in control logic and scrubbing through the on-board Flash memory or JTAG interface. The team is suggested to consider the strategy for the radiation tolerance after contacting the TGC JATHub board group. Note that the JATHub boards will be installed in the same minirack.

A: The SEU mitigation are presented in slide 64.

SPR report recommendation

- EIL4 will be replaced with triplet modules during the Phase-II upgrade, and has total 126 monitoring channels. Section 3.2 and Table 5.4 shall be updated to reflect the upgrade plan.
- The radiation tolerance requirements in Table 10.1 shall be updated wrt the new safety factors in the RETF2020 report.
- The simulated radiation level at the minirack is smaller than the values shown in Table 10.1 and shall be updated.
- The magnetic field tolerance shall be specified, even though the expected magnetic field is low.
- “The operating voltage of the TGCs is 2.85 kV.” in section 3.3 shall be updated to “The operating voltage of the TGCs is 2.80 kV.”

EMCI electrical interfaces: Vita 57.1 pinout connector

	K	J	H	G	F					
	HPC	HPC	LPC	LPC	HPC	E	D	C	B	A
	VREF_B_M	GND	VREF_A_M	GND	PG_M2C	HPC	LPC	LPC	HPC	HPC
2	GND	CLK3_BIDIR_P	PRSNTR_M2C_L	CLK1_M2C_P	GND					
3	GND	CLK3_BIDIR_N	GND	CLK1_M2C_N	GND					
4	CLK2_BIDIR_P	GND	CLK0_M2C_P	GND	HA00_P_CC					
5	CLK2_BIDIR_N	GND	CLK0_M2C_N	GND	HA00_N_CC					
6	GND	HA03_P	GND	LA00_P_CC	GND					
7	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P					
8	HA02_N	GND	LA02_N	GND	HA04_N					
9	GND	HA07_P	GND	LA03_P	GND					
10	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P					
11	HA06_N	GND	LA04_N	GND	HA08_N					
12	GND	HA11_P	GND	LA08_P	GND					
13	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	gpio_7				
14	HA10_N	GND	LA07_N	GND	HA12_N	gpio_8				
15	GND	HA14_P	GND	LA12_P	GND					
16	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	gpio_9				
17	HA17_N_CC	GND	LA11_N	GND	HA15_N	gpio_10				
18	GND	HA18_P	GND	LA16_P	GND					
19	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P					
20	HA21_N	GND	LA15_N	GND	HA19_N					
21	GND	HA22_P	GND	LA20_P	GND					
22	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P					
23	HA23_N	GND	LA19_N	GND	HB02_N					
24	GND	HB01_P	GND	LA22_P	elink_clk_p5	GND				
25	HB00_P_CC	HB01_N	LA21_P	LA22_N	elink_clk_n5	HB04_P				
26	HB00_N_CC	GND	LA21_N	GND	HB04_N					
27	GND	HB07_P	GND	LA25_P	GND					
28	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P					
29	HB06_N_CC	GND	LA24_N	GND	HB08_N					
30	GND	HB11_P	elink_clk_p2	GND	LA29_P	elink_out_p1	GND			
31	HB10_P	elink_out_p2	HB11_N	elink_clk_n2	LA28_P	elink_in_p5	LA29_N	elink_out_n1	HB12_P	elink_out_p6
32	HB10_N	elink_out_n2	GND	LA28_N	elink_in_n5	GND			HB12_N	elink_out_n6
33	GND	HB15_P	elink_clk_p4	GND	LA31_P	GND				
34	HB14_P	elink_out_p3	HB15_N	elink_clk_n4	LA30_P	elink_in_p1	LA31_N	HB16_P	GPIO_11	
35	HB14_N	elink_out_n3	GND	LA30_N	elink_in_n1	GND			HB16_N	GPIO_12
36	GND	HB18_P	elink_clk_p3	GND	LA33_P	GND				
37	HB17_P_CC	HB18_N	elink_clk_n3	LA32_P	elink_clk_p4	LA33_N			HB20_P	elink_in_p4
38	HB17_N_CC	elink_clk_n1	GND	LA32_N	elink_clk_n4	GND			HB20_N	elink_in_n4
39	GND	VIO_B_M2C	GND	VADJ	VADJ	GND			VADJ	VADJ
40	VIO_B_M2C	GND	VADJ	GND	VADJ	GND			VADJ	VADJ

RMS Noise of DRS4 at the mezzanine

<https://iopscience.iop.org/article/10.1088/1748-0221/17/01/P01023>

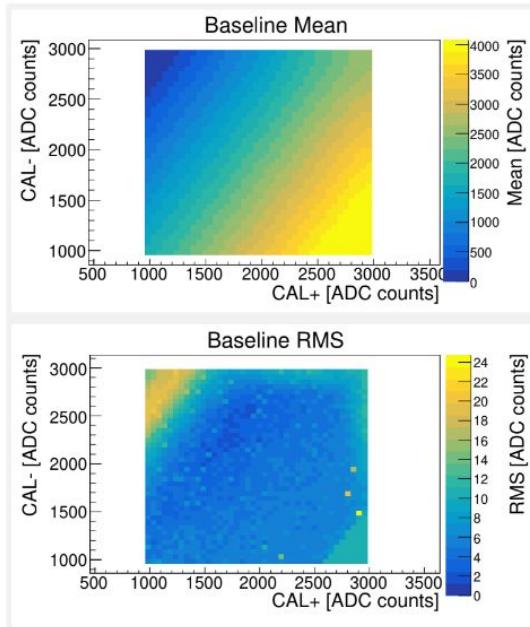


Figure 4. Mean values (top) and RMS (bottom) of the ADC count measuring the DRS4 cells for the different combinations of CAL+ and CAL- are shown in the color scale. CAL+ and CAL- DC voltages were varied with steps of 50 DAC count, and single baseline measurements were done at each point.

Square wave digitizing using CMB-2mezzanine board

<https://iopscience.iop.org/article/10.1088/1748-0221/17/01/P01023>

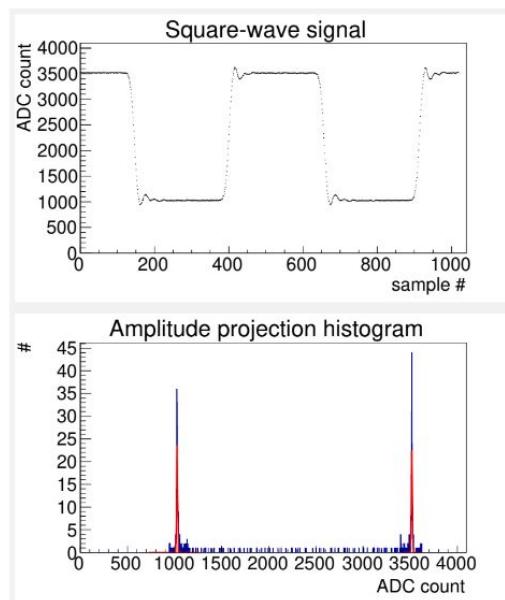
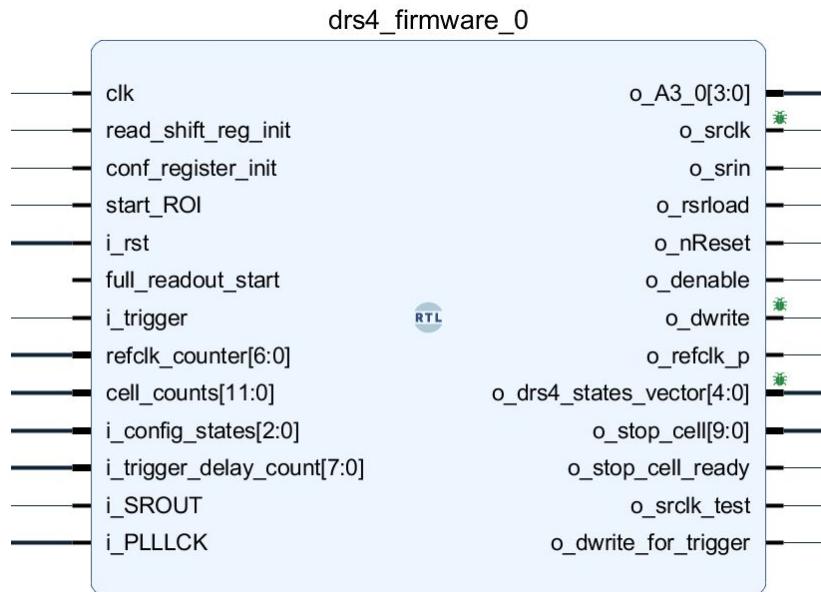
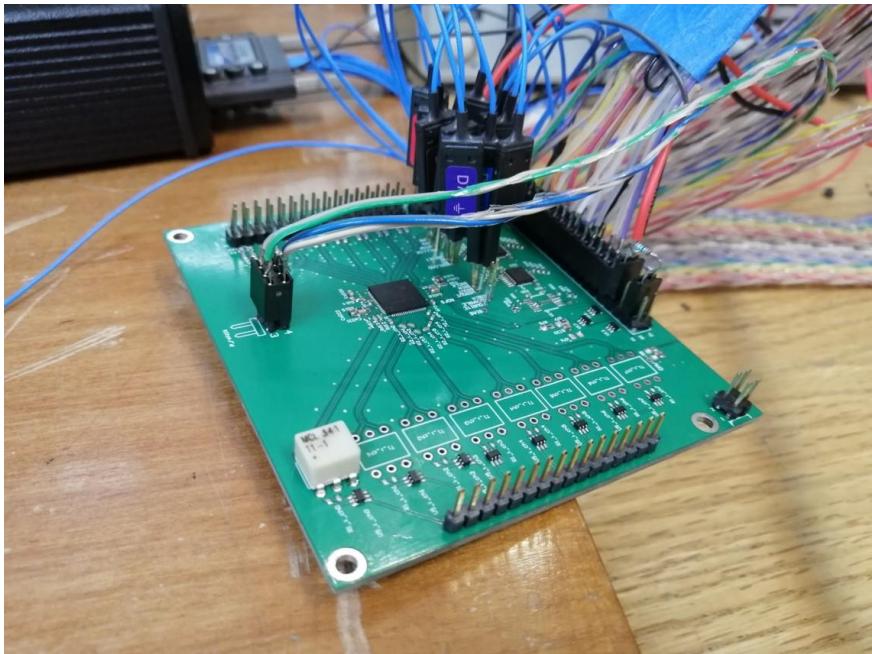
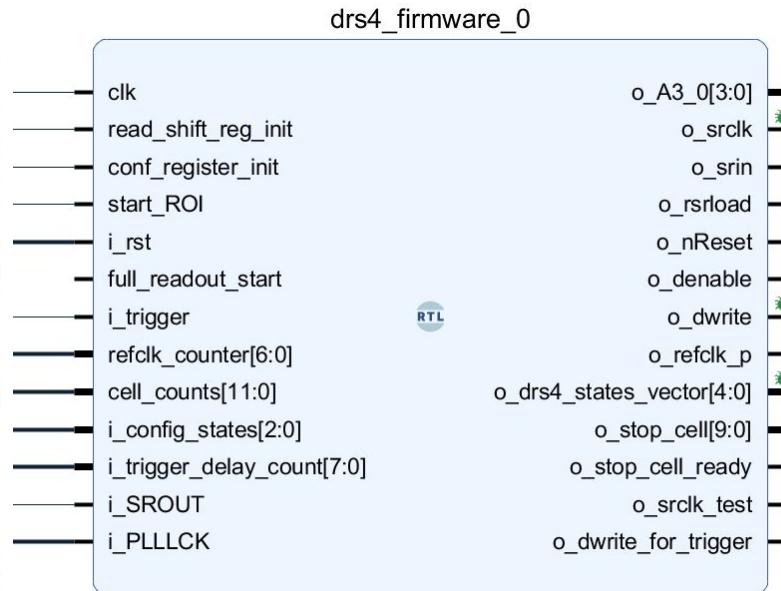
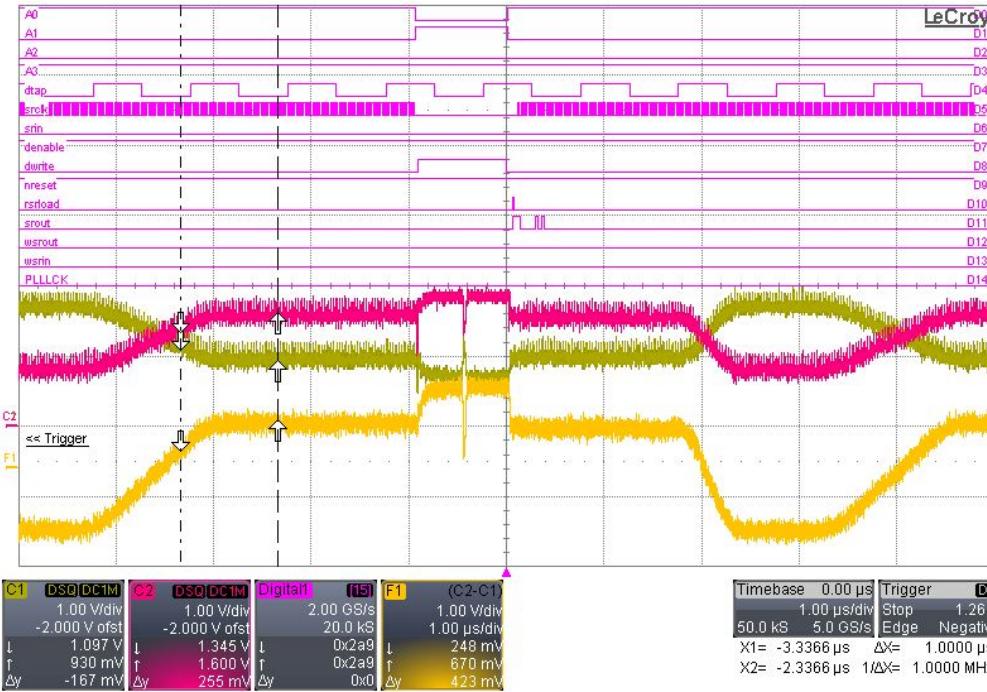


Figure 6. At the top a square signal of 4MHz and 500mV peak-to-peak amplitude. At the bottom a projection histogram of the amplitude of the top picture. The plateau of the square-wave signal produce normal distributions in the histogram. The mean of the distribution are 1027 and 3517.

Firmware: DRS4 control

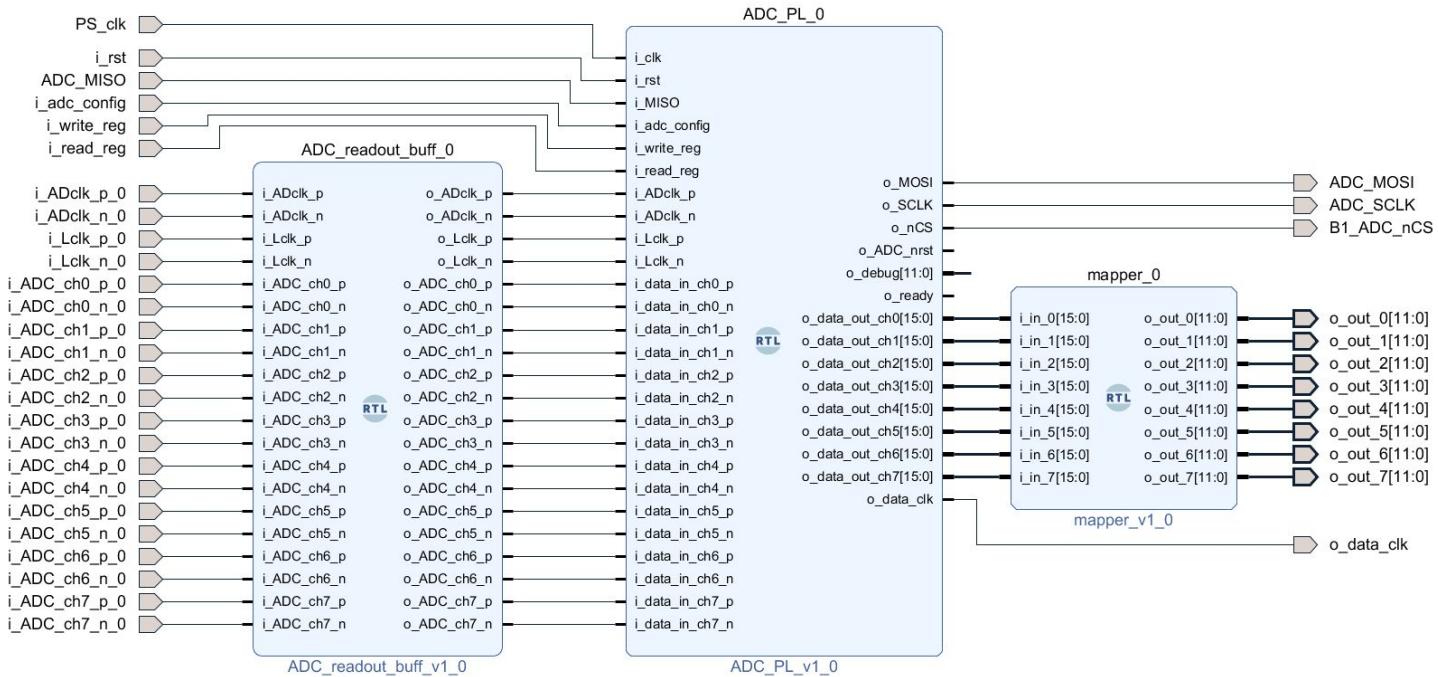


Firmware: DRS4 control



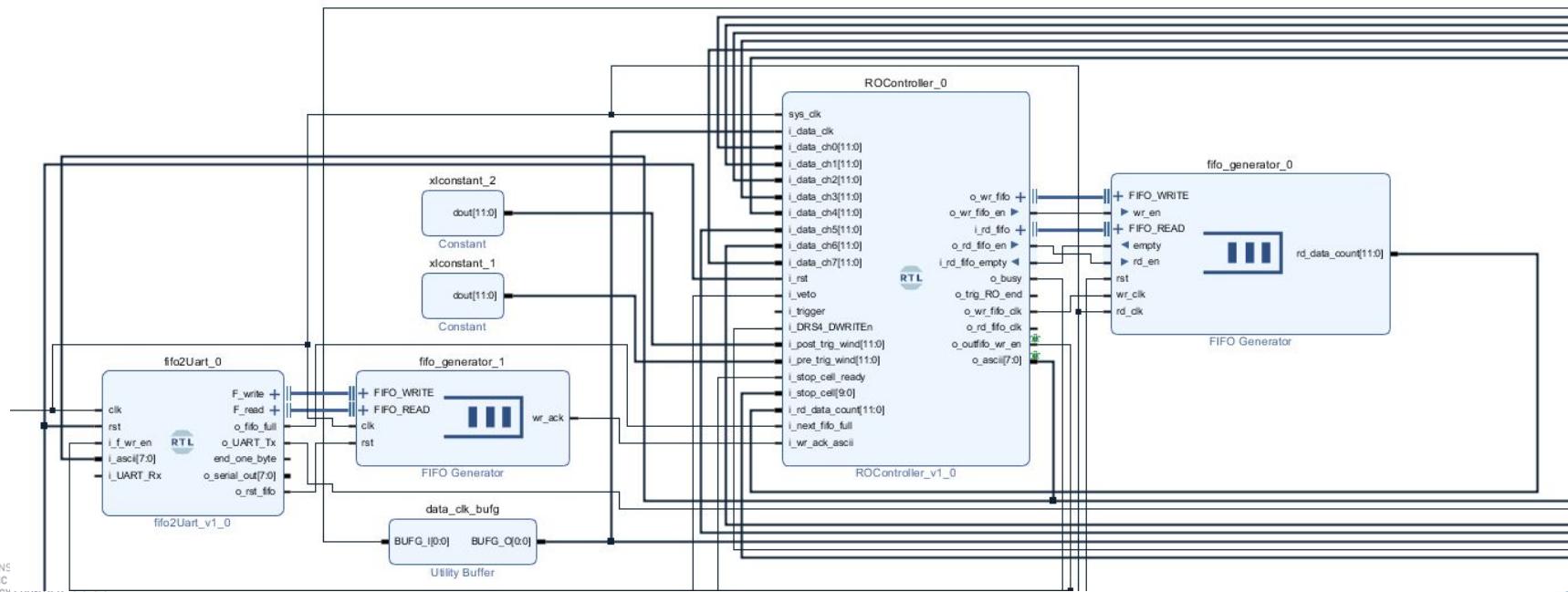
Firmware: ADC Analog readout

First stage: Buffer and SerDes



Firmware: ADC Analog readout

Second stage: Storage of values in FIFO when trigger occurs



EMCI/EMP test

The EMP emulation can be done using the firmware available on gitlab

<https://gitlab.cern.ch/emci-emp/emp-firmware>. In order to directly use the firmware, a development board zcu102 (3300 eur) or Trenz TE0807 with a carrier board and SFP+ connector should be used, that are from family Zynq Ultrascale+ with an operating system loaded.

EMCI, which use IpGBT, needs a clock signal, that get from the downstream optical link to which it is connected to work properly.

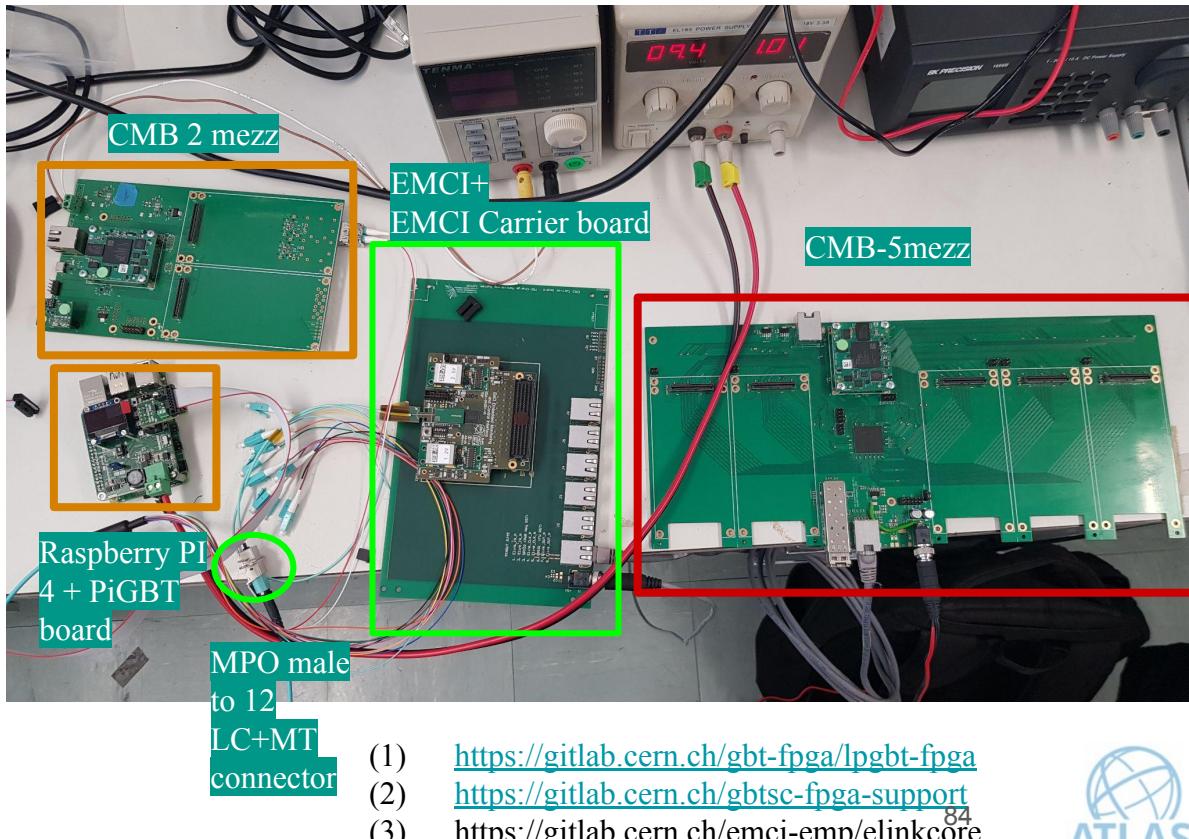
The firmware to readout EMCI data from the optical link will be done using the firmware available from IpGBT gitlab repository in (1) and (2).

This is a complementary branch of work for us.

EMCI/EMP: Test setup

The following boards will be used:

- CMB-2 mezzanine to emulate EMP, adapting the IpGBT firmware available in (1) and (2) to the Zynq7000 TE0715.
- EMCI board and the Carrier board.
- CMB-5 mezzanine prototype to send data using Elink firmware (3).



EMCI/EMP: Test setup

The board function are the following:

- CMB-2mezz: EMP emulator
- EMCI Carrier board:Receive data from Elink data
- CMB-5mezz: Elinks firmware
- Raspberry: Control IpGBT on EMCI

