AN1275: Impedance Matching Network Architectures

This application note introduces the important concept of impedance matching between source and load in RF circuit applications with the aid of VSWR, reflection coefficient, and Smith chart concepts. Various types of impedance matching network architectures (2, 3, 4, or more element) are discussed in detail, and mathematical approaches to matching network design, supported by two solved numerical examples, are presented.

Although the design example in this application note discusses the matching procedure for EFR32 Series 1 2.4 GHz devices, the theory and steps for designing a matching network are valid for any type of RF source and load.

Please refer to"AN923: EFR32 Sub-GHz Matching Guide", "AN930.1: EFR32 Series 1 2.4 GHz Matching Guide", and "AN930.2: EFR32 Series 2 2.4 GHz Matching Guide" for the exact matching component values for the respective devices.

KEY FEATURES

- Voltage Standing Wave Ratio (VSWR), Reflection Coefficient
- Complex Conjugate Impedance Matching Network
- Introduction to Smith Chart
- 2 element – L Networks
- 3 element – Pi and T Networks
- 4 element – Wideband Networks
- Design of Matching Network – Numerical and AWR simulation example

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1. Introduction

A simple RF application circuit consists of a Generator/Source (e.g. RFIC) that generates an RF signal and consists of a load (e.g., an antenna that radiates the generated RF signal). For any efficient RF circuit, it is necessary to maximize the power transfer between the source and the load by minimizing the losses and internal reflections. In DC circuits, maximum power will be transferred between the source to its load if the load resistance equals to source resistance.

In the case of time-varying signals, the impedance of the source and load acts little differently when it comes to transferring signals. To understand this difference lets analyze two conditions:

[A] When Both Source and Load Impedances are Purely Real

As the impedance is a real number, there is no imaginary component to it. Hence, Voltage and Current waveforms are in-phase with each other and thus both voltage and current signals reach from source to the load at the same time.

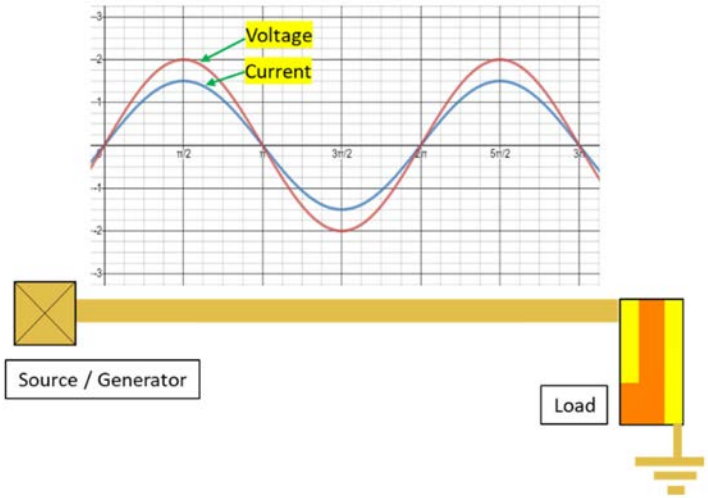


Figure 1.1. Voltage and Current Waveform for Real Impedance

[B] When Either Source or Load is Complex

As the impedance is a complex number, it will consist of both real and imaginary components. The real component can be classified as the resistance while the imaginary component can be classified as the reactance. The reactance in the circuit adds delay in the current waveform and thus the delay in the signal being delivered to the load. This delay causes the current waveform to lag the voltage waveform making them out of phase. Due to this, reflections between the source and the load are generated. These reflected signals are added to the incident signal resulting in standing waves which is given by the parameter VSWR.

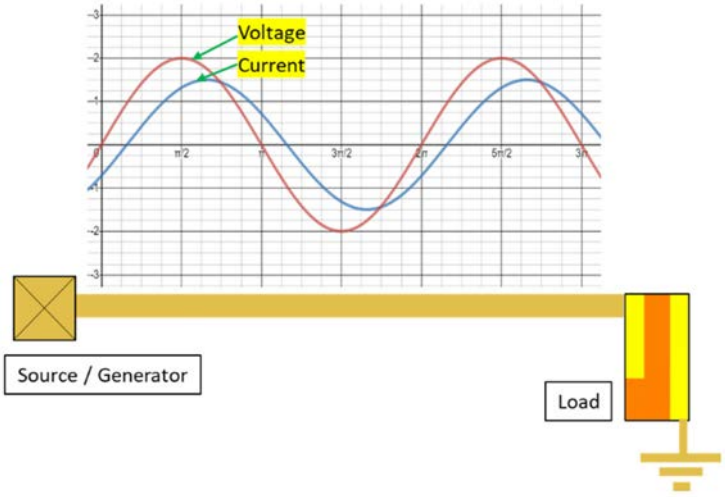


Figure 1.2. Voltage and Current Waveform for Complex Impedance

2. Reflection Coefficient, VSWR, and Impedance Matching

2.1 Voltage Standing Wave Ratio (VSWR)

Voltage Standing Wave Ratio (VSWR) is the ratio of the peak amplitude of a standing wave to the minimum amplitude of the standing wave. A minimum value of VSWR is desired for maximum power transfer between the source and the load.

$$VSWR = \frac{1 + |\Gamma|}{1 - |\Gamma|}$$

2.2 Reflection Coefficient (Γ)

The amount of energy that is reflected to the source defines the strength of the impedance mismatch between the source and the load. The reflection coefficient (Γ–gamma) provides power that is reflected from the load due to impedance mismatch in the network. If there is a serious impedance mismatch between the source and the load, then almost all of the energy can be reflected to the source which can damage the source.

The following table defines the relation between return loss and mismatch loss.

Table 2.1. Return Loss vs. Mismatch Loss

$S_{11}[dB]$	$\Gamma = 10^{\frac{S_{11}}{20}}$	$Mismatch\ \ Loss\ \ [dB] = -10 \times Log_{10}(1 - \Gamma^2)$	$Mismatch\ \ Loss\ \ (\%) = (1 - \Gamma^2) \times 100$
–20	0.1	0.04	99
–15	0.17782	0.13	96.84
–10	0.31622	0.45	90
–5	0.56234	1.65	68.38
–3	0.70794	3.02	49.88
–0.1	0.98855	16.42	2.28

From the above table, if the S_{11} value is –3 dB, only 50% of the power is delivered to the load, and the remaining 50% (3 dB) of the power is lost. Whereas if the S_{11} value changes to –10 dB, 90% of the power is delivered to the load and only 0.45 dB power is lost. It can also be seen that if the S_{11} value is reduced further; the mismatch loss improves by little. Generally, an S_{11} value of –10 dB to –15 dB is recommended because improving the S_{11} value further than –10 dB will only improve the mismatch loss by a minimal value i.e., the mismatch loss will be 0.13 dB or 0.04 dB when the S_{11} value is –15 dB or –20 dB respectively.

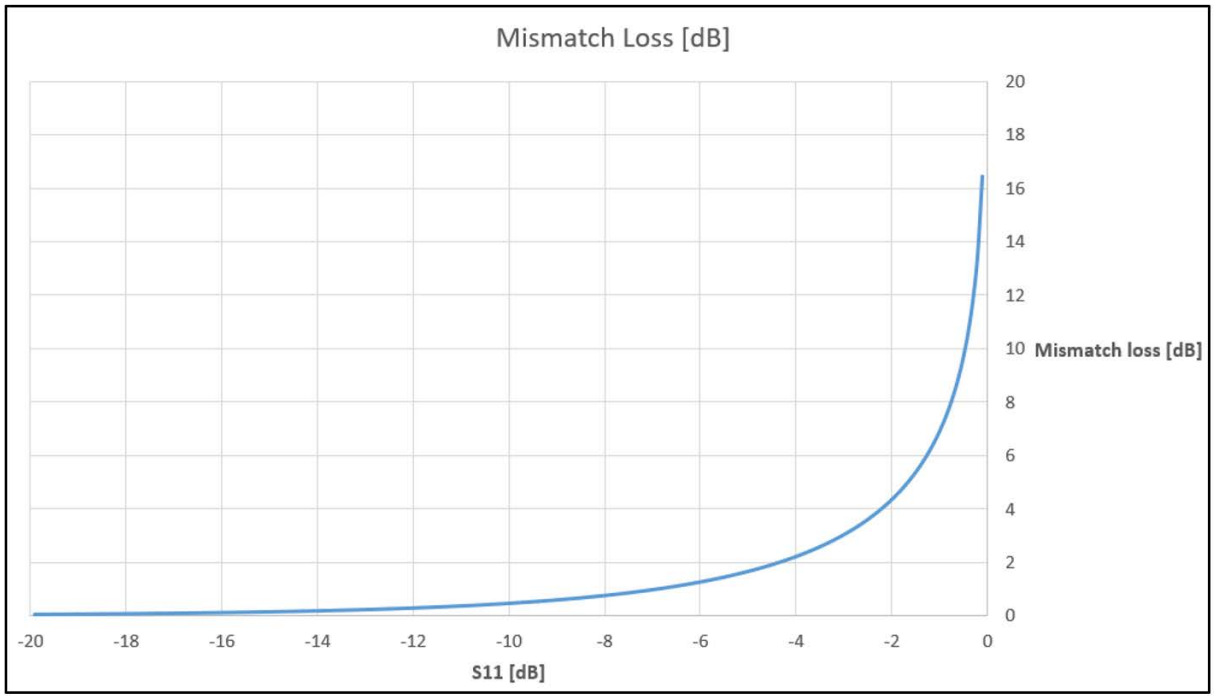


Figure 2.1. Mismatch Loss (dB)

$$\Gamma = \frac{Z_L - Z_O}{Z_L + Z_O}$$

Where:

Z_L = Load Impedance

Z_O = Characteristic Impedance

From the above equations, it can be seen that when $Z_L = Z_O$ (Load impedance is matched to the characteristic impedance), the reflection coefficient (Γ) = 0, making VSWR = 1. Thus, the minimum value of VSWR that can be achieved is 1.

2.3 Impedance Matching

For the time-varying signals, the maximum power transfer occurs when the load impedance is equal to the complex conjugate of the source impedance. The term complex conjugate is simply having the impedance with the equal real part but with an opposite polarity of the reactance.

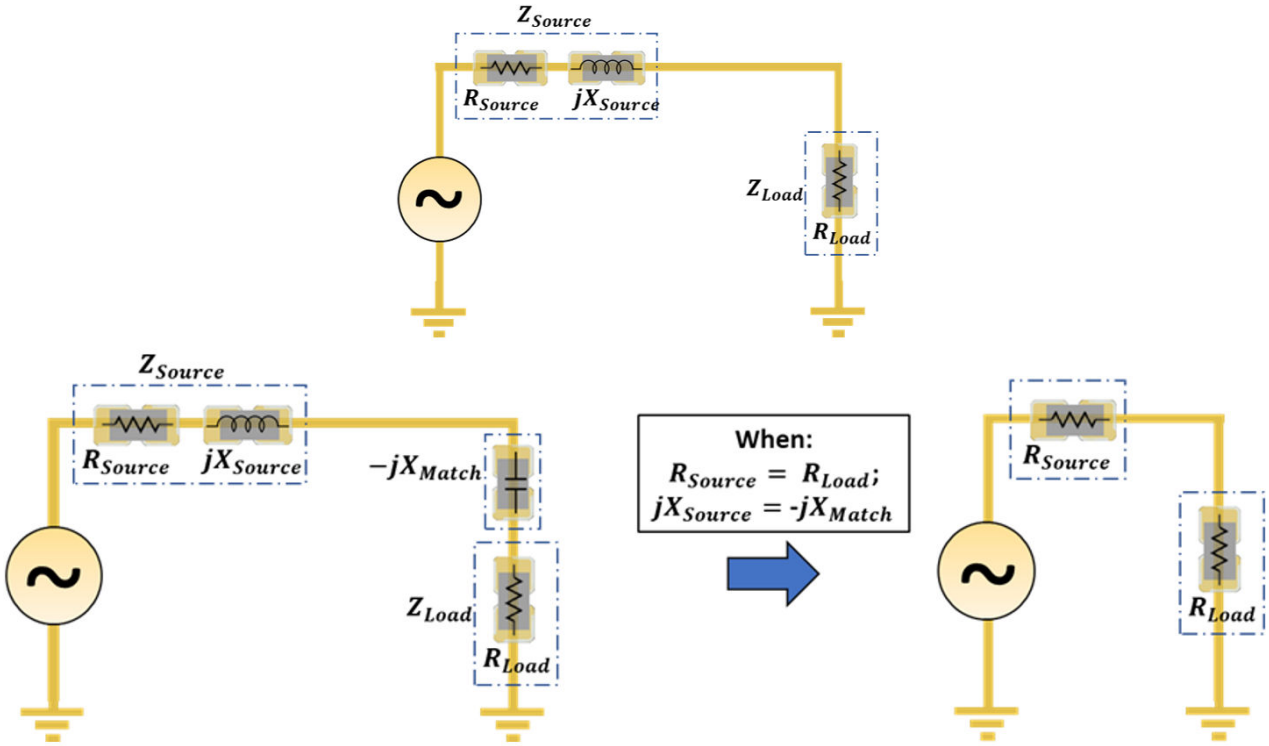


Figure 2.2. Impedance Transformation by Adding a Complex Conjugate Matching Component

From the above figure, we can see that the complex source impedance (R_{Source} + jX_{Source}) can be matched with the load impedance (R_{Load} + j0) by introducing a matching component ($-jX_{Match}$) in the circuit that has equal and opposite reactance from the source. By introducing this component, the opposite reactance gets canceled thereby matching source and the load (assuming $R_{Source} = R_{Load}$). If the impedances are matched between the source and the load, theoretically, all of the energy will be transferred from source to the load.

The process of designing and implementing an additional circuitry between the load and the source is called impedance matching. From the above figure, it can be seen that the impedance matching network creates a condition in which the source reactance is resonated with an equal and opposite load reactance, thus leaving only pure resistance value at the source and the load. This can be done by forcing the load impedance to change into a complex conjugate of the source impedance. Note that, since the reactance in the circuit is frequency-dependent, the perfect impedance match between the source and the load will also occur at a particular frequency. The frequency band over which the impedance is matched can be determined by the value of the "Q" factor of the matching network, which depends on the network architecture.

$$BW = \frac{F}{Q}$$

Where:

BW = –3 dB Bandwidth

F = Operating frequency

Q = The measure of energy stored in reactance to that being dissipated

In some applications, due to the restriction of small and limited PCB sizes, the antennas used have higher Q. Designing a high Q matching network for a high Q antenna can lead to performance issues that are caused by the technical spreading of the matching components. Thus, to compensate for any component spreading, and to avoid any performance degradation, it is important to keep the Q factor of the matching network low. Therefore, the value of Q is an important parameter that should be chosen carefully while designing the matching network as it results in a tradeoff with the bandwidth over which the impedance will remain matched.

3. The Smith Chart

The Smith chart is a graphical tool that is a combination of a family of constant resistance circles located along the X axis and family of arc of constant reactance circles located along the Y axis. Each point along the circumference of each circle has the same value of resistance as that on any other point of the same circle. The outermost constant resistance circle, defines the outer boundary of the Smith chart. The center line of the Smith chart represents the axis; therefore, it is called the real axis.

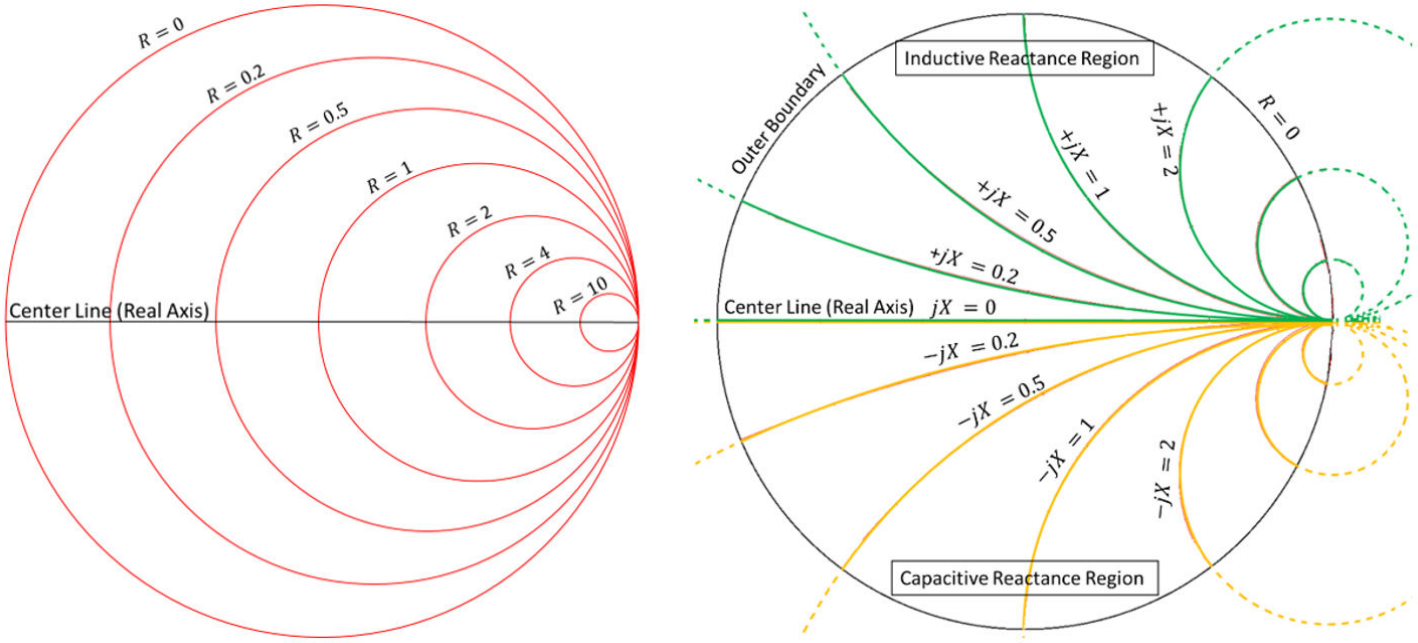


Figure 3.1. Constant Resistance Circles (Left) and Constant Reactance Circles (Right)

In the right image in the above figure, all green-colored arcs above the center line of the chart represent positive reactance (+jX), and, thus, the region above the centerline of the Smith chart is called the inductive reactance region. Similarly, all yellow-colored arcs below the center line of the chart represent negative reactance (–jX), and, thus, the region below the centerline of the Smith chart is called the capacitive reactance region. All arcs within the inductive or capacitive reactance regions of the Smith chart are limited by the outer boundary of the chart. The condition in which the reactance point can lie beyond the boundary line depends upon the concept of negative resistance, which is not used in impedance matching and is not discussed in this application note.

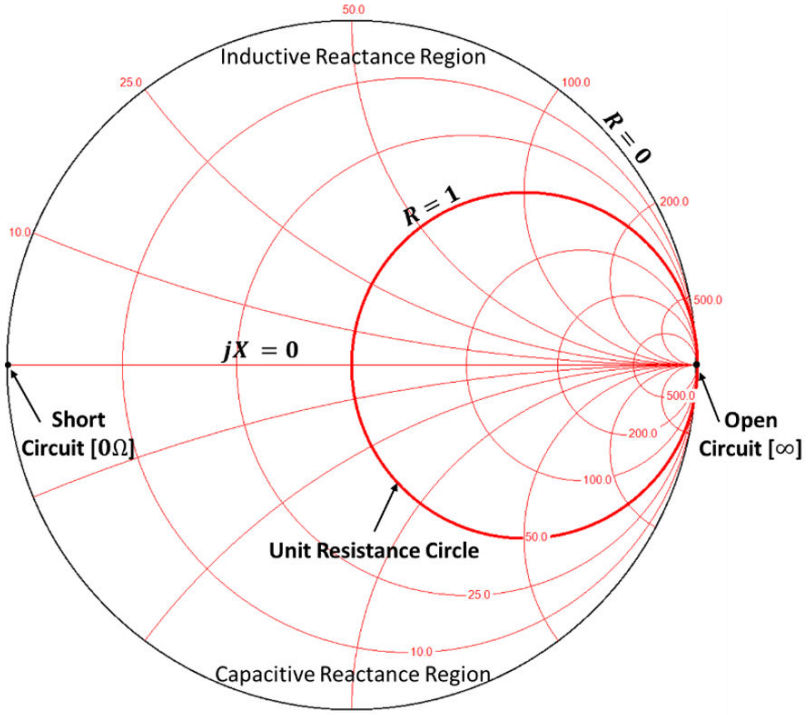


Figure 3.2. Impedance Chart

The chart formed by combing constant resistance circles and reactance arcs as shown above is called an impedance chart. The impedance value (Mathematically expressed as Z = R ± jX) can be plotted directly on the Smith chart by finding the intersection point of the respective real (R) and imaginary (±jX) circle on the Smith chart. The following figure shows two different examples of plotting impedance points on an impedance chart.

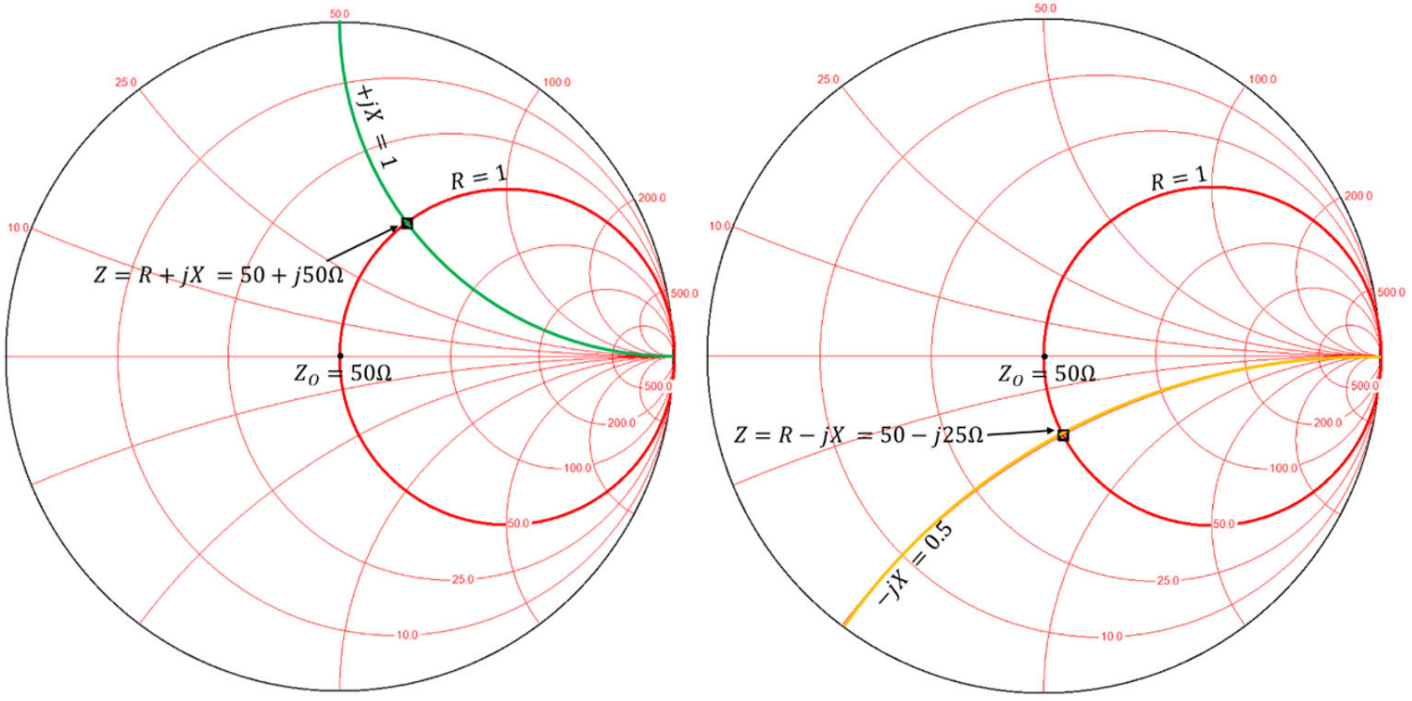


Figure 3.3. Examples of Plotting Impedance Points on a Smith Chart

It should also be noted that, for large values of impedance, if plotted on a Smith chart, they will lie on the extreme right of the impedance chart making the measurements difficult. Thus, the impedance chart is constructed with normalized values of resistance and reactance circles, and, similarly, all of the impedance points are plotted in their normalized form. A normalized value is obtained from dividing each impedance point by the characteristic impedance of the circuit, thereby changing the impedance resolution scale of the Smith chart.

The impedance chart is useful to determine or manipulate the load impedance by adding series components (capacitor or an inductor) in the circuit in a graphical plot. However, if a parallel component is added, first the impedance point (Z) has to be converted into an admittance (Y) point. In mathematical terms, an admittance point is obtained by taking the inverse of the impedance.

$$Y = \frac{1}{Z}$$

$$Y = G \pm jB$$

This can also be achieved by rotating the impedance point to the opposite side by 180° on the Smith chart. If we convert the impedance point to admittance, we also have to convert the resistance (R) and reactance (X) components into their equivalent conductance (G) and susceptance (B) points. The admittance chart can be obtained by plotting constant conductance circle and susceptance arcs as shown in the figure below, which can, alternatively, be obtained by inversing the impedance chart altogether or by rotating the impedance chart by 180°. Because we have rotated the impedance chart, the positive and negative reactance arcs are also flipped,. i.e., in the admittance chart, the upper half represents negative susceptance (–jB), which still remains in the inductive region, and the lower half represents positive susceptance (+jB), which also remains in the capacitive region.

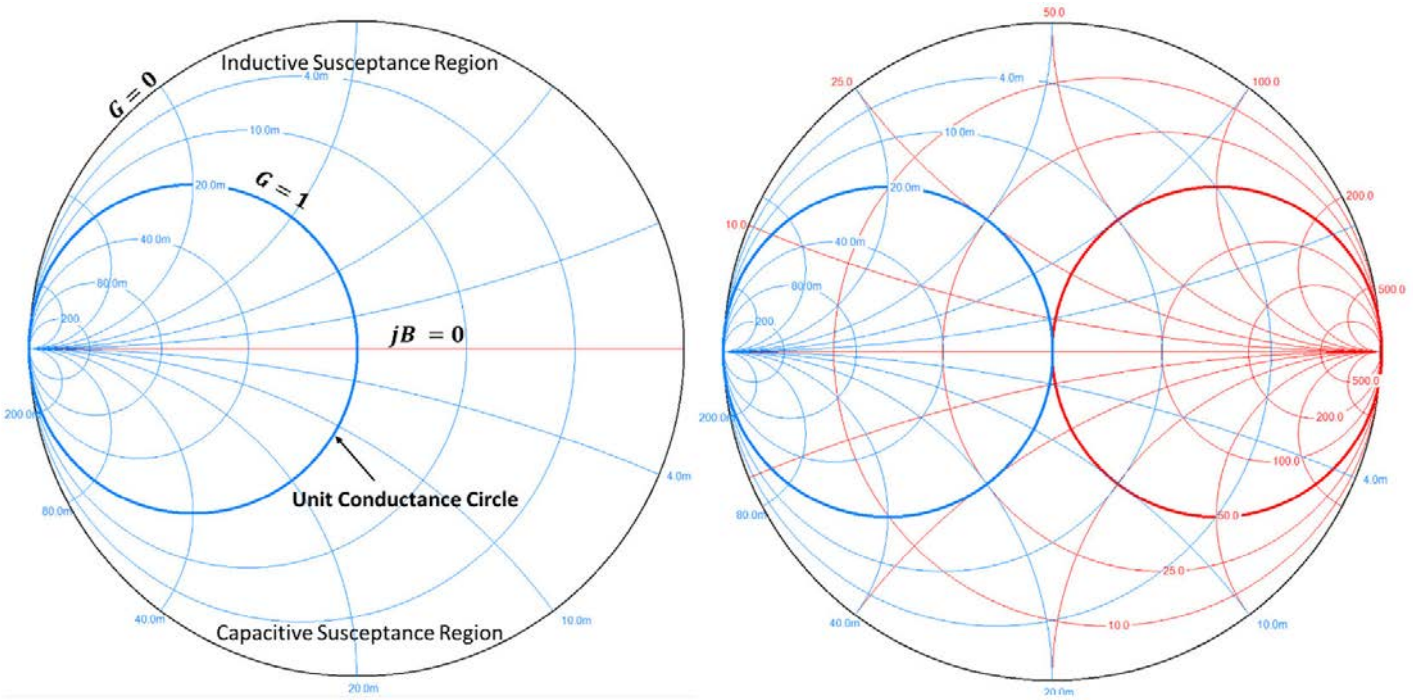
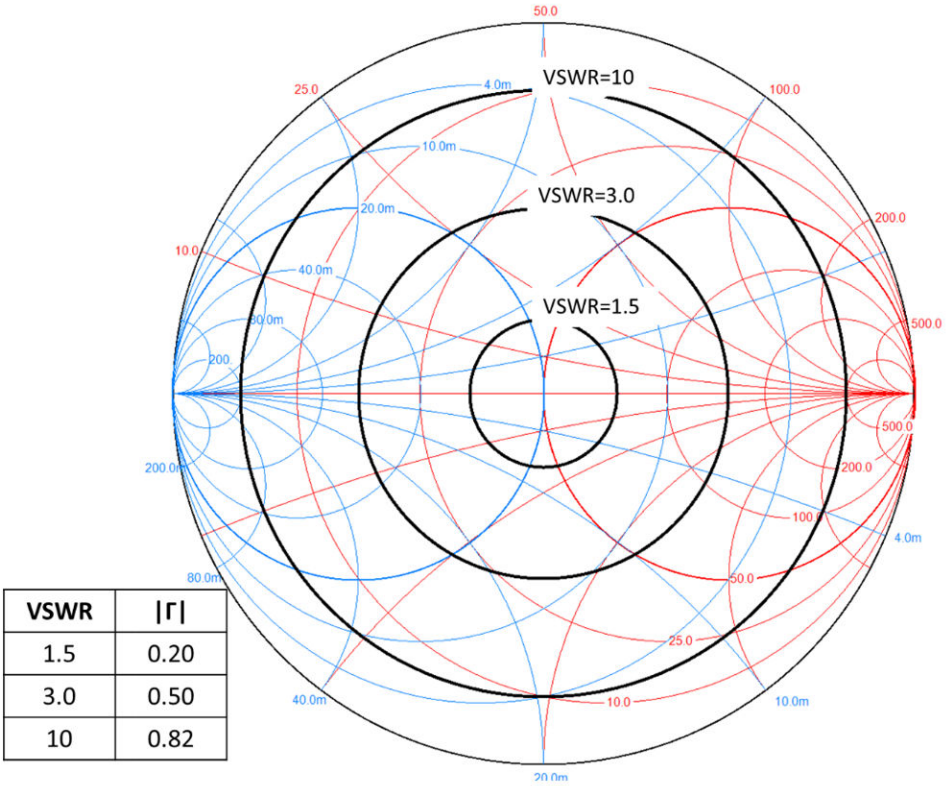


Figure 3.4. Admittance Chart (Left) and Impedance and Admittance Charts Plotted Together (Right)

If we superimpose the impedance and admittance charts, we obtain a very useful graphical chart that now provides us a visual aid to see the effect of the addition of a series or a parallel component to the impedance/admittance point on a single Smith chart without the need to rotate the points on the chart. The reflection coefficient (Γ) and the bandwidth of the designed matching network can also be graphically viewed on the chart by plotting the VSWR circles and Constant Q reference circles as shown in the following two figures, respectively.



VSWR	|Γ|
1.5	0.20
3.0	0.50
10	0.82

Figure 3.5. VSWR Reference Circles on a Smith Chart

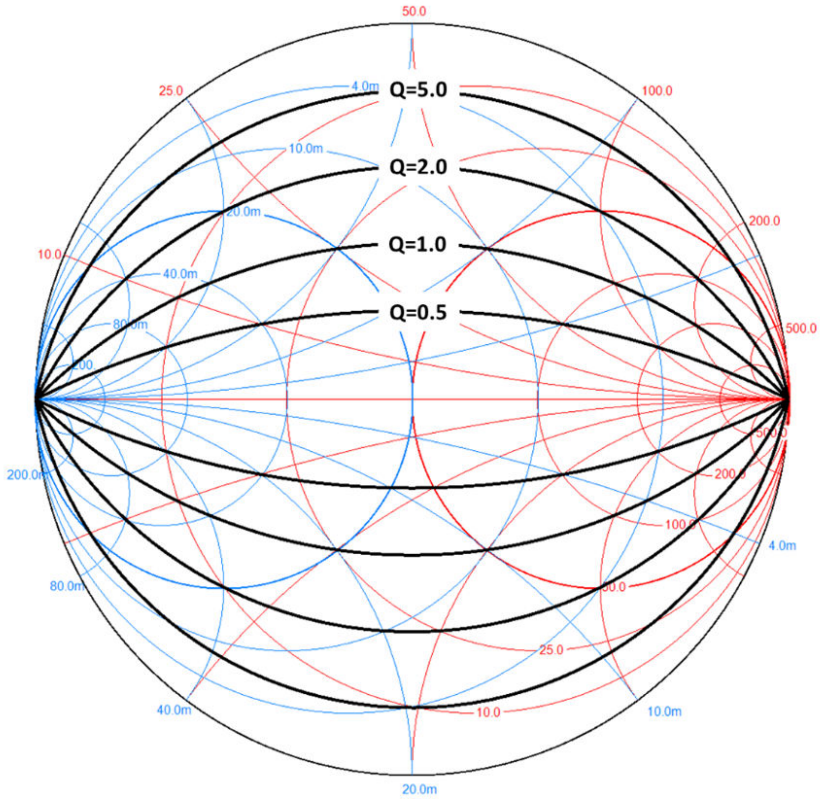


Figure 3.6. Constant Q Reference Circles on Smith Chart

4. Two-Element Matching Network Architecture

4.1 The L Network

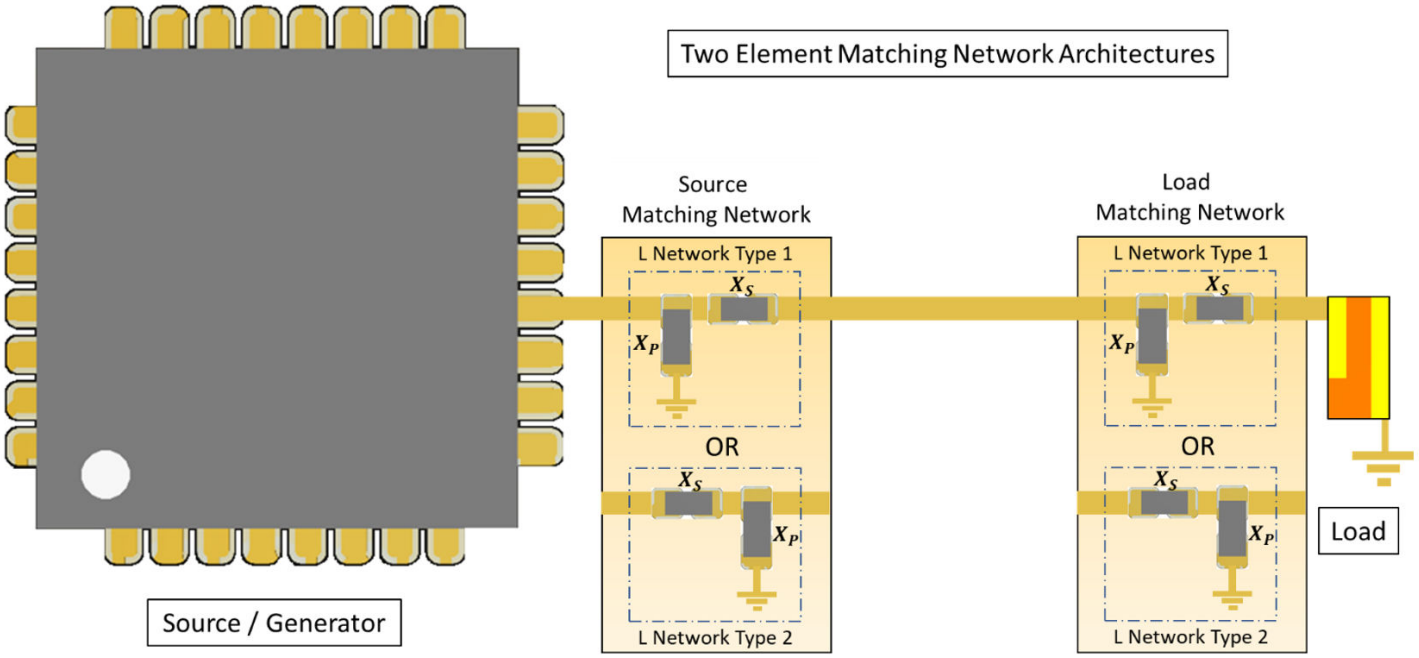


Figure 4.1. Two Element Impedance Matching Network Architecture at Source and Load

The L network has its name due to the component orientation of the matching network which resembles an “L” shape. It is the basic building block of any other matching network architecture discussed here and also the most widely used network architecture as it has the simplest form and is easiest to design. Compared to other network architectures, the L network has an advantage of low component loss as the number of components required to match the impedance is low. As per the above figure, there are two possible architectures to form a two-element L shaped matching network i.e. Parallel-Series or Series-Parallel network. A combination of a capacitor(s) and an inductor(s) can be chosen to match the impedance of the load. When the series component is a capacitor and the parallel component is an inductor, the series capacitor will block dc into the load and the inductor will act as a short at low frequencies. Thus, the network is considered be in High-pass configuration. Similarly, when the series component is an inductor and the parallel component is a capacitor, the inductor will allow dc into the load but will attenuate at higher frequencies and the capacitor will act as a short at high frequencies. Thus, the network is considered to be in low-pass configuration.

The function of the parallel component of the L matching network is to transform a larger impedance down to smaller value equating the real part of the impedances between source and the load. Similarly, the function of the series component is to cancel out any reactive components present in the circuit by resonating with equal and opposite reactance. The result of the two components together leaves the source driving an equal load for maximum power transfer. This is how impedance transformation is achieved by introducing a two-element network between the source and the load. The question of determining whether the parallel component will be on the left or on the right side of the series component can be answered by finding out which side has a higher real impedance part that needs to be brought down. If the load impedance is higher than the source, then the parallel component will lie on the right side of the series component (assuming the load is on the right and source is on the left in the circuit). Please refer to Figure 4.3 Type 1 and Type 2 LL/CC Permissible and Forbidden Regions on Smith Chart on page 14 for the special case in which parallel components can be used on the source or load side irrespective of which has a higher impedance value.

4.2 Design Formulas

$$Q_S = Q_P = \sqrt{\frac{R_P}{R_S} - 1}$$

$$Q_S = \frac{X_S}{R_S}$$

$$Q_P = \frac{R_P}{X_P}$$

$$X_C = \frac{1}{2 \times \pi \times F \times C}$$

$$X_L = 2 \times \pi \times F \times L$$

Where:

Q_S = Q of the series leg

Q_P = Q of the parallel leg

R_S = series resistance

R_P = parallel resistance

X_S = series reactance

X_P = parallel reactance

F = operating frequency

C = capacitance

L = inductance

The quantities such as series and parallel reactance can be capacitive or can be inductive, which depends upon the desired configuration of the matching network. There are eight possible configurations of the L-network as shown below.

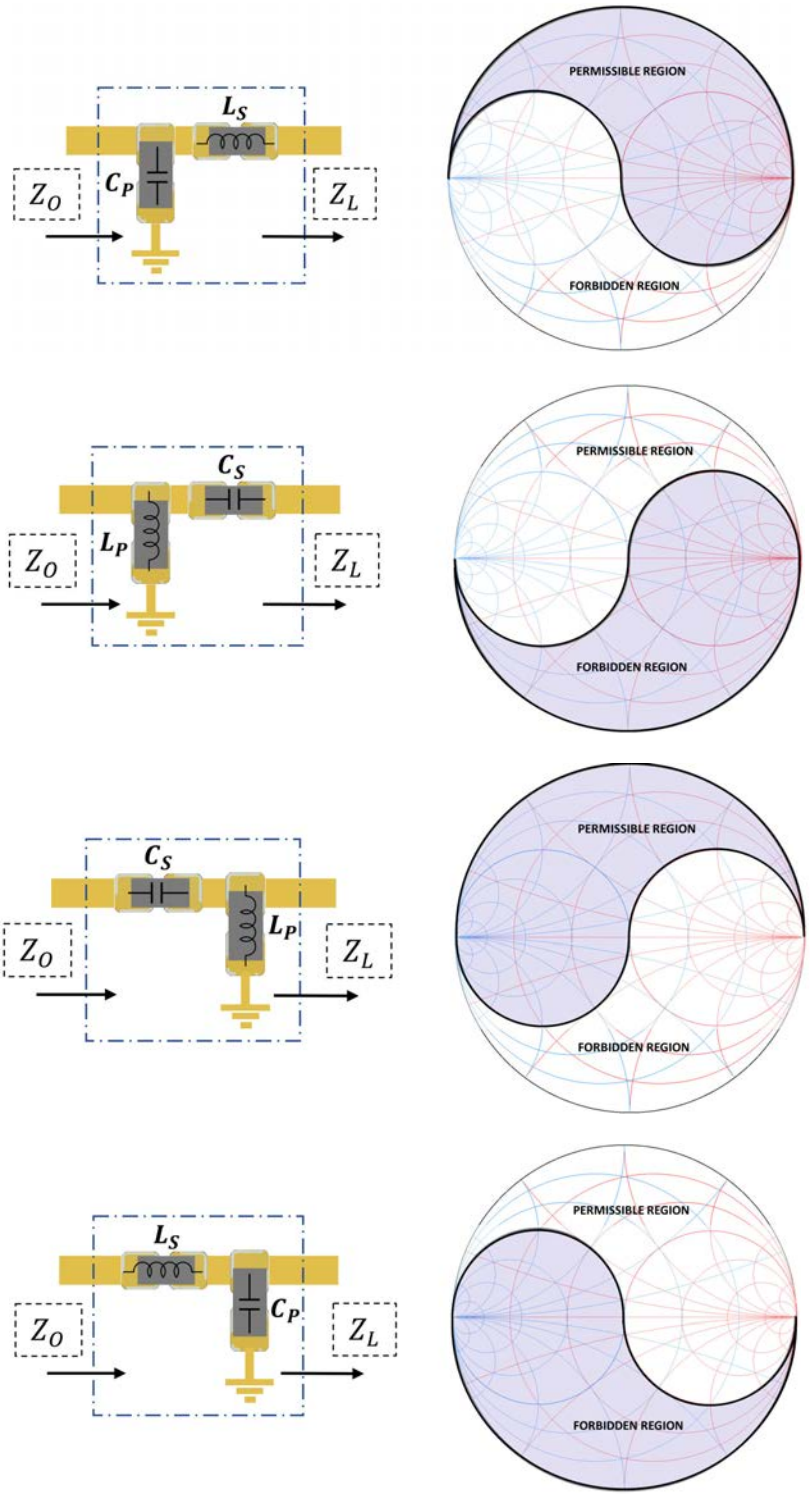


Figure 4.2. Type 1 and Type 2 LC Permissible and Forbidden Regions on Smith Chart

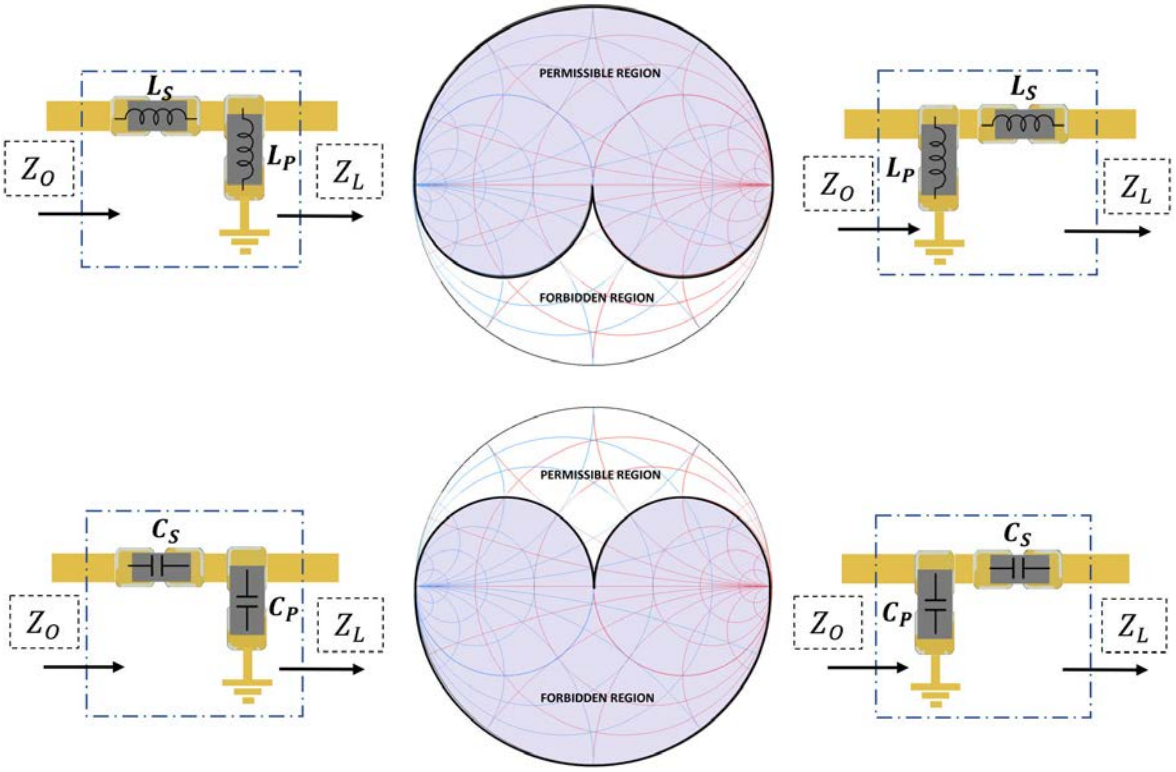


Figure 4.3. Type 1 and Type 2 LL/CC Permissible and Forbidden Regions on Smith Chart

From the preceding figures, we can see that if we want to use a typical type of two-element network configuration, then the impedance to be matched should lie in the “Permissible Region”. If the impedance to be matched lies in the “Forbidden Region”, then that particular matching network configuration cannot be used as it is impossible to bring the impedance towards the characteristic impedance point (Origin/ center) of the Smith chart.

The configuration where the two quantities are of same type, (L_S – L_P) *and* (L_P – L_S) *or* (C_S – C_P) *and* (C_P – C_S), are only valid when the load has low resistance and low conductance at the same time. We can also see that (L_S – L_P) *and* (L_P – L_S) can only match capacitive loads lying outside both unit circles and (C_S – C_P) *and* (C_P – C_S) can only match inductive loads lying outside both unit circles as shown in the above figure.

However, the configuration where the two quantities are of the opposite type is valid for any kind of load and thus covers wider possible locations of the impedance to be matched on the Smith chart. We can also see that the permissible region allowed for configuration with same type of quantities can also be covered using the configuration with a different type of quantities. For example, the permissible region for (L_P – C_S) *or* (L_S – C_P) is equal to the permissible region for (C_S – C_P) *or* (C_P – C_S) plus unit conductance circle or plus unit resistance circle respectively. Hence the configurations with components of opposite types are generally preferred and will be used wherever applicable in the following sections of this application note.

Most of the time, the source and the load have their own stray reactance which might complicate the calculations. Hence this stray reactance can be used as a part of the impedance matching network simplifying the calculations.

There are two possible approaches to handling complex impedances:

- **Absorption**—This approach absorbs any stray reactance into the impedance matching network by smartly placing each impedance matching component with the stray reactance. Example: Place the parallel element like a capacitor parallel to the stray capacitance. (See 7.1.2 High-Pass Configuration.)
- **Resonance**—This approach resonates with any stray reactance with an equal and opposite reactance at the operating frequency. (See 7.1.1 Low-Pass Configuration.)

Sometimes the stray reactance is much larger than the calculated required reactance, hence a combination of both approaches can be used

The biggest drawback of the two-element matching network is that the source and load resistance or impedance are determined but the Q of the network is defined. i.e. The limitation of the two-element network is that the designer does not have control over the value of

the Q of the network because the value of Q is a function of the value of the resistance of the series and the parallel matching components. Thus, while designing the L matching network the designer may end up with a fixed Q or with a fixed bandwidth which may or may not satisfy the circuit requirements.

5. Three-Element Matching Network Architecture

As per the previous definition, the Q of the network defines the bandwidth of the matching network, which proves to be a very important parameter when designing an impedance matching network for an RFIC chip. The applications where a wideband matching network is required, a two-element match would be sufficient. But for the applications that need to limit the bandwidth, it might not be possible to achieve a high Q matching network with L-matching network architecture.

In the case of a matching network on the antenna side, a two-element matching network is usully sufficient. Sometimes, however, the antenna is so narrowband (High Q) that it cannot be matched using just two-elements as neither of the two components would be optimal for matching the antenna over its frequency band. Hence, a three-element network would be required as the three-element network provides additional degree of freedom to match the antenna out of all possible combinations even if the antenna has high Q.

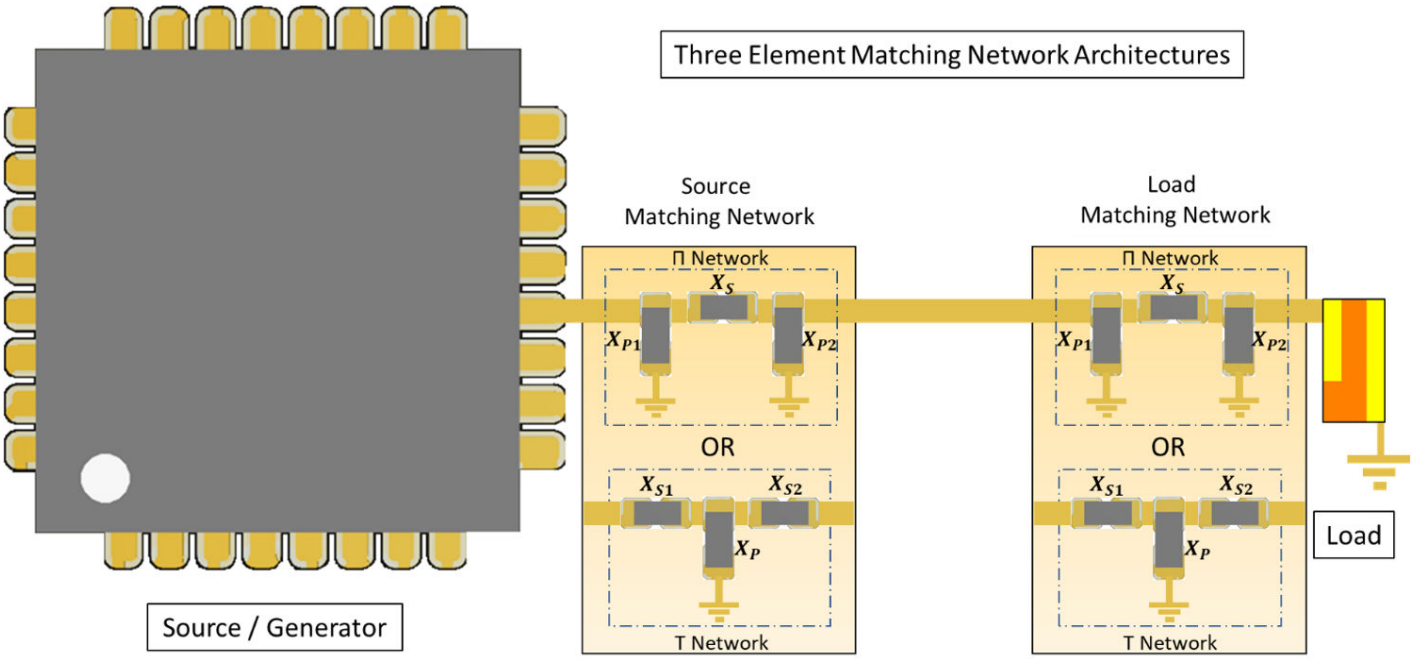


Figure 5.1. Three-Element Impedance Matching Network Architecture

A three-element matching network provides flexibility to the designer to choose any practical value of the circuit Q which is higher than that can be possibly achieved just by a two elements match. i.e. The circuit Q established while designing an L network will be the minimum circuit Q that can be chosen for a three-element network. There are two possible three-element matching network architectures:

- **Pi Network**—Component Orientation resembles with Greek Letter Π.
- **T Network**—Component Orientation resembles Latin Alphabet T.

5.1 The Pi Network

The Pi network can be constructed just by connecting two L networks back to back. Connecting two L networks creates an additional virtual/imaginary component (called virtual resistance and denoted as “R”) that is located at the junction of the two L networks. Note that the virtual resistance is not a physical component present in the Pi network rather it is a virtual component only used and calculated to determine the values of the components of both individual L networks.

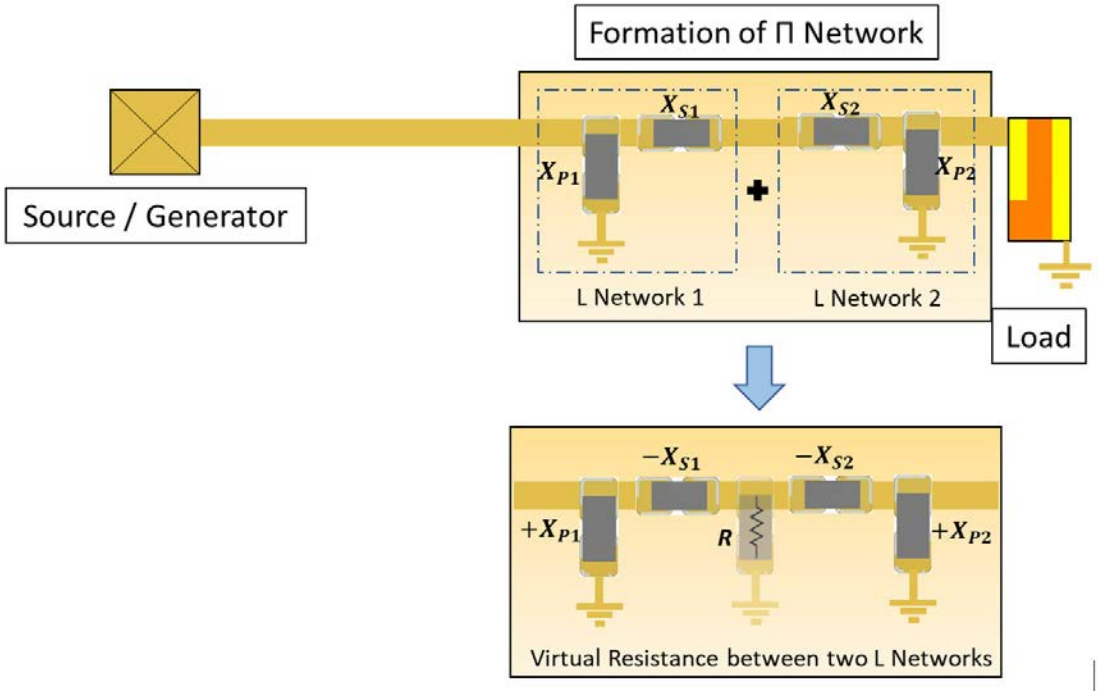


Figure 5.2. Formation of a Pi Matching Network

Please note that the negative sign in the above figure does not indicate negative reactance (i.e. capacitor) of the component. The polarity (+/-) signs associated with the components is to denote that the components with opposite signs have opposite reactance. i.e., within L Network 1, if X_{S1} is a capacitor then X_{P1} should be an inductor, and, similarly, in L Network 2, if X_{S2} is an inductor, then X_{P2} should be a capacitor, and vice versa. The above condition has been taken into consideration to force the use of the network configuration with components of opposite types.

The function of the virtual resistance is to bring down the larger impedance of the network and match with the lower impedance of the network. This can be achieved by using a parallel component in the network; thus, the virtual resistance would be virtually placed parallel in the network. As the virtual resistance is formed and connected to the series component of the network, the value of R will be lower than the Source or the Load resistance. The value of R can be determined by the Q of the network. As the biggest advantage of having a three-element network is to be able to choose Q, the value of R can be calculated by the following formula:

$$Q = \sqrt{\frac{R_H}{R} - 1} \quad or \quad R = \frac{R_H}{Q^2 + 1}$$

Where:

R_H = Higher terminating resistance in the network (Source or Load)

R = Virtual Resistance

Once the value of R gets determined, the individual component of the respective L network’s value can be calculated, and thus two separate L networks (4 elements) are formed with the help of the virtual resistance. The two series components of each L network can be now combined by adding their reactance. The type of the resultant component will be dependent on the polarity of the final reactance and thus a three-element matching network with the desired Q is obtained.

5.2 The T Network

The T network is the second type of three-element matching network architecture. The T network can be constructed by placing one L network vertically mirrored with the second L network. Similar to the three-element Pi network, there is a virtual resistance formed between the junction of the two L networks. The only difference here is that the virtual resistance value is larger than the load or the source resistance. This is achieved by connecting the parallel legs of both networks together, leaving the series resistance acting as the terminating resistors.

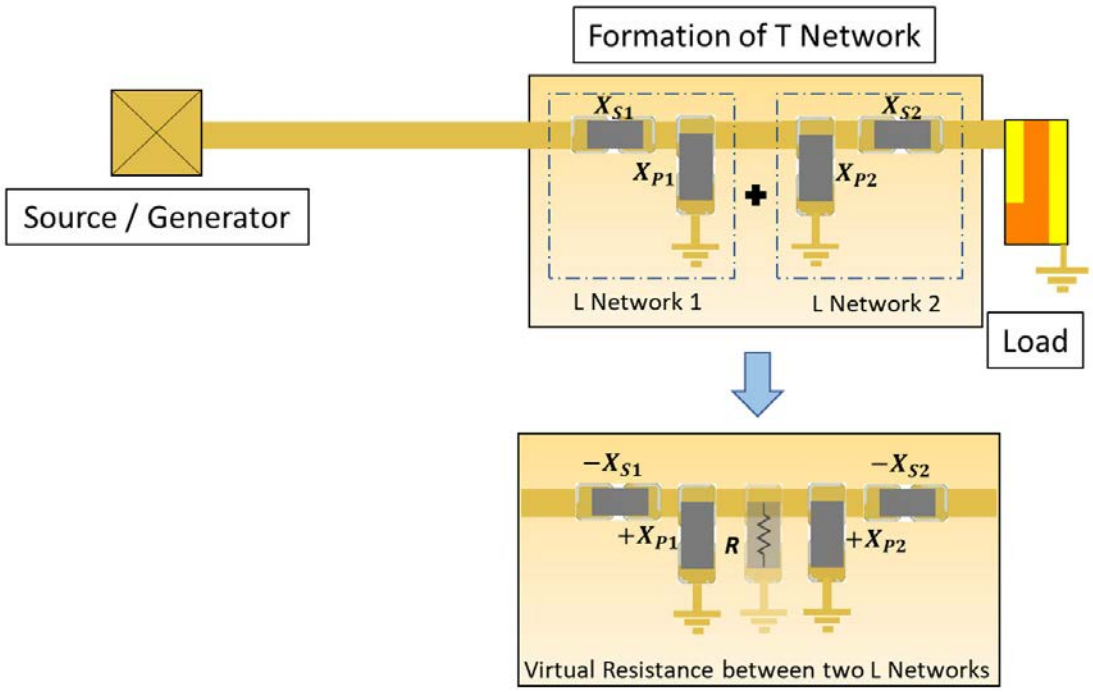


Figure 5.3. Formation of a T Matching Network

The Q of the T network is determined by the L network that has the highest Q. The L network with the highest Q will always occur on the end which has the smallest terminating resistor. The formula to calculate the loaded Q of the T network is as follows:

$$Q = \sqrt{\frac{R}{R_{Smaller}} - 1}$$

Where:

R = Virtual Resistor

$R_{Smaller}$ = Smallest terminating resistance

As can be seen, the formula to calculate the Q of the network is exactly the same as that for Pi network. During the construction of T Networks, we had to flip/mirror one of the L networks, which leads to the flipping of the virtual resistance.

Once the Q of the matching network has been defined, the virtual resistance can be calculated thereby obtaining the reactance value of each element of the two L networks. As the parallel elements share the common point in the network, the network can be further reduced by combining the reactance of both parallel components. Similar to the three-element Pi network, the polarity of the component that has higher value defines the type of the resultant component in the network.

For efficient filter designs, it is important to understand which structure should be used for a typical application. The LPF configuration of a structure presents a low or high impedance at the harmonic frequencies to suppress them. High-impedance LPF reflects the harmonics back to the source while the low-impedance LPF shunts the harmonic energy to the GND plane. High-impedance LPF typically uses a T-network structure starting with the series Inductor, whereas low-impedance LPF uses a Pi network structure starting with a parallel Capacitor. Hence the impedance of the load and/or source at the harmonic frequency will determine which structure of the network would be efficient. The recommended approach is given as follows:

1. Use a T network architecture between low-value impedances (< 50 Ω).
2. Use a Pi network architecture between high-value impedances (> 50 Ω).

6. Four or More Element Matching Network Architecture

6.1 Wideband Matching Networks

The matching network architectures discussed so far either had their Q as a function of the component's value (For L Network) or the Q was chosen to be higher than that could be achieved by L networks (For Pi and T Networks). Higher Q correlates to Narrower network bandwidth characteristics. Thus, we can say that the Pi or T networks have Narrower bandwidth than L networks, and similarly, the L networks have a wider bandwidth than Pi or T networks.

The applications that need impedance matching over a wide variety of frequency range demands for an impedance matching network that has wider bandwidth than a single L network. This can be achieved by implementing a constant Q curve technique (shown in 6.1 Wideband Matching Networks) i.e., by using more than one L Network in the same configuration. Cascading an L network with another L network in the same configuration results in a wideband matching network which is also called as a Low Q networks.

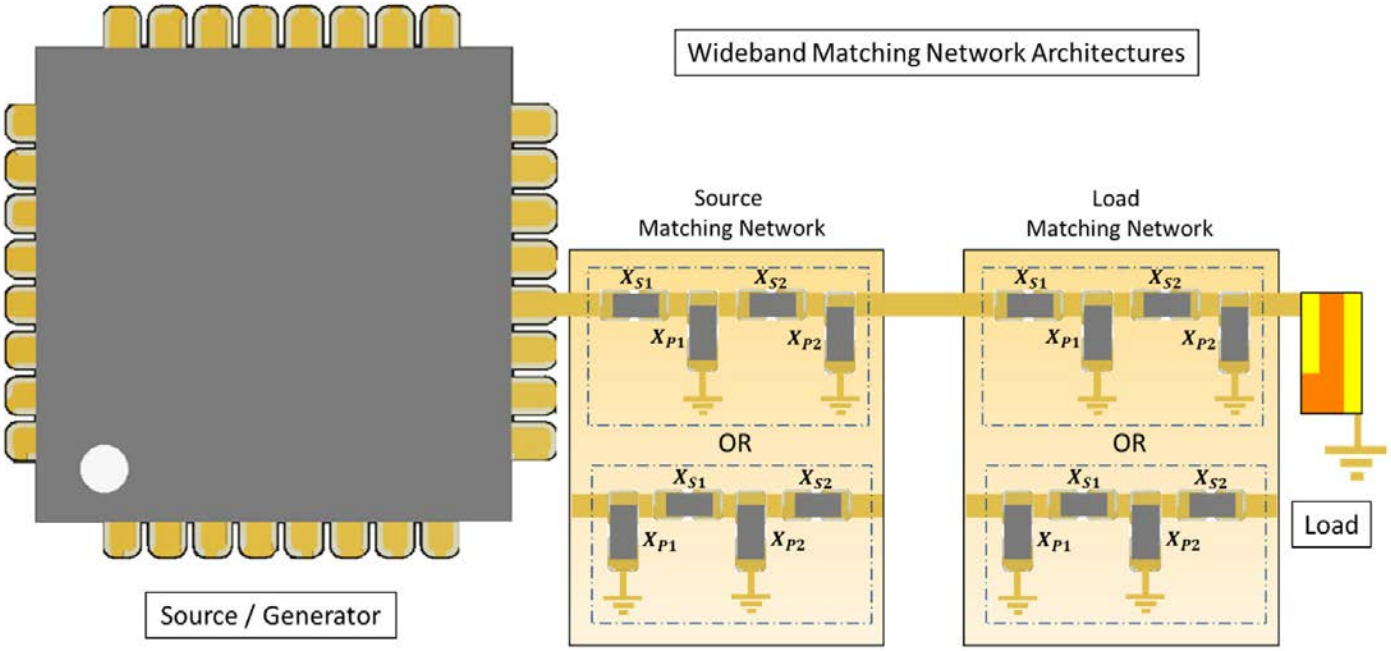


Figure 6.1. Four or More Element Wideband Impedance Matching Network Architecture

There are two types of wideband matching network architecture; one has virtual resistance in series with the L networks and the other has the virtual resistance in parallel with the L networks. For both of these wideband networks, the value of the virtual resistor must be larger than the smallest termination impedance and also must be smaller than the largest termination impedance. The net result of connecting two L networks in series with each other is a range of loaded-Q values that is less than the value of Q that could have been achieved by a single L network.

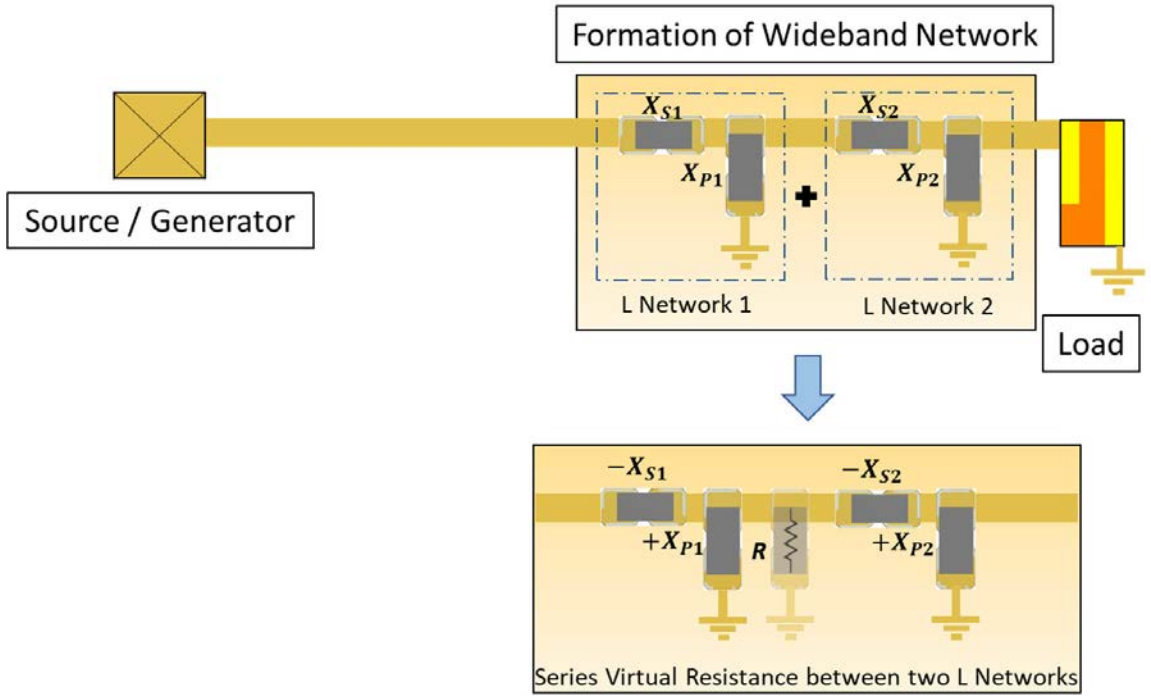


Figure 6.2. Formation of Wideband Matching Network Architecture - Type 1

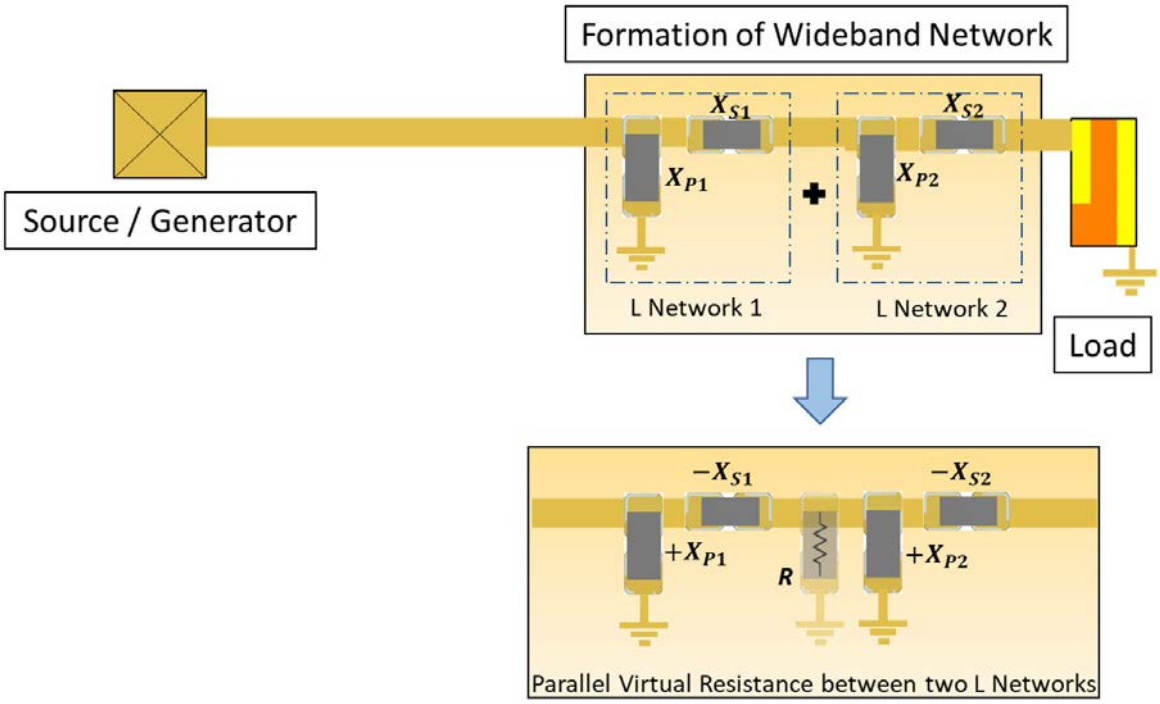


Figure 6.3. Formation of Wideband Matching Network Architecture - Type 2

The minimum Q (or the maximum bandwidth) that can be obtained for these networks is when the value of the virtual resistor is the mean of the two impedances being matched.

$$R = \sqrt{R_{Source} \times R_{Load}}$$

The formula to calculate the loaded Q of the wideband network is as follows:

$$Q = \sqrt{\frac{R}{R_{Smaller}} - 1} \quad = \quad \sqrt{\frac{R_H}{R} - 1}$$

Where:

$R_{Smaller}$ = Smallest terminating resistance in the network

R_H = Highest terminating resistance in the network

To obtain an even wider bandwidth, more L network blocks can be cascaded. This allows the designer to control the matching network's internal impedance without compromising / changing the Q of the network at the cost of addition on the components.

The following Smith chart examples show a matching exercise where the same load impedance is matched using two different matching network architectures.

6.2 Constant Q Lines: Two-Element vs. Four-Element Matching Networks

From the following figure, it can be seen that the load has been matched using only two elements, while the matching network's Q is greater than 0.5 (Q ~ 0.7).

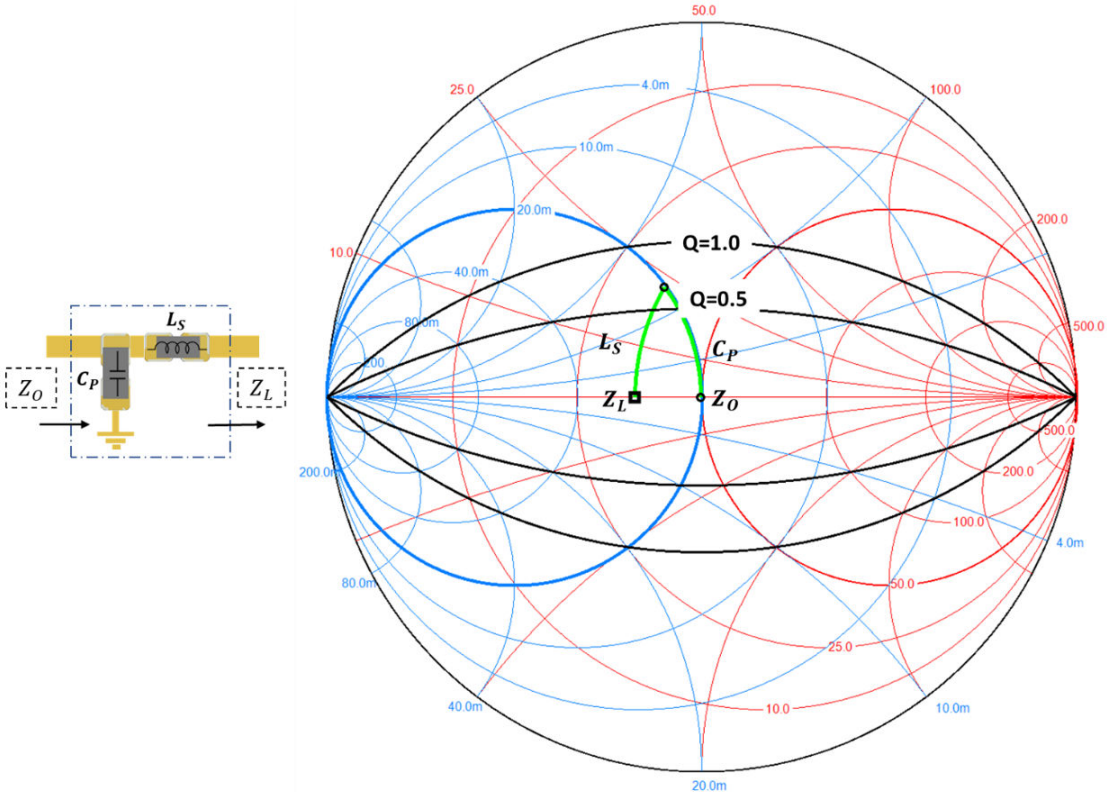


Figure 6.4. Two Element Matching Network with Q = 0.7

From the following figure, we can see that the same load has been matched to characteristic impedance using 4 elements while the Q of the matching network is under 0.5 (Q ~ 0.46).

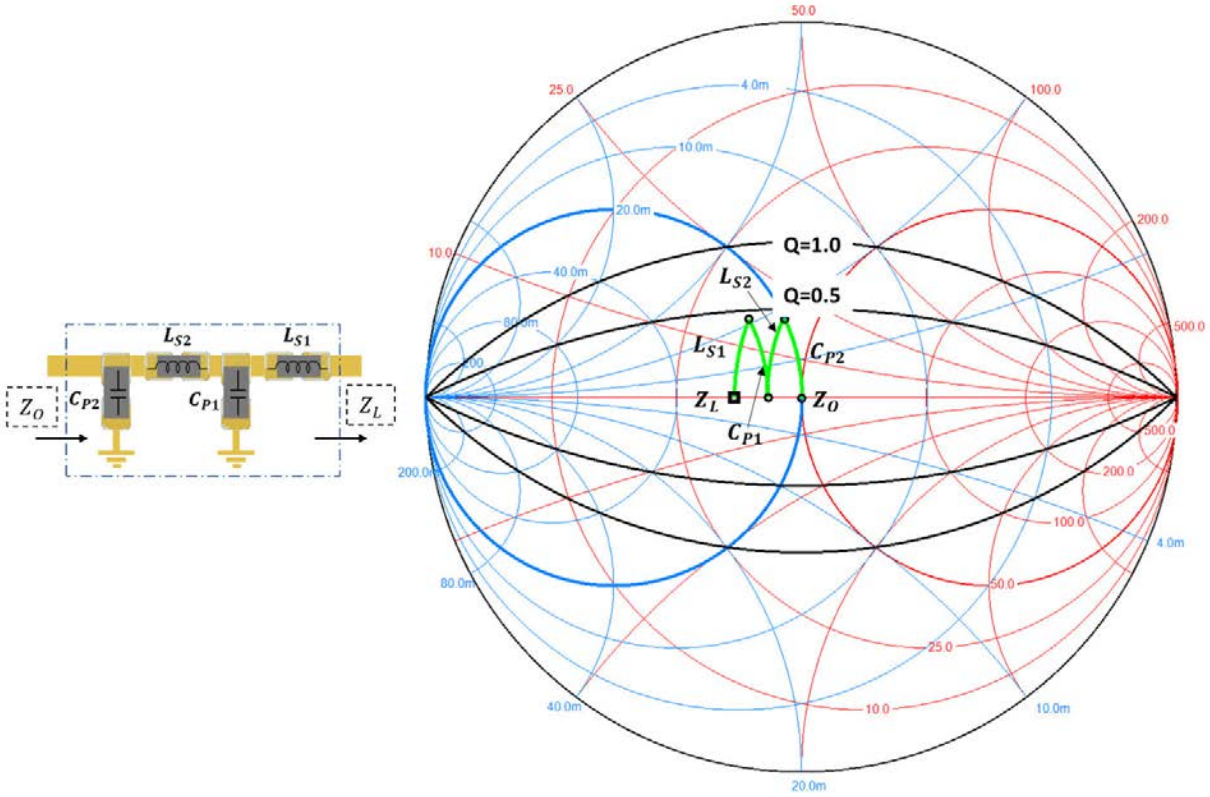


Figure 6.5. Four Element Matching Network with Q = 0.46

From the above two examples, we can see that by adding more components or by cascading multiple L networks, we can obtain a Low Q matching network or also called as wideband matching network for the same value of impedances.

7. Numerical Example

As we are now familiar with the theory behind the construction and working of each matching network architecture, let's try to design a matching network for a known practical source impedance with a practical antenna. This Application note will discuss two problem statements that cover the whole generic RF path from the source to load. The whole RF path can be divided into two sections:

1. RFIC to 50 Ω.
2. 50 Ω to the Antenna

Each problem statement will focus on individual points describing step by step guidance on impedance matching exercise.

7.1 Problem Statement 1

The optimum termination impedance for EFR32 Series 1 RFIC for 2.4 GHz is Z_{Load_Opt} = ~23 + j11.5 Ω. The center frequency of operation is 2445 MHz. Design a two-element matching network presenting optimum load impedance to the EFR32 Series 1 RFIC and match its impedance to a 50 Ω load connected by a 50 Ω trace.

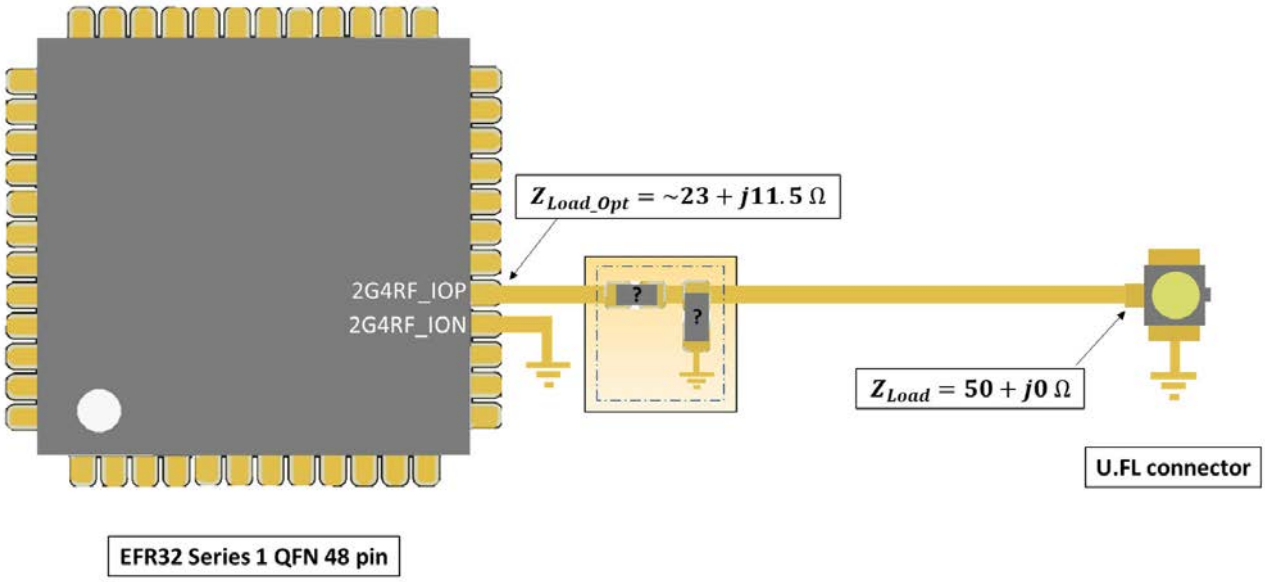


Figure 7.1. Graphical Representation for Problem Statement 1

Solution

In the problem statement it is mentioned that the optimum impedance for the RFIC is 23 + j11.5 Ω. We know that the input of the matching network will be connected to the RFIC, thus for maximum power transfer to occur between the RFIC and the network, the matching network's input impedance should be complex conjugate of the RFIC's output impedance. Hence, source impedance in this example will be with respect to the input of the matching network i.e., Z_{Source} = 23 – j11.5 Ω. In this example, from the problem statement we know the following information:

Z_{Source} = 23 – j11.5 Ω

R_{Source} = 23 Ω

X_{Source} = –j11.5 Ω

F = 2445 MHz

Z_{Load} = 50 + j0 Ω

R_{Load} = 50 Ω

Let's start with the design. We know that in two-element L type matching network, there can be two possible architectures. To determine whether the parallel component will be before the series component or after, we will need to determine who has higher impedance, source or the load. From the given data, the load impedance is higher when compared to the source impedance, thus the parallel component will be on the right side (towards the load). Hence the EFR matching network will be a series-parallel two element network.

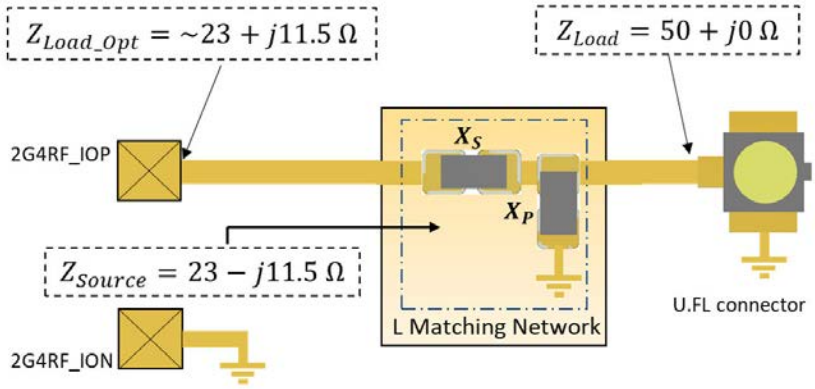


Figure 7.2. Type 2 L-Network Architecture

From the above image and given information, we can see that $R_{Source} = R_S$ and $R_{Load} = R_P$.

Let's find out the Q of the two-element matching network.

$$Q_S = Q_P = \sqrt{\frac{R_P}{R_S} - 1}$$

$$= \sqrt{\frac{50}{23} - 1}$$

$$= \sqrt{\frac{27}{23}}$$

$$\mathbf{Q_S = Q_P = 1.08}$$

Hence the series reactance for the matching network is:

$$Q_S = \frac{X_S}{R_S}$$

$$X_S = Q_S \times R_S$$

$$X_S = 1.08 \times 23$$

$$\mathbf{X_S = 24.84 \quad \Omega}$$

Similarly, the parallel reactance for the matching network is:

$$Q_P = \frac{R_P}{X_P}$$

$$X_P = \frac{R_P}{Q_P}$$

$$X_P = \frac{50}{1.08}$$

$$\boldsymbol{X_P = 46.29 \quad \Omega}$$

There are two possible configurations in the two-element L type matching network:

- **Low Pass Configuration**—Series Inductor and Parallel Capacitor
- **High Pass Configuration**—Series Capacitor and Parallel Inductor

Considering that we are designing the RFIC matching network, we want to block higher frequencies (harmonics) from passing through the antenna. Hence the desired matching network for our problem statement should be a low pass configuration. But we will solve for both configurations and find out component values in both scenarios.

7.1.1 Low-Pass Configuration

In the low-pass configuration, the series component is an inductor whereas the source reactance is a capacitor (determined from the negative sign in the source reactance), hence we will use resonance method to calculate the component values.

In this method first we will remove the stray capacitor by resonating it with a series inductor ($L_{Resonating}$) at the center frequency with exact same reactance as that of the capacitor. As we know that, equal reactance of opposite polarity cancels each other, We add +j11.5 Ω (Positive sign denotes it is an inductor) in series with –j11.5 Ω capacitor. Once we have removed the stray reactance from the circuit, we can now calculate the series and parallel components of the matching network.

In low pass configuration, the parallel component is a capacitor, hence $X_P = X_C$:

$$X_C = \frac{1}{2 \times \Pi \times F \times C}$$

$$C = \frac{1}{2 \times \Pi \times F \times X_C}$$

$$C = \frac{1}{2 \times 3.14 \times 2445 \times 10^6 \times 46.29}$$

$$\boldsymbol{C = 1.40 \quad pF}$$

Similarly, we will calculate the series component of the matching network $X_L = X_S$.

$$X_L = 2 \times \Pi \times F \times L'$$

$$L' = \frac{X_L}{2 \times \Pi \times F}$$

$$L' = \frac{24.84}{2 \times 3.14 \times 2445 \times 10^6}$$

$$\boldsymbol{L' = 1.61 \quad nH}$$

The above value of L' is not the final matching network's value. In addition to the calculated values of C and L', we had added a series inductor ($L_{Resonating}$) to resonate the source capacitance in the circuit. Thus, we have three matching elements, which can be reduced to a two-element circuit by adding the two series inductors together. Hence,

$$L_{Resonating} = \frac{11.5}{2 \times 3.14 \times 2445 \times 10^6}$$

$$\boldsymbol{L_{Resonating} = 0.74nH}$$

$$L = L_{Resonating} + L'$$

$$L = 0.74 + 1.61$$

$$\boldsymbol{L = 2.35 \quad nH}$$

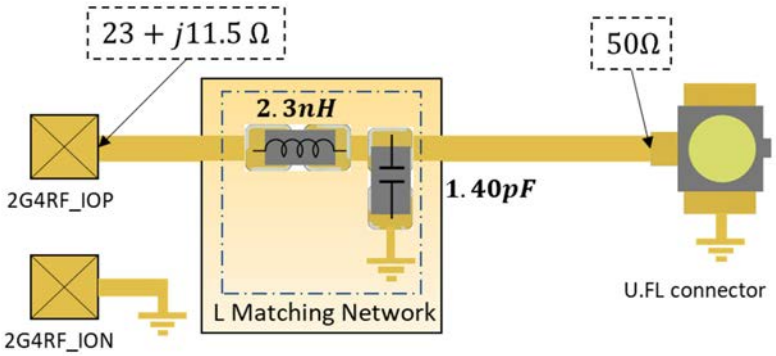


Figure 7.3. Low-Pass Configuration

7.1.2 High-Pass Configuration

In high pass configuration, the series element in the matching network is a capacitor and the source reactance is also a capacitor, hence we will use the absorption method to calculate the component's value.

In this method, we will try to utilize the stray reactance into the matching network and thus reduce the circuit component's value.

In high pass configuration, the parallel component is an inductor, hence $X_P = X_L$.

$$X_L = 2 \times \Pi \times F \times L$$

$$L = \frac{X_L}{2 \times \Pi \times F}$$

$$L = \frac{46.29}{2 \times 3.14 \times 2445 \times 10^6}$$

$$\boldsymbol{L = 3.01 \quad nH}$$

Similarly, in high pass configuration, the series component is a capacitor with series reactance X_S = 24.84 Ω. We already have a series source reactance X_{Source} = 11.5 Ω, thus the total component reactance required by the matching network is:

$$X_{Total} = X_S - X_{Source}$$

$$X_{Total} = 24.84 - 11.5$$

$$\boldsymbol{X_{Total} = 13.34 \quad \Omega}$$

Hence calculating the capacitor's value in the matching network:

$$X_{Total} = \frac{1}{2 \times \Pi \times F \times C}$$

$$C = \frac{1}{2 \times \Pi \times F \times X_C}$$

$$C = \frac{1}{2 \times 3.14 \times 2445 \times 10^6 \times 13.34}$$

$$\boldsymbol{C = 4.88 \quad pF}$$

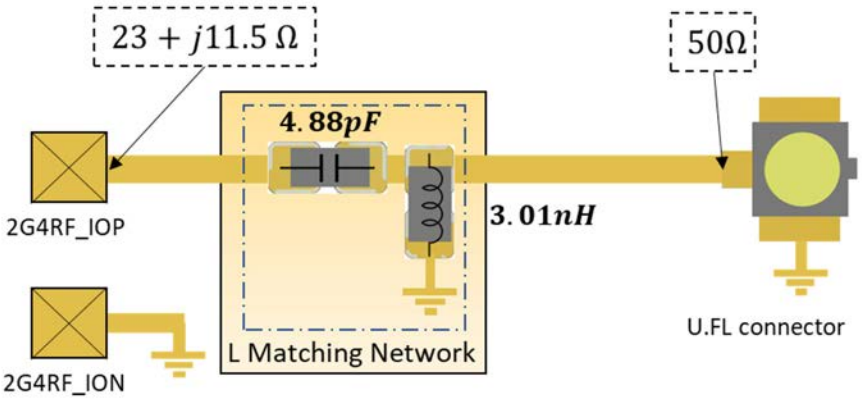


Figure 7.4. High-Pass Configuration

Hence by adding a two-element L type matching network, we have matched source impedance with 50 Ω impedance. Please note that the component values calculated above are for the ideal lossless components. In practical applications, we will need to consider SMD component losses and parasitics along with the PCB parasitics. The steps to consider these practical SMD and PCB losses for a two-element network are given in "AN930.1: EFR32 Series 1 2.4 GHz Matching Guide".

7.2 Problem Statement 2

A chip antenna was mounted on a 4-layer PCB of 62 mil thickness and the impedance value of ~21 + j1.15 Ω was measured right at the feed point of the antenna. Design an impedance matching network to match the antenna with 50 Ω source impedance operating at 2445 MHz with 500 MHz bandwidth and passes dc current.

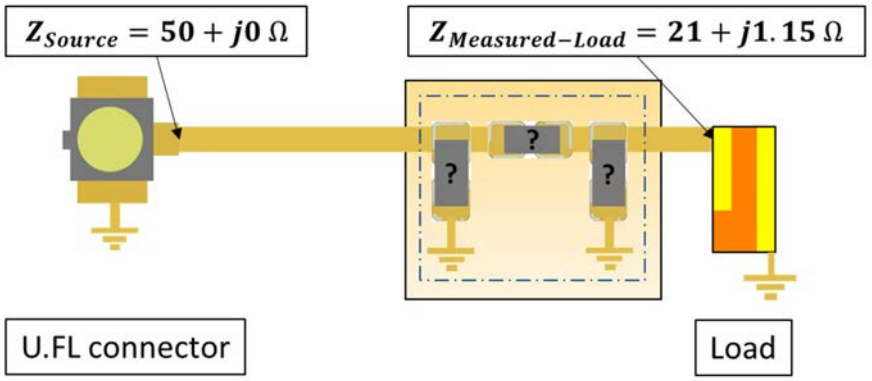


Figure 7.5. Graphical Representation for Problem Statement 2

Solution

In this numerical example, the load impedance given is 21 + j1.15 Ω. For maximum power transfer to occur between the load and the source, we will have to design an impedance matching network which has output impedance that is complex conjugate of the load impedance along with the specified parameter of bandwidth. Hence the output impedance towards the load side for designing the matching network is 21 – j1.15 Ω. It is also given that the matching network should pass dc current, which denotes that the series component of the matching network should be an inductor. (Please note that the criteria of passing dc current is just a choice for this design statement, however usually we would want to block the dc current from being passed to the antenna). From the problem statement we know the following information:

Z_{Source} = 50 + j0 Ω

R_{Source} = 50 Ω

F = 2445 MHz

BW = 500 MHz

Z_{Output} = 21 – j1.15 Ω

R_{Load} = 21 Ω

X_{Load} = – j1.15 Ω

From the given information, we know that the bandwidth of the matching network required is 500 MHz, thus we need to calculate the required Q of the matching network which can be found out from the formula:

$$BW = \frac{F}{Q}$$

$$Q_{Reqd} = \frac{F}{BW_{Reqd}}$$

$$Q_{Reqd} = \frac{2445 \times 10^6}{500 \times 10^6}$$

$$\mathbf{Q_{Reqd} = 4.89}$$

As the required Q of the matching network is 4.89, let's find out the Q and bandwidth that can be obtained from the two-element matching network. To design a two-element impedance matching network for the given load impedance, we will have the parallel component on the source side.

$$Q_S = Q_P = \sqrt{\frac{R_P}{R_S} - 1}$$

$$Q_S = Q_P = \sqrt{\frac{50}{21} - 1}$$

$$\boldsymbol{Q_{\text{Two-Element}} = 1.17}$$

The bandwidth provided by a two-element matching network would be:

$$BW = \frac{F}{Q_{Two\text{-}Element}}$$

$$BW = \frac{2445 \times 10^6}{1.17}$$

$$\boldsymbol{BW_{\text{Two-Element}} = 2 \quad GHz}$$

Thus, a two-element matching network does not satisfy the requirements of the problem statement. Thus, we will need to design a three-element matching network, specifically a Pi network. To design a three-element matching network, we need to identify the virtual resistance within the network:

$$R = \frac{R_H}{Q^2 + 1}$$

$$R = \frac{50}{4.89^2 + 1}$$

$$\boldsymbol{R = 2.007 \quad \Omega}$$

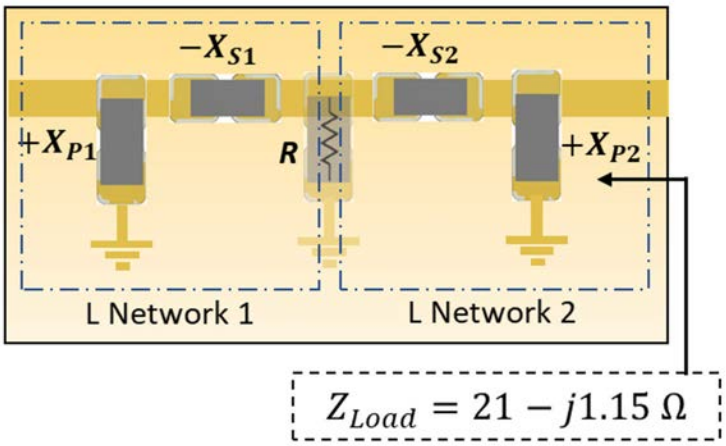


Figure 7.6. Deconstruction of a Pi Network

7.2.1 For L Network 1

As now we have the virtual resistance formed between the two L networks, let's calculate the L-Network 1 (Network towards the source) using the following formulas:

$$Q_{P1} = \frac{R_{P1}}{X_{P1}}$$

$$X_{P1} = \frac{R_{Source}}{Q_{Reqd}}$$

$$X_{P1} = \frac{50}{4.89}$$

$$\boldsymbol{X_{P1} = 10.22 \quad \Omega}$$

Now we will calculate the series component of the first two-element network. In the Pi network, we know that the virtual resistance resides in the series arm of the L network, hence we will substitute $R_S = R$ and $Q_S = Q_{Reqd} = Q_1$:

$$Q_S = \frac{X_S}{R_S}$$

$$X_{S1} = Q_1 \times R$$

$$X_{S1} = 4.89 \times 2.00$$

$$\boldsymbol{X_{S1} = 9.78 \quad \Omega}$$

This completes the design of the L section on the source side of the network.

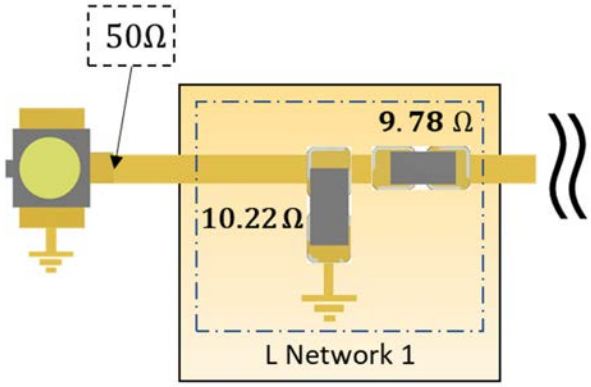


Figure 7.7. Completed L-Section on Network Source Side

7.2.2 For L Network 2

In the given numerical example, the chip antenna has a complex impedance that consists of a series reactance. The matching network that we are designing is a Pi network that has a parallel component on the side of the load. Hence to easily absorb the series reactance within the Pi network, we will have to convert the load components into its parallel equivalent circuit. Hence, we will calculate the following:

$$Q_{S_{Load}} = Q_{P_{Load}} = \frac{X_{S_{Load}}}{R_{S_{Load}}}$$

$$Q_{P_{Load}} = \frac{1.15}{21}$$

$$\boldsymbol{Q_{P_{Load}} = 0.054}$$

From the obtained Q of the load, we will find out the equivalent parallel circuit components of the load ($R_{P_{LOAD}}$ and $X_{P_{LOAD}}$):

$$R_{P_{Load}} = R_{S_{Load}} \times \left[\left(Q_{P_{Load}}\right)^2 + 1\right]$$

$$R_{P_{Load}} = 21 \times \left[(0.054)^2 + 1\right]$$

$$\boldsymbol{R_{P_{Load}} = 21.06 \quad \Omega}$$

$$X_{P_{Load}} = \frac{R_{P_{Load}}}{Q_{P_{Load}}}$$

$$X_{P_{Load}} = \frac{21.06}{0.054}$$

$$\boldsymbol{X_{P_{Load}} = 421.05 \quad \Omega}$$

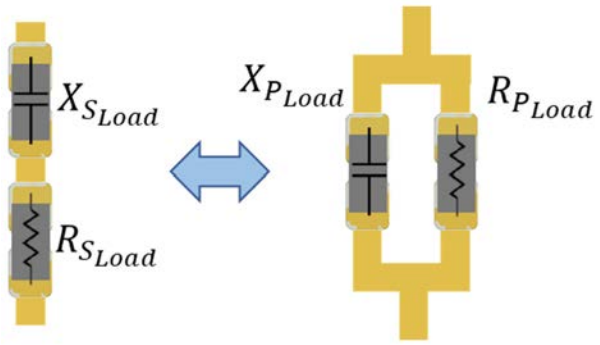


Figure 7.8. Load Transformation (Series to Parallel Equivalent)

Now, we have the parallel equivalent circuit of the complex load such that the load reactance can now be absorbed by the matching network. As the reactance has a negative sign, it denotes that the load has a capacitive reactance. Hence, we will calculate the capacitor's value:

$$X_{P_{Load}} = \frac{1}{2 \times \Pi \times F \times C_{Stray}}$$

$$C_{Stray} = \frac{1}{2 \times \Pi \times F \times X_{P_{Load}}}$$

$$C_{Stray} = \frac{1}{2 \times 3.14 \times 2445 \times 10^6 \times 421.05}$$

$$\boldsymbol{C_{Stray} = 0.154 \quad pF}$$

Now as we have modified the complex load, we will now calculate the Q for the L-Network 2 which is defined by the ratio of $R_{P_{LOAD}}$ to R, Hence we will find out the Q of the L-Network 2 using the same formula:

$$Q = \sqrt{\frac{R_{P_{Load}}}{R} - 1}$$

$$Q_2 = \sqrt{\frac{21.06}{2} - 1}$$

$$\boldsymbol{Q_2 = 3.087}$$

As we have the Q value of the L-Network 2, we will use this value to find out parallel component of the second network:

$$X_{P2} = \frac{R_{P_{Load}}}{Q_2}$$

$$X_{P2} = \frac{21.06}{3.087}$$

$$\boldsymbol{X_{P2} = 6.822 \quad \Omega}$$

Similar to L-Network 1, we will use the virtual resistance to calculate the series component in the L-Network 2 along with the Q of the second circuit.

$$Q_2 = \frac{X_{S2}}{R}$$

$$X_{S2} = Q_2 \times R$$

$$X_{S2} = 3.087 \times 2.00$$

$$\boldsymbol{X_{S2} = 6.174 \quad \Omega}$$

This completes the design of the Second L section on the load side of the network.

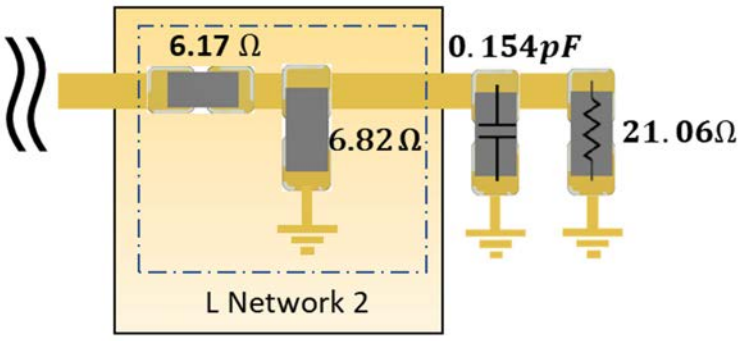


Figure 7.9. Completed L-Section on Network Load Side

As we have all the required reactance of the matching network, we will put together Network 1 and Network 2 and form a three-element Pi network. For combining the two networks into one, we will add the series reactance of each network together:

$$X_{S_{Total}} = X_{S1} + X_{S2}$$

$$X_{S_{Total}} = 9.78 \quad + \quad 6.174$$

$$\boldsymbol{X_{S_{Total}} = 15.954 \quad \Omega}$$

Calculating the Pi network's component values:

$$C_{P1} = \frac{1}{2 \times \Pi \times F \times X_{P1}}$$

$$C_{P1} = \frac{1}{2 \times 3.14 \times 2445 \times 10^6 \times 10.22}$$

$$\boldsymbol{C_{P1} = 6.37 \quad pF}$$

$$X_{S_{Total}} = 2 \times \Pi \times F \times L$$

$$L = \frac{X_{S_{Total}}}{2 \times \Pi \times F}$$

$$L = \frac{15.954}{2 \times 3.14 \times 2445 \times 10^6}$$

$$\boldsymbol{L = 1.04 \quad nH}$$

$$C'_{P2} = \frac{1}{2 \times \Pi \times F \times X_{P2}}$$

$$C'_{P2} = \frac{1}{2 \times 3.14 \times 2445 \times 10^6 \times 6.822}$$

$$\boldsymbol{C'_{P2} = 9.54 \quad pF}$$

The required parallel component for matching the load, we need a 9.54 pF capacitor, but we already have a stray capacitance within the load of C_{Stray} = 0.154 pF. Thus, we will only need to physically install:

$$C'_{P2} - C_{Stray} = (9.54 - 0.154) \quad pF$$

$$\boldsymbol{C_{P2} = 9.38 \quad pF}$$

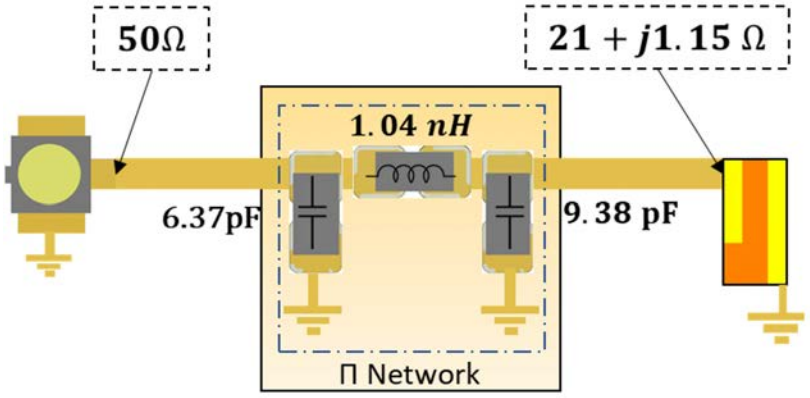


Figure 7.10. Final Three-Element Pi Matching Network

If there was no hard requirement of the network bandwidth in numerical example 2, then we could have quickly designed a wideband 2-element matching network.

For numerical example purpose, while we designed a high-Q matching network in the example 2, it should be noted that by designing a high-Q matching network does not always guarantee that lower harmonics will be obtained at the output and thus does not mean that a High-Q matching network is desired all the time. In some cases, the source impedance at the fundamental frequency might be different at different harmonic frequencies. Thus, if the load impedance is close to the complex conjugate of the source impedance at the harmonic frequency, we may see increase in the harmonic level even when the bandwidth of the matching network is narrow.

Taking an example from EFR32 series 1 LNA match mentioned in "AN923: EFR32 sub-GHz Matching Guide", the differential LNA pins of the RFIC has very high input impedance, thus designing a complex conjugate RFIC match to deliver maximum power will result into very narrowband matching network. Designing a High-Q (narrowband) network can lead to some problems such as difficulty in tuning the network as the network can become extremely sensitive to component value variations. We know that any electronic component has a (±) tolerance level due to which the component's value can slightly change from the desired value. Due to this change in the value, the narrowband matching network can now have its frequency response shifted from the desired frequency to another frequency. Thus, the matching network's bandwidth should be chosen carefully as per the design constraints and its requirements.

7.3 Simulation Example

For comparative analysis of L and Pi networks, let's check their performance by simulating the reflection coefficient (Γ) also denoted as S_{11} - Scattering parameter. We will use the component values from numerical Example 2 for the Pi network and will calculate the component values for the equivalent L network as per design steps given in numerical example 1. Hence, we obtain parallel component as C = 1.52 pF and series component as L = 1.68 nH for the equivalent L network.

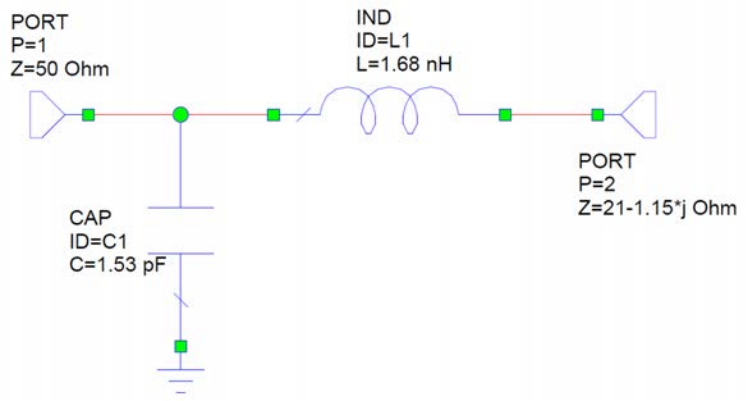


Figure 7.11. L-Matching Network Schematic

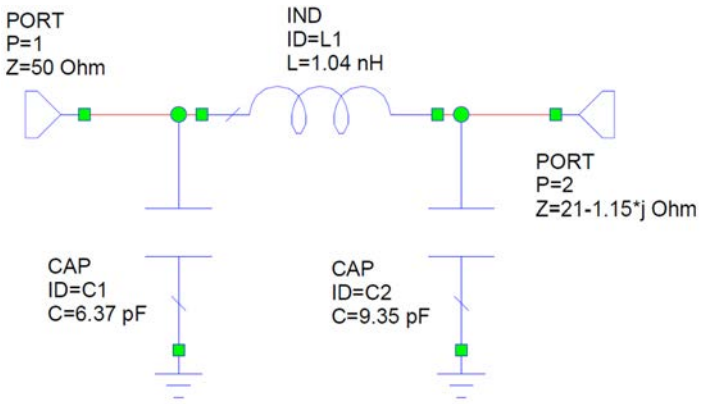


Figure 7.12. Pi-Matching Network Schematic

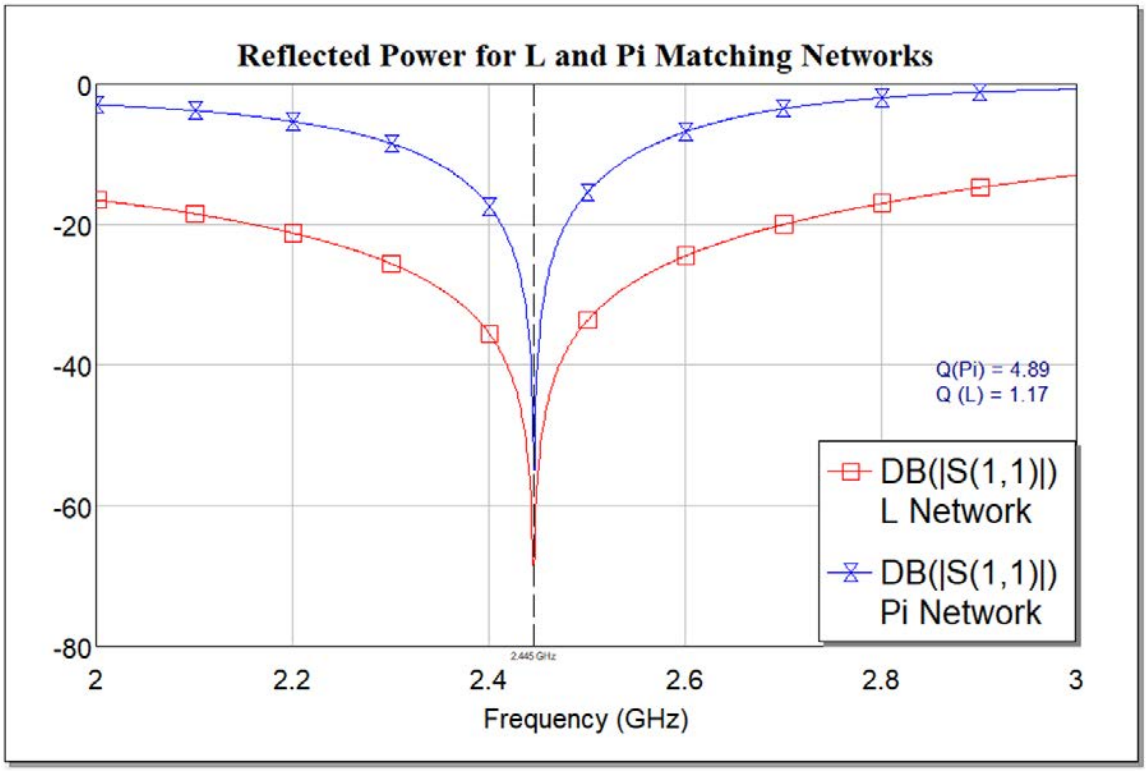


Figure 7.13. Magnitude Plot for Reflected Power (in dB) for Q(L) = 1.17 and Q(Pi) = 4.89

From the above simulated S_{11} plot we can see that both matching networks, Pi and L network has minimum reflection at the desired frequency i.e. 2.445 GHz. However, we can also see that the S_{11} value of the L network is below –12 dB for the entire 2 to 3 GHz frequency range, which suggests that basically the matching network passes all signals in the entire range and thus there is no attenuation of the unwanted signals in the entire 2 to 3 GHz frequency range.

For the Pi network we can see that the signals below 2.35 GHz and signals above 2.52 GHz have S_{11} values above –12 dB, which suggests that the Pi network attenuates the signals arriving below and above those frequencies. Hence, we can say that the Pi network is more selective in transforming impedance of the signal and has narrower reflection curve when compared to the L network. The selectivity of the signals is because of the chosen Q of the Pi network. If we design the Pi network with Q that is slightly greater than the Q obtained for L network, we will see that the curve obtained for Pi network is also similar to the curve obtained for the L network.

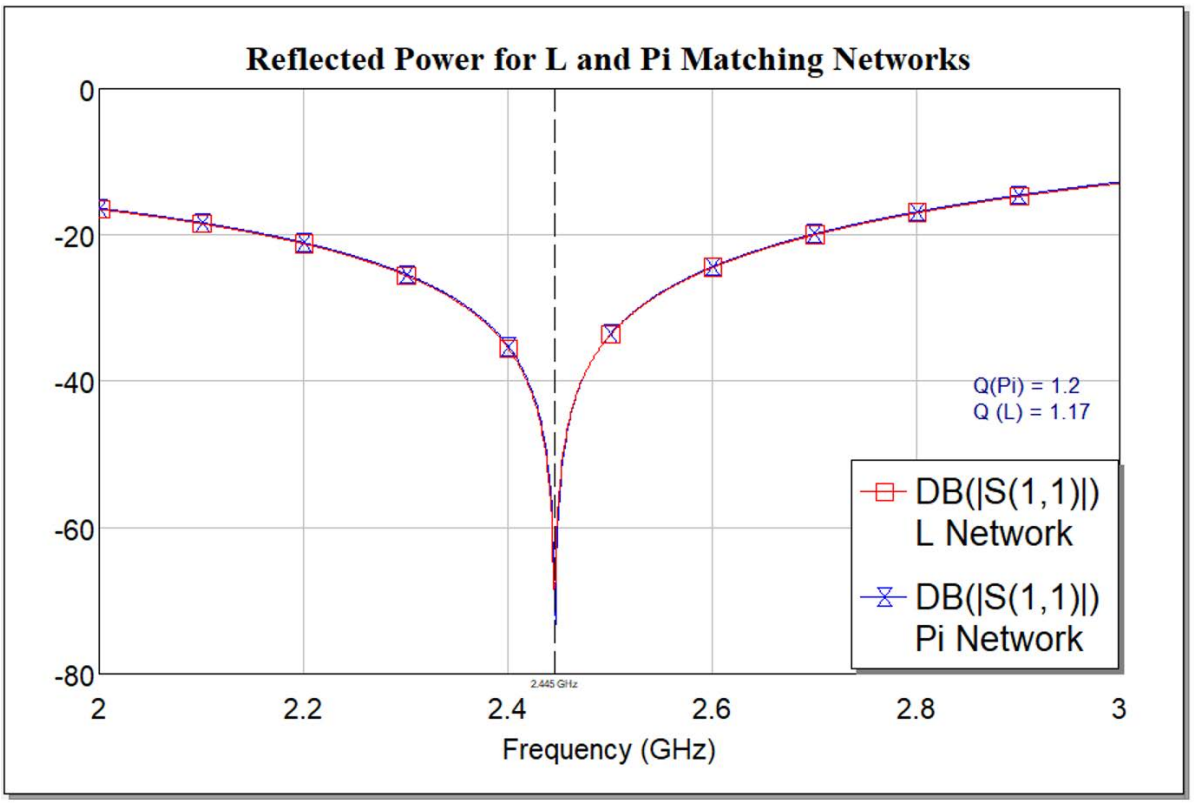


Figure 7.14. Magnitude Plot for Reflected Power (in dB) for Q(L) = 1.17 and Q(Pi) = 1.2

7.4 Antenna Matching Networks

In applications that use an antenna as the load, on the antenna side, it is hard to determine the exact load impedance without practically measuring it on the custom PCB. Thus, it becomes difficult to predict the architecture of the antenna matching network before fabricating the PCB. For this reason, it is always a good idea to add a three-element Pi shaped antenna matching network placeholder so that the designer can later tune the antenna by adding an appropriate matching component.

Reserving a three-element Pi shaped placeholder in the prototype board gives the following advantages:

1. In most RF applications, Low Pass configuration is desired. i.e., a series inductor is desired in the matching network. If we choose to use a T-network, we will need two series inductors which can prove to be expensive and more lossy. Whereas in a Pi network, only one series inductor would be required.
2. If the RF application does not need to limit the RF signal bandwidth, the same three element placeholder can be used to support either of the two element L type matching network architectures for matching the source and the load.

Apart from the second numerical example, there can be a possibility that the end application uses a PCB trace antenna (such as Inverted-F Antenna) instead of using the chip antenna. PCB trace antennas have an advantage over the chip variant as the dimensions of the antenna trace can be changed to change its impedance which results tuning the antenna without the need of additional circuitry.

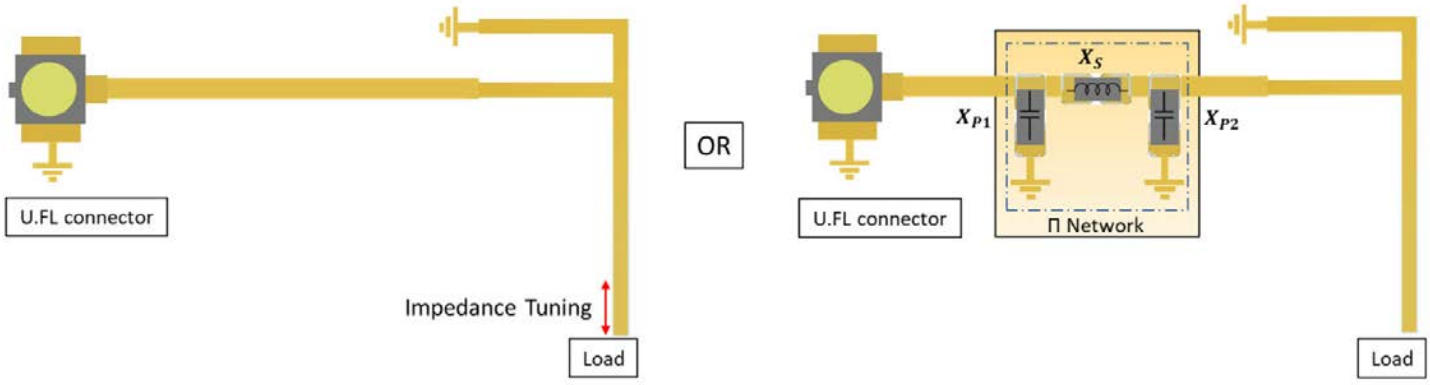


Figure 7.15. PCB Trace Antenna Tuning Methods

Even if the trace antenna can be tuned by changing its dimensions, there may be an application that needs to limit the signal bandwidth of the system. This could only be determined after the board is fabricated and tested. Thus, as stated above, it is always a good idea to reserve a space near the antenna for the three element Pi shaped antenna matching network placeholder even if a PCB trace antenna is being used. For more information on designing the Inverted-F PCB trace Antenna and other single-ended PCB antennas, please refer to "AN1088: Designing with an Inverted-F 2.4 GHz PCB Antenna" and "AN853: Single-Ended Antenna Matrix Design Guide".

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