FUJITSU

HIGH-SPEED CMOS SINGLE-CHIP 4-BIT MICROCOMPUTER WITH MULTI I/O & A/D CONVERTER

MB88550H SERIES

TM317-B872: February 1987

HIGH-SPEED CMOS SINGLE-CHIP 4-BIT MICROCOMPUTER WITH MULTI I/O AND A/D CONVERTER

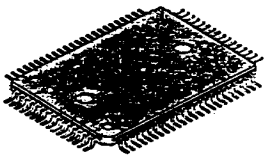
The Fujitsu MB88550H series CMOS single-chip 4-bit microcomputer family is a high-speed version of the MB88550 series. Its architechture and instruction set are the same as the MB88550 series, but its minimum instruction execution time is reduced to 1.5 µs min. using an 8 MHz crystal or external clock with a prescaler (at 4 MHz without a prescaler).

The MB88550H series consists of MB88551H and MB88552H. Differences between MB88551H and MB88552H is only ROM size. MB88551H contains a 8K x 8-bit and MB88552H contain 6K x 8-bit program memory (mask ROM). Both devices contains a 256 x 4-bit data memory (static RAM), 68 I/O lines (including a serial I/O port with a 4-bit buffer), an 8-bit timer/counter, a 5-bit resolution programmable successive approximation type A/D converter with 4 multiplex analog input, a 9-bit programmable pulse generator, and a clock generator. Its instruction set is the same as the MB88550 series, and the instruction execution time is 1.5 µs min. at a 8 MHz crystal with a prescaler. The device is fabricated by silicon-gate CMOS process, and packaged in an 80-pin plastic flat package (suffix -PF). It operate with +5V power supply over the temperature range of -30°C to +70°C.

CMOS technology allows the device to operate with low power dissipation (8 mA typ. at fc=2 MHz), and further the standby function (if implemented) enables data retention with lower current (20 µA max. at V_{CC}=6.0V).

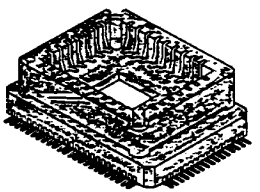
For user's development of the MB88550H series based system, Fujitsu provides the MB88400/500 cross-assembler and host-emulator which run on the CP/M-86 or PC-DOS machines (cross-assembler also run on the Intellec series III MDS), the MB2115 series evaluation board system, and the MB88558H piggyback EPROM evaluation devices which have 8K x 8-bit EPROM (MBM27C64). These development tools enables users to minimize their development time and cost.

MB88551H-PF/MB88552H-PF



80-PIN PLASTIC FLAT PACKAGE
(DIP-80P-M01)

MB88558H-CF



80-PIN CERAMIC MODULE
(MQP-80C-P01)

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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FEATURES

- CMOS Single Chip 4-bit Microcomputer

- Program Memory:
  - o MB88551H: 8K x 8-bit mask ROM
  - o MB88552H: 6K x 8-bit mask ROM

- Data Memory: 256 x 4-bit static RAM

- Three Selectable Output Port (E-, R-Ports) Circuits, Every 4-bit Port with Mask Option:
  - o Standard open-drain
  - o Standard pull-up
  - o High-current open-drain

- 68 I/O Lines:
  - o R-Port: Four 4-bit parallel or 16 individual input/output
  - o E-Port: Thirteen 4-bit parallel I/O or 52 individual output. Following E-Ports have another functions:
    - E24-E29: Serial I/O, interrupt input, timer/counter input, timing output, standby release input
    - E30-E31: Pulse generator I/O
    - E32-E35: Analog inputs

- Selectable LED Direct Drivable E-, R-Port (High-current open-drain output: 10mA) with Mask Option

- 8-bit Programmable Timer/Counter with Auto-loading Function/two Clock Modes:
  - o Internal (Timer)
  - o External (Counter)

- Software Selectable 4-/8-bit Serial Buffer with 3 Software Shift Clock Modes:
  - o Internal clock
  - o External clock
  - o Software clock

- 5-bit Programmable Successive Approximation Type A/D Converter with 4-multiplex Analog Inputs and Sample-hold Circuit

- On-chip 9-bit Programmable Pulse Generator

- On-chip Clock Generator with 2 Mask Options:
  - o External crystal/ceramic resonator or external clock drive
  - o External RC-network or external clock drive

- Selectable 1/2 Clock Prescaler for Expanding Clock Range with Mask Option

- Single Level Four Prior Source Maskable Interrupt:
  - o External
  - o Clock
  - o Timer/counter overflow
  - o Serial buffer full/empty

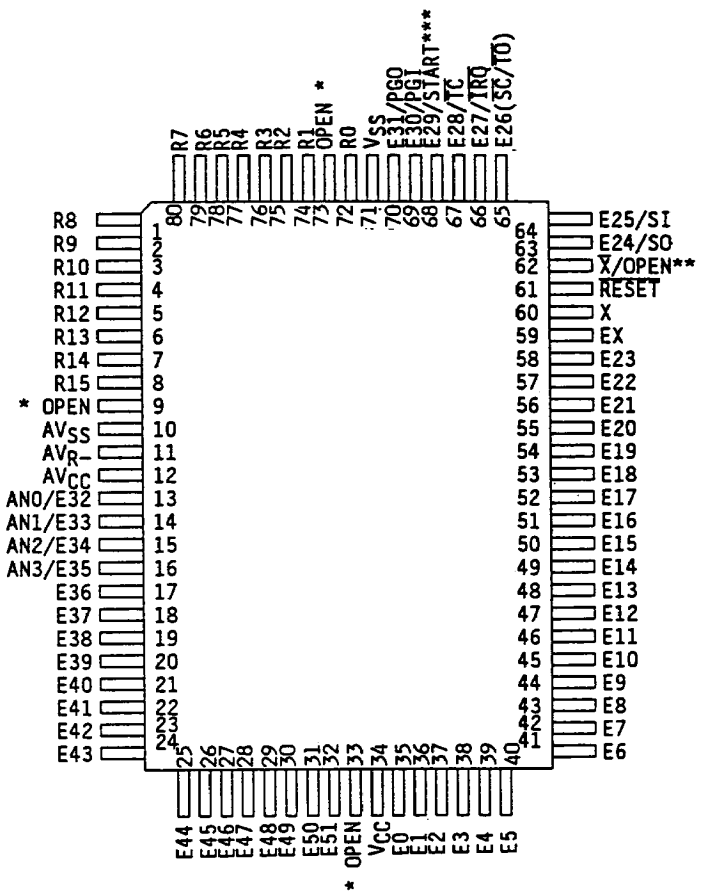
- 8-nesting Levels for Subroutine Call

FEATURES (Continued)

- Instruction Set : Same the MB88550 series
  - o Number of instructions : 82
  - o Instruction length/cycle: 1, 2, or 3 byte(s)/1 , 2, or 3 cycle
  - o Execution time : 1.5 µs min. at 8 MHz clock with prescaler
- On-chip Power-on Reset Circuit
- Low Power Standby Function: Software initiation and hardware release
- Two Selectable Selectable Output Port Level During Reset with Mask Option:
  - o High level
  - o Low level
- Two Selectable Output State During Standby with Mask Option:
  - o Hold
  - o High impedance
- Two Software Selectable Oscillation States During Standby:
  - o Idle
  - o Stop
- Standby off Reset with Mask Option
- Watch-dog Timer Function
- Low Power Dissipation with Mask Option:
  - o 8 mA at fc=2 MHz typ. (Active mode)
  - o 10 µA at fc=0 MHz max. (Standby mode)
- +5V Power Supply (VCC):
  - o 4.5V to 5.5V (Active mode)
  - o 3.5V to 6.0V (Standby mode)
- Analog Power Supply (AVCC): 4.5V to 5.5V
- Wide Operation Temperature Range: T_A= -30 °C to +70 °C
- Silicon Gate CMOS Technology
- Package Type: 80-pin Plastic Flat Package
- Powerful development support:
  - o CP/M-86, PC-DOS, or Intellec series III MDS cross assemblers (SM07415-A012/SMXXXXX-XXXX/SM05215-A010)
  - o CP/M-86 or PC-DOS host-emulator software for monitoring evaluation board and symbolic debugging (SM07415-G022/SMXXXX-XXXX)
  - o MB2115 evaluation board (MB2115-01, -02, -04, and -36A) for software debugging
  - o MB88558H CMOS piggyback EPROM evaluation

Fig. 1: PIN ASSIGNMENT

MB88551H/MB88552H



Note:
* This pin should not to be connect.
** If selected oscillation output by mask option, pin 62 is $\overline{X}$. If not, pin 62 not, pin 62 is OPEN.
*** If selected standby by mask option, pin 68 is START pin. If not, pin 68 is E29 pin.

Fig. 2: LOGIC SYMBOL

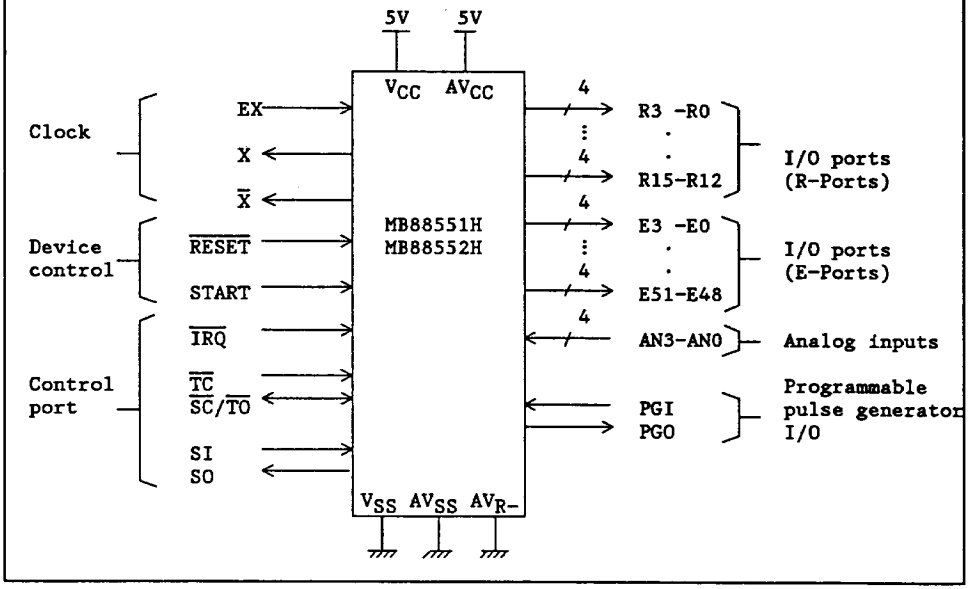


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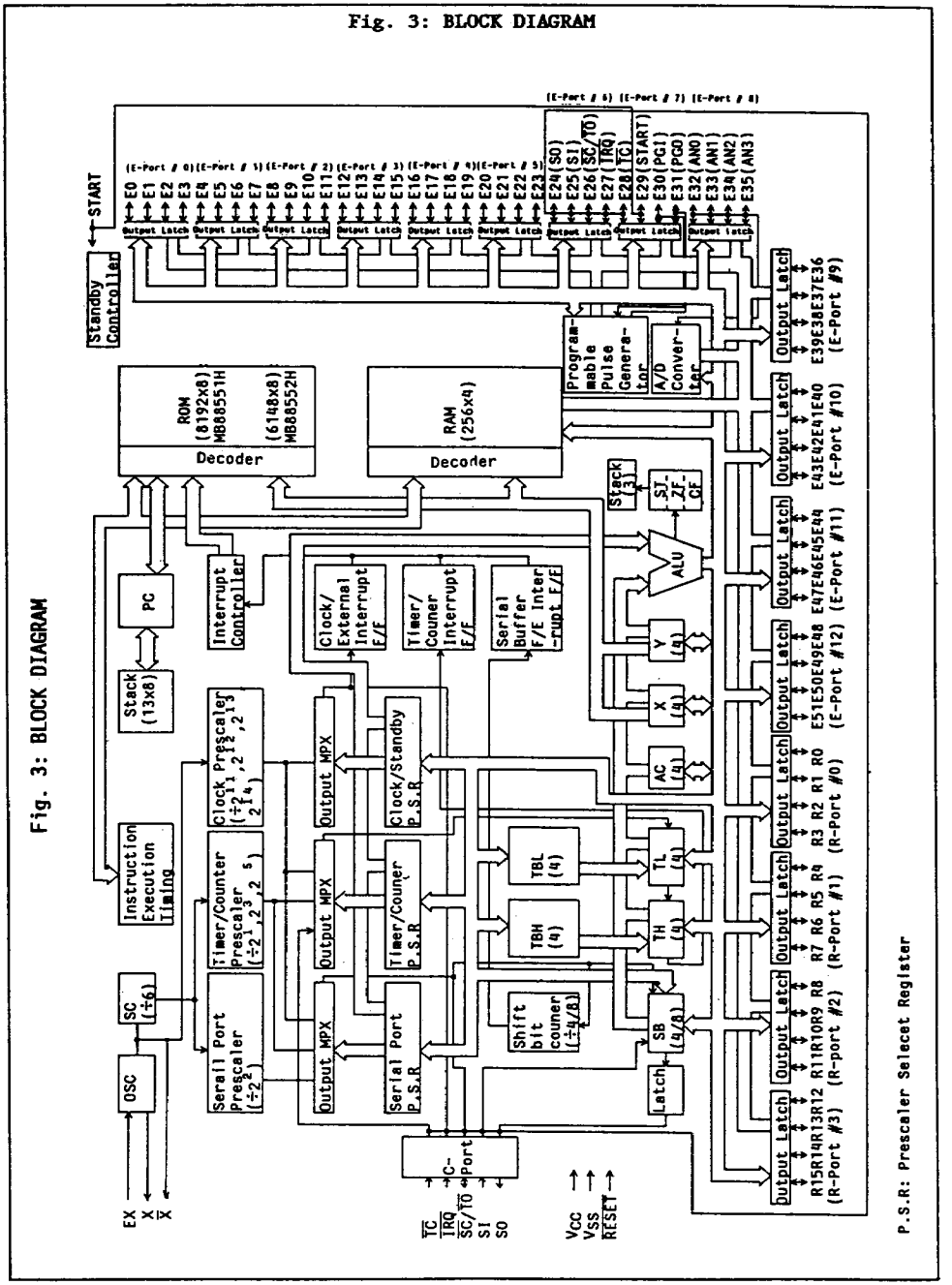
Fig. 3: BLOCK DIAGRAM



PIN DESCRIPTION

Fig. 1 and Table 1 show the pin assignment and pin description of the MB88550H Series.

Table 1: PIN DESCRIPTION

Symbol	Pin No.	Type	Name & Function
• Power Supply			
V_{CC}	34	–	+5V DC power supply pin.
V_{SS}	71	–	Ground pin.
• Clock			
EX	59	I	**Oscillator Input:** Input to the inverting amplifier that forms the on-chip oscillator. An external crystal/ ceramic resonator or RC-network is connected between the EX and X pins. Either of these two oscillation methods can be selected using mask option. When an external oscillator is used, the EX pin receives the external oscillator signal. This pin is a non-hysteresis input when the crystal/ ceramic oscillator is selected, and a hysteresis input when the RC-network oscillation is selected.
X	60	O	**Oscillator Output:** Output of the inverting amplifier that forms the on-chip oscillator, and input to the internal clock generator. An external crystal/ceramic resonator or RC-network is connected between the EX and X pins. Either of these two oscillation methods can be selected using mask option. When an external oscillator is used, the X pin should be left open.
$\overline{X}$	62	O	**Clock Output:** If selected oscillation output by mask-option, this pin output clock.
• Device Control			
$\overline{RESET}$	61	I/O	**Reset:** This pin function as an external reset input or power-on reset output. External reset input: A reset input to the internal reset circuit. A low level on the $\overline{RESET}$ pin forcedely stops the MCU's operation, and initializes its internal state. After the $\overline{RESET}$ pin returns high, the MCU re-starts execution of program from address #0. The $\overline{RESET}$ pulse must be low for at least two instruction cycles while the oscillator is stably running after power-on. This pin is a hysteresis input with an internal pull-up resistor. An external capacitor from the $\overline{RESET}$ pin to the VSS pin (and the internal pull-up resistor), whose time constant should be greator than the reset time required (12 clock periods) composes the external reset circuit.

Table 1: PIN DESCRIPTION (Continued)

Symbol	Pin No.	Type	Name & Function
• Device Control (Continued)			
$\overline{\text{RESET}}$	61	I/O	Power on reset output: A reset output from the on-chip reset control circuit. Normally this output is high during the active operation except the reset mode. The rising of the VCC voltage after power on outputs a low level on the $\overline{\text{RESET}}$ pin, and then automatically returns high after it has passed 2^{18} clock periodes since the oscillator starts by power on. This pin is a hysteresis input with an internal pull-up resistor.
START	68	I	**Start**: A standby release input to the internal standby control and status registers that control and monitor the on-chip standby control circuit. A high level on the START pin during the stanbdy mode sets te standby release flag (STF) in the stanbdy status register, resets the standby enable flag (STBE) in the standby control registor, and triggers the standby release sequence to return the MCU to the active mode. Before the START pulse is applied, the VCC voltage must return to the active operation range (4.5V to 5.5V) when the battery backup is used. Also, the START pin must be low before the standby mode is initiated. The START pin state (logical level) is reflected in the standby release input (START) flag (STIF) in the standby status register, regardless of during the standby mode or active mode, and besides even when the standby function is not implemented using mask option. Therefore, the START pin state can be sensed by reading the standby status register using IN instruction (with Y=8). This pin is a hysteresis input with an internal pull-down resistor. If selected the E-Port by mask option, this pin is E29 pin.
• C-Port			
$\overline{\text{IRQ}}$	66	I	**Interrupt Request**: A maskable external interrupt input to the on-chip interrupt control circuit. The falling edge of the $\overline{\text{IRQ}}$ pulse sets the external interrupt request flag (IRF) in the interrupt flag register regardless of enabling or disabling the external interrupt. If the external interrupt is enabled in advance by EN instruction, the interrupt sequence starts at once. Otherwise, the IRF flag is internally held as an interrupt source. Also, the $\overline{\text{IRQ}}$ pin state (logical level), which is reflected in the external interrupt input flag (IF) regardless of enabling or disabling the external interrupt, is testable using TSTI instruction. (When $\overline{\text{IRQ}}$ = L, IF = 1; otherwise IF = 0.) This pin is a hysteresis input with an internal pull-up resistor, and common to E27 pin.

Table 1: PIN DESCRIPTION (Continued)

Symbol	Pin No.	Type	Name & Function
• C-Port (Continued)			
$\overline{TC}$	10	I	**Timer/Counter:** An external count clock input to the on-chip 8-bit timer/counter. The falling edge of the $\overline{TC}$ pulse increments the timer/counter by one bit, when the external count clock (counter) mode is enabled by EN instruction programming the timer/counter prescaler select register using OUT instruction (with Y = B). Also, the $\overline{TC}$ pin state (logical level), which is reflected in the timer/counter input flag (TCF) in the timer/counter prescaler select register regardless of enabling or disabling the external count clock (counter) mode, is testable by reading the prescaler select register using IN instruciton (with Y = B). (When $\overline{TC}$ = L, TCF = 1; otherwise TCF = 0.) This pin is inactive as a count clok input when the external count clock mode is not selected or the timer/counter is disabled by DIS instruction or reset. This pin is a hysteresis input with an internal pull up resistor.
$\overline{SC}/\overline{TO}$	65	I/O	**Shift Clock/Timing Output:** One of the shift clock input ($\overline{SC}$), shift clock output ($\overline{SC}$), or synchronous timing output ($\overline{TO}$) is enabled using EN instruction.
		I	$\overline{SC}$: 1) Shift clock input to the on-chip serial port: When the external shift clock mode is enabled for the serial port, the falling edge of the external $\overline{SC}$ clock shifts the contents of the internal serial buffer one bit right (from MSB to LSB). This input is inactive when the external clock mode is not selcted or the serial port disabled by DIS instruction or reset. This pin is a hysteresis input. 2) Shift clock output from the on-chip serial port: When the internal shift clock mode is enabled, the internal shift clock shifts the contents of the serial buffer one bit right. In this mode, the internal timing signal selected is output onto the $\overline{SC}$ pin for synchronization.
		O	$\overline{TO}$: Synchronous timing output: When the timing output is enabled, the internal timing signal (which is generated by the on-chip state counter outputs, $\phi 1$ and $\phi 2$) is output onto the $\overline{TO}$ pin. By DIS instruction or reset, the $\overline{TO}$ pin is disabled and stops issuing the timing output. This $\overline{SC}/\overline{TO}$ pin is common to E26 pin.

Table 1: PIN DESCRIPTION (Continued)

Symbol	Pin No.	Type	Name & Function
• C-Port (Continued)			
SI	64	I	**Serial Data Input**: Data input to the on-chip serial port. The rising edge of the external ($\overline{SC}$) or internal shift clock shifts the data bit on the SI pin into the MSB of the serial buffer register when the serial port is enabled by EN instruction. Also, the SI pin state (logical level) is reflected in the serial data input flag (SIF) in the serial port prescaler select register regardless of enabling or disabling the serial port. Therefore, the SI pin can be sensed by reading the prescaler register using IN instrution (with Y = A). This pin is a non-hysteresis input with an internal pull-up resistor and common to E25 pin.
SO	63	O	**Serial Data Output**: Data output with latch of the on-chip serial port. The falling edge of the external ($\overline{SC}$) or internal shift clock shifts the LSB data of the serial buffer register to the serial port output latch, regardless of enabling or disabling to serial port. The content of the output latch directly appeares on the SO pin. This pin is a CMOS pull up output, and is set high by reset. This pin is common to E24 pin.
PGI	69	I	**Programmable Pulse Generation Start Input**: Programmable pulse generation started by TADT instruction, 9-bit pulse generation timer counted by rising or falling of PGI pin.
PGO	70	O	**Programmable Pulse Generator Output**: When 9-bit pulse generation timer is overflow, first PGO pin output is fall. And secondly overflow, PGO pin output is rise.
• I/O Ports			
R3 -R0, R7 -R4, R11-R8, R15-R12	76-74,72 80-77, 4- 1, 8- 5,	I/O	**R-Port**: This port functions as four 4-bit parallel input (non-latched)/output (latched) port, or 16 individual input (non-latched)/output (latched) lines, depending on instructions. Parallel I/O: Each port is named as R-Port #0 (R3-R0), R-Port #1 (R7-R4), R-Port #2 (R11-R8), and R-Port #3 (R15-R12), and indirectly addressed by the Y-register. A 4-bit data on an addressed port is input into the accumulator by IN instruction. (Before IN instruction, the addressed port must be setup to "1" (input mode).) And further the R-Port #3 is directly input into accumulator by INK instruction. A 4-bit data in the accumulator is output onto an addressed port of R-Port #0 to #3 by OUT instruction.

Table 1: PIN DESCRIPTION (Continued)

Symbol	Pin No.	Type	Name & Function
• I/O Ports (Continued)			
R3 -R0, R7 -R4, R11-R8, R15-R12	76-74,72 80-77, 4- 1, 8- 5,	I/O	Individual I/O: Each line of R15 to R0 is indirectly addressed by the Y-register, and addressed line is individually set/reset by SETR/RSTR instruction, and further each line of R-Port #0 (R3-R0) is directly set/reset by SETD/RSTD instruction. All lines are testable using TSTR instruction, and further each line of R-Port #2 (R11-R8) is directly testable by TSTD instruction. (Before TSTR and TSTD instructions, the addressed line must be setup to "1" (input mode).) For R-Port pins, one of standard pull-up, standard open-drain, or high-current open-drain output can be selected using mask option. And output port level during reset, either each of R-Port is the high level or and low can be selected by mask option, every 4 bit. This port are set high (standard pull-up) or high-Z (standard and high-current open-drain) by reset.
E3 -E0, E7 -E4, E11-E8, E15-E12, E19-E16, E23-E20, E27-E24, E31-E28, E35-E32, E39-E36, E43-E40, E47-E44, E51-E48	38-35, 42-39, 46-43, 50-47, 54-51, 58-55, 66-63, 70-67, 16-13, 20-17, 24-21, 28-25, 32-29	I/O	E-Ports: This functions as thirteen 4-bit parallel input (non-latched)/output (latched) port, or 52 individual output (latched) lines. Parallel I/O: Each port is named as E-Port #0 (E3-E0), E-Port #1 (E7-E4) ... E-Port #C (E51-E48), and indirectly addressed by Y-resister. A 4-bit data on an addressed port is input into the accumulator by INX (before INX instruction, the addressed port must be setup to "1" (input mode).)instruction. A 4-bit data in the accumulator is output onto an addressed port of E-Port #0 to #C by OUTX instruction and further in the E-Port #0 (E3-E0) and E-Port #1 (E7-E4) 4-bit data in the accumulator is directly output onto the E-Port #0, and E-Port #1 by OUTP, OUTO instruction. Individual output: Each line of E51 to E0 can be individually outputs by combined of ANDX, ORX, and OUTX instruction. All E-Port except of E-Port #8 (E35-E32), standard pull-up, standard open-drain, or high-current open-drain can be selected by the mask option, every 4-bit. And E35 to E32 is only can be select a high-current open-drain or standard open-drain. And output port level during reset. Either each of E-Port is the high level and low can be selected by mask option, every 4-bit. This port are set high (standard pull-up) or high-Z (standard and high-current open-drain) by reset.
OPEN	73,33	-	Open: This pin should not to be connect.

Table 1: PIN DESCRIPTION (Continued)

Symbol	Pin No.	Type	Name & Function
• A/D Converter			
AV_{CC}	12	-	A/D converter supply voltage.
AV_{SS}	10	-	A/D converter ground pin.
A_{VR-}	11	-	A/D converter reference voltage.
AN3-AN0	16-13	I	**5-bit Resolution A/D Converter Input:** There are four programmable approximation 5 bits resolution A/D conversion, the analog input port is selected with the analog input select register (Y=D). The A/D converter is activiate by writing 1 to bit 0 of the control register (Y=9). Upon completion of A/D conversion results go into the A/D data register (high-order) (Y=F); the last two bits go into the A/D data register (low-order) (Y=E). This analog input is common to E35 to E32. In standby mode, this function doesn't worked, and A/D converted data is not hold.

DIFFERENCES BETWEEN MB88550 SERIES AND MB88550H SERIES

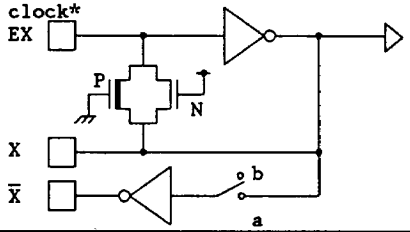
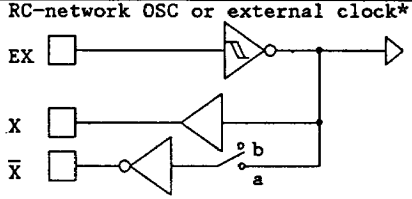
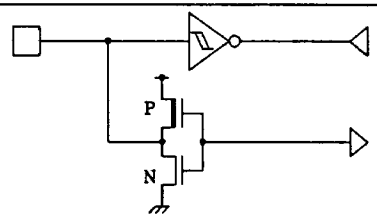
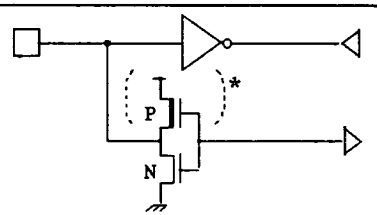
Table 2: DIFFERENCES BETWEEN MB88550 SERIES AND MB88550H SERIES

Item \ Device	MB88550 series	MB88550H series
Clock -Oscillation range -Min. instruction execution time	· 0.5 MHz to 3.0 MHz (Without prescaler) 1 MHz to 6 MHz (With prescaler) · 2.0 µs using 6.0 MHz with prescaler	· 2.0 MHz to 4.0 MHz (Without prescaler) 4MHz to 8MHz (With prescaler) · 1.5 µs using 8.0 MHz with prescaler
Members	· MB88551-PF · MB88552-PF	· MB88551H-PF · MB88552H-PF

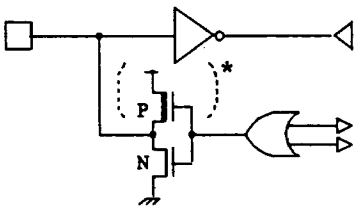
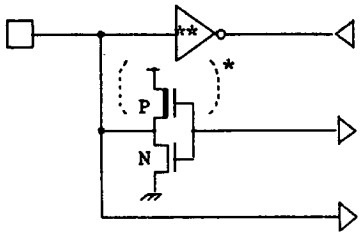
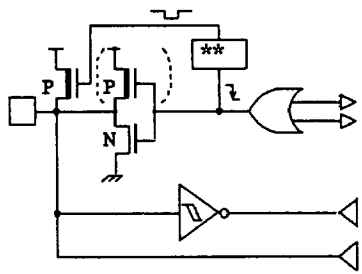
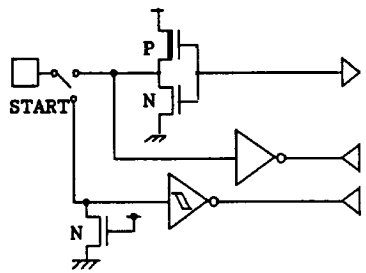
INPUT/OUTPUT CIRCUITS

All input-only pins are internally pulled up, and all output-only and input/output pins except E- and R-Ports have push-pull output buffer (standard pull-up). E- and R-Ports can have push-pull (standard pull-up) or open-drain (standard or high-current) buffer using mask option.

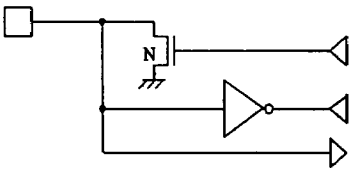
Table 3: INPUT/OUTPUT CIRCUIT

Pin	Circuit	Remarks
EX X $\overline{X}$	• Crystal/Ceramic OSC or external clock* 	1. Non-hysteresis inverter 2. Feedback resistor: Approx. 2 MΩ typ. (at V_{CC}=5V) * When only external clock drive is used, we recommend RC-network OSC. Oscillation output option a: Yes b: No
EX X $\overline{X}$	• RC-network OSC or external clock* 	1. Hysteresis inverter 2. Without feedback resistor * When only external clock drive is used, we recommend RC-network OSC. Oscillation output option a: Yes b: No
$\overline{RESET}$		• Hysteresis inverter • With output pull-up resistor (P-ch. Tr.): approx. 300kΩ
R-Port E23-E0 E51-E36		• Output port option 1: Standard pull-up: pull-up resistor: P-ch. Tr. approx. 10kΩ *2: Standard/high-current open-drain: Without P-ch. pull-up resistor

Input/Output Circuit (Continued)

Pin	Circuit	Remarks
E24/SO E31/PG0		• Output port option 1: Standard pull-up: pull-up resistor: P-ch. Tr. approx. 10kΩ *2: Standard/high-current open-drain: without P-ch. pull-up resistor
E25/$\overline{SI}$ E27/$\overline{IRQ}$ E28/$\overline{TC}$ E30/PGI		• Output port option 1: Standard pull-up: pull-up resistor: P-ch. Tr. approx. 10kΩ *2: Standard/high-current open-drain: without P-ch. pull-up resistor **$\overline{IRQ}$, $\overline{TC}$: Hysteresis inverter
E26($\overline{SC}$/$\overline{TO}$)		• Output port option 1: Standard pull-up: pull-up resistor: P-ch. Tr. approx. 10kΩ *2: Standard/high-current open-drain: without P-ch. pull-up resistor ** A circuit is added to temporarily turn on the transistor connected to the power supply and to immediatly, raise the pin to the high level by the timing H output to the pin.
E29/START		E29: • Output port option 1: Standard pull-up: pull-up resistor: P-ch. Tr. approx. 10kΩ 2: Standard/high-current open-drain: without P-ch. pull-up resistor START: With N-ch. pull-down resistor approx. 300kΩ

Input/Output Circuit (Continued)

Pin	Circuit	Remarks
E32/AN0 to E35/AN3		• Open-drain output

USER MASK OPTIONS

The MB88550H series has the following mask options, which must be specified by the customer on the attached data release form when devices are ordered.

Table 4: MB88550H SERIES USER MASK OPTIONS

Optional Feature	Symbol	Option	Option No.	Note
Clock prescaler	CLK	No	0	f_C=2.0 MHz to 4.0 MHz
		Yes	1	f_C=4.0 MHz to 8.0 MHz
Oscillation circuit	OSC	Crystal/Ceramic OSC or external clock	0	When only external clock drive is use, we recommend RC-network oscillator.
		RC-network OSC	1	Recommend a without clock prescaler.
Port scramble		No	0	
		Yes	1	Port scramble is appointed every 4-bit.
Output port (R-, E-Port) type	PORT	High-current open-drain	1/K	
		Standard open-drain	2/L	
		Standard pull-up	3/M	Except E35 to E32
Output port level during reset	RST	High level	0	
		Low level	1	
Oscillation output	CLO	No	0	
		Yes	1	
Standby function	STRT	No	0	Pin 68 used as E29
		Yes	1	Pin 68 used as START
Output port state during standby	STATE	Hold	0	
		High-Z	1	
Standby off reset function	SOR	No	0	Output port level of E0-E24 during reset is fixed at low. And other port is high.
		Yes	1	
Watch dog timer	WDR	No	0	
		Yes	1	

Table 4: USER MASK OPTIONS (Continued)

When port scramble selected, output port circuit option table.

PIN NO.	PIN NAME	OUTPUT PORT OPTION	OUTPUT PORT DURING RESET
1 to 4	R8 to R11	☐ HIGH CURRENT OPEN-DRAIN ☐ STANDARD OPEN-DRAIN ☐ STANDARD PULL-UP	☐ HIGH LEVEL ☐ LOW LEVEL
5 to 8	R12 to R15	☐ HIGH CURRENT OPEN-DRAIN ☐ STANDARD OPEN-DRAIN ☐ STANDARD PULL-UP	
13 to 16	E32/AN0 to E35/AN3	☐ HIGH CURRENT OPEN-DRAIN ☐ STANDARD OPEN-DRAIN	☐ HIGH LEVEL ☐ LOW LEVEL
17 to 20	E36 to E39	☐ HIGH CURRENT OPEN-DRAIN ☐ STANDARD OPEN-DRAIN ☐ STANDARD PULL-UP	☐ HIGH LEVEL ☐ LOW LEVEL
21 to 24	E40 to E43	☐ HIGH CURRENT OPEN-DRAIN ☐ STANDARD OPEN-DRAIN ☐ STANDARD PULL-UP	☐ HIGH LEVEL ☐ LOW LEVEL
25 to 28	E44 to E47	☐ HIGH CURRENT OPEN-DRAIN ☐ STANDARD OPEN-DRAIN ☐ STANDARD PULL-UP	☐ HIGH LEVEL ☐ LOW LEVEL
29 to 32	E48 to E51	☐ HIGH CURRENT OPEN-DRAIN ☐ STANDARD OPEN-DRAIN ☐ STANDARD PULL-UP	☐ HIGH LEVEL ☐ LOW LEVEL
35 to 38	E0 to E3	☐ HIGH CURRENT OPEN-DRAIN ☐ STANDARD OPEN-DRAIN ☐ STANDARD PULL-UP	☐ HIGH LEVEL ☐ LOW LEVEL
39 to 42	E4 to E7	☐ HIGH CURRENT OPEN-DRAIN ☐ STANDARD OPEN-DRAIN ☐ STANDARD PULL-UP	☐ HIGH LEVEL ☐ LOW LEVEL
43 to 46	E8 to E11	☐ HIGH CURRENT OPEN-DRAIN ☐ STANDARD OPEN-DRAIN ☐ STANDARD PULL-UP	☐ HIGH LEVEL ☐ LOW LEVEL
47 to 50	E12 to E15	☐ HIGH CURRENT OPEN-DRAIN ☐ STANDARD OPEN-DRAIN ☐ STANDARD PULL-UP	☐ HIGH LEVEL ☐ LOW LEVEL
51 to 54	E16 to E19	☐ HIGH CURRENT OPEN-DRAIN ☐ STANDARD OPEN-DRAIN ☐ STANDARD PULL-UP	☐ HIGH LEVEL ☐ LOW LEVEL
55 to 58	E20 to E23	☐ HIGH CURRENT OPEN-DRAIN ☐ STANDARD OPEN-DRAIN ☐ STANDARD PULL-UP	☐ HIGH LEVEL ☐ LOW LEVEL
63 to 66	E24/SO to E27/$\overline{IRQ}$	☐ HIGH CURRENT OPEN-DRAIN ☐ STANDARD OPEN-DRAIN *5 ☐ STANDARD PULL-UP	☐ HIGH LEVEL ☐ LOW LEVEL
67 to 70	E28/$\overline{TC}$ to E31/PG0	☐ HIGH CURRENT OPEN-DRAIN ☐ STANDARD OPEN-DRAIN *6 ☐ STANDARD PULL-UP	☐ HIGH LEVEL ☐ LOW LEVEL *6
72, 74 75, 76	R0 to R3	☐ HIGH CURRENT OPEN-DRAIN ☐ STANDARD OPEN-DRAIN ☐ STANDARD PULL-UP	☐ HIGH LEVEL ☐ LOW LEVEL
77 to 80	R4 to R7	☐ HIGH CURRENT OPEN-DRAIN ☐ STANDARD OPEN-DRAIN ☐ STANDARD PULL-UP	☐ HIGH LEVEL ☐ LOW LEVEL

*5 Output port of E26($\overline{SC}$/$\overline{TO}$) is applied to only standard pull-up.
*6 When the standby function is selected, E29/START is input port.

NOTES ON OPERATION

- **Latch-up Prevention**

  Latch-up may occur in CMOS devices following treatments:

  (1) The voltage higher than V_{CC} or lower than V_{SS} is applied to input or output pin.
  (2) The voltage exceeding the absolute maximum ratings is applied between V_{CC} and V_{SS} pins.
  (3) MCU power supply (V_{CC}) power-on after analog power supply (AV_{CC}) power-on.

  If latch-up occurs, the supply current increases greatly, and the device may be thermally destroyed. Therefore, applied voltages should not exceed the maximum ratings.

- **Treatment of Unused Pins**

  Unused input pins should be externaly pulled up or down with resistors because such unused input pins may cause some malfunction if they are left open. (However, the X pin should be open when an external clock oscillator is used.)

- **External Capacitors for Crystal Oscillation**

  Fig. 6 gives an aim of an area where the on-chip oscillator has stable oscillator characteristics and short oscillation stabilization time when an average crystal resonator is used.

  The external capacitor should be adjusted to individual crystal resonators when precise oscillation frequency is required. It is recommended to use crystal with a frequency higher than required oscillation frequency, together with the on-chip divided-by-two prescaler, because crystal resonators with lower oscillation frequency generally tends to have longer stabilization time and wider characteristics variation.

- **Supply Voltage**

  Malfunction may occur even within the recommended operating supply voltage if the supply voltage changes rapidly. Therefore, the supply voltage should be regulated as well as possible. The following conditions are recommended for the power supply:

  (1) V_{CC} ripple (peak-to-peak value) at commercial frequency (50Hz to 60Hz): Less than 10% of typical V_{CC} value.
  (2) V_{CC} transient change rate (such as at switching of power supply): Less than 0.1V/ms.

INSTRUCTION SET DESCRIPTION

The MB88550H series instruction set includes 82 instructions, 78% of which are single-byte and single-cycle, 18% two-byte two-cycles, 1% two bytes three-cycles, and 2% three-bytes and three-cycles. The MB88550H series instruction set is same as the MB88550 series instruction set, and is divided into ten functional groups:

- Register-to-register transfer
- Register-to-memory transfer
- Constant transfer
- Arithmetic and logical operations
- Bit manipulation
- Control
- Input/Output
- Branch
- Flag manipulation
- Other

Tables 5 and 6 summarize the MB88550H series instruction set.

Table 5: INSTRUCTION SET SUMMARY

	Mnemonic +operand	Code (Hex.)	Flag/Status ZF	CF	ST	Byte/ Cycle	Operation
Register-to-Register Transfer	TATC	05	·	·	·	1/1	TH←(X), TL←(AC)
	TADT	06	·	·	·	1/1	DT_9←(CF), DT_{8-4}←(X), DT_{3-0}←(AC)
	TAS	07	·	·	·	1/1	SB←(AC)
	TAY	04	·	·	·	1/1	Y←(AC)
	TSA	17	·	·	·	1/1	4-bit mode: AC←(SB_L), 8-bit mode: AC←(SB_L), X←(SB_H)
	TTCA	15	·	·	·	1/1	X←(TH), AC←(TL)
	TAPW	16	·	·	·	1/1	PW_9←(CF), PW_{8-4}←(X), PW_{3-0}←(AC)
	TYA	14	↕	·	·	1/1	AC←(Y)
	XX	1B	↕*1	·	·	1/1	(AC)⇌(X)
Register-to-Memory Transfer	L	0D	↕	·	·	1/1	AC←{M(X,Y)}
	LS	2B	↕	·	·	1/1	SB←{M(X,Y)}
	ST	1D	·	·	·	1/1	M(X,Y)←(AC)
	STDC	1A	·	·	↓C	1/1	M(X,Y)←(AC), Y←(Y)-1
	STIC	0A	·	·	↓C	1/1	M(X,Y)←(AC), Y←(Y)+1
	STS	2A	↕	·	·	1/1	M(X,Y)←(SB)
	X	0B	↕*1	·	·	1/1	(AC)⇌{M(X,Y)}
	XD D	50-53*	↕*1	·	·	1/1	(AC)⇌{M(0,D)}; D=0 to 3 (X=0, Y=D)
	XYD D	54-57*	↕*2	·	·	1/1	(Y) ⇌{M(0,D)}; D=4 to 7 (X=0, Y=D)
Constant Transfer	CLA	90	↓	·	·	1/1	AC←0 (Included in LI instruction)
	LI imm	90-9F*	↕	·	·	1/1	AC←imm; imm=0 to 15
	LXI imm	58-5F*	↕	·	·	1/1	X3←0, X2 to X0←imm; imm=0 to 7
	LXID	3D90-3D9F*	↕	·	·	2/2	X←imm; imm=0 to 15
	LRXA imm	3D20-3D3F*	·	·	·	2/3	X ←{ROM(imm | X | Y)}d, d=7-4 AC←{ROM(imm | X | Y)}d, d=3-0 imm=0 to 31
	LYI imm	80-8F*	↕	·	·	1/1	Y ←imm; imm=0 to 15
Arithmetic & Logical Operations	ADC	0E	↕	↕	↓C	1/1	AC←(AC)+{M(X,Y)}+(CF)
	AI imm	3D80-3D8F	↕	↕	↓C	1/1	AC←(AC)+imm; imm=0 to 15
	AND	0F	↕	·	↓Z	1/1	AC←(AC)∩{M(X,Y)}
	C	2E	↕	↕	↓Z	1/1	{M(X,Y)}-(AC)
	CI imm	B0-BF*	↕	↕	↓Z	1/1	imm-(AC); imm=0 to 15
	CYI imm	A0-AF*	·		↓Z	1/1	imm-(Y) ; imm=0 to 15

Table 5: INSTRUCTION SET SUMMARY (Continued)

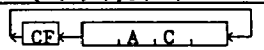
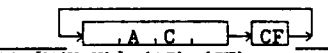
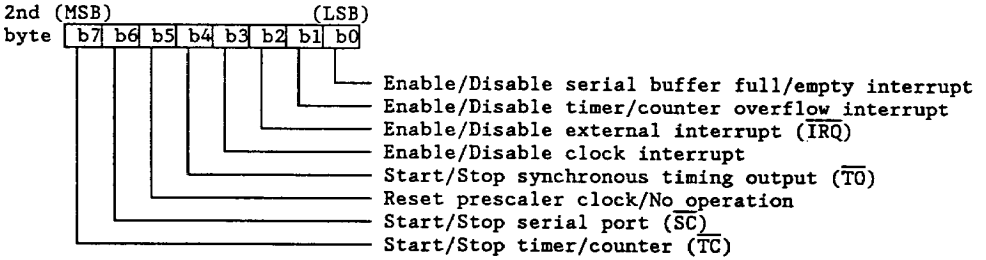
	Mnemonic +Operand	Code (Hex.)	Flag/Status ZF	CF	ST	Byte/ Cycle	Operation
Arithmetic & Logical Operation	DAA	10	·	↕	↓C	1/1	AC←(AC)+6 if (AC)>9 or (CF)=1
	DAS	11	·	↕	↓C	1/1	AC←(AC)+10 if (AC)>9 or (CF)=1
	DCA	3D8F	↕	↕	↓C	1/1	AC←(AC)+15 (Included in AI instruc-
	DCM	19	↕	·	↓C	1/1	M(X,Y)←{M(X,Y)}-1 tion)
	DCY	18	·	·	↓C	1/1	Y←(Y)-1
	EOR	2F	↕	·	↓Z	1/1	AC←{M(X,Y)}⊕(AC)
	ICA	3D81	↕	↕	↓C	1/1	AC←(AC)+1 (Included in AI instruc-
	ICM	09	↕	·	↓C	1/1	M(X,Y)←{M(X,Y)}+1 tion)
	ICX	3DAC	·	·	↓C	2/2	X← (X)+1
	ICY	08	↕	·	↓C	1/1	Y←(Y)+1
	NEG	2D	·	·	↓Z	1/1	AC←(AC)+1
	OR	1F	↕	·	↓Z	1/1	AC←{M(X,Y)}∪(AC)
	ROL	0C	↕	↕	↓C	1/1	
	ROR	1C	↕	↕	↓C	1/1	
	SBC	1E	↕	↕	↓C	1/1	AC←{M(X,Y)}-(AC)-(CF)
Bit Manipulation	RBIT bp	34-37*	·	·	·	1/1	{M(X,Y)}bp←0; bp=0 to 3
	SBIT bp	30-33*	·	·	·	1/1	{M(X,Y)}bp←1; bp=0 to 3
	RBA bp	3DA4 3DA7 *	·	·	·	2/2	(AC)bp←0 ; bp=0 to 3
	SBA bp	3DA0 3DA3 *	·	·	·	2/2	(AC)bp←1 ; bp=0 to 3
	TBA bp	4C-4F*	·	·	↓Z	1/1	(AC)bp-1 ; bp=0 to 3
	TBIT bp	38-3B*	·	·	↓Z	1/1	{M(X,Y)}bp-1; bp=0 to 3
Control	EN imm	3E00-3EFF*	·	·	·	2/2	Enable the internal resources by the operand byte (2nd byte); *3
	DIS imm	3F00-3FFF*	·	·	·	2/2	Disable the internal resources by the operand byte (2nd byte); *3
	RST	3DAD	·	·	·	2/2	System initialization
Input/ Output	IN	13	↕	·	·	1/1	AC←(R)Y ; Y=0 to 3 (Port #) AC←(REG)Y; Y=8 to 12, 14, 15
	INK	12	↕	·	·	1/1	AC←(K)
	INX	3DAA	·	·	·	2/2	AC←E(Y) ; Y=0 to 12
	OUT	03	·	·	·	1/1	(R)Y←(AC); Y=0 to 3 (Port #) (REG)Y←(R);Y=8 to 11, 13
	OUTO	01	·	·	·	1/1	E3-E0←(AC)
	OUTP	02	·	·	·	1/1	E8-E4←(AC)
	OUTX	3DAB	·	·	·	2/2	(E)Y←AC; Y=0 to 12
	ANDX	3DA8	·	·	·	2/2	E←(AC)∩{(E)Y}; Y=0 to 12
	ORX	3DA9	·	·	·	2/2	E←(AC)∪{(E)Y}; Y=0 to 12
	RSTD d	44-47*	·	·	·	1/1	(R)d←0; d=0 to 3 (Bit # of port #0)
	RSTR	22	·	·	·	1/1	(R)Y←0; Y=0 to 15 (Bit #)
	SETD d	40-43*	·	·	·	1/1	(R)d←1; d=0 to 3 (Bit # of port #0)
	SETR	20	·	·	·	1/1	(R)Y←1; Y=0 to 15 (Bit #)
	TSTD d	48-4B*	·	·	↓Z	1/1	(R)d-1; d=8 to 11 (Bit #)
	TSTR	24	·	·	↓Z	1/1	(R)Y-1; Y=0 to 15 (Bit #)
Branch	CALL addr	6000-6FFF*	·	·	·	2/2	If ST=1, Subroutine call for addr; addr=0 to 4095. ST=0, Not Subroutine Call.
	CALX addr	3D4000-3D5FFF*	·	·	·	3/3	If ST=1, Subroutine call for addr; addr=0 to 8191. *4 ST=0, Not subroutine call.

Table 5: INSTRUCTION SET SUMMARY (Continued)

	Mnemonic +Operand	Code (Hex.)	Flag/Status ZF	CF	ST	Byte/ Cycle	Operation
Branch	JMP addr	C0-FF*	·	·	·	1/1	If ST=1, Branch to addr; addr=0 to 63 ST=0, No Branch.
	JPXY addr	3D00-3D1F*	·	·	·	2/2	Branch always to addr on page #n;
	JPL addr	7000-7FFF*	·	·	·	2/2	If ST=1, Branch to addr; addr=0 to 4095. ST=0, No branch.
	JPLX addr	3DC000-3DDFFF*	·	·	·	3/3	If ST=1, Branch to addr; addr=0 to 8191. *4 ST=0, No Branch.
	RTI	3C	·	·	·	1/1	Return from interrupt routine
	RTS	2C	·	·	·	1/1	Return from subroutine
Flag Manipulation	RSTC	23	·	↓	·	1/1	CF←0
	SETC	21	·	↑	·	1/1	CF←1
	TSTC	28	·	·	↓CF	1/1	(CF)-1
	TSTI	25	·	·	↓IF	1/1	(IF)-1, (If $\overline{IRQ}$=L, IF=1)
	TSTS	27	·	·	↓SF	1/1	(SF)-1, SF←0
	TSTV	26	·	·	↓VF	1/1	(VF)-1, VF←0
	TSTZ	29	·	·	↓ZF	1/1	(ZF)-1
Other	NOP	00	·	·	·	1/1	No operation

Notes:

*1: ZF is set or reset depending on contents of AC after instruction execution.
*2: ZF is set or reset depending on contents of Y after instruction execution.
*3: Each bit of the operand (the second byte) functions as follows:



*4: addr=6144 to 8191 for MB88551H only

Symbols and Abreviations

Symbols	Meaning
←	Is transferred to
⇄	Is exchanged with
+	Arithmetic plus
-	Arithmetic minus
⊕	Logical exclusive or
∩	Logical OR
∪	Logical AND
$\overline{\quad}$ (Overline)	Negation
( )	Contents of parenthesis
↑	Set to "1" always
↓	Set to "0" always
↕	Affected (set or reset) by operation results
↓C	Set to "0" due to carry (not carry flag)
↓CF	Set to "0" due to carry flag
↓IF	Set to "0" due to interrupt flag
↓SF	Set to "0" due to serial buffer full/empty flag
↓VF	Set to "0" due to timer/counter overflow flag
↓Z	Set to "0" due to zero (not zero flag)
↓ZF	Set to "0" due to zero flag
·	Not affected

Abbreviation	Meaning
AC	Accumulator
addr	Jump address
bp	Bit pointer (that is part of the instruction code)
C	Carry
CF	Carry flag
d	Direct line number (that is part of the instruction code)
DT	Program delay timer for programmable pulse generator
E	E-Port (#0: E3-E0, #1: E7-E4,... #B: E47-E43, #C: E51-E48)
(E)Y; Y=n	E-Port #n specified by Y-register (E=0 to C)
IF	Interrupt flag
imm	Immediate data
$\overline{\text{IRQ}}$	Interrupt request
LSB	Least significant bit
M(X,Y)	Data memory (RAM) location indirectly addressed by data pointer (X- and Y-registers)
M(0,D)	Data memory (RAM) location directly addressed by "D" bits in the instruction code, in page #0 (X=0)
MSB	Most significant bit
PW	Pulse width latch for programmable pulse generator
R	R-Port (#0: R3-R0, #1: R7-R4, #2: R11-R8, #3: R15-R12)
(R)Y; Y=n	① R-Port #n specified by Y-register (Y=0 to 3) ② R-Port bit n specified by Y-register (Y=0 to 15)
(R)d; d=n	R-Port bit n specified by "d" bits in the instruction code
SBH	Serial buffer high register
SBL	Serial buffer low register
SF	Serial buffer full/empty flag
ST	Status flag
TH	Timer/counter high byte
TL	Timer/counter low byte
VF	Timer/counter overflow flag
X	X-register (that indicates page # in data memory RAM)
Xn	The n-th bit X-register
Y	Y-register
Z	Zero
ZF	Zero flag

Table 6: INSTRUCTION CODES SUMMARY

L / H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	OUTO	OUTP	OUT	TAY	TATC	TADT	TAS	ICY	ICM	STIC	X	ROL	L	ADC	AND
1	DAA	DAS	INK	IN	TYA	TTCA	TAPW	TSA	DCY	DCM	STDC	XX	ROR	ST	SBC	OR
2	SETR	SETC	RSTR	RSTC	TSTR	TSTI	TSTV	TSTS	TSTC	TSTZ	STS	LS	RTS	NEG	C	EOR
3	SBIT bp				RBIT bp				TBIT bp				RTI	* EXT	EN imm	DIS imm
4	SETD d				RSTD d				TSTD d				TBA bp			
5	XD D				XYD D				LXI imm							
6	CALL addr															
7	JPL addr															
8	LYI imm															
9	(CLA)	LI imm														
A	CYI imm															
B	CI imm															
C	JMP addr															
D																
E																
F																

NOTE: : 1-byte/1-cycle instruction : 2-bytes/2-cycles instruction

* See the next page

Table 6: INSTRUCTION CODES SUMMARY (Continued)
Extended instruction

3DL / 3DH	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	JPXY addr															
1																
2	LRXA imm															
3																
4	CALX addr															
5																
6	NOT USE															
7																
8	(ICA)	AI imm														(DCA)
9	LXID imm															
A	SBA				RBA				ANDX	ORX	INX	OUTX	ICX	RST	NOT USE	
B	NOT USE															
C	JPLX															
D																
E	NOT USE															
F																

Note: : 3 bytes/3 cycles instruction

PRODUCT LINE-UP AND DEVELOPMENT TOOLS

The MB88550H series consists of the MB88551H and MB88552H. The MB88558H are available as piggyback EPROM evaluation devices for MB88550H series. Refer to Table 7.

Table 7: MB88550H SERIES PRODUCT LINE-UP & DEVELOPMENT TOOLS

	MB88551H-PF	MB88552H-PF	MB88558H-CF-10X
ROM Size	8K x 8 bits (On-chip mask ROM)	6K x 8 bits (On-chip mask ROM)	8K x 8 bits (Piggyback EPROM)
RAM Size (Directly addressed locations)	256 x 4 bits (0-7)	256 x 4 bits (0-7)	256 x 4 bits (0-7)
I/O Port:	Total 68 lines	Total 68 lines	Total 68 lines
-Input-only Port	0	0	0
-Output-only Port	0	0	0
-I/O Port	68	68	68
-Control Port	5 (Including serial I/O)	5 (Including serial I/O)	5 (Including serial I/O)
Output Port Type	· Standard pull-up · Standard open-prain · High-current open-drain (Mask option)	· Standard pull-up · Standard open-drain · High-current open-drain (Mask option)	· Standard pull-up(101/201) · High-current open-drain (102/103/202) (Mask option)
Stack Depth (Nesting Level)	8 levels	8 levels	8 levels
Timer/Counter:	Yes (Auto loading)	Yes (Auto loading)	Yes (Auto loading)
-Buffer Size	8 bits	8 bits	8 bits
-Clock Source	Internal/External	Internal/External	Internal/External
Serial I/O:	Yes	Yes	Yes
-Buffer Size	4/8 bits	4/8 bits	4/8 bits
-Clock Source	Internal/External	Internal/External	Internal/External
-Output Latch	Yes	Yes	Yes
Clock Generator:	Yes	Yes	Yes
-Oscillator Type	· Crystal/External · RC-network/ External (Mask option)	· Crystal/External · RC-network/ External (Mask option)	· Crystal/External (Fixed)
-Clock Frequency (With prescaler)	2 MHz-4 MHz (4 MHz-8 MHz)	2 MHz-4 MHz (4 MHz-8 MHz)	- (4 MHz-8 MHz)
Clock Prescaler (Divid-by-two)	Yes/No (Mask option)	Yes/No (Mask option)	Yes (Fixed)
Interrupt Function	Yes	Yes	Yes
-Nesting Level	Single level	Single level	Single level
-Interrupt Sources	4 Sources	4 Sources	4 Sources
Programmable Pulse Generator	Yes (9 bit)	Yes (9 bit)	Yes (9 bit)
A/D Converter	Yes	Yes	Yes
Method:	· Programmable successive approximation	· Programmable successive approximation	· Programmable successive approximation
-Resolution	· 5 bit	· 5 bit	· 5 bit
-Channel	· 4 channel	· 4 channel	· 4 channel

PRODUCT LINE-UP AND DEVELOPMENT TOOLS

Table 7: MB88550H SERIES PRODUCT LINE-UP & DEVELOPMENT TOOLS (Continued)

	MB88551H-PF	MB88552H-PF	MB88558H-CF-XXX
Standby Function: -Initiation Method -Oscillator State During Standby -Output State During Standby -Standby Off Reset Function	· Yes/No (Mask option) · Software · Idle · Stop(Software selectable) · Hold · High-Z (Mask option) · Yes/No (Mask option)	· Yes/No (Mask option) · Software · Idle · Stop(Software selectable) · Hold · High-Z (Mask option) · Yes/No (Mask option)	· Yes(101/102/103) · No(201/202) · Software · Idle · Stop(Software selectable) · Hold (102/103) · High-Z (101) (Mask option) · No
Output Port Level During Reset	· High/Low (Mask option)	· High/Low (Mask option)	· High(101/102/201/202) · R0-R7:L, Other:H (103)
Watch Dog Timer Function	· No · Yes (Mask option)	· No · Yes (Mask option)	· No (Fixed)
Number of Instructions	82	82	82
Instruction Length/Cycle	1/1, 2/2, 2/3, or 3/3	1/1, 2/2, 2/3, or 3/3	1/1,2/2, 2/3, or 3/3
Min. Instruction Execution Time	1.5 µs at 8 MHz (With prescaler)	1.5 µs at 8 MHz (With prescaler)	1.5 µs at 8 MHz (With prescaler)
Power Supply: VCC: -Active -Standby Analog Supply(AVCC)	Single +5V · 4.5V to 5.5V · 3.5V to 6.0V · 4.5V to 5.5V	Single +5V · 4.5V to 5.5V · 3.5V to 6.0V · 4.5V to 5.5V	Single +5V · 4.5V to 5.5V · 3.5V to 6.0V · 4.5V to 5.5V
Operating Temperature range:	-30°C to +70°C	-30°C to +70°C	-30°C to +70°C
Process	CMOS	CMOS	CMOS
Package	80-pin plastic flat package	80-pin plastic flat package	80-pin ceramic module
Development Tools: -Hardware -Software	MB2115-01 : CRT unit (Common) MB2115-02 : Monitor board with keyboard (Common) MB2115-04 : EPROM writer (Common) MB2115-36A : DUE board SM05215-A010: Intellec series III MDS cross-assembler SM07415-A012: CP/M-86 cross-assembler SMXXXXX-XXXX: PC-DOS cross-assembler SM07415-G022: CP/M-86 host emulator SMXXXXX-XXXX: PC-DOS host emulator		

ELECTRICAL CHARACTERISTICS

- **ABSOLUTE MAXIMUM RATINGS†**

Parameter	Symbol	Rating			Unit	Remarks
		Min.	Typ.	Max.		
Supply Voltage	V_{CC}	V_{SS}-0.3		V_{SS}+7.0	V	
	V_{SS}		0		V	
Analog Supply Voltage	AV_{CC} AV_{R-}	V_{SS}-0.3		V_{SS}+7.0	V	Should not exceed V_{CC}.
Input Voltage	V_{IN}	V_{SS}-0.3		V_{SS}+7.0	V	Should not exceed V_{CC}+0.3V
Output Voltage	V_{OUT}	V_{SS}-0.3		V_{SS}+7.0	V	Should not exceed V_{CC}+0.3V
Output Low Current	I_{OL}			20	mA	
Total Output Low Current	ΣI_{OL}			80	mA	
Power Dissipation	P_D			600	mW	
Operating Ambient Temperature	T_A	-30		+70	°C	
Storage Temperature	T_{STG}	-55		+150	°C	

† Permanent device damage may occur if the above ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

- **RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	Value			Unit	Remarks
		Min.	Typ.	Max.		
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	Active operation range
		3.5		6.0	V	Standby operation range
	V_{SS}		0		V	
Analog Supply Voltage	AV_{CC}	4.5		5.5	V	
	AV_{R-}	0		AV_{CC}	V	
Input High Voltage	V_{IH}	0.7·V_{CC}		V_{CC}+0.3	V	E-, R-Ports SI, PGI, EX(crystal/ceramic)
	V_{IHS}	0.8·V_{CC}		V_{CC}+0.3	V	START, EX(RC-network), IRQ, TC, SC/TO, RESET,
Input Low Voltage	V_{IL}	V_{SS}-0.3		0.3·V_{CC}	V	E-, R-Ports SI, PGI, EX(crystal/ceramic)
	V_{ILS}	V_{SS}-0.3		0.2·V_{CC}	V	START, EX(RC-netwarok), IRQ, TC, SC/TO, RESET
Operating Ambient Temperature	T_A	-30		+70	°C	

• **DC CHARACTERISTICS** (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin/Port	Conditions	Value			Unit
				Min.	Typ.	Max.	
Output High Voltage	V_{OH}	E-, R-Ports (Standard pull-up), $\overline{X}$ (Selected by mask option)	V_{CC}=4.5V I_{OH}=-200μA	2.4			V
			V_{CC}=4.5V I_{OH}=-10μA	4.0			V
Output Low Voltage	V_{OL}	E-, R-Ports (All output option), $\overline{RESET}$, $\overline{X}$ (Selected by mask option)	V_{CC}=4.5V I_{OL}=1.8mA			0.4	V
			V_{CC}=4.5V I_{OL}=3.6mA			0.6	V
		E-,R-Ports(High-current open-drain)	V_{CC}=4.5V I_{OL}=10mA			2.0	V
Input Leakage Current	I_{IH}	EX	V_{CC}=5.5V V_{IH}=5.5V			60	μA
	I_{IL}	E-, R-Ports (Standard pull-up)	V_{CC}=5.5V V_{IL}=0.4V			-1.8	mA
		$\overline{EX}$, $\overline{RESET}$	V_{CC}=5.5V V_{IL}=0.4V			-60	μA
Open-drain Output Leakage Current	I_{LEAK}	E-,R-Ports(High-current/standard open-drain)	V_{CC}=5.5V V_{OH}=5.5V (N-ch. Tr off)		0.1	10	μA
Total I/O Leakage Current (High-Z)	ΣI_{IZ}	E-, R-Ports (High-Z during standby mode)	V_{CC}=6.0V(Standby) V_{IN}=0V to 6.0V			±25	μA
Supply Current	I_{CC}	V_{CC}	V_{CC}=5.0V(Typ.) fc=2MHz(Operation) All outputs open		5		mA
	I_{CCH}	V_{CC} (Standby mode)	V_{CC}=6.0V(Max.) fc=0Hz(Standby) All outputs open			15	μA
Input Capacitance	C_{IN}	All pins except V_{CC}, V_{SS}	fc=1MHz		10	20	pF

- **AC CHARACTERISTICS**

CLOCK TIMING (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin/ Port	Conditions	Value Min.	Value Max.	Unit	Remarks
Clock Frequency	f_C	EX, X	Crystal/ceramic or RC-network OSC, external clock drive Figs. 4 and 5	2	4	MHz	Without prescaler
				4	8		With prescaler
Clock Cycle Time	t_{cyc}	EX, X	Figs. 4 and 5	0.25	0.5	µs	
Input Clock Pulse Width	P_{WCH}, P_{WCL}	EX	External clock drive (with X open) Figs. 4 and 5	100		ns	Without prescaler
				50			With prescaler
Input Clock Rise/Fall Time	t_{cr}, t_{cf}	EX	External clock drive (with X open) Figs. 4 and 5	5	200	ns	

Fig. 4: CLOCK TIMING

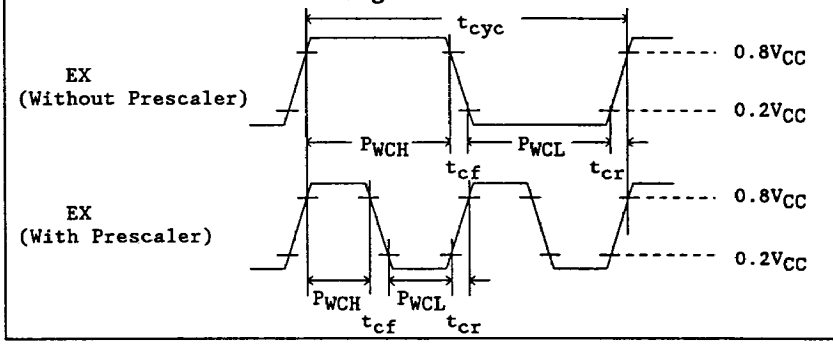
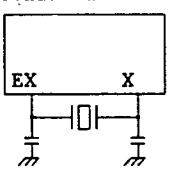
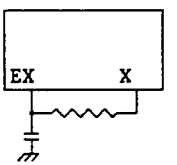


Fig. 5: CLOCK CIRCUIT CONFIGURATIONS

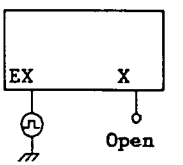
(1) Crystal/Ceramic Oscillation



(2) RC-Network * Oscillation

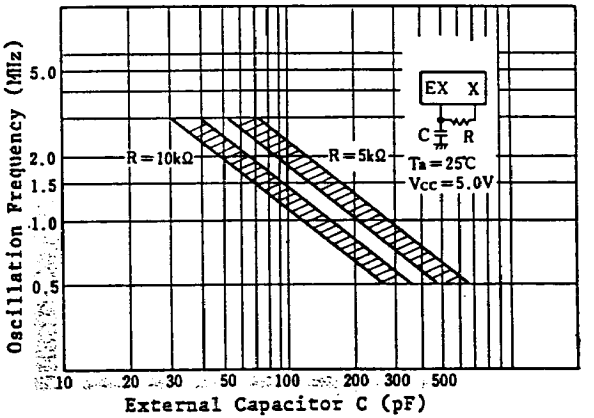


(3) External Clock Drive



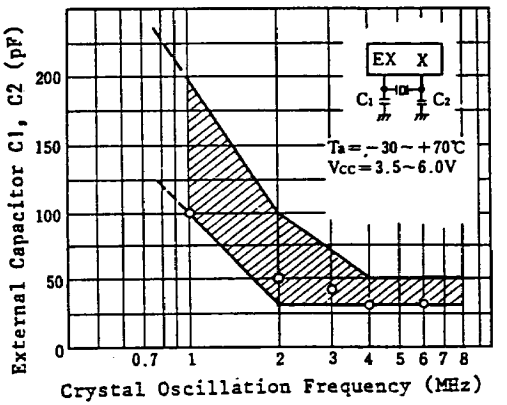
* When the RC-network oscillation is used, the following conditions must be met:
1) The prescaler is not used.
2) V_{CC}=5V±10%
3) T_A=−30°C to +70°C
4) f_C does not exceed 4MHz (Max. setting clock frequency is about 3.2 MHz at V_{CC}=5V and T_A=25°C.)

Fig. 6: RC-NETWORK OSCILLATION CHARACTERISTICS (EXAMPLE)



Note:
When the RC-network oscillations is used, the following conditions must be met: 1) The prescaler is not used. 2) V_{CC}=5V±10%
3) T_A=-30°C to 70°C 4) f_C does not exceed 4.0 MHz.

Fig. 7: CRYSTAL OSCILLATION CHARACTERISTICS (EXAMPLE)



Notes:
1) The cross-hatched portion shows an area where the on-chip oscillator has stable oscillation characteristics and short oscillation stabilization time when an average crystal resonator is used. This chart gives an aim value of the external capacitor to realize a desired oscillation frequency. When an exact oscillation frequency is needed, a capacitor value should be determined, adjusting to individual crystal resonator characteristics.

2) Generally speaking, crystal resonators with lower oscillation frequency tend to have longer oscillation stabilization time and wider characteristic variations which affect on-chip oscillator characteristics. So, we recommend to use high-frequency crystal resonator with on-chip 1/2 prescaler.

• **OUTPUT TIMING** (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin/Port	Conditions	Value		Unit
				Min.	Max.	
E-, R-Ports Delay Time	t_{EDH}	E-Port, R-Port	Fig. 8 *1		1000	ns
	t_{EDL}				350	
Serial Port Delay Time	t_{SDH}	SO	Fig. 8		1000	ns
	T_{SDL}				350	
Pulse Generator Output Port Delay Time	t_{PDH}	PGO	Fig. 8		1000	ns
	T_{PDL}				350	

Note:
*1. A 10 kΩ pull-up is required when open-drain output is used.
*2. All the output loading values are 50 pF + 1TTL. See figure below.

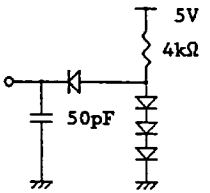
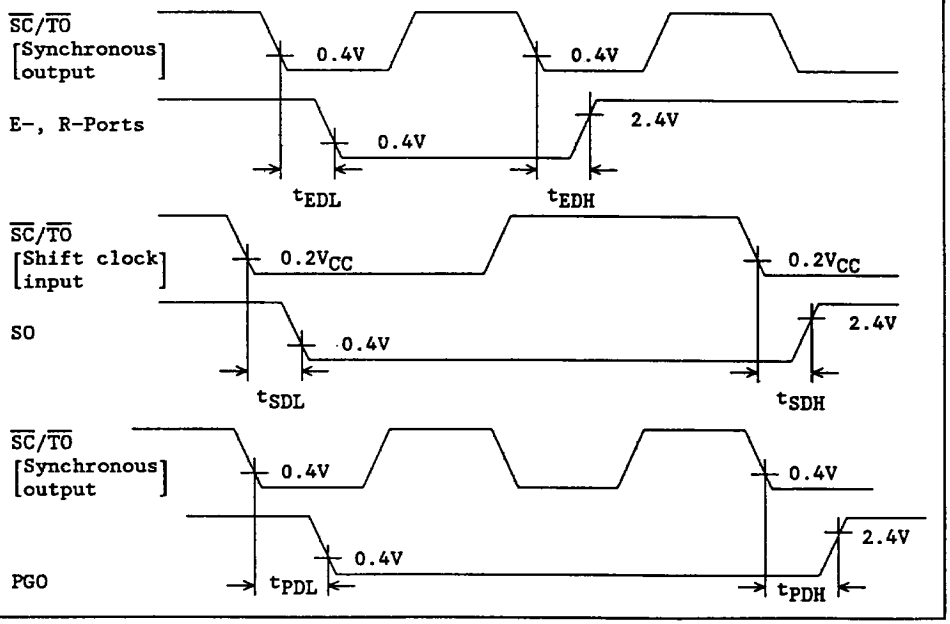


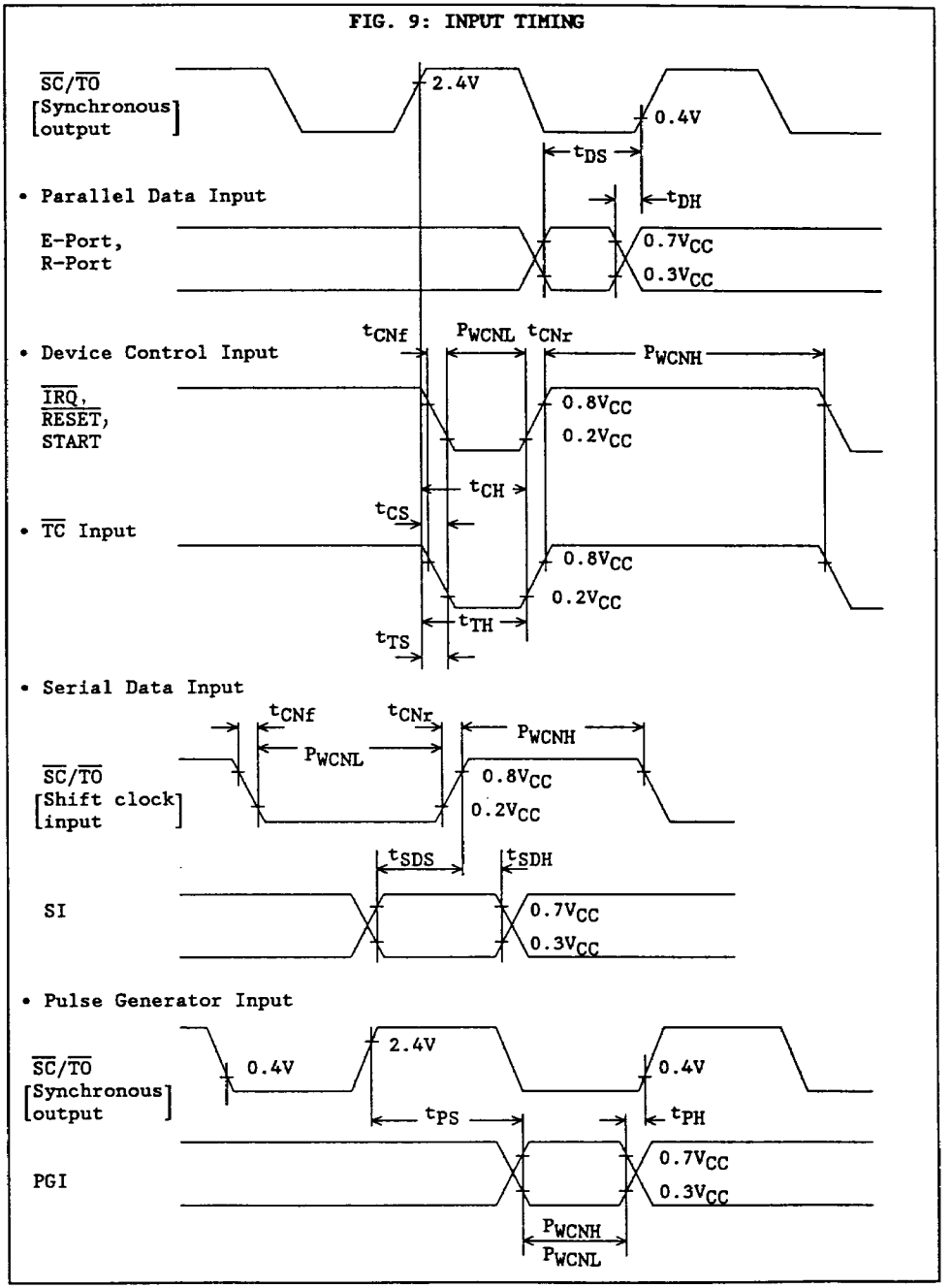
Fig. 8: OUTPUT CLOCK TIMING



INPUT TIMING (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin/Port	Conditions	Value		Unit
				Min.	Max.	
Input Data Setup Time	t_{DS}	E-Port, R-Port	Fig. 9	$t_{cyc}+1000$		ns
Input Data Hold Time	t_{DH}				$t_{cyc}-50$	
SI Input Setup Time	t_{SDS}	SI	Fig. 9	600		ns
SI Input Hold Time	t_{SDH}			600		
Device Control Setup Time (Synchronous mode)	t_{CS}	$\overline{RESET}$	Fig. 9		$2t_{cyc}-200$	ns
		$\overline{IRQ}$			$2t_{cyc}-200$	
Device Control Hold Time (Synchronous mode)	t_{CH}	$\overline{RESET}$	Fig. 9	$8t_{cyc}+50$		ns
		$\overline{IRQ}$		$2t_{cyc}+50$		
Timing Input Setup Time (synchronous mode)	t_{TS}	$\overline{TC}$	Fig. 9		$2t_{cyc}-200$	ns
Timing Input Hold Time (Synchronous mode)	t_{TH}	$\overline{TC}$	Fig. 9	$2t_{cyc}+50$		ns
Pulse Generator Trigger Input Setup Time (synchronous mode)	t_{PS}	PGI	Fig. 9		$5t_{cyc}-200$	ns
Pulse Generator Trigger Input Hold Time (Synchronous mode)	t_{PH}	PGI	Fig. 9	$5t_{cyc}+50$		ns
Control Signal Low Level Time (Asynchronous mode)	P_{WCNL}	$\overline{SC}/\overline{TO}$	Fig. 9	$6t_{cyc}+250$		ns
		$\overline{IRQ}$, $\overline{TC}$, PGI		$6t_{cyc}+250$		
		$\overline{RESET}$		$12t_{cyc}+250$		
Control Signal High Level Time (Asynchronous mode)	P_{WCNH}	$\overline{SC}/\overline{TO}$	Fig. 9	$12t_{cyc}+250$		ns
		$\overline{RESET}$, $\overline{TC}$, $\overline{IRQ}$, PGI		$6t_{cyc}+250$		
		START		500		
Control Signal Rise and Fall Time	t_{CNr}, t_{CNf}	START, $\overline{SC}/\overline{TO}$, $\overline{IRQ}$, $\overline{RESET}$, $\overline{TC}$, PGI	Fig. 9	Should be less than 200ns		

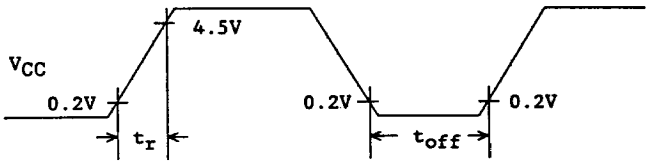
FIG. 9: INPUT TIMING



- **POWER-ON RESET**

Parameter	Symbol	Condi-tions	Value		Unit	Remarks
			Min.	Max.		
Power Supply Rise Time	t_r	Fig. 10	0.05	50	ms	Required for operation of the power-on reset circuit
Power Supply Shut-off Time	t_{off}	Fig. 10	1		ms	Required for accurate circuit operation repeatability

Fig. 10: POWER-ON RESET TIMING



Note:
Power supply should be raised smoothly.

- **A/D CONVERTER CHARACTERISTICS**
  (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min.	Typ.	Max.	
Resolution						5	Bit
Linearity Error			T_A=25°C AV_{CC}=5.0V AV_{R-}=0V			±1.0	LSB
Differential Linearity Error						±0.9	LSB
Zero Transition Voltage	V_{OT}			8	78	148	mV
Full-Scale Transition Voltage	V_{FST}			+4696	+4766	+4836	mV
Conversion Time			108 x t_{CYC}	27 *1		154*2	µs
Analog Port Input Current	I_{AIN}	AN3-0				5	µA
Analog Input Voltage		AN3-0		AV_{R-}		AV_{CC}	V
Reference Voltage		AV_{R-}		0	0	AV_{CC}	V
Supply Current	I_A	AV_{CC}	AV_{CC}=5.0V fc=2 MHz All outputs open		3		mA
Standby Supply Current	IA_H	AV_{CC}	AV_{CC}=5.5V fc=0 MHz standby mode, All outputs open			5	µA
Reference Voltage Supply Current	I_R	AV_{CC} AV_{R-}	AV_{CC}-AV_{R-} AV_{CC}=5.0V, AV_{R-}=0V		0.6		mA

Notes:
1. Error between analog inputs is within 1/2 LSB when AV_{R+}-AV_{R-}=5.0V
2. Full-scale and offset can be adjust by an appropriate setting of AV_{R-}.
3. Error becomes relatively larger as $|AV_{CC}-AV_{R-}|$ becomes smaller.

*1 fc=8.0 MHz (with prescaler)
*2 fc=2.0 MHz (without prescaler)

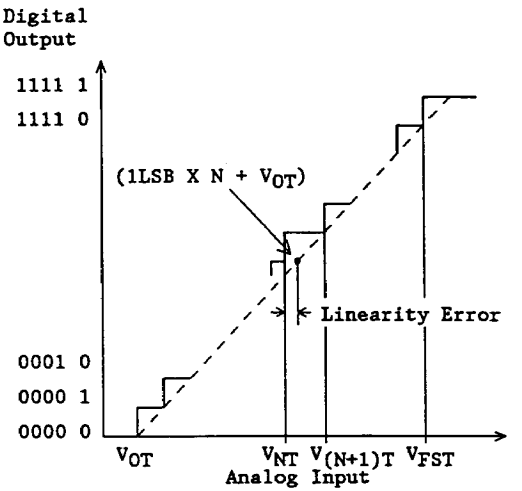
- Resolution
  The minimum variation in an analog signal that can be discriminated by the A/D converter. (An analog voltage can be divided into 2^5=32 parts.)

- Linearity Error
  The difference between the line connecting the device zero transition point ("0 0000" ⟷ "0 0001") with the full scale transition point ("1 1111" ⟷ "1 1110"), the actual conversion characteristics.

- Differential Linearity Error
  The difference from ideal input voltage required to change the output voltage code by 1LSB.

• A/D CONVERTER CHARACTERISTICS

Fig. 9: A/D TRANSFER CHARACTERISTICS



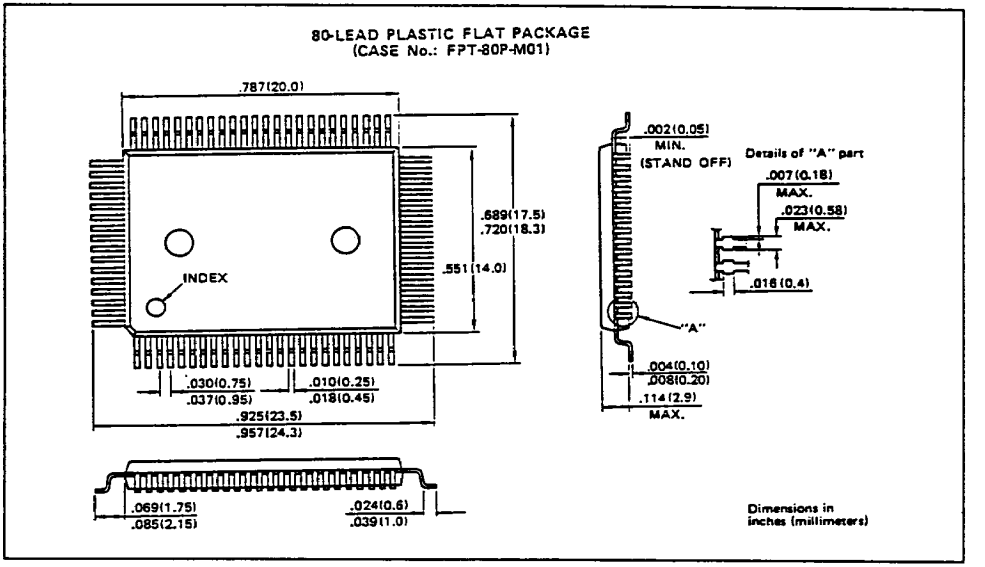
$$1LSB = \frac{V_{FST} - V_{OT}}{30}$$

$$\text{Linearity Error} = \frac{V_{NT} - (1LSB \times N + V_{OT})}{1LSB} \quad (LSB)$$

$$\text{Differential Linearity Error} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \quad (LSB)$$

PACKAGE DIMENSION

• MB88551H-PF/MB88552H-PF: 80-PIN PLASTIC FLAT PACKAGE



• MB88558H-CF: 80-PIN CERAMIC MODULE