Exam rules for projects

Preliminary note

Once the project is assigned, the project referent will share the student(s) assigned to the project a dedicated folder which is hosted on the *One Drive* storage space of the project referent: students will have full modification permission to the shared folder and its content. A copy of the project specifications (PDF document) will be stored inside the shared folder dedicated to the project.

Project rules

1. Put inside the shared folder all the files concerning RTL design, testbench and verification (RTL files and Modelsim) and implementation on FPGA (Quartus Prime), so that project referent can run simulation and implementation on FPGA on its own.
   - Even if developing several testbenches (for debug), not all testbenches have to be uploaded, but just the one (or the ones) that can be considered as "official release" for verification.
   - Please, follow the organization of folders and files illustrated during lectures (i.e. set of folders *db/*, *tb/*, *modelsim/* and *quartus/*). In case of additional files:
     i. put eventual test vectors file(s) inside *modelsim/* folder.
     ii. put eventual file(s) for Static Timing Analysis (file *.sdc*) inside *quartus/* folder.

2. Produce a project report as described in the section below.
   - Points 1, 2, 3, 4 and 5 are mandatory.
   - Point 6 is optional and it is aimed to increase the final evaluation.

   The project report shall be sent by email with the HDL files (design and testbench) to:
   - Professor Sergio Saponara (sergio.saponara@unipi.it)
   - Project referent (as Carbon Copy – CC)

   Project report can be either Word file or PDF file and HDL files can be either SystemVerilog files (.sv) or PDF files.

Project report: structure and content

1. **Specification analysis**
   Elaboration of specifications and requirements to demonstrate how they have been parsed and used: a sort of introduction which describes the project.

2. **Block diagram and design choices (RTL design module)**
   Description of the design architecture, with block diagrams, schematics (functional and/or architectural), FSM diagrams, etc.

3. **Expected waveforms**
   Snapshot(s) and image(s), by screenshot or export from Modelsim, of waveforms showing significant signals and significant behaviour of signals, with description and/or comments.

4. **Testbench (block diagram, testbench design choices, comments on test-plan)**
   Similar to point 2, architectural and/or functional description of the testbench and verification methodology/approach.

5. **Implementation of RTL design on FPGA and results**
   Results of FPGA implementation of the design by means of Quartus tool, with comments (and

snapshot, if suitable) of Quartus reports.

6. **Optional – Static Timing Analysis (STA)**
   Description and comments of STA results (maximum frequency, …), with snapshots, if suitable. Please, attach also the timing constraints file (SDC or PDF format) to the project report.