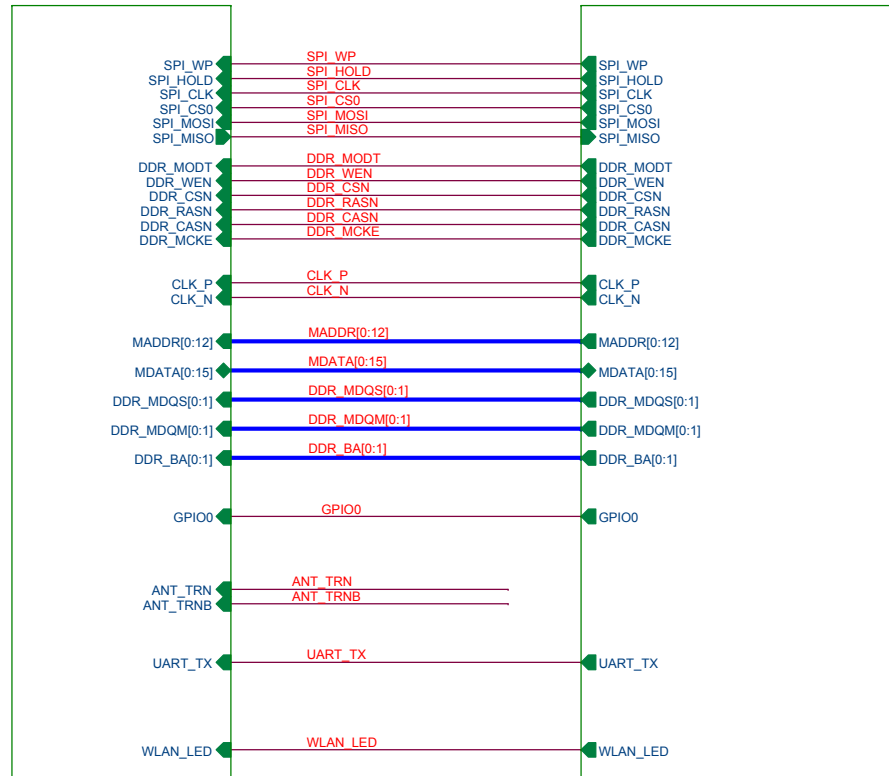


2-MEMORY



2-MEMORY

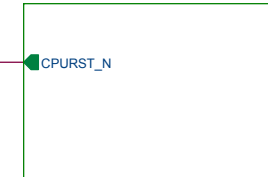
3-WLAN



3-WLAN

1-CPU-MT7620N

4-POWER

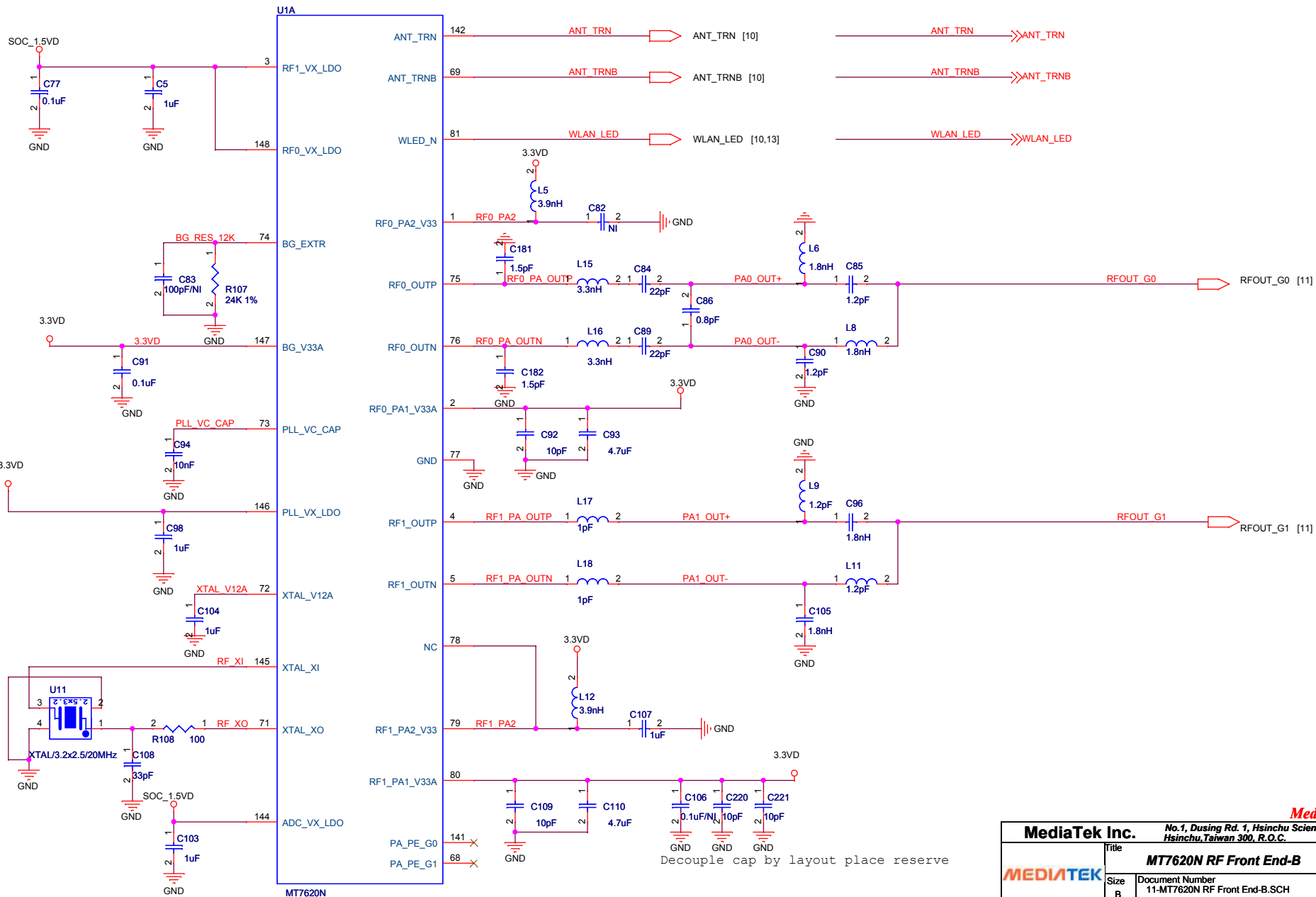


4-POWER

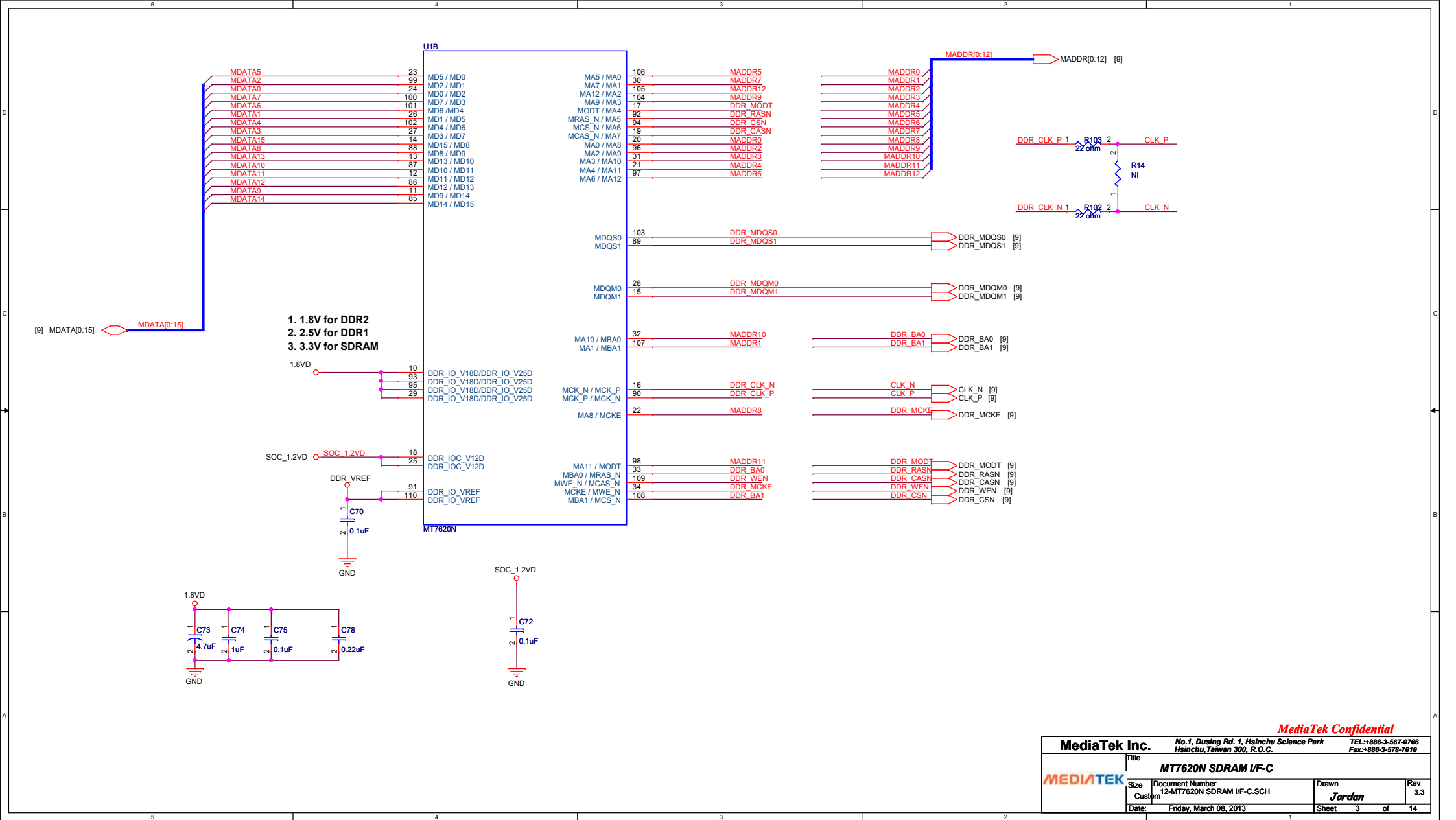
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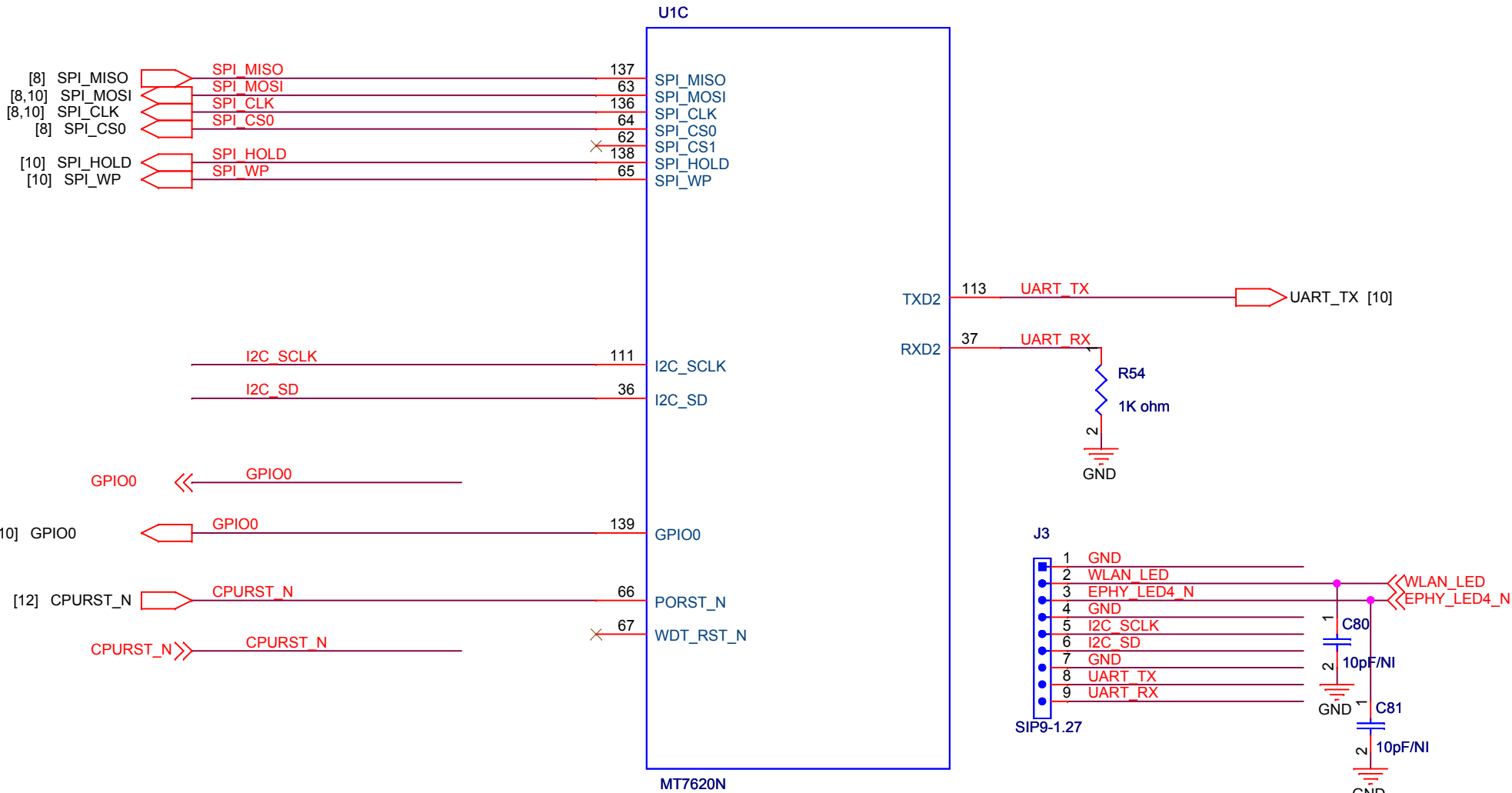
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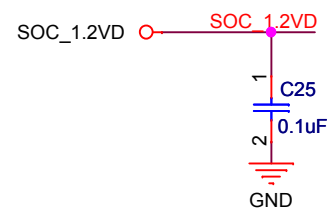
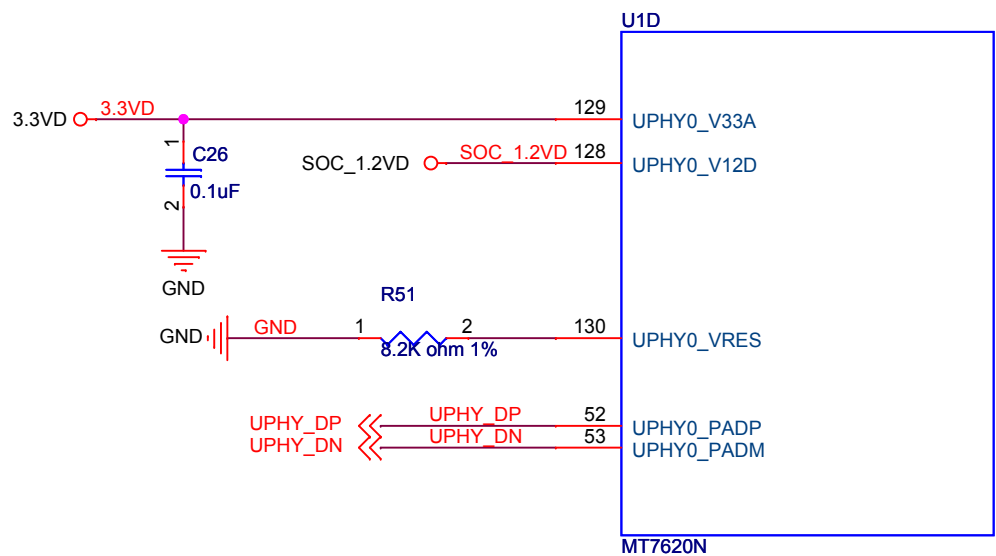
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	Title		11n 2.4G AP-MT7620N		
	Size	Document Number	Drawn	Rev	
	B	11n 2.4G AP-MT7620N.SCH	Jordan	3.3	
	Date:		Friday, March 08, 2013	Sheet	1 of 14




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		MT7620N RF Front End-B		
Size B	Document Number	11-MT7620N RF Front End-B.SCH	Drawn	Rev 3.3
Date:	Friday, March 08, 2013	Sheet	2 of 14	

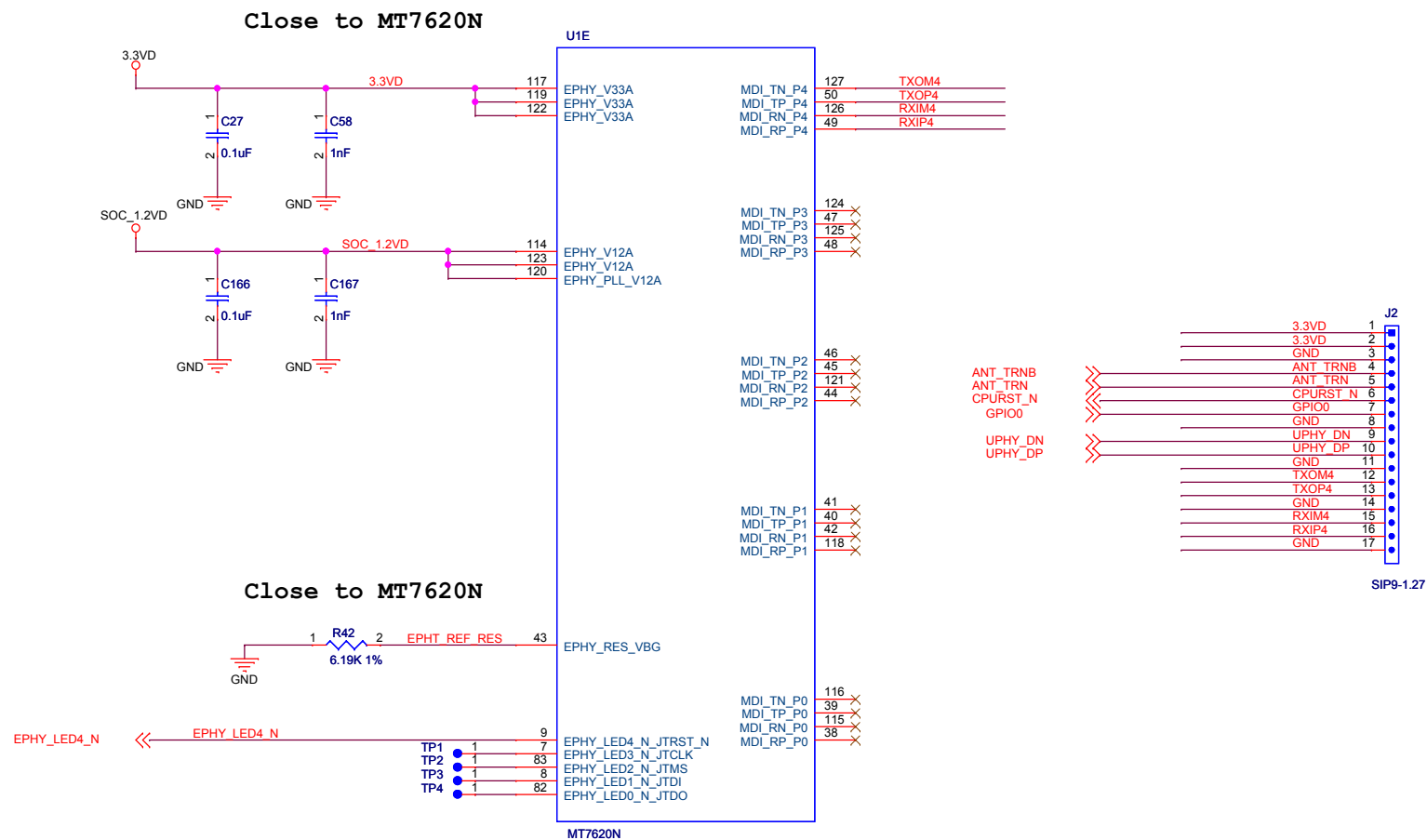




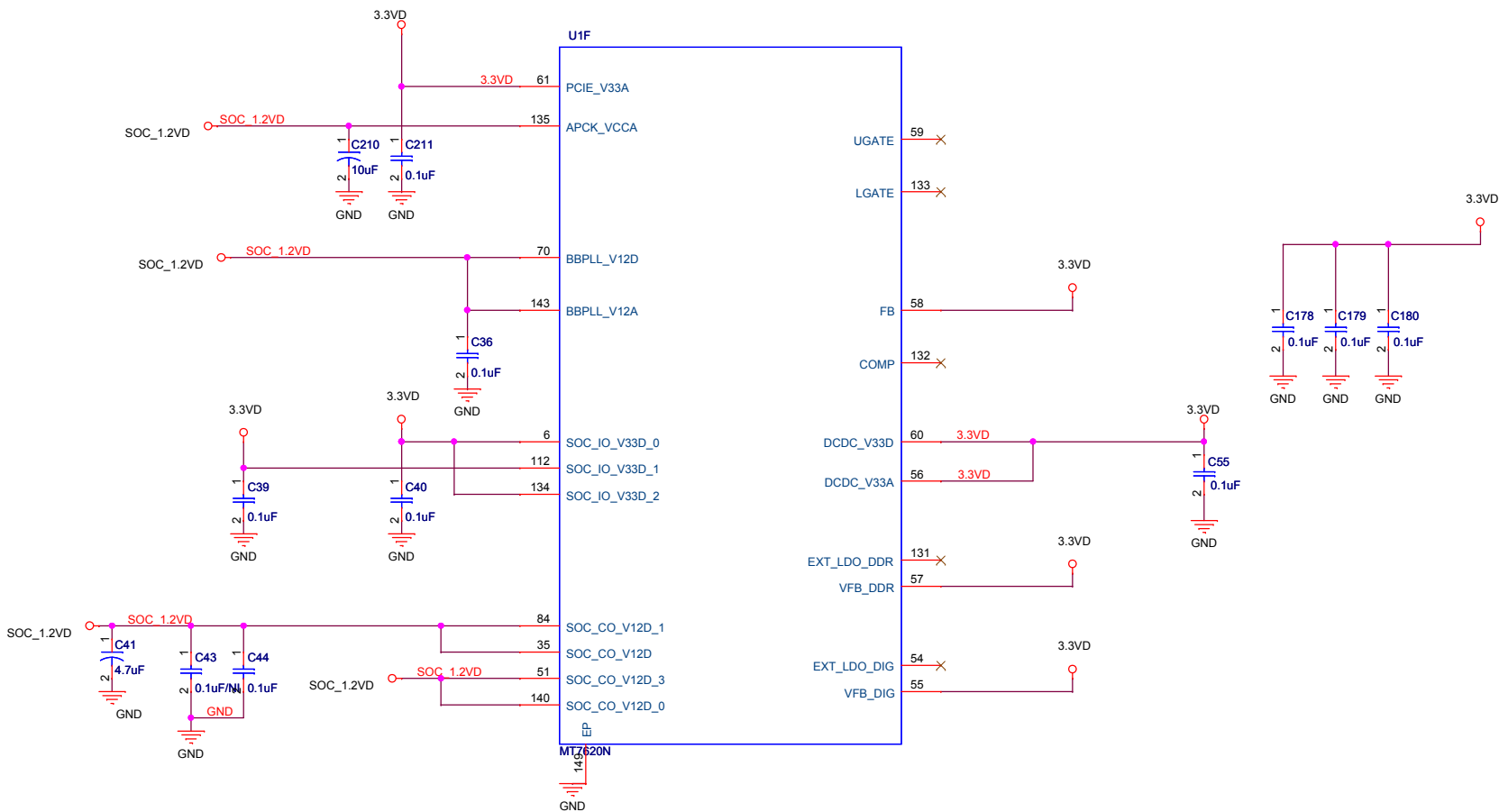


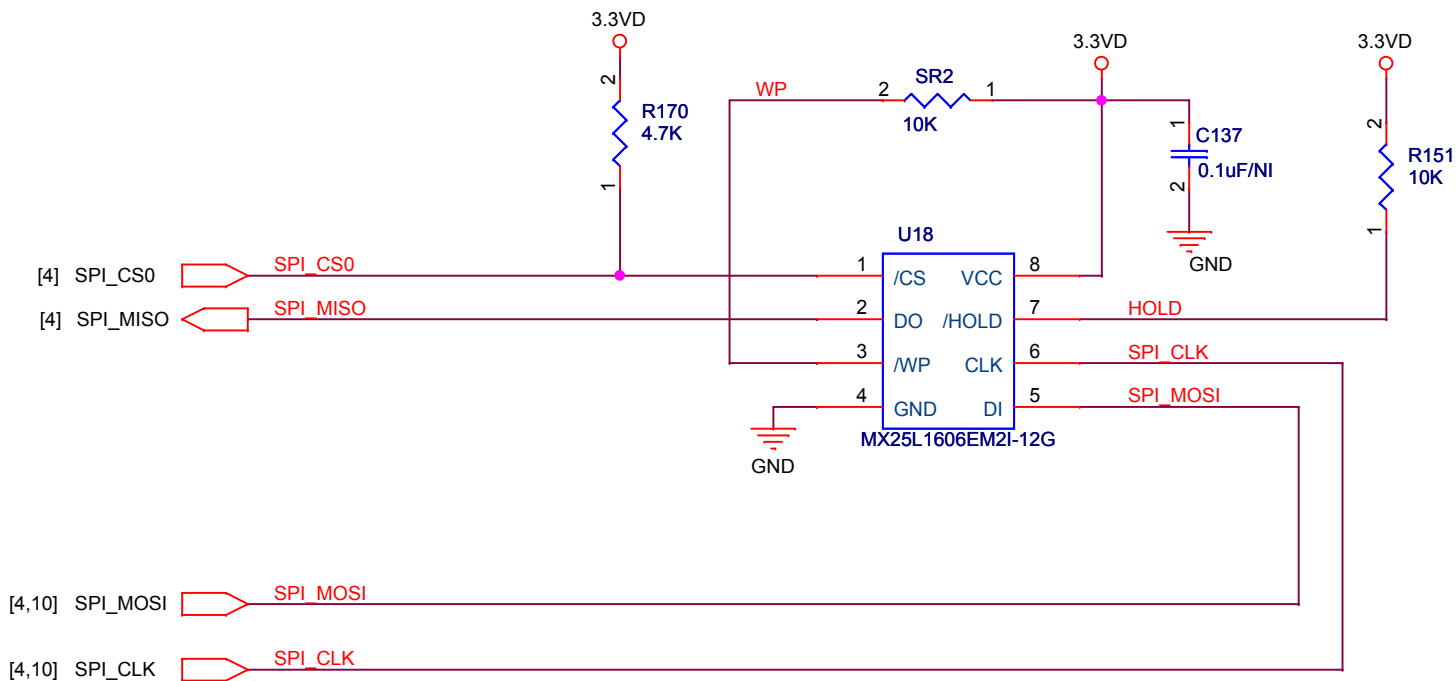
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	Title				
	MT7620N USB-D				
	Size A	Document Number 14-MT7620N USB-D.sch		Drawn Jordan	Rev 3.3
	Date:	Friday, March 08, 2013		Sheet 5 of 14	




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		Title MT7620N Ethernet-E		
Size B	Document Number	Drawn	Rev	
	15-MT7620N Ethernet-E.SCH	Jordan	3.3	
Date:	Friday, March 08, 2013	Sheet	6 of	14





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	Title SPI Flash				
	Size A	Document Number 21-SPI Flash.SCH		Drawn Jordan	Rev 3.3
	Date:	Friday, March 08, 2013		Sheet 8 of 14	

[3] MDATA[0:15]

MDATA[0:15]

[3] MADDR[0:12]

MADDR[0:12]

[3] DDR_BA0

[3] DDR_BA1

[3] DDR_MCKE

[3] DDR_CSN

[3] DDR_RASN

[3] DDR_CASN

[3] DDR_WEN

DDR_BA0

DDR_BA1

DDR_MCKE

DDR_CSN

DDR_RASN

DDR_CASN

DDR_WEN

L2

L3

L1

L8

K7

L7

K5

BA0

BA1

BA2

CK_P

CK_N

CS

RAS

CAS

WE

A0

A1

A2

A3

A4

A5

A6

A7

A8

A9

A10

A11

A12

A13

(2Gb)

DDR2 SDRAM

512Mb (32Mb x 16)

~2Gb (128Mb x 16)

DDR2 SDRAM

512Mb (32Mb x 16)

~2Gb (128Mb x 16)

DDR2 SDRAM

512Mb (32Mb x 16)

~2Gb (128Mb x 16)

DDR2 SDRAM

512Mb (32Mb x 16)

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512Mb (32Mb x 16)

~2Gb (128Mb x 16)

DDR2 SDRAM

512Mb (32Mb x 16)

~2Gb (128Mb x 16)

DDR2 SDRAM

512Mb (32Mb x 16)

~2Gb (128Mb x 16)

DDR2 SDRAM

512Mb (32Mb x 16)

~2Gb (128Mb x 16)

DDR2 SDRAM

1.8VD

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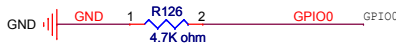
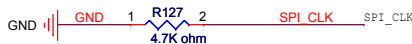
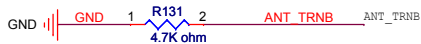
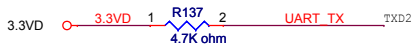
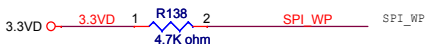
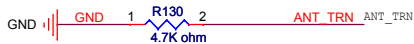
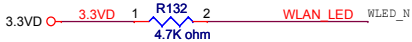
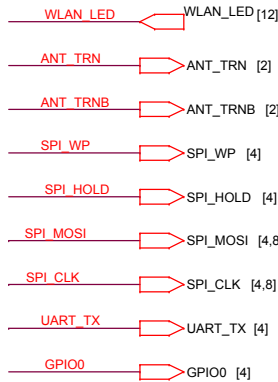
VDD

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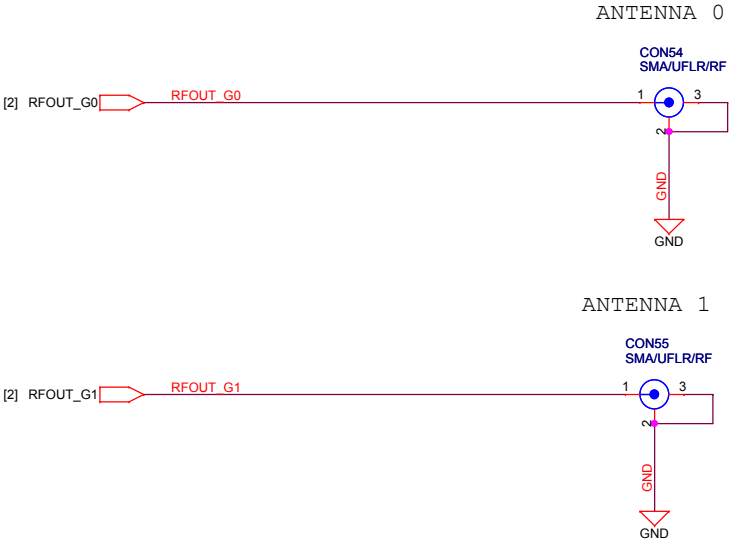
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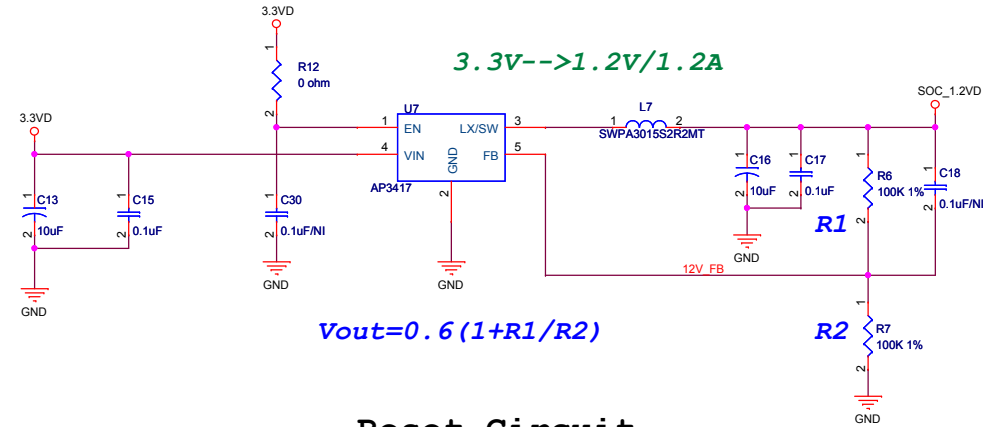
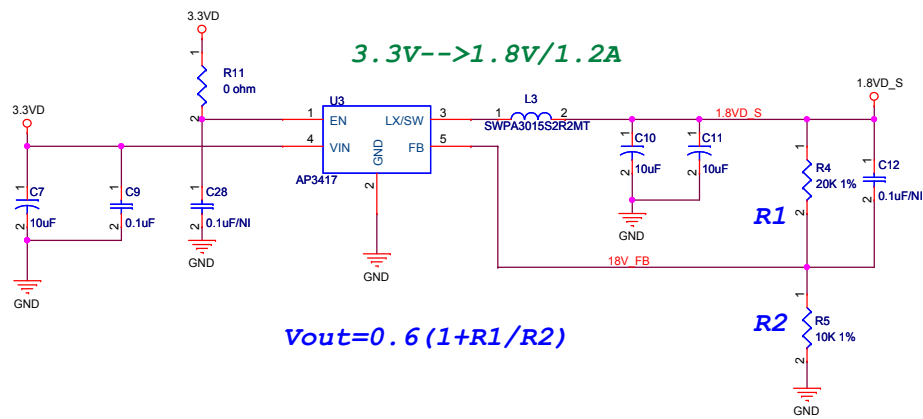
MT7620N Boot Up Strapping

Pin Name	Description	Value
WLED_N	DRAM_FROM_EE For non scan mode:	0: DRAM configuration from EEPROM 1: DRAM configuration from Auto Detect
ANT_TRN	DBG_JTAG_MODE	0: EPHY_LED 1: JTAG MODE
ANT_TRNB	XTAL_FREQ_SEL	0: 20MHz 1: 40MHz
{SPI_WP, SPI_HOLD}	DRAM_TYPE	01: DDR1 (CPU/3) TSOP Package 10: DDR2 (CPU/3) FBGA Package * 11: SDRAM (CPU/5) (LVTTTL 3.3 V) TSOP Package
{SPI_MOSI SPI_CLK, TXD2, GPIO0 }	CHIP_MODE[3:0]	A vector to set chip function/test/debug modes. In non-test/debug operation, 0010: Normal mode (boot from SPI 3Byte Addr)

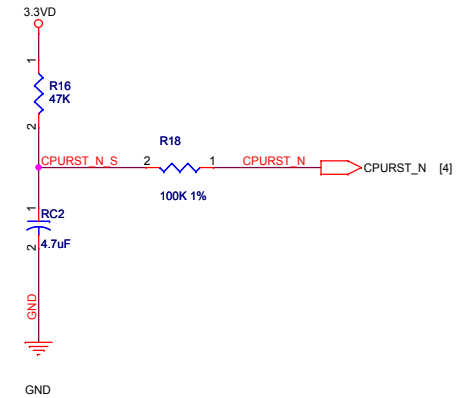
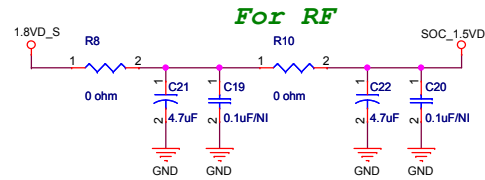
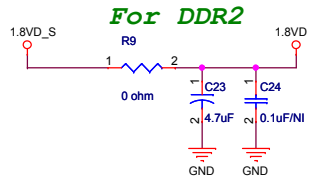
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	Config		
	Size B	Document Number 23-Config.SCH	Drawn Jordan
	Date:	Friday, March 08, 2013	Rev 3.3
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3.3V DC Vin



Reset Circuit



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Size		Document Number		Drawn	
CUSTOMER		5-Power - Reset.SCH		Jordan	
Date:		Friday, March 08, 2013		Sheet 12 of 14	
				Rev 3.3	