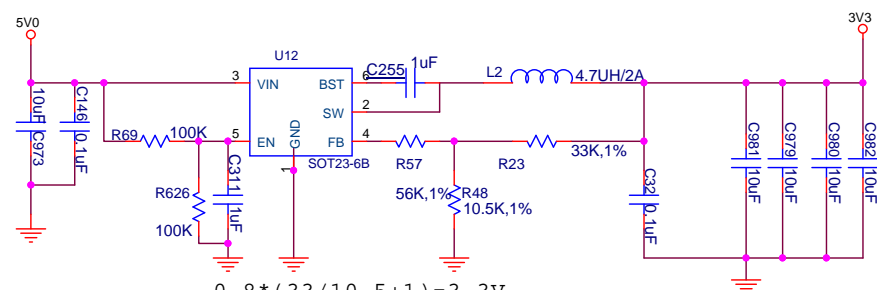
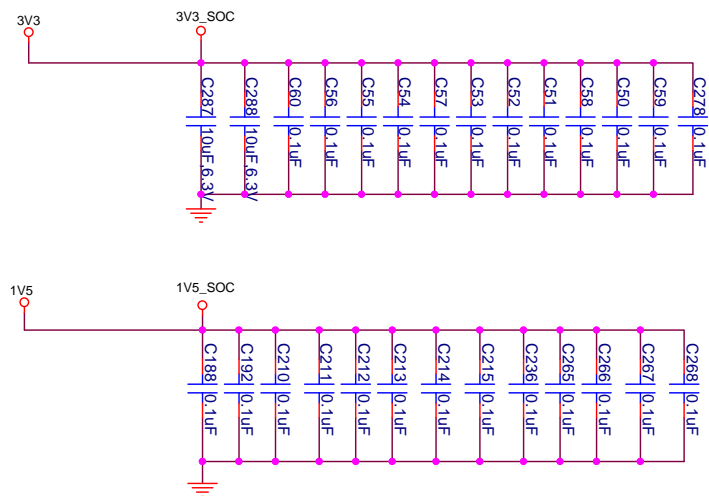


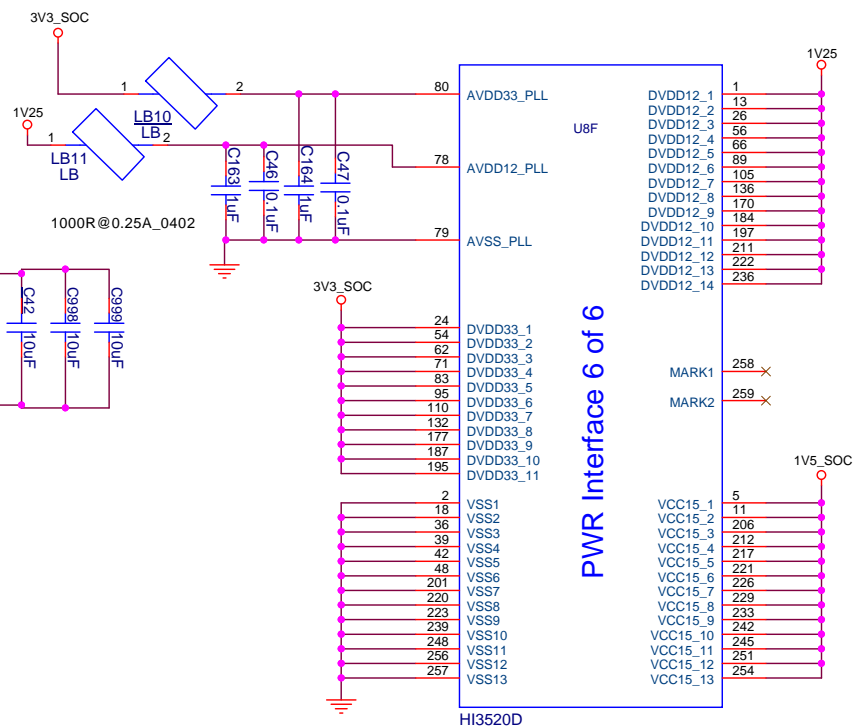
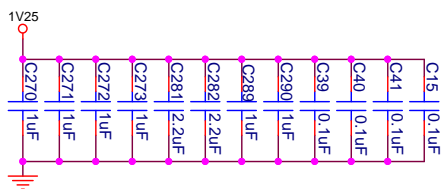
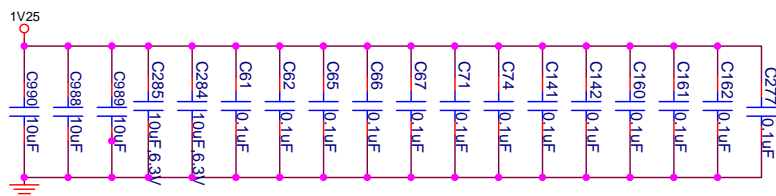
DC\_041



# Hi3520D POWER\_GND



The kind and quantity of the caps must be the same as that for the Hi3520D demo board.

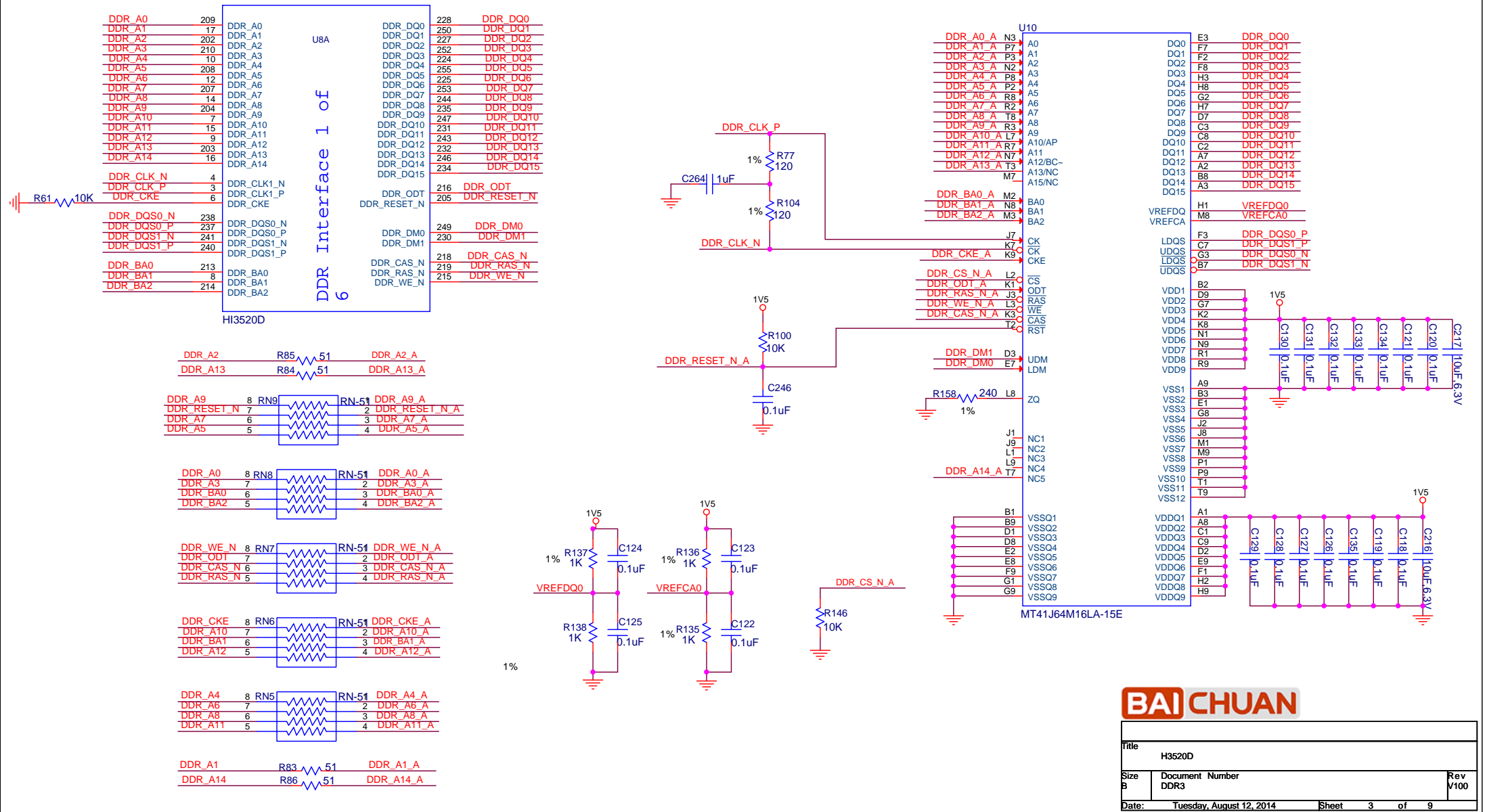


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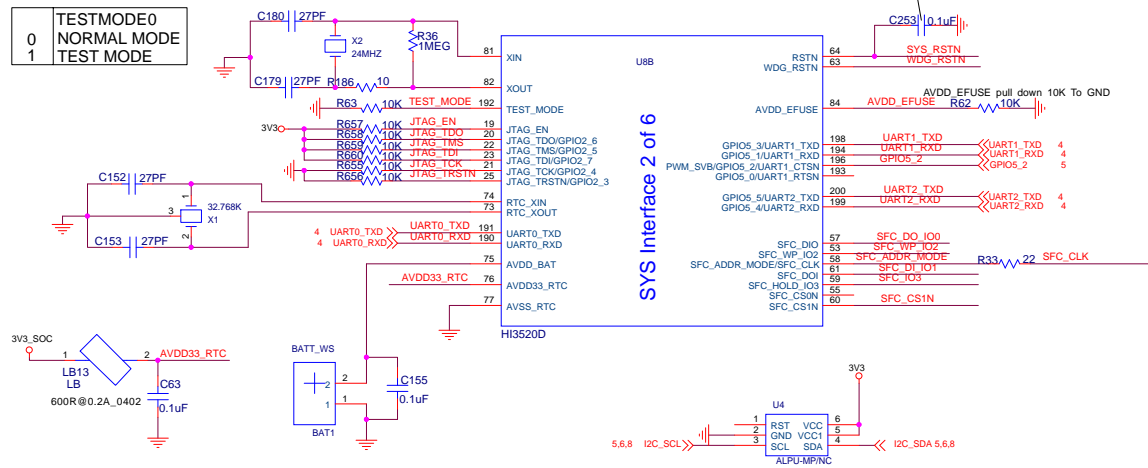
# Hi3520D DDR3

The routing design for the DDR must be the same as that for the Hi3520D demo board.



# Hi3520D SYS\_RST\_JTAG

put this Cap close to Hi3520D

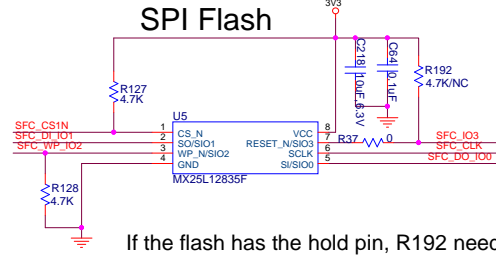
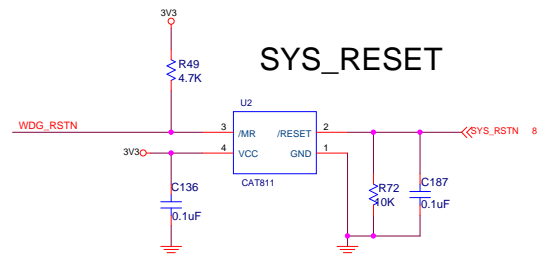


SFC_ADDR_MODE	JTAG_EN
0 3 Byte mode	0 Disable JTAG
1 4 Byte mode	1 Enable JTAG

SFC_ADDR_MODE	JTAG_EN
0 3 Byte mode	0 Disable JTAG
1 4 Byte mode	1 Enable JTAG

SFC\_ADDR\_MODE 0

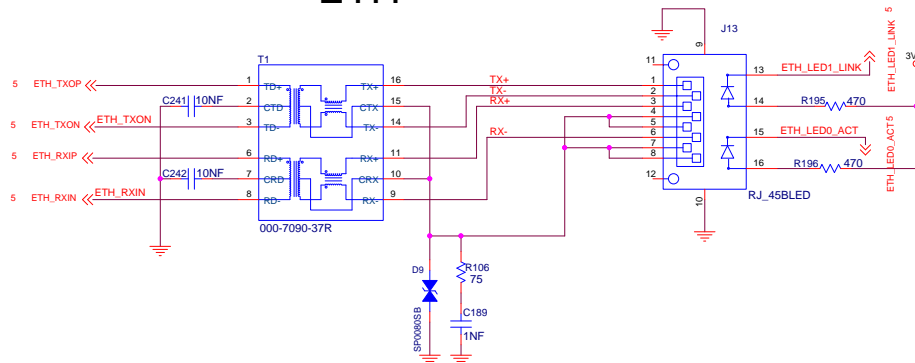
R74 4.7K



If the flash has the hold pin, R192 need to pull up.

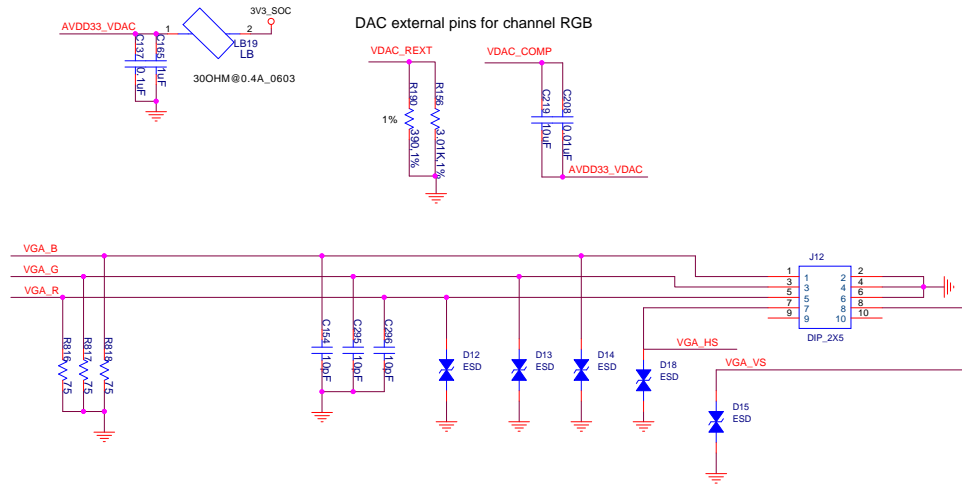
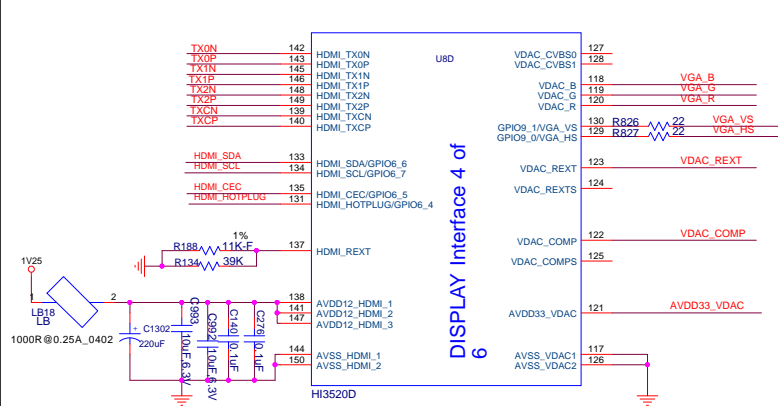
The USB differential trace impedance is 90 OHM  
9/5/9 trace width is OK for two-layer board

## ETH

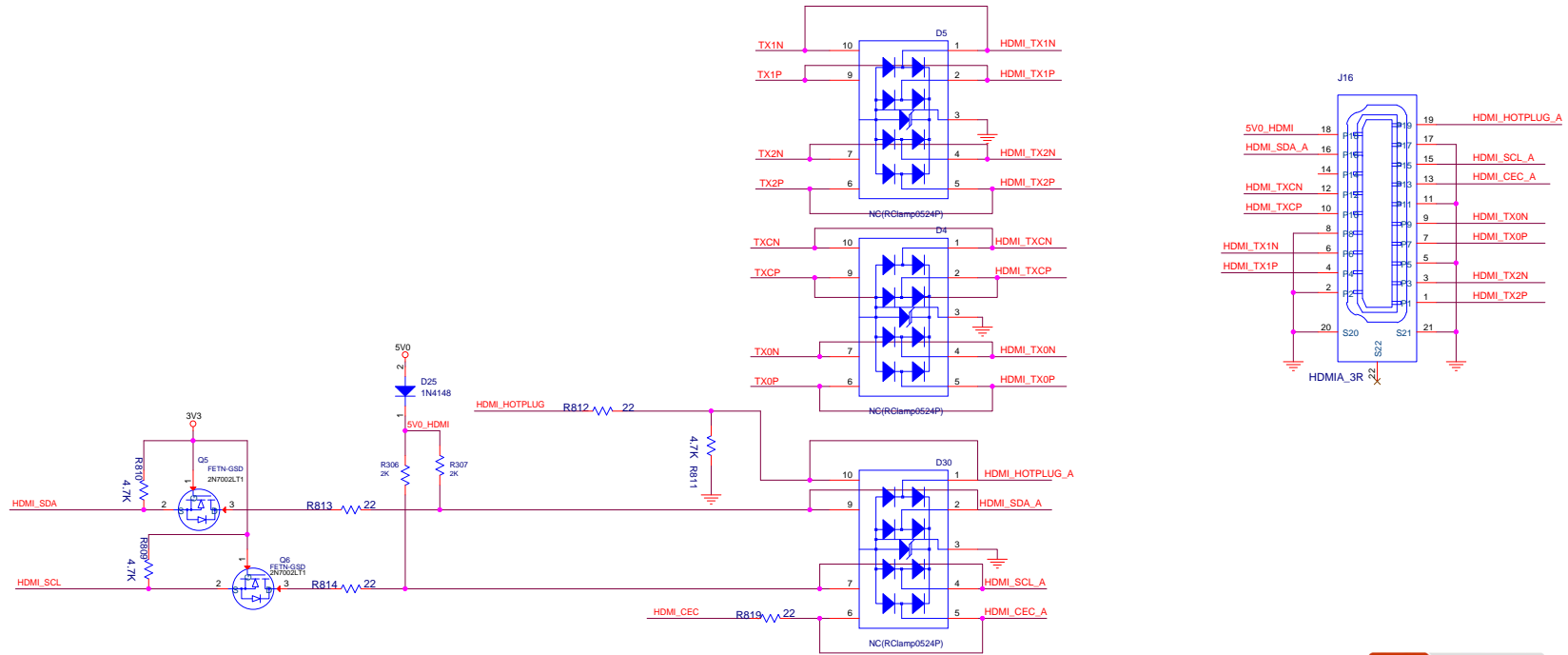




# DISPLAY



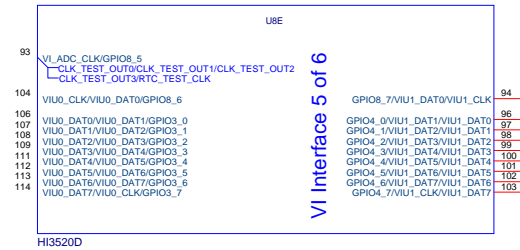
## HDMI



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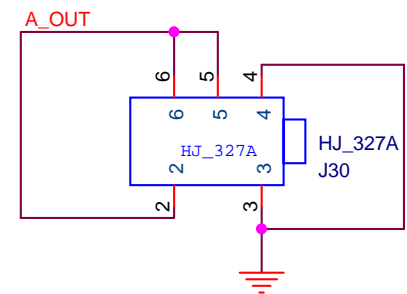
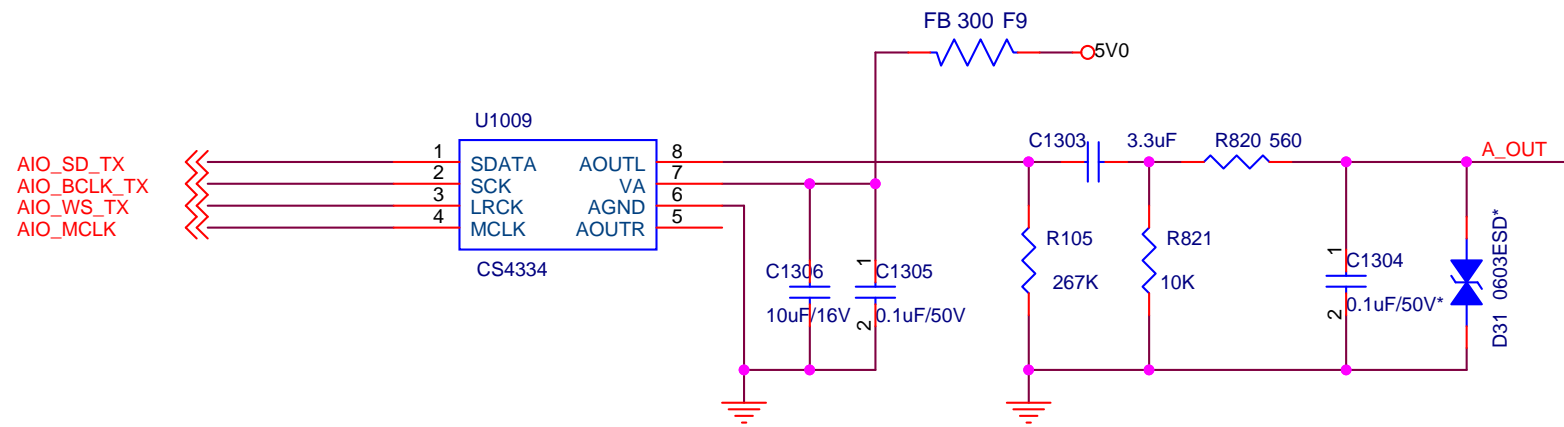
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- 1) 2xBT.656@108MHz for 8D1/CIF real-time inputs.
- 2) 1xBT.656@144MHz for 4x960H real-time inputs.  
But only 4x960H(not 8x960H) real-time inputs can be Supported.You can choose VIU0 or VIU1.
- 3) 2xBT.656@148MHz for 2x720P real-time inputs.The Demo board does not have this funtion.
- 4) 2xBT.656 can combin into 1xBT.1120@74/148MHz for 1x720P/1080P real-time input.  
The Demo board does not have this funtion.
- 5) VI\_ADC\_CLK can output 24MHz 27MHz and 54MHz.
- 6) You can change the VI\_DATA order form DAT0 to DAT7,or from DAT7 to DAT0.



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WIFI\_EN >> WIFI\_EN

