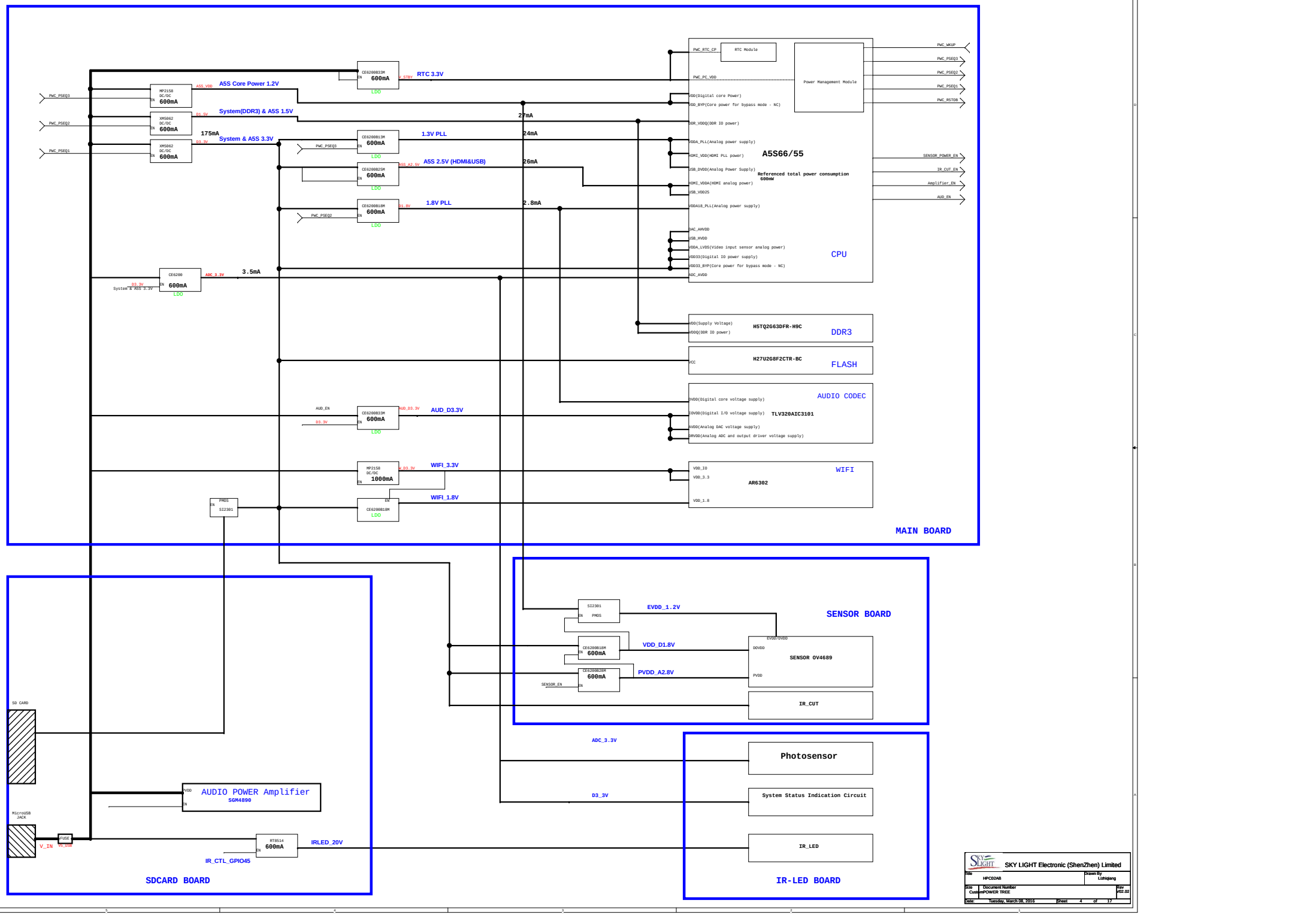

MAIN BOARD
RTC 3.3V
A5S Core Power 1.2V
System(DDR3) & A5S 1.5V
System & A5S 3.3V
1.3V PLL
A5S 2.5V (HDMI&USB)
1.8V PLL
3.5mA
27mA
24mA
26mA
2.8mA
175mA
A5S66/55
Referenced total power consumption
600mW
CPU
DDR3
H5TQ2G63DFR-H9C
FLASH
H27U2G8F2CTR-BC
AUDIO CODEC
TLV320AIC3101
AUD_D3.3V
WIFI_3.3V
WIFI_1.8V
WIFI
AR6302
SENSOR BOARD
EVDD_1.2V
VDD_D1.8V
PVDD_A2.8V
SENSOR 0V4689
IR_CUT
ADC_3.3V
D3_3V
Photosensor
System Status Indication Circuit
IR_LED
IR-LED BOARD
SDCARD BOARD
SD CARD
AUDIO POWER Amplifier
SGM4890
MicroUSB JACK
IRLED_20V
IR_CTL_GPIO45
SKY LIGHT Electronic (ShenZhen) Limited
HPC02AB
Drawn By Lishiqiang
Document Number POWER TREE
Rev V02.02
Tuesday, March 08, 2016
Sheet 4 of 17

A5S Power-On-Config Setting

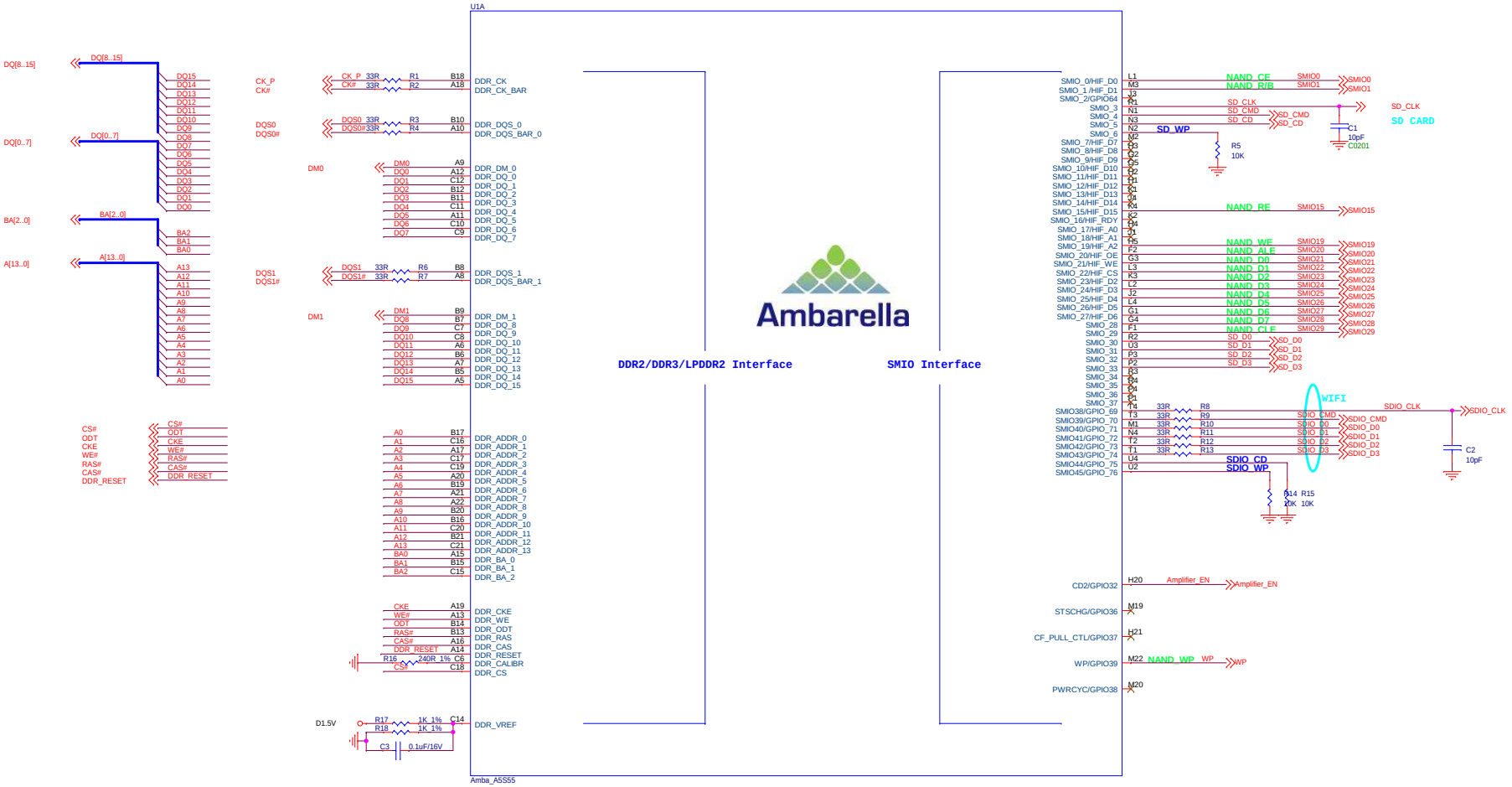
A5S Power-On-Config (VD0_OUT0~15)
==========
VD0_OUT0
Boot Media Select
0: NAND flash
1: Reserved
==========
VD0_OUT[3:1]
Clock: iDSP / vDSP / DRAM
000: 126 / 108 / 300 MHz
001: 120 / 96 / 300 MHz
010: 108 / 108 / 240 MHz
011: 96 / 96 / 192 MHz
100: 117 / 108 / 300 MHz
101: 117 / 96 / 300 MHz
110: 117 / 108 / 240 MHz
111: 96 / 96 / 192 MHz
==========
VD0_OUT4
PLL_UNLOCK_TRIG_RESET
0: disable generating GRST when core PLL out of lock (default)
1: enable generating GRST when core PLL out of lock
==========
VD0_OUT5
NAND Flash Page Size
0: 512 Bytes
1: 2K Bytes
==========
VD0_OUT6
NAND Read Confirm
0: No "Read Confirm" needed
1: Requirs "Read Confirm"
==========
VD0_OUT7
Select ENET
0: disable
1: enable
==========
VD0_OUT8
Boot Bypass
0: disable (no boot bypass)
1: enable
==========
VD0_OUT9
Flash Fast Boot Mode
0: disable
1: enable
==========
VD0_OUT10
IO Flash BOOT
0: USB
1: Flash
==========
VD0_OUT11
Reserved
Set to 0
==========
VD0_OUT12
EMA Select
Set to 0
==========
VD0_OUT13
ARM Sync Lock Mode
0: disable
1: enable
==========
VD0_OUT14
ARM Mode Change Issue Reset
0: GRST_L not issued when switching between ARM sync/async modes
1: GRST_L issued when switching between ARM sync/async modes
==========
VD0_OUT15
RMII Select
Set to 0
==========

A5S Power-On-Config (VD1_OUT0~15)
==========
VD1_OUT0
SPI Boot
0: USB / Flash
1: SPI
==========
VD1_OUT1
HIF Enable
0: disable
1: enable host interface
==========
VD0_OUT2
Reserved
Set to 0
==========
VD1_OUT3
HIF Type
0: Intel
1: Motorola
==========
VD1_OUT4
RDY Polarity
0: HIF_RDY active low
1: HIF_RDY active high
==========
VD1_OUT5
HIF Secure Mode
0: normal
1: secure mode
==========
VD1_OUT6
Reserved
Set to 0
==========
VD1_OUT7
USB Clock Source Select
0: choose internal clock for USBPHY
1: choose external clock for USBPHY
==========
VD1_OUT[9:8]
Reserved
Set to 0
==========
VD1_OUT[10]
REF_CLK for USB
Set to 1
==========
VD1_OUT[11]
Reserved
Set to 0
==========
VD1_OUT[12]
Reserved
Set to 0
==========
VD1_OUT[14:13]
SYS_CONFIG
00: use power-on-config set on external pins
01: select pre-set option 1
10: select pre-set option 2
11: illegal
==========
VD1_OUT[15]
Config Source Select
0: depends on that configured by VD1_OUT[14:13]
1: on-chip EEPROM (Efuse)
==========

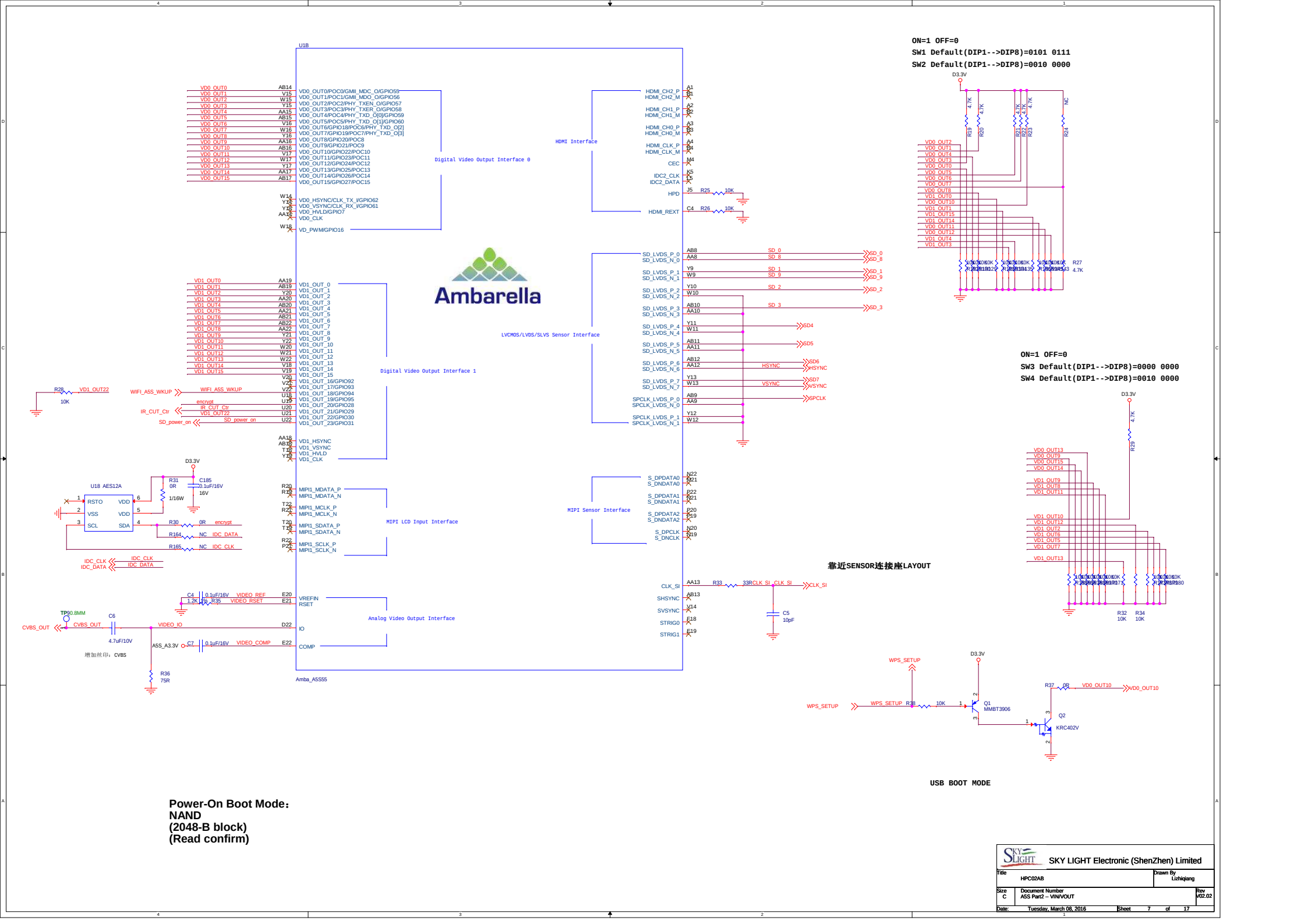
Note：
all GPIO pins(89 Pins) are in Hi-Z state during reset assertion and are initialized to be inputs.

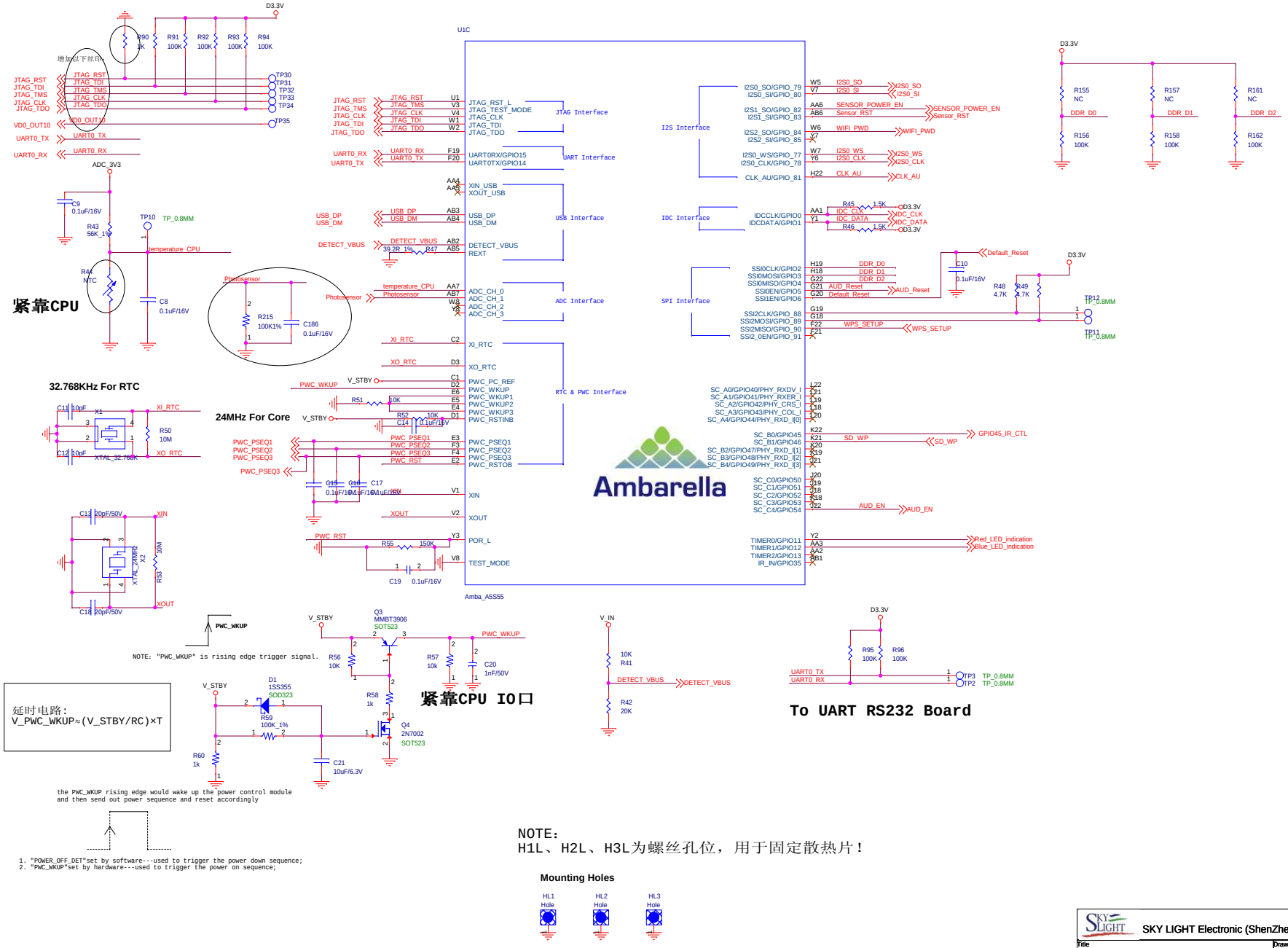
System GPIO Table

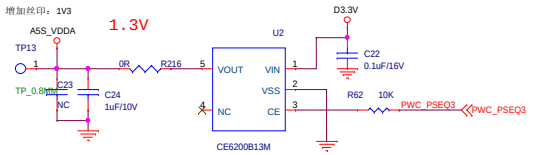
SKY LIGHT Electronic (ShenZhen) Limited			
Title: HPC02AB		Drawn By: Lizhiqiang	
Size: C	Document Number: GPIO Table		Rev: V02.02
Date: Tuesday, March 08, 2016	Sheet 5 of 17		

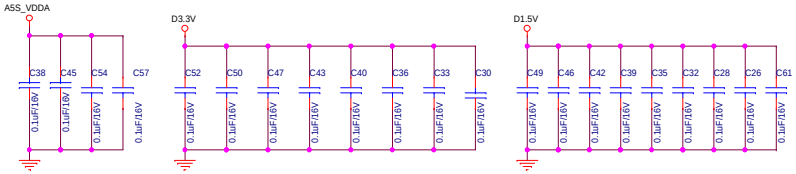


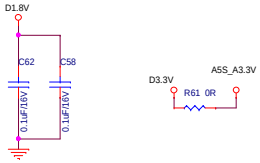
SKY LIGHT Electronic (ShenZhen) Limited			
Title: HPC02AB		Drawn By: Lizhiqiang	
Size: C	Document Number: A5S Part1 -- DDR AND SDIO		Rev: V02.02
Date: Tuesday, March 08, 2016	Sheet 6 of 17		


ON=1 OFF=0
SW1 Default(DIP1-->DIP8)=0101 0111
SW2 Default(DIP1-->DIP8)=0010 0000
ON=1 OFF=0
SW3 Default(DIP1-->DIP8)=0000 0000
SW4 Default(DIP1-->DIP8)=0010 0000
靠近SENSOR连接座LAYOUT
USB BOOT MODE
Power-On Boot Mode:
NAND
(2048-B block)
(Read confirm)
SKY LIGHT Electronic (ShenZhen) Limited
HPC02AB
Lizhiqiang
A5S Part2 – VIN/VOUT
Tuesday, March 08, 2016
Amba_A5S55


D3.3V
U1C
增加以下丝印
JTAG_RST
JTAG_TDI
JTAG_TMS
JTAG_CLK
JTAG_TDO
VDD_OUT10
UART0_TX
UART0_RX
ADC_3V3
紧靠CPU
temperature_CPU
Photosensor
32.768KHz For RTC
24MHz For Core
XI_RTC
XO_RTC
XTAL_32.768K
XTAL_24MHZ
XIN
XOUT
V_STBY
PWC_WKUP
PWC_RST
PWC_PSEQ1
PWC_PSEQ2
PWC_PSEQ3
JTAG Interface
UART Interface
USB Interface
ADC Interface
RTC & PWC Interface
I2S Interface
IDC Interface
SPI Interface
Amba_A5S55
Ambarella
SD_WP
GPIO45_IR_CTL
AUD_Reset
AUD_EN
Default_Reset
WPS_SETUP
Red_LED_indication
Blue_LED_indication
DETECT_VBUS
V_IN
Q3
MMBT3906
SOT523
D1
1SS355
SOD323
Q4
2N7002
SOT523
紧靠CPU IO口
To UART RS232 Board
NOTE: "PWC_WKUP" is rising edge trigger signal.
延时电路:
V_PWC_WKUP≈(V_STBY/RC)×T
the PWC_WKUP rising edge would wake up the power control module
and then send out power sequence and reset accordingly
1. "POWER_OFF_DET"set by software---used to trigger the power down sequence;
2. "PWC_WKUP"set by hardware---used to trigger the power on sequence;
NOTE:
H1L、H2L、H3L为螺丝孔位，用于固定散热片！
Mounting Holes
HL1 Hole
HL2 Hole
HL3 Hole
SKY LIGHT Electronic (ShenZhen) Limited
Title HPC02AB
Drawn By Lizhiqiang
Size C
Document Number A5S Part3 -- IOs
Rev V02.02
Date: Tuesday, March 08, 2016
Sheet 8 of 17



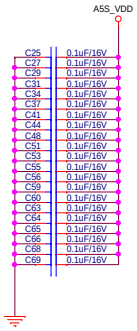




Parameter	Comments	Minimum	Typical	Maximum	Ripple
ADC_AVDD		3.0 V	3.3 V	3.46 V	2%
DAC_AHVDD		3.0 V	3.3 V	3.46 V	2%
DDR_VDDQ	DDR2 Mode	1.7 V	1.8 V	1.9 V	2%
	DDR3 Mode	1.43 V	1.5 V	1.57 V	2%
	LPDDR2 Mode	1.14 V	1.2 V	1.3 V	2%
	LPDDR Mode	1.7 V	1.8 V	1.9 V	2%
HDMI_VDD		1.25 V	1.3 V	1.35 V	2%
HDMI_VDDA		2.375 V	2.5 V	2.625 V	2%
M_VDD11_PLL		VDDA_PLL	VDDA_PLL	VDDA_PLL	2%
MS_VDD18		1.7 V	1.8 V	1.9 V	2%
USB_DVDD		1.15 V	1.2 V	1.25 V	2%
USB_HVDD		3.0 V	3.3 V	3.46 V	2%
USB_VDD25		2.375 V	2.5 V	2.625 V	2%
VDD		1.15 V	1.2 V	1.25 V	2%
VDD33		2.8 V	3.3 V	3.5 V	2%
VDD_BYP		VDD	VDD	VDD	2%
VDD33_BYP		VDD33	VDD33	VDD33	2%
VDDA_LVDS	LVDS Mode	2.375 V	2.5 V	2.625 V	2%
	1.8-V LVCMOS	1.7 V	1.8 V	1.9 V	2%
	2.5-V LVCMOS	2.375 V	2.5 V	2.625 V	2%
	2.8-V LVCMOS	2.7 V	2.8 V	2.9 V	2%
	3.3-V LVCMOS	2.8 V	3.3 V	3.5 V	2%
VDDA_PLL		1.25 V	1.3 V	1.35 V	2%
VDDA18_PLL (VDDA25_PLL ball map)		1.7 V	1.8 V	1.9 V	2%

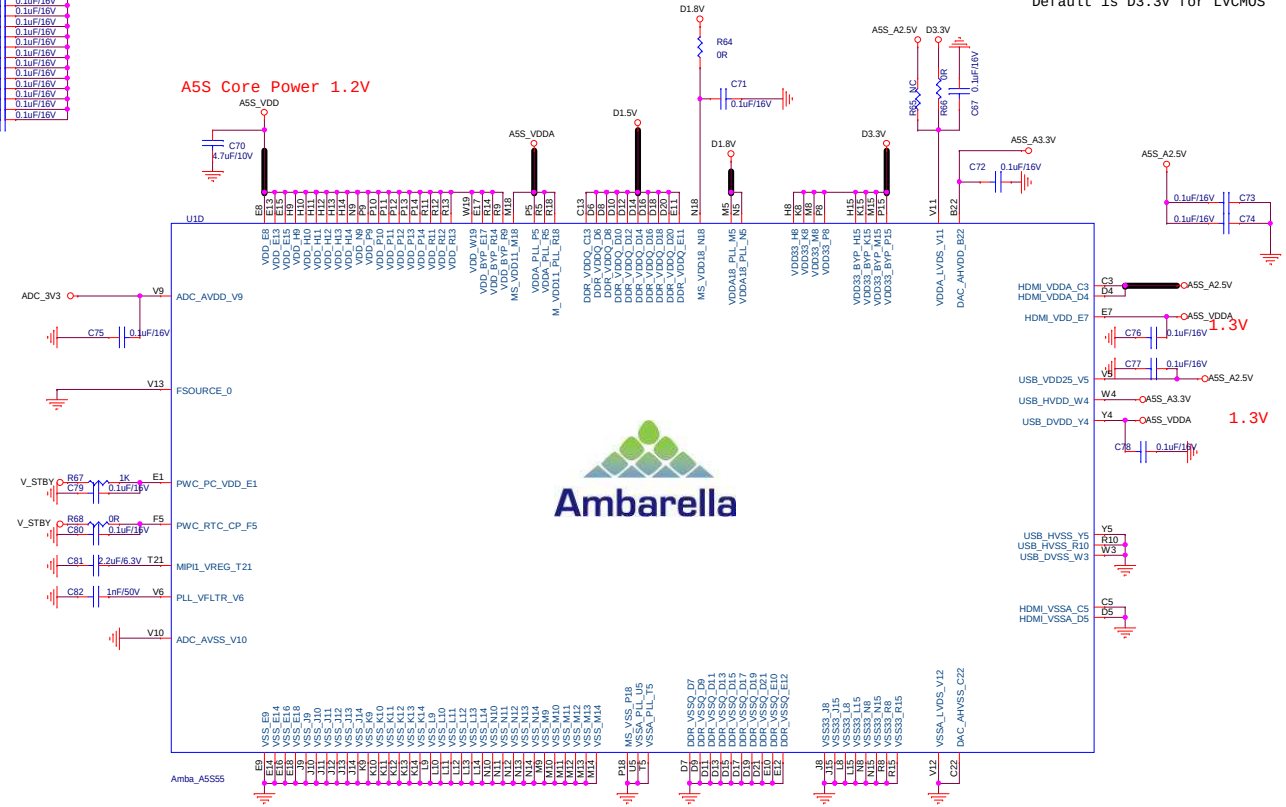
SKYLIGHT.com

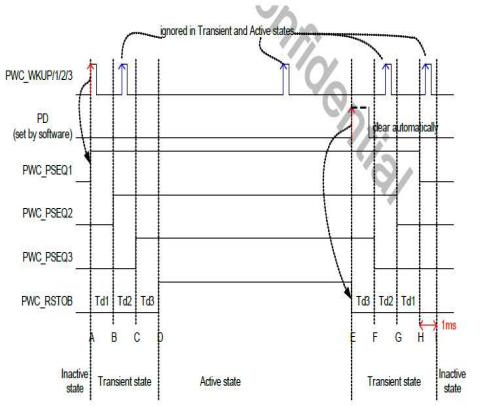
A5S Decoupling Capacitors & LC Filter



Default is D3.3V for LVCMOS

A5S Core Power 1.2V

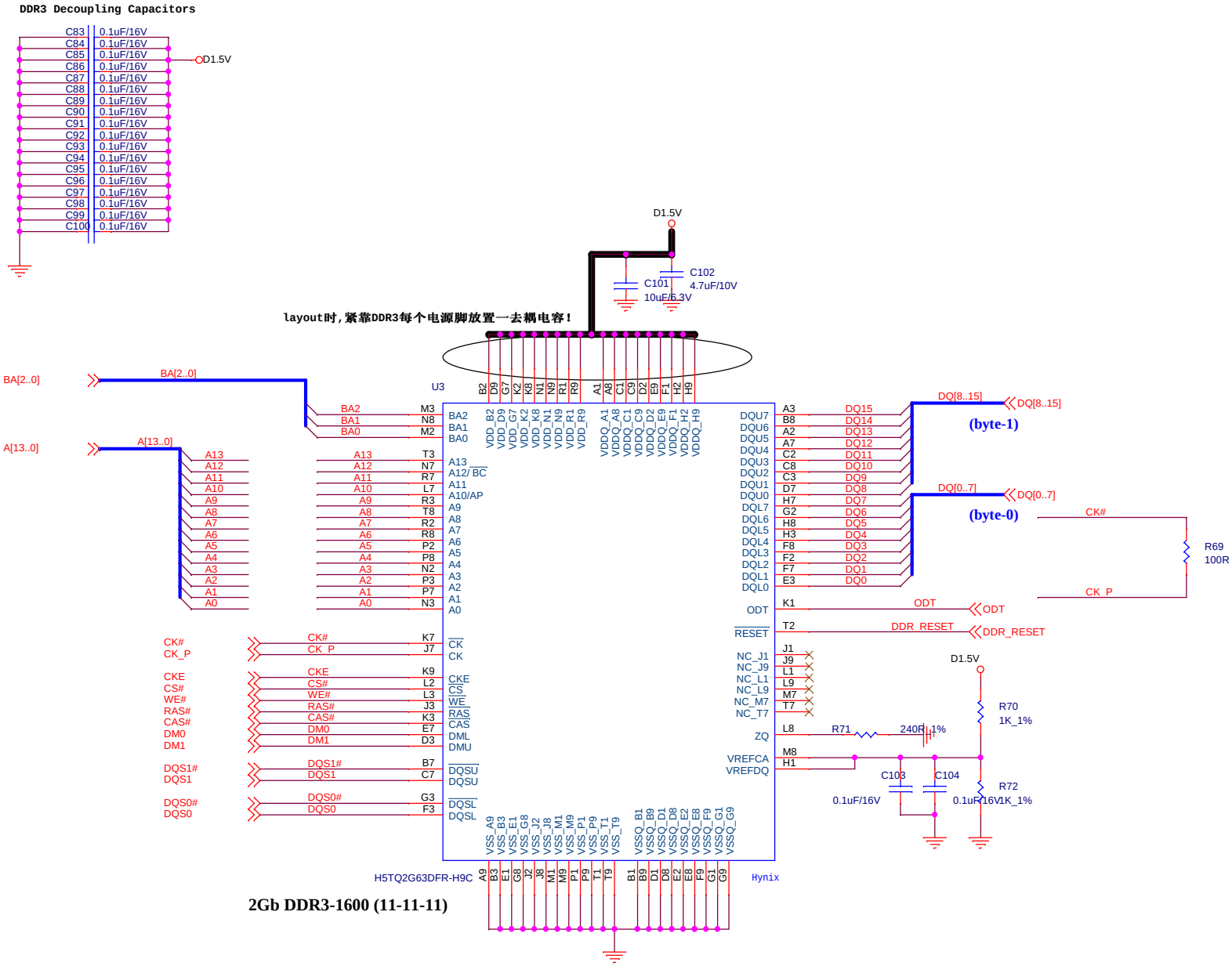




Power On/Off Sequence

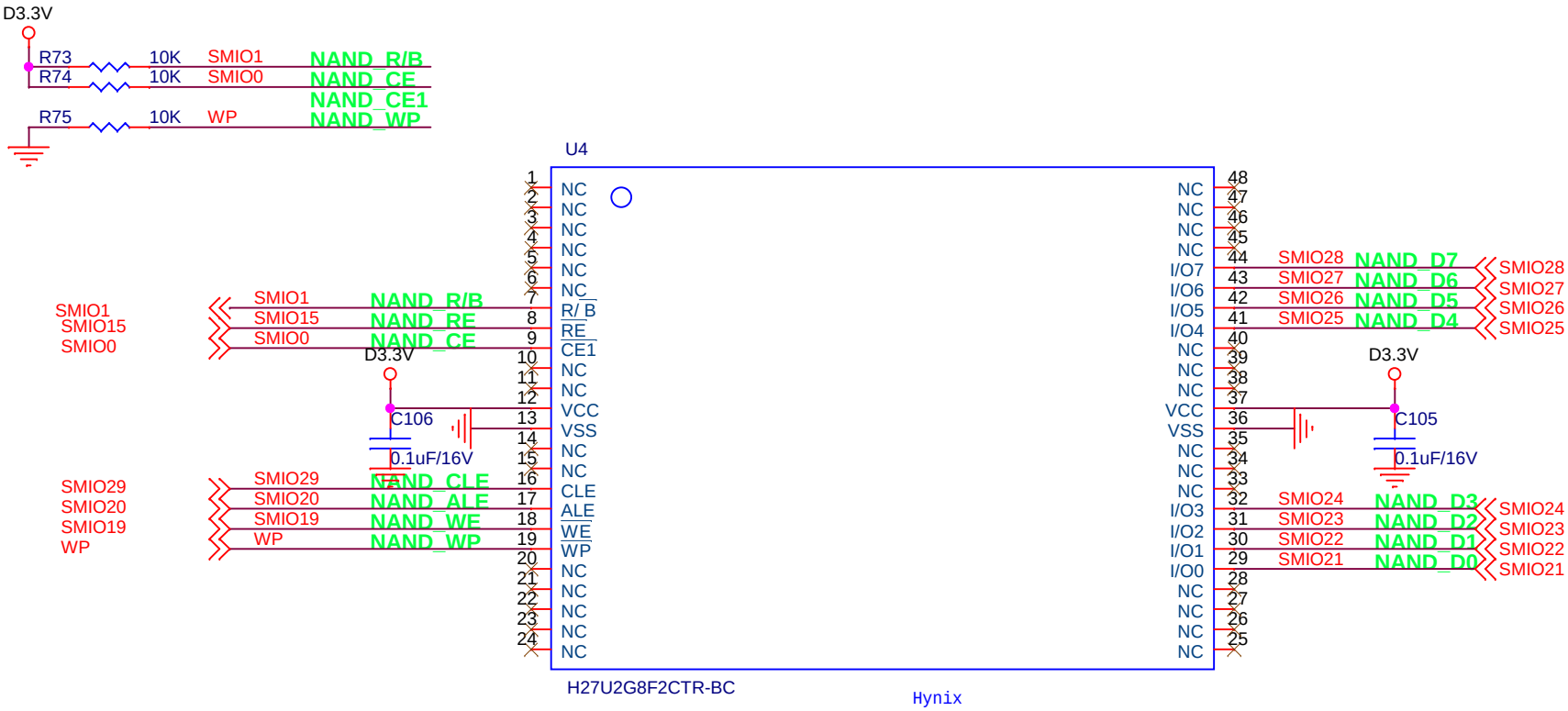
Confidential

SKY LIGHT	SKY LIGHT Electronic (ShenZhen) Limited		
Title: HPC02AB		Drawn By: Lizhiqiang	
Size: C	Document Number: A5S Part4 -- POWER		Rev: V02.02
Date: Tuesday, March 08, 2016	Sheet 9 of 17		



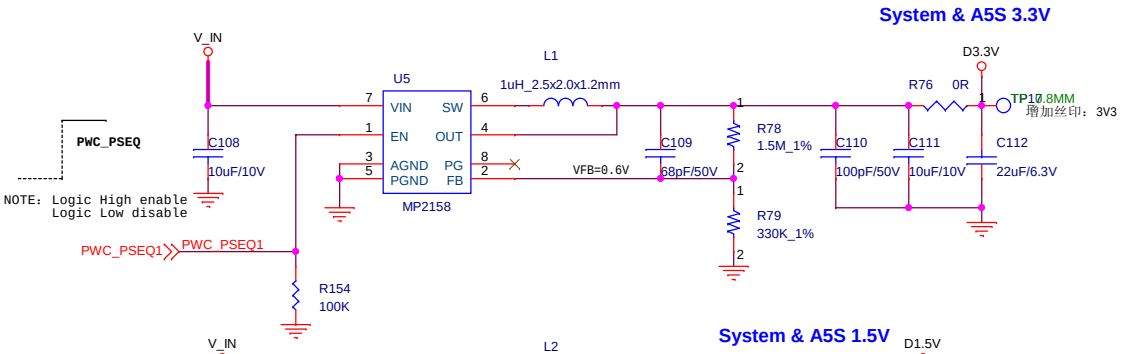
SKY LIGHT Electronic (ShenZhen) Limited

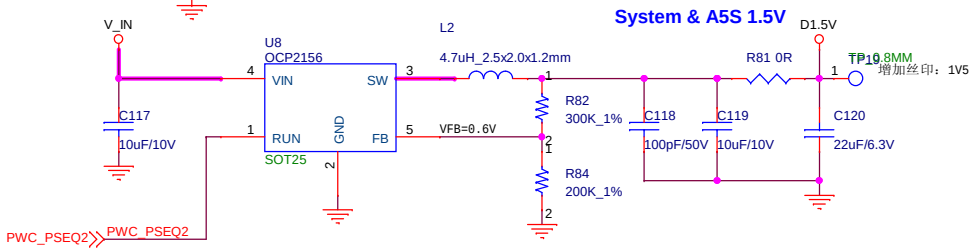
Title: HPC02AB		Drawn By: Lizhiqiang	
Size: B	Document Number: DDRIII-128Mx16		Rev: V02.02
Date: Tuesday, March 08, 2016	Sheet 10 of 17		

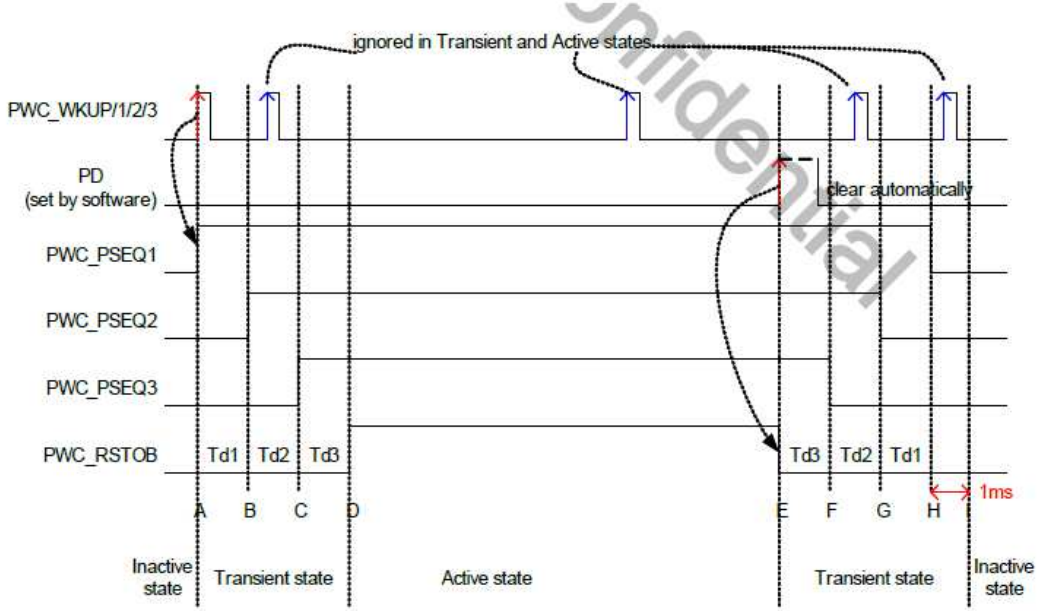


SKY LIGHT Electronic (ShenZhen) Limited

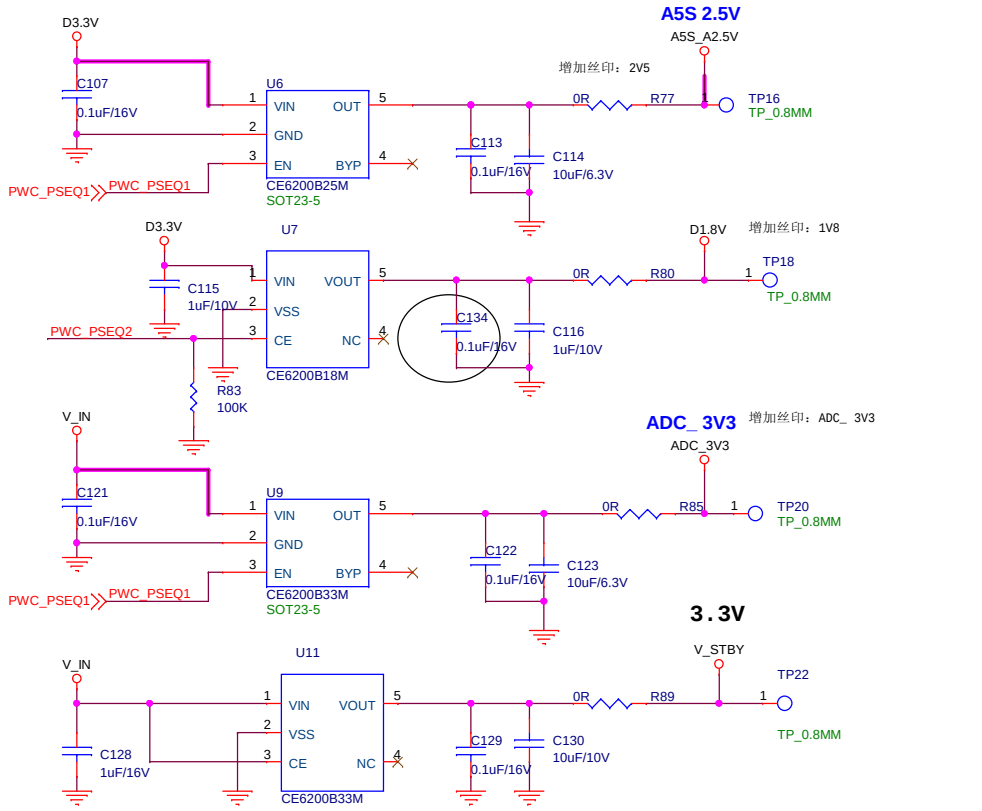
Title: HPC02AB		Drawn By: Lizhiqiang
Size: A	Document Number: FLASH-256Mx8	Rev: V02.02
Date: Tuesday, March 08, 2016	Sheet 11 of 17	



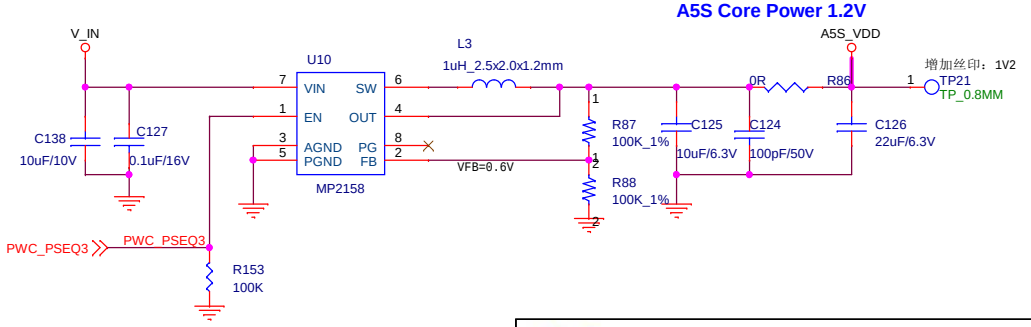




Power On/Off Sequence

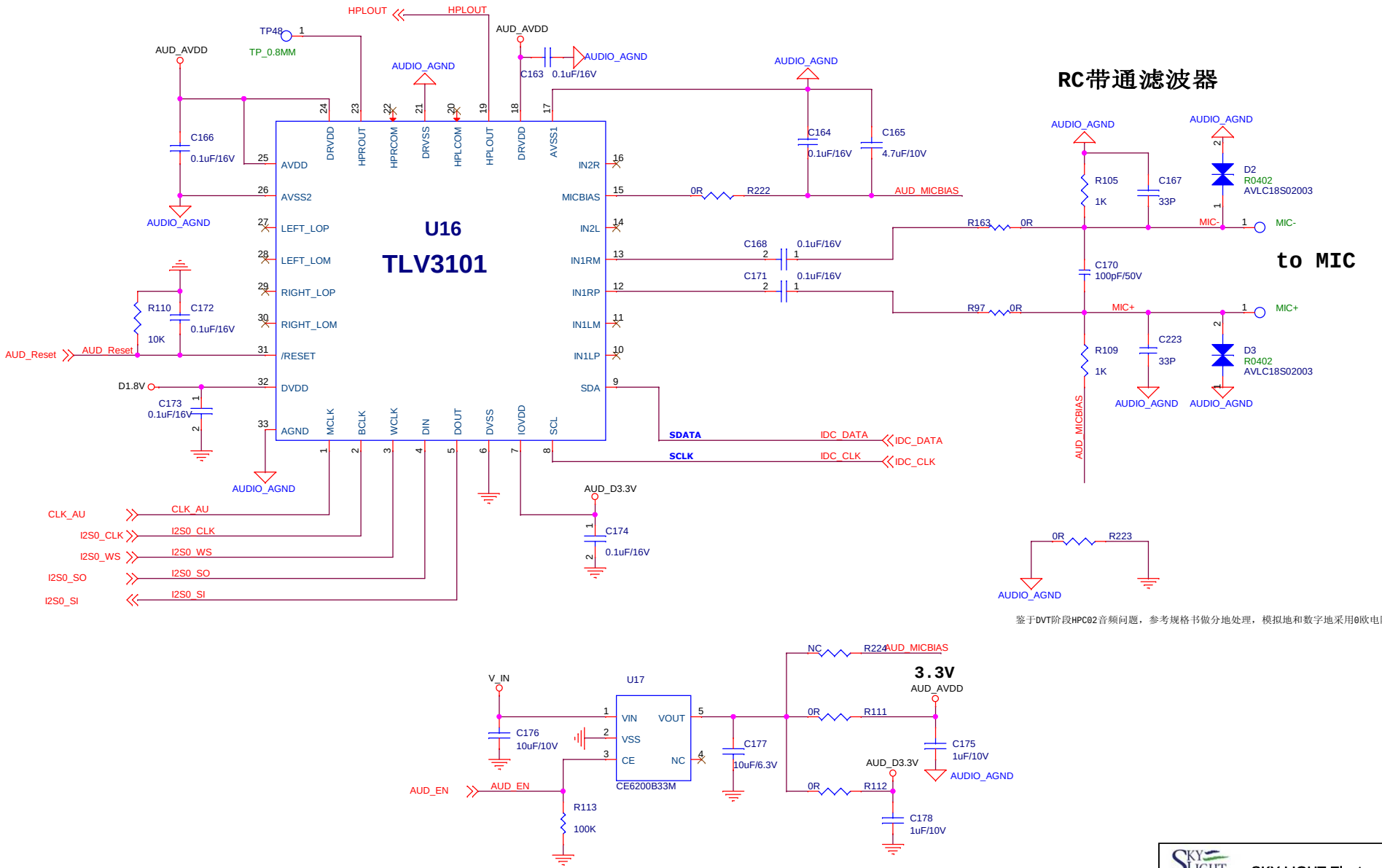


RTC Power Circuit

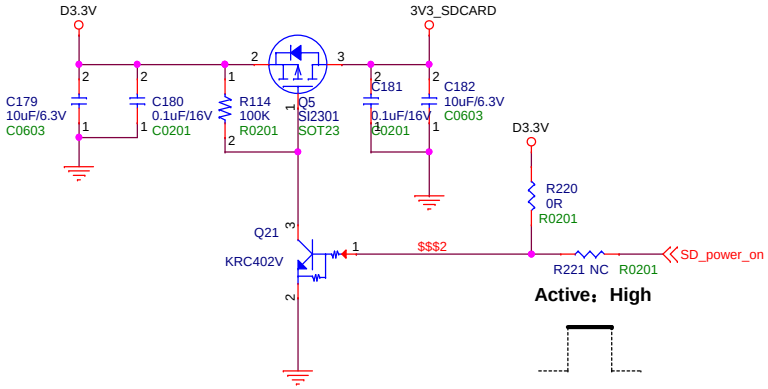


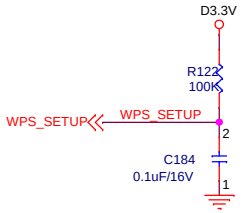
SKY LIGHT Electronic (ShenZhen) Limited		
Title: HPC02AB		Drawn By: Lizhiqiang
Size: B	Document Number: Power manager	Rev: V02.02
Date: Tuesday, March 08, 2016	Sheet 12 of 17	

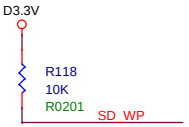
Confidential

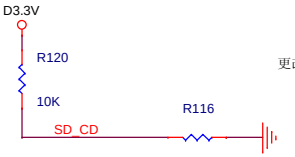


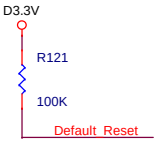
SKY LIGHT Electronic (ShenZhen) Limited			
Title: HPC02AB		Drawn By: Lizhiqiang	
Size: B	Document Number: Audio Codec		Rev: V02.02
Date: Tuesday, March 08, 2016	Sheet 13 of 17		



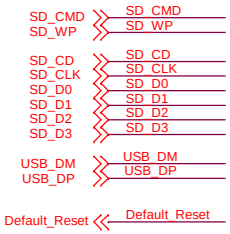


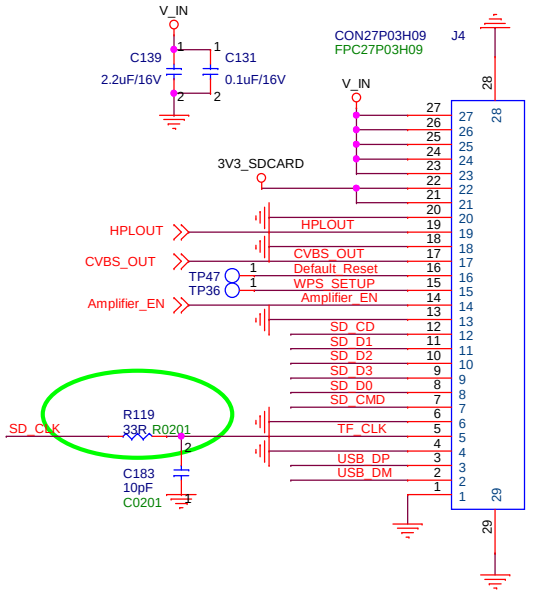






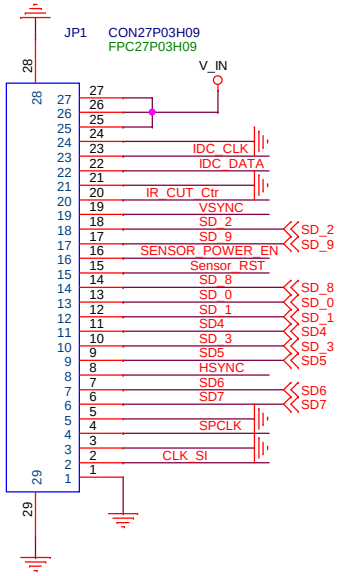
更改SD卡9_PIN CD脚接至SD_CD加上拉20150330

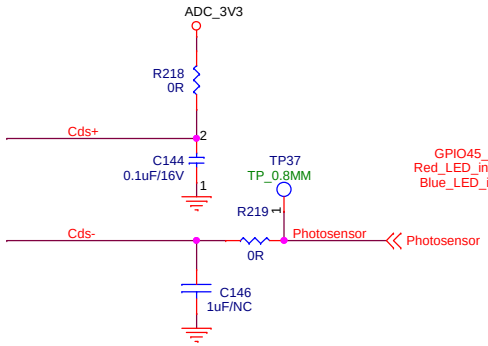


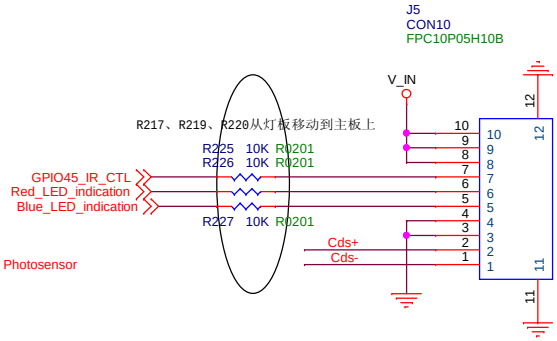


SKY LIGHT Electronic (ShenZhen) Limited

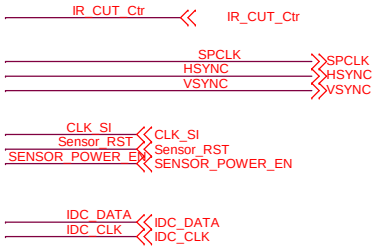
Title: HPC02AB		Drawn By: wangguanming	
Size: B	Document Number: TF Card-Connector		Rev: V02.03
Date: Monday, March 14, 2016	Sheet 14 of 17		







To IRLED Board

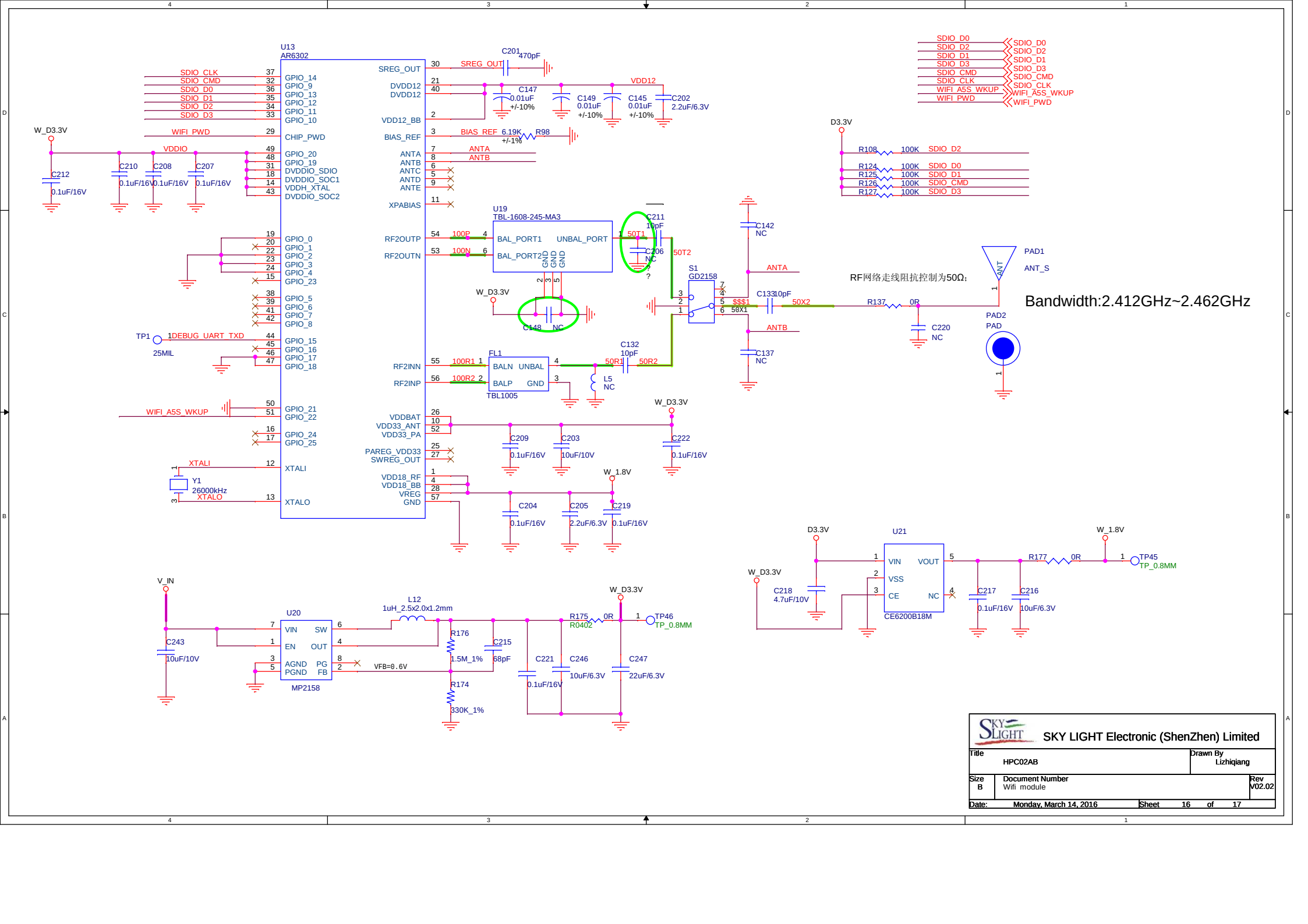


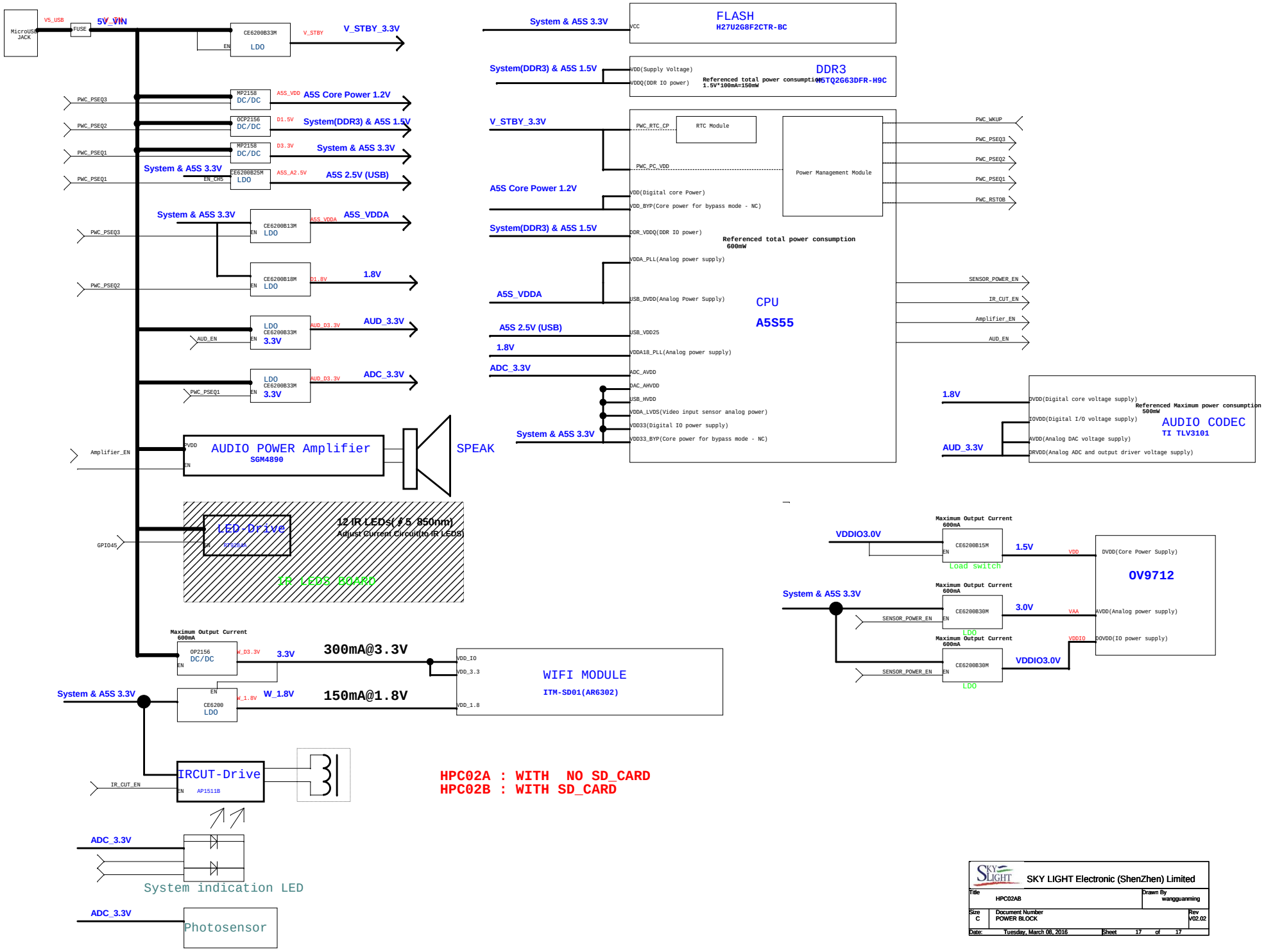
To Sensor Board（FPC座子）

FPC座 27Pin PH0.3

Sensor型号为：OV9712

Sky Light Electronic (Shen Zhen) Limited		
Title: HPC02AB		Drawn By: wangguanming
Size: B	Document Number: Sensor-OV9712	Rev: V02.02
Date: Tuesday, March 08, 2016	Sheet 15 of 17	


U13
AR6302
SDIO_CLK
SDIO_CMD
SDIO_D0
SDIO_D1
SDIO_D2
SDIO_D3
WIFI_PWD
VDDIO
W_D3.3V
C212
0.1uF/16V
C210
0.1uF/16V
C208
0.1uF/16V
C207
0.1uF/16V
GPIO_14
GPIO_9
GPIO_13
GPIO_12
GPIO_11
GPIO_10
CHIP_PWD
GPIO_20
GPIO_19
DVDDIO_SDIO
DVDDIO_SOC1
VDDH_XTAL
DVDDIO_SOC2
GPIO_0
GPIO_1
GPIO_2
GPIO_3
GPIO_4
GPIO_23
GPIO_5
GPIO_6
GPIO_7
GPIO_8
TP1
25MIL
DEBUG_UART_TXD
GPIO_15
GPIO_16
GPIO_17
GPIO_18
WIFI_A5S_WKUP
GPIO_21
GPIO_22
GPIO_24
GPIO_25
XTALI
Y1
26000kHz
XTALO
XTALI
XTALO
SREG_OUT
DVDD12
DVDD12
VDD12_BB
BIAS_REF
ANTA
ANTB
ANTC
ANTD
ANTE
XPABIAS
RF2OUTP
RF2OUTN
RF2INN
RF2INP
VDDBAT
VDD33_ANT
VDD33_PA
PAREG_VDD33
SWREG_OUT
VDD18_RF
VDD18_BB
VREG
GND
C201
470pF
C147
0.01uF
+/-10%
C149
0.01uF
+/-10%
C145
0.01uF
+/-10%
C202
2.2uF/6.3V
VDD12
BIAS_REF
6.19K
+/-1%
R98
ANTA
ANTB
100P
100N
U19
TBL-1608-245-MA3
BAL_PORT1
UNBAL_PORT
BAL_PORT2
GND
GND
GND
C211
10pF
C206
NC
50T1
50T2
C148
NC
W_D3.3V
S1
GD2158
$$$1
50X1
C142
NC
ANTA
ANTB
C137
NC
C133
10pF
50X2
RF网络走线阻抗控制为50Ω;
R137
0R
C220
NC
PAD1
ANT_S
PAD2
PAD
Bandwidth:2.412GHz~2.462GHz
100R1
100R2
FL1
BALN
UNBAL
BALP
GND
TBL1005
C132
10pF
50R1
50R2
L5
NC
C209
0.1uF/16V
C203
10uF/10V
C222
0.1uF/16V
W_1.8V
C204
0.1uF/16V
C205
2.2uF/6.3V
C219
0.1uF/16V
SDIO_D0
SDIO_D2
SDIO_D1
SDIO_D3
SDIO_CMD
SDIO_CLK
WIFI_A5S_WKUP
WIFI_PWD
D3.3V
R108
100K
R124
100K
R125
100K
R126
100K
R127
100K
U21
VIN
VOUT
VSS
CE
NC
CE6200B18M
C218
4.7uF/10V
C217
0.1uF/16V
C216
10uF/6.3V
R177
0R
TP45
TP_0.8MM
V_IN
U20
VIN
SW
EN
OUT
AGND
PGND
PG
FB
MP2158
C243
10uF/10V
L12
1uH_2.5x2.0x1.2mm
R176
1.5M_1%
C215
68pF
R174
330K_1%
VFB=0.6V
C221
0.1uF/16V
C246
10uF/6.3V
C247
22uF/6.3V
R175
0R
R0402
TP46
TP_0.8MM
SKY LIGHT Electronic (ShenZhen) Limited
Title
HPC02AB
Drawn By
Lizhiqiang
Size
B
Document Number
Wifi module
Rev
V02.02
Date:
Monday, March 14, 2016
Sheet
16
of
17



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Title: HPC02AB		Drawn By: wangguanming	
Size: C	Document Number: POWER BLOCK		Rev: V02.02
Date: Tuesday, March 08, 2016	Sheet 17 of 17		