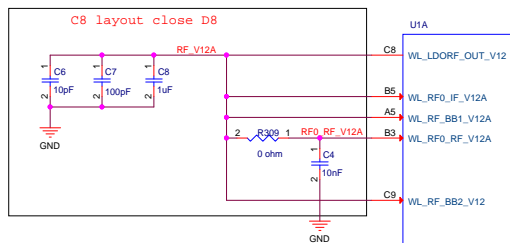
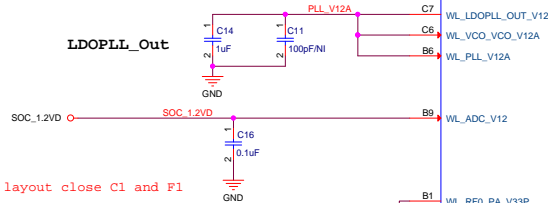


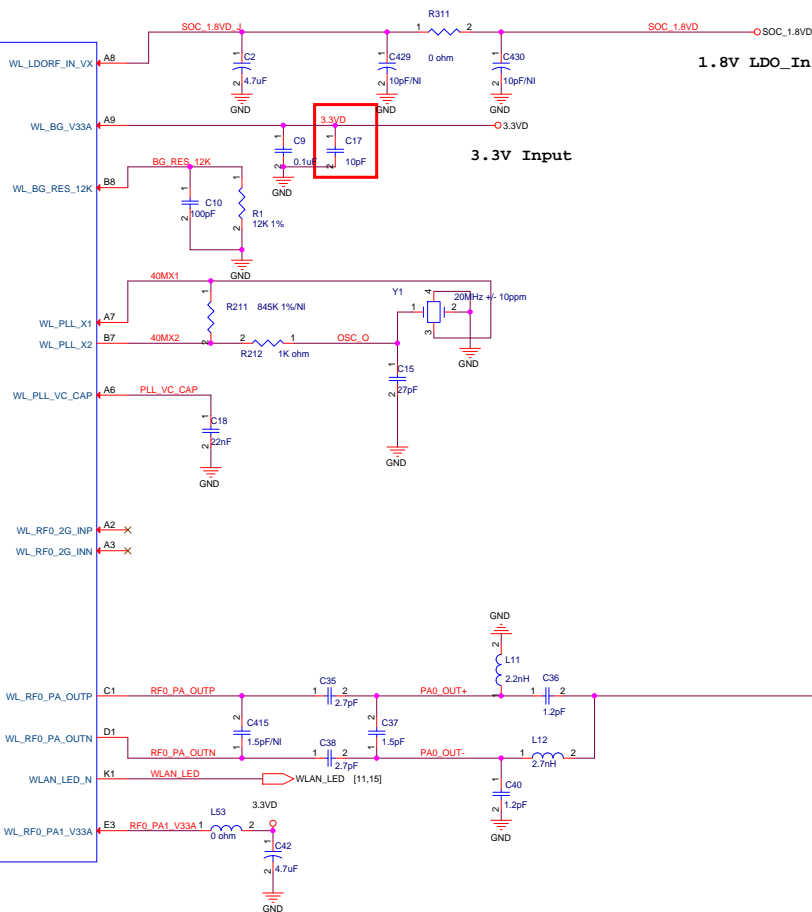
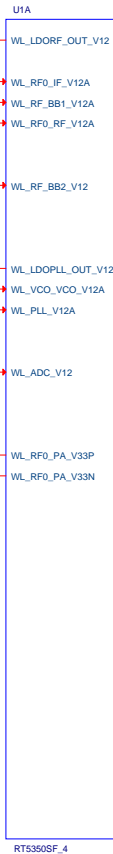
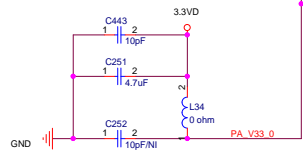
LDORF\_Out

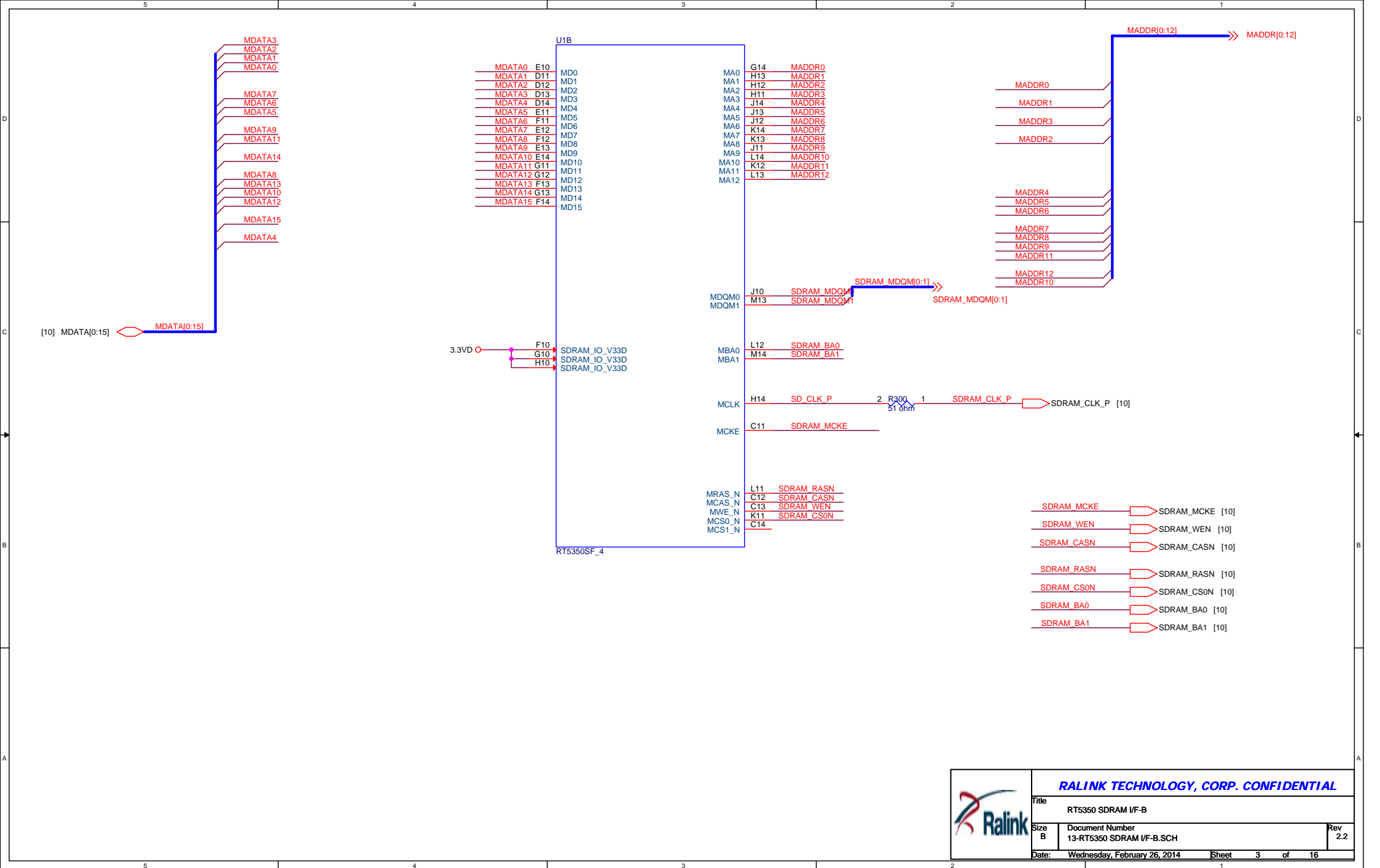


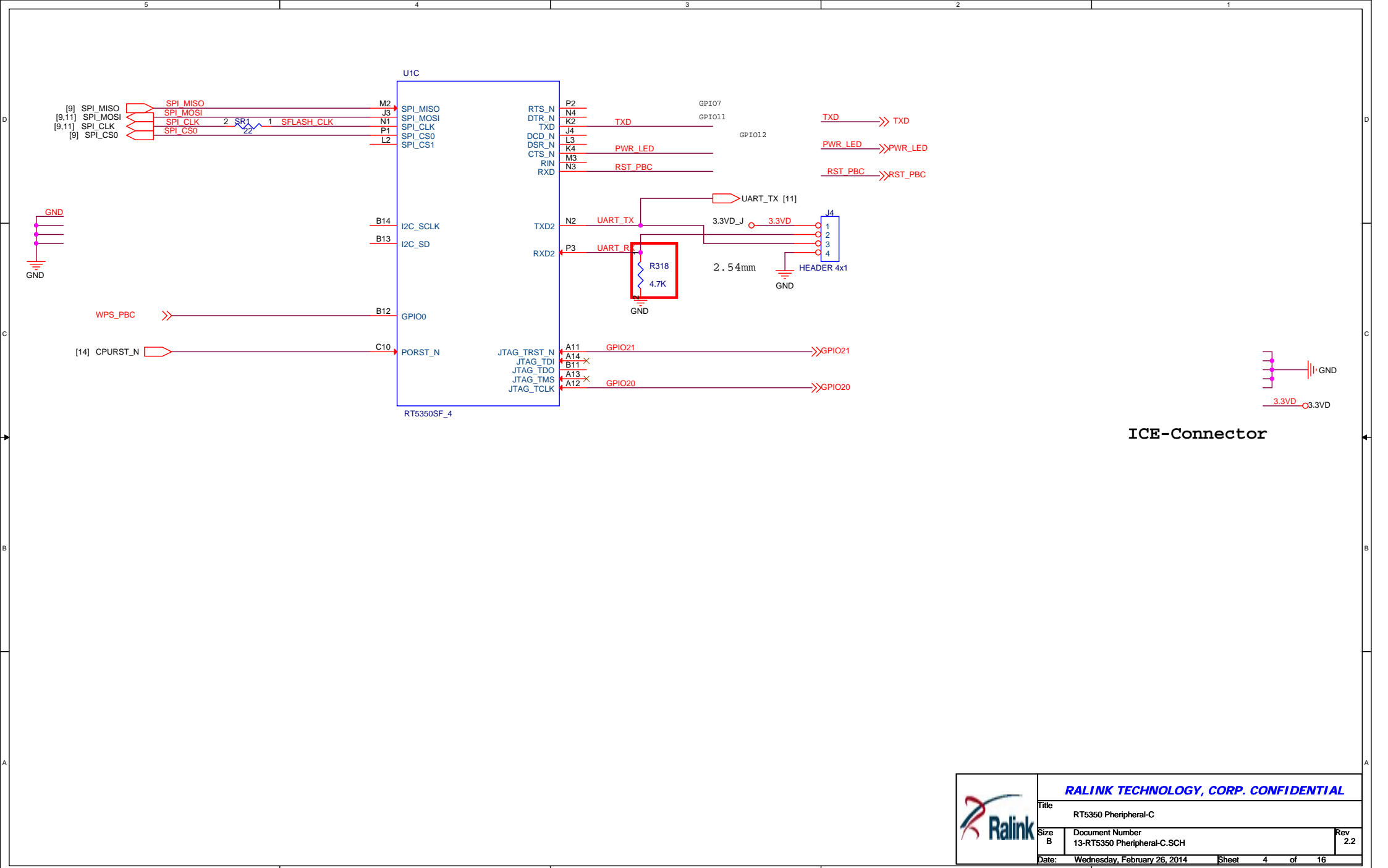
LDOPLL\_Out

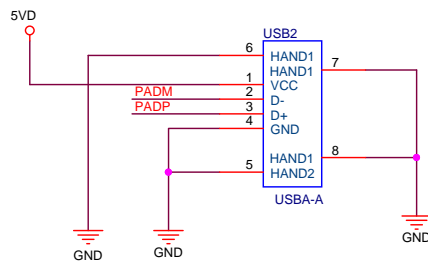
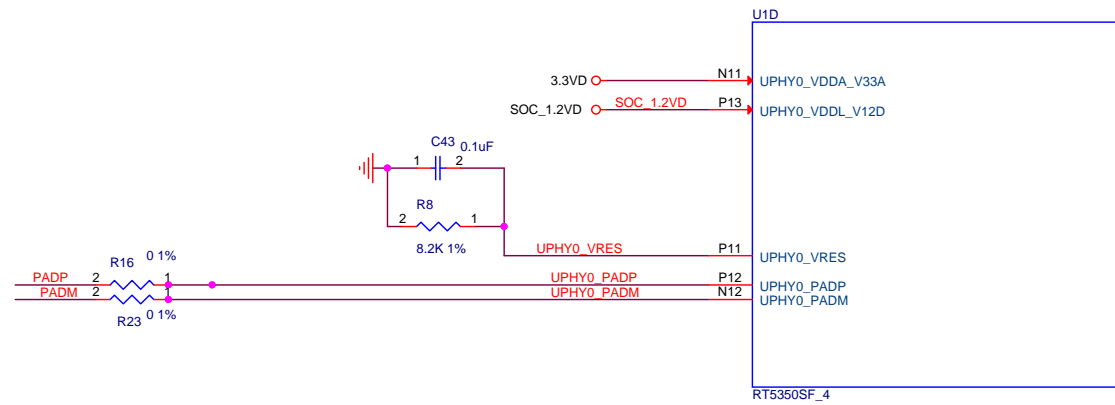


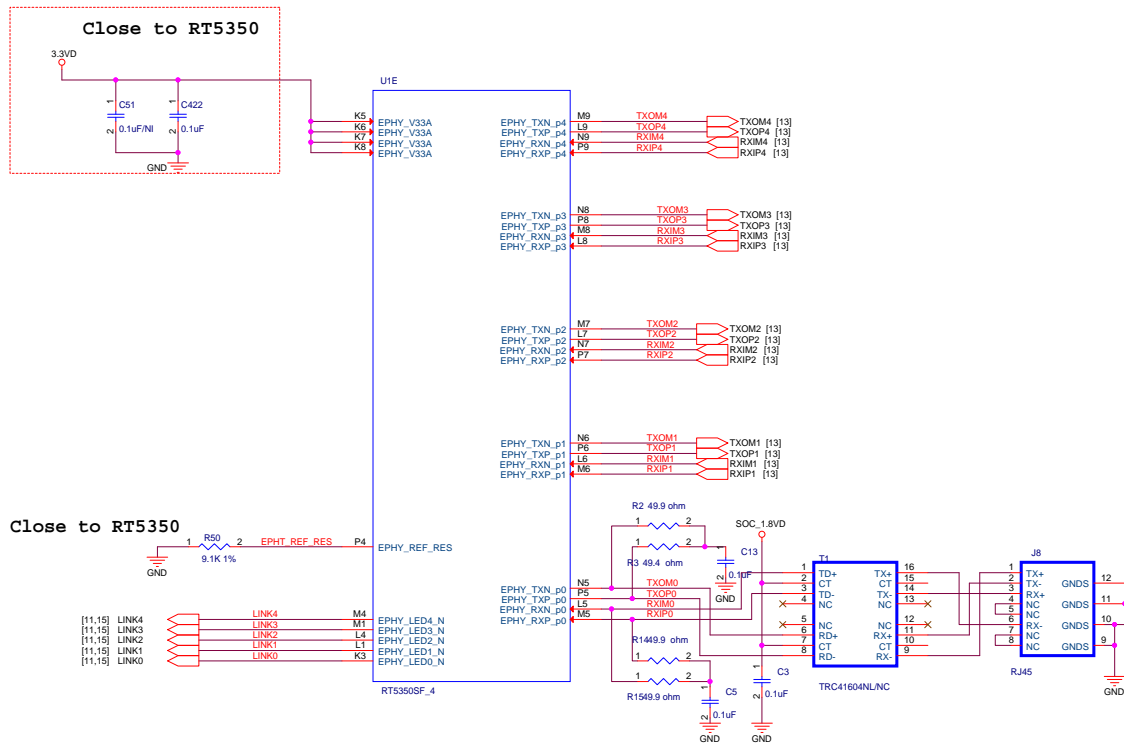
L34 ,C252 layout close C1 and F1

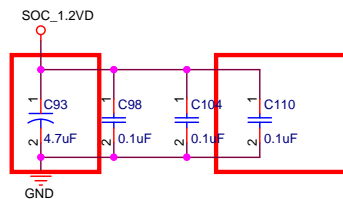
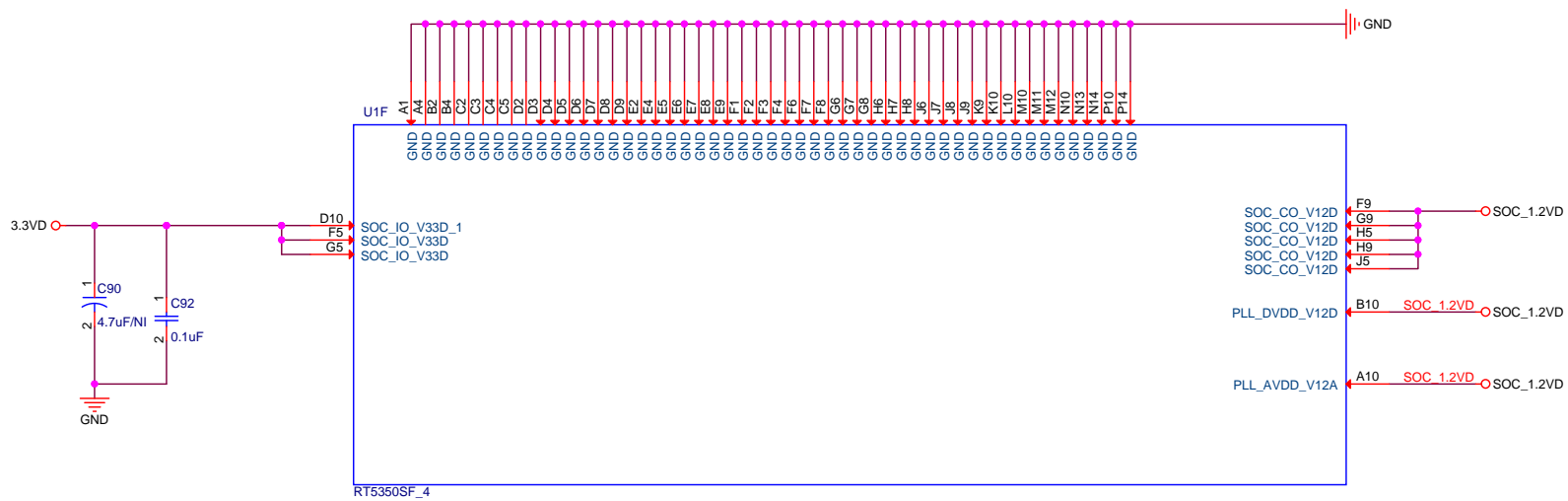


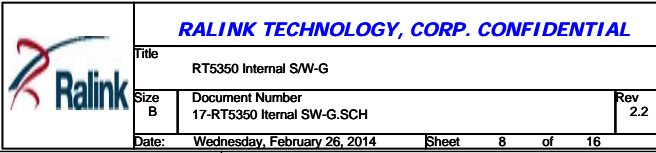


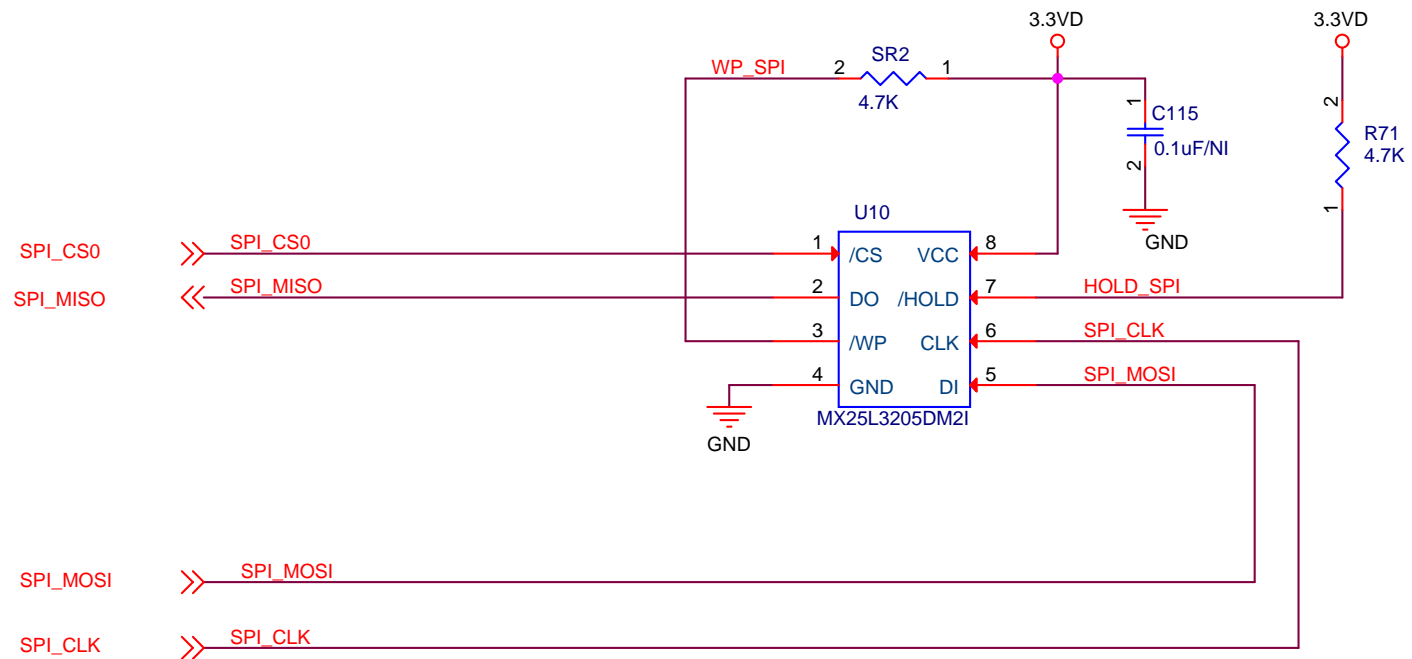









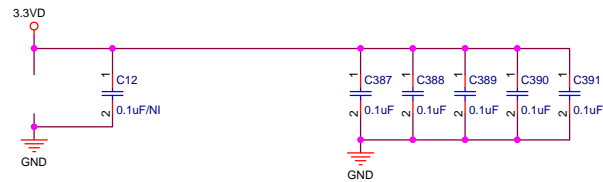
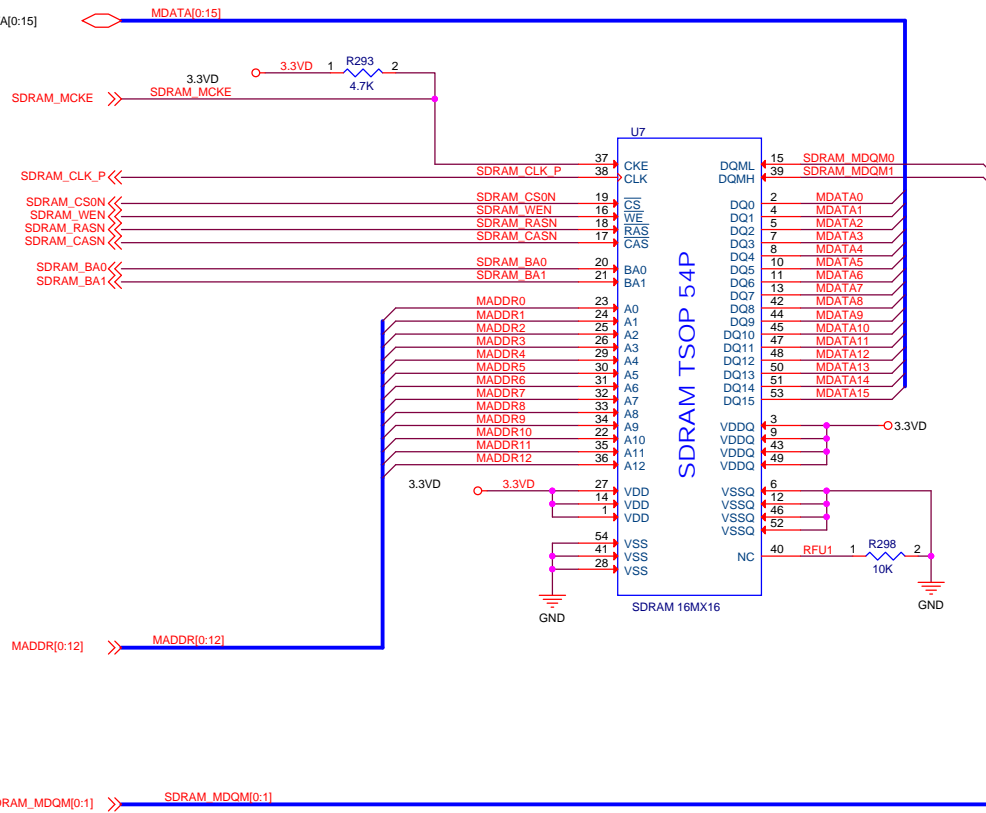


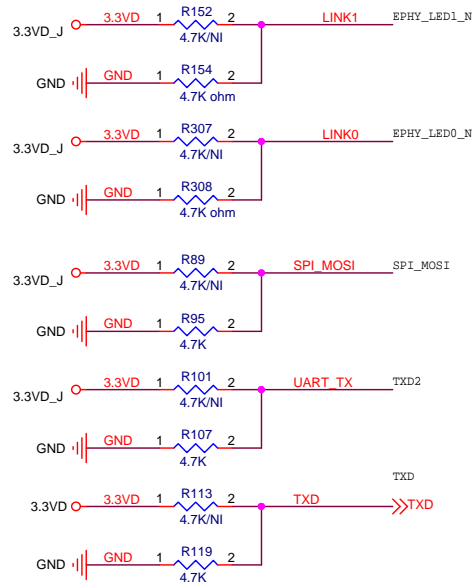
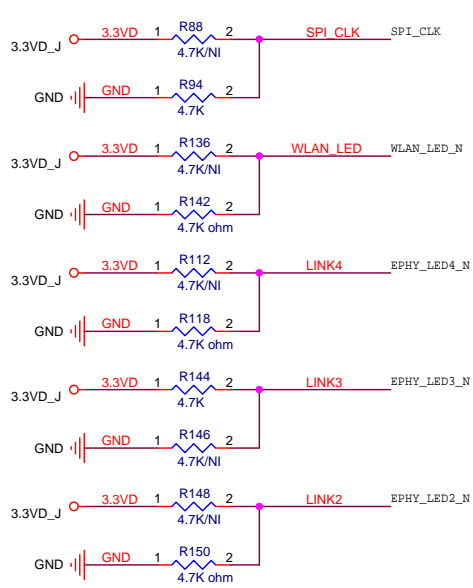
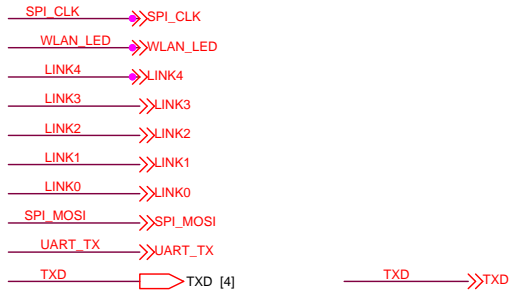


		<b>RALINK TECHNOLOGY, CORP. CONFIDENTIAL</b>	
		Title SPI Flash	
Size A	Document Number 21-SPI Flash.SCH		Rev 2.2
Date: Wednesday, February 26, 2014		Sheet	9 of 16



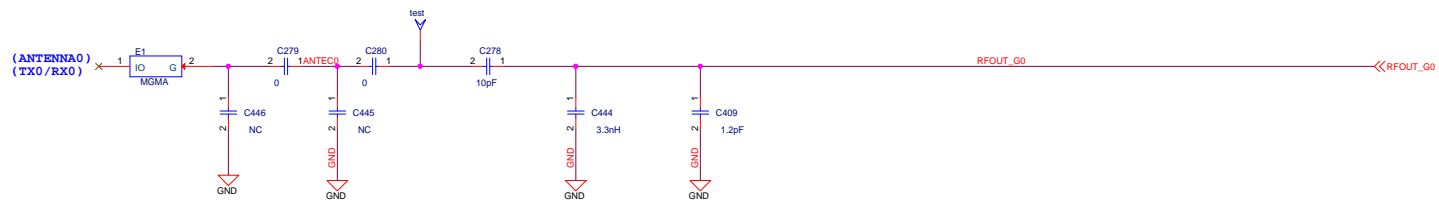
[3] MDATA[0:15]

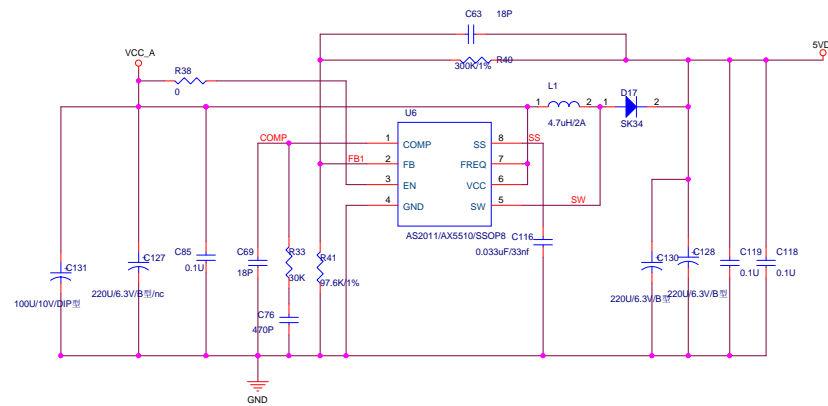
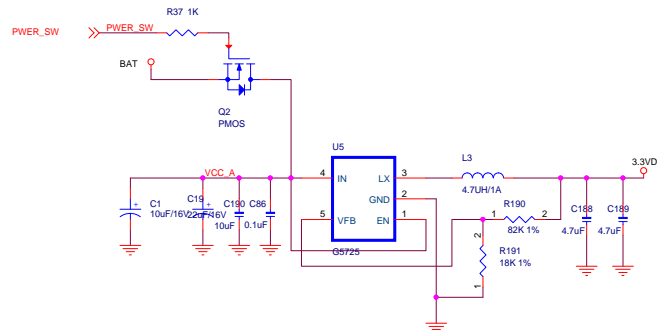
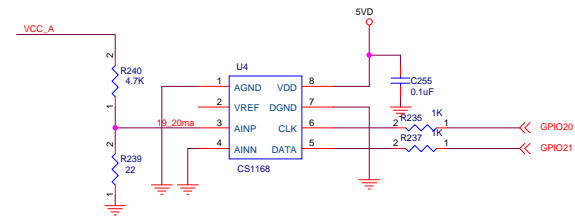
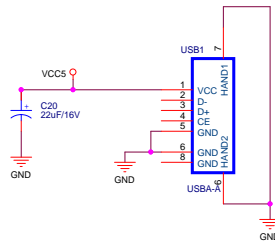




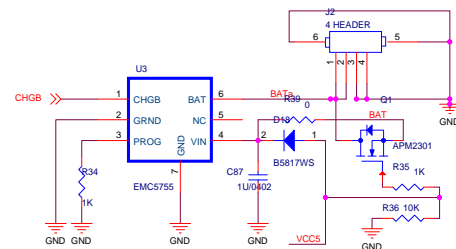
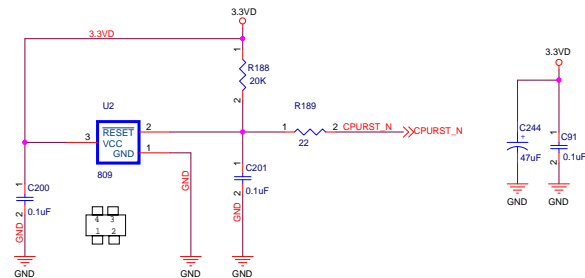
## RT5350 Boot Up Strapping

Pin Name	Description	Value=0	Value=1
SPI_CLK	XTAL_FREQ_HI	20MHz	40MHz
WLAN_LED_N	Big Endian	Little Endian	Big Endian
EPHY_LED4_N	DRAM_FROM_EE	from boot strapping	from EEPROM
{EPHY_LED3_N, EPHT_LED2_N}	DRAM_SIZE	INIC/AP(SDR) 0: 2MB/8MB 1: 8MB/16MB <b>2: 16MB/32MB</b> 3: 32MB/64MB	
{EPHY_LED1_N, EPHT_LED0_N}	CPU_CLK_SEL	CPU clock select <b>0: 360MHz</b> 1: Reserved 2: 320MHz 3: 300MHz	
{SPI_MOSI, TXD2, TXD}	CHIP_MODE[2:0]	A vector to set chip function/test/debug modes <b>0 : Normal mode(boot from SPI serial flash)</b> 1 : iNIC-USB mode 2 : Reserved 3 : Reserved 4 : Reserved 5 : iNIC-PHY mode 6 : SCAN mode 7 : TEST/DEBUG mode	

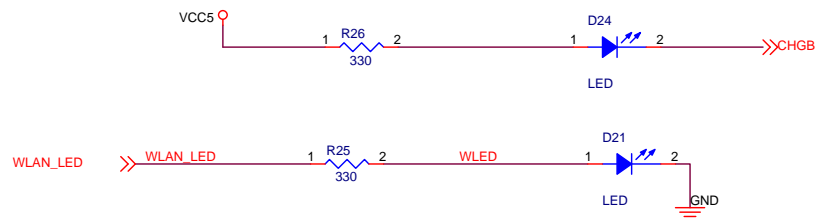




## Reset Circuit



GPIO13



Wireless ACT LED

GPIO9



System/Power LED

WAN Port LED

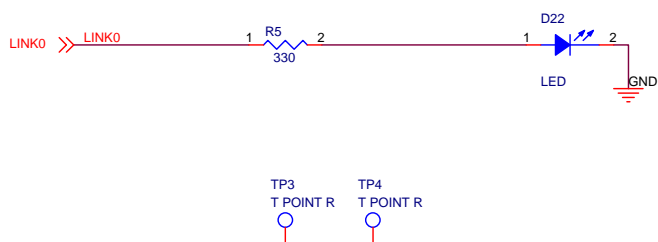
LAN3 Port LED GPIO0

LAN2 Port LED

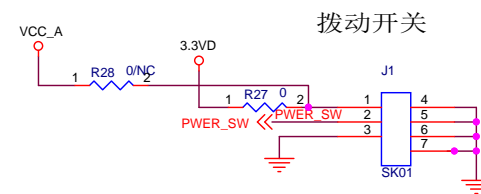
LAN1 Port LED

LAN0 Port LED

GPIO14

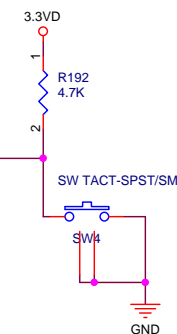


GPIO10

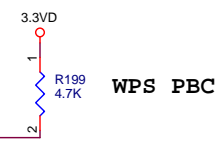



RST\_PBC

Software Reset/  
Factory Default



WPS\_PBC



		<b><i>RALINK TECHNOLOGY, CORP. CONFIDENTIAL</i></b>			
		Title LED			
Size B	Document Number 6-LED.SCH			Rev 2.2	
	Date: Wednesday, February 26, 2014			Sheet 15 of 16	

