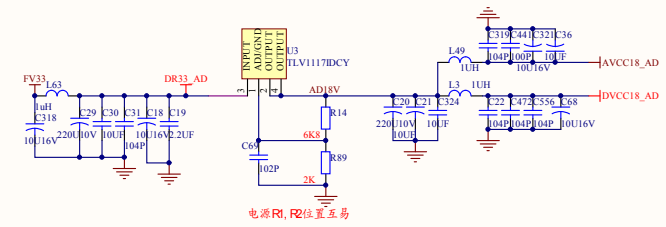
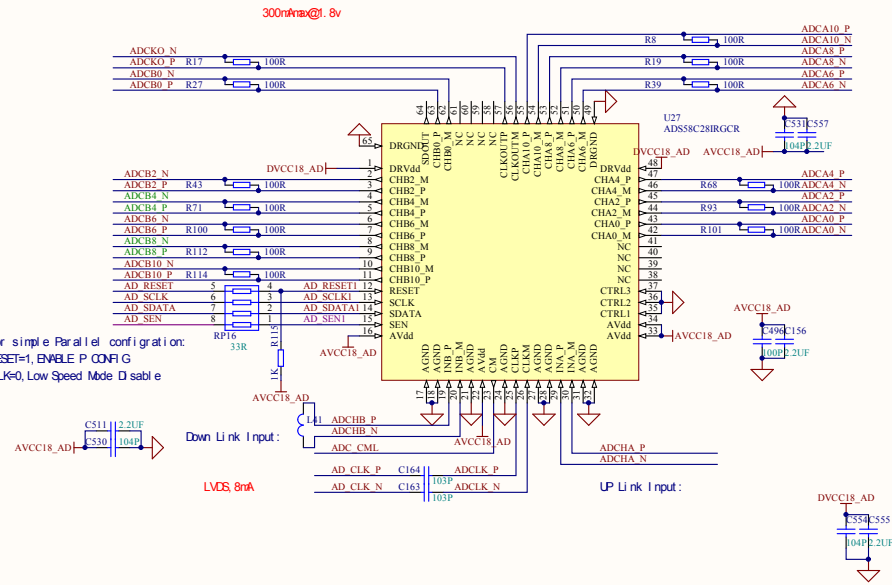
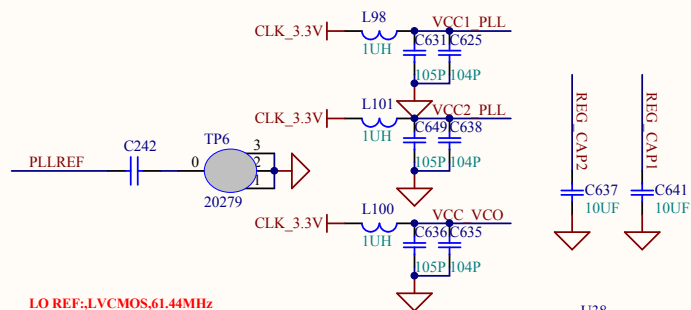


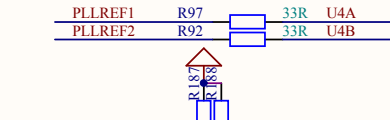
For simple Parallel configuration:
RESET=1, ENABLE P CONFIG
SCLK=0, Low Speed Mode Disable



Title		
TD_PICO_v2.1		
Size	Number	Revision
A4		v2.1
Date:	3/6/2015	Sheet of
File:	D:\v5_ADC_SchDoc	Drawn By: Timba.Ye



LO REF: LVCMOS, 61.44MHz



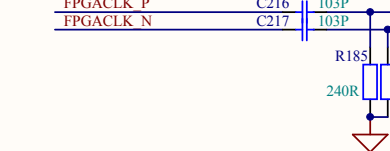
ADC: 122.88MHz: LVDS



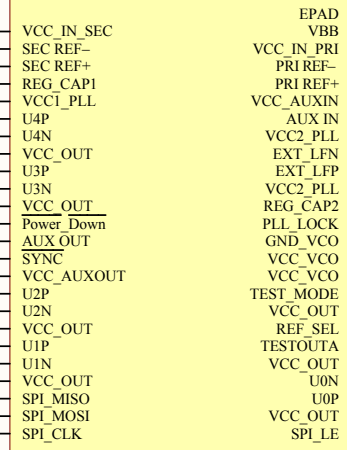
DAC: 122.88MHz: LVPECL



FPGA: 122.88MHz: LVPECL

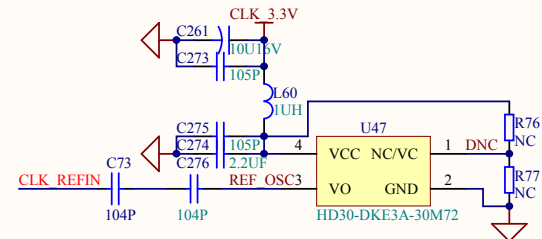
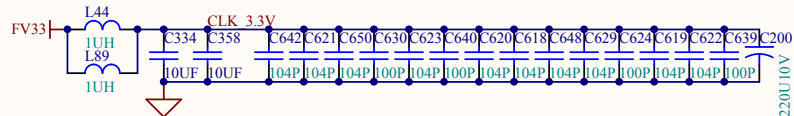


U38

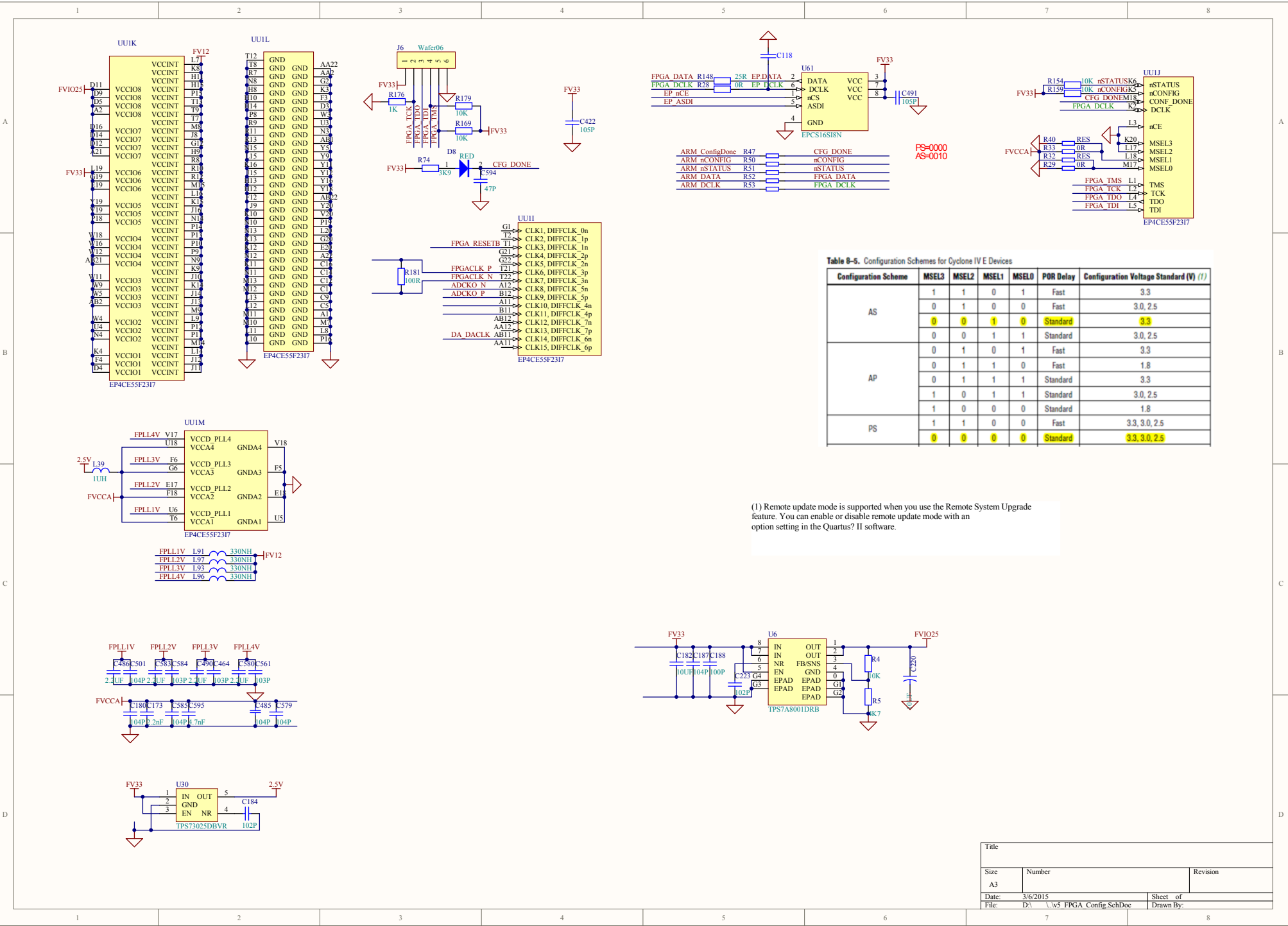


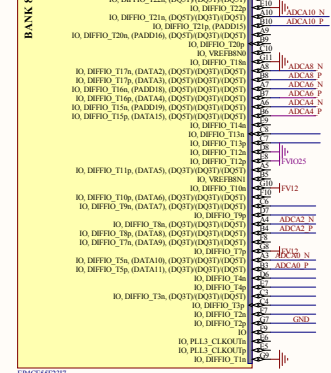
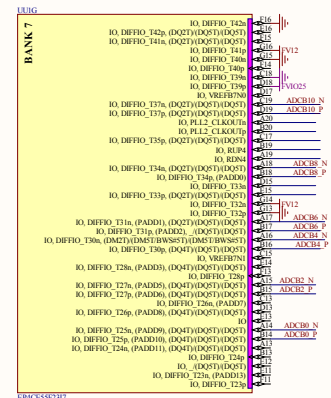
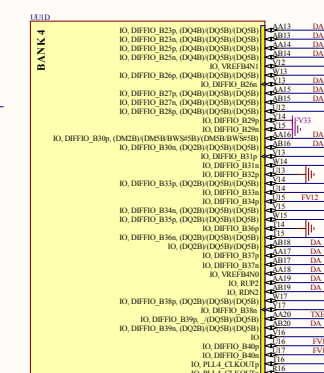
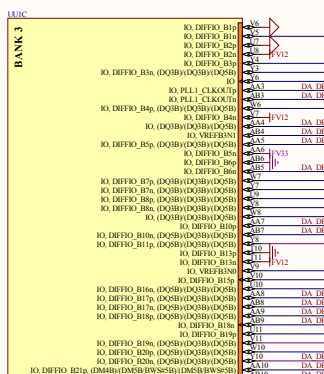
CDCE62005RGZ

CLK LE1
CLK CLK1
CLK MOSI
CLK MISO1



Title			DigPico v1.0_CLK	
Size	Number		Revision	
A4			v1.0	
Date:	3/6/2015		Sheet of	Timbo.Ye
File:	D:\...v5_CLK.SchDoc		Drawn By:	





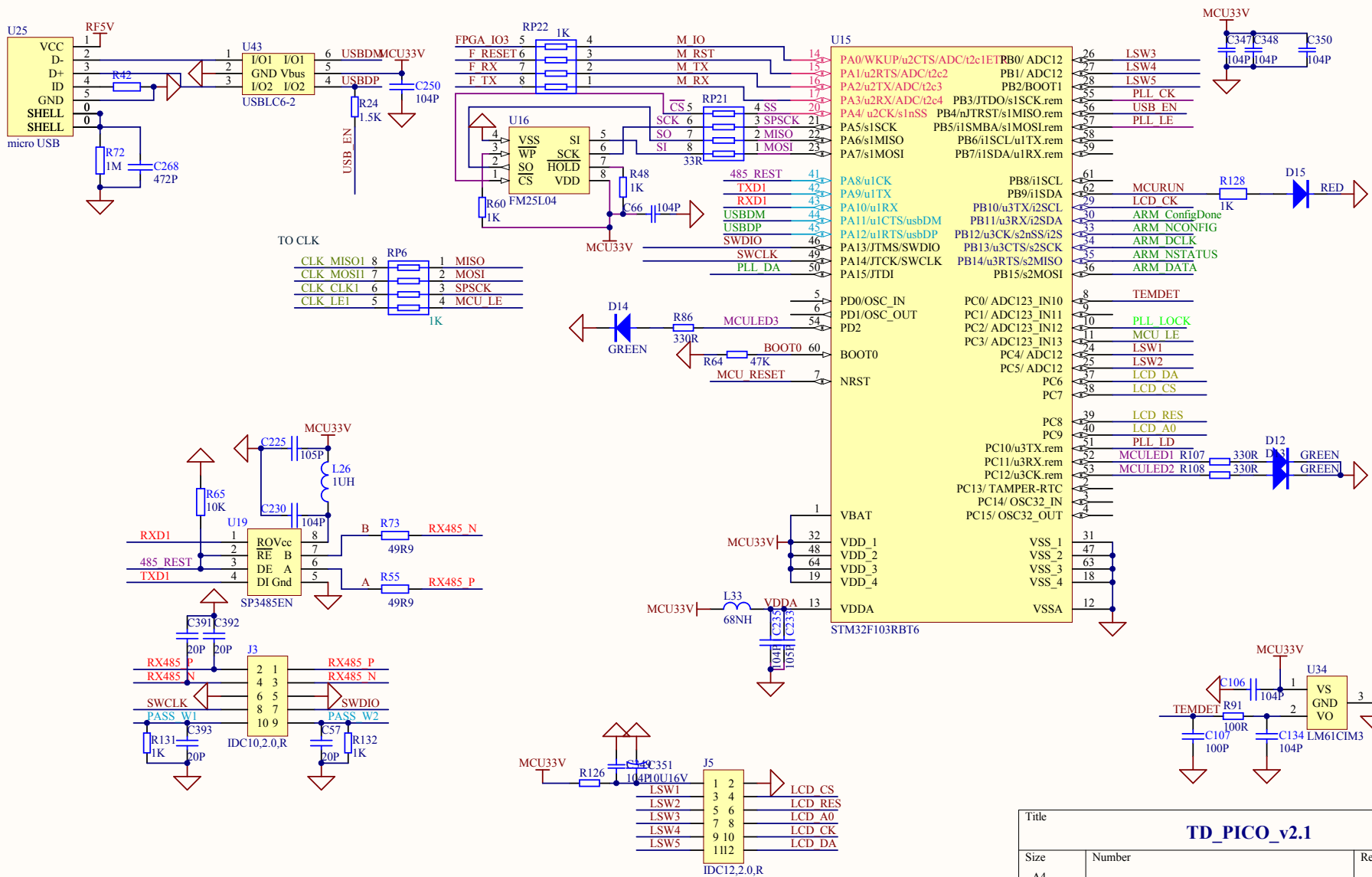
Title	
Size A2	Revision
Date 3/6/2015	Sheet of
File D:\3\3-5_FPGAlonSchDoc	Drawn By:

1

2

3

4



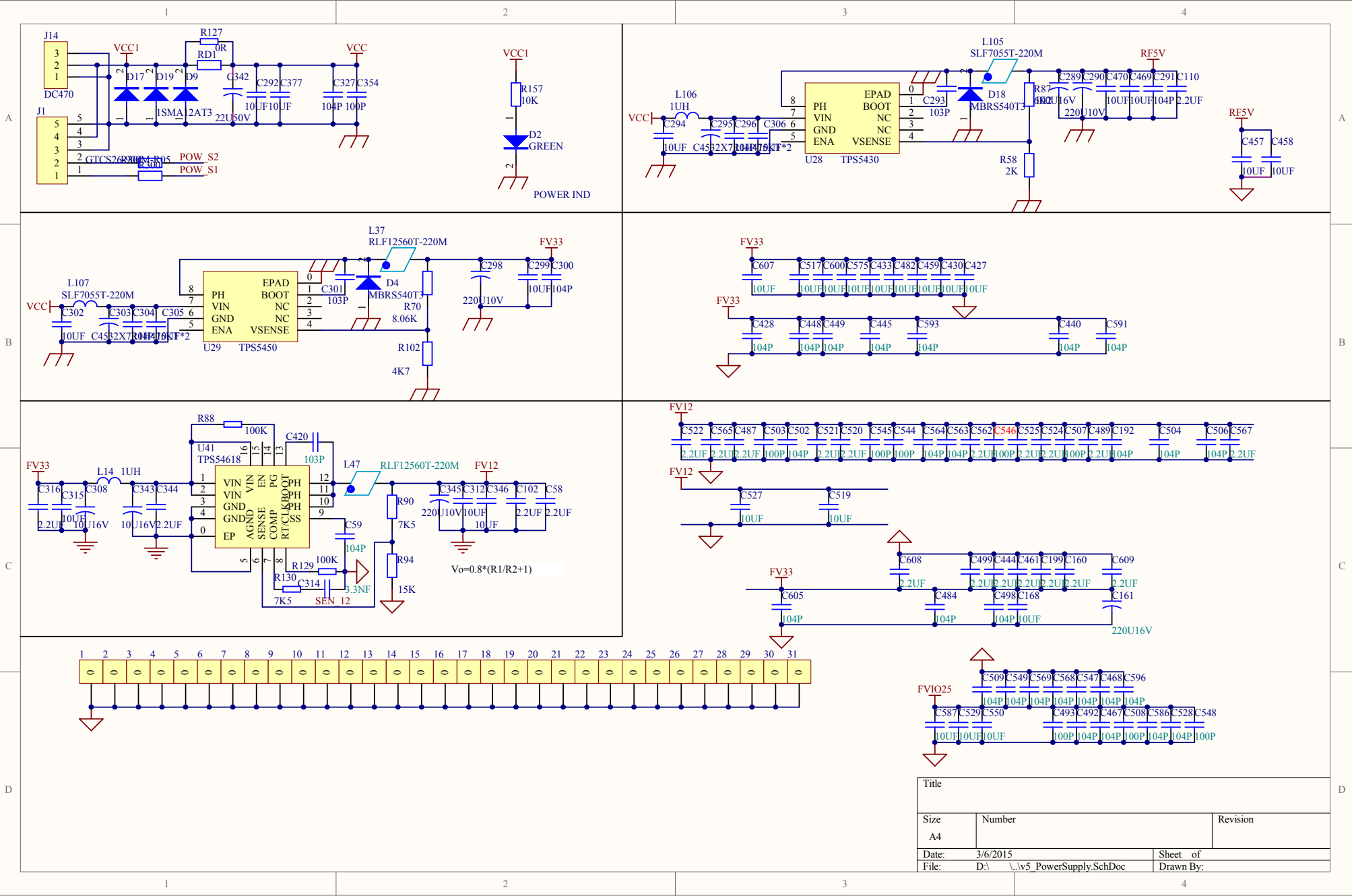
Title		
TD_PICO_v2.1		
Size	Number	Revision
A4		v2.1
Date:	3/6/2015	Sheet of
File:	D:\... \v5 MCU.SchDoc	Drawn By: Timbo.Ye

1

2

3

4



1.RLM6302_P MOS
BSS138_N MOS

Defaul t : SW2=1, SW1=0, DN ON

MSDMSW=1 MSUPSW=0 DN ON
BSDMSW=1 BSUPSW=0 DN ON
BMSW=0 BSUPSW=1 UP ON

Defaul t : SW2=1, SW1=0, BS To M6 ON

Title		TD_P co v2.1	
Size	A3	Number	Ti rito. Ye
Date:	3/6/2015	Revision	v2.1
File:	D:\c\w5 RF&PLL SchDoc	Sheet of	
		Drawn By:	