

Project:

MOKU_ADC_FMC_V1-1.PrjPcb

EARTH SCIENCES
ELECTRONICS ANU

Title:

ADC 1

Size:

A4

DocumentName:

ADC1.SchDoc

Revision:

*

Print Date: 8/07/2015

Print Time: 10:40:31 AM

Sheet 2 of 8

File: S:\JOBFILES\Outside\Tablet Oscilloscope\ADC Daughter Board\ADC1.SchDoc

Drawn by: T.Redman

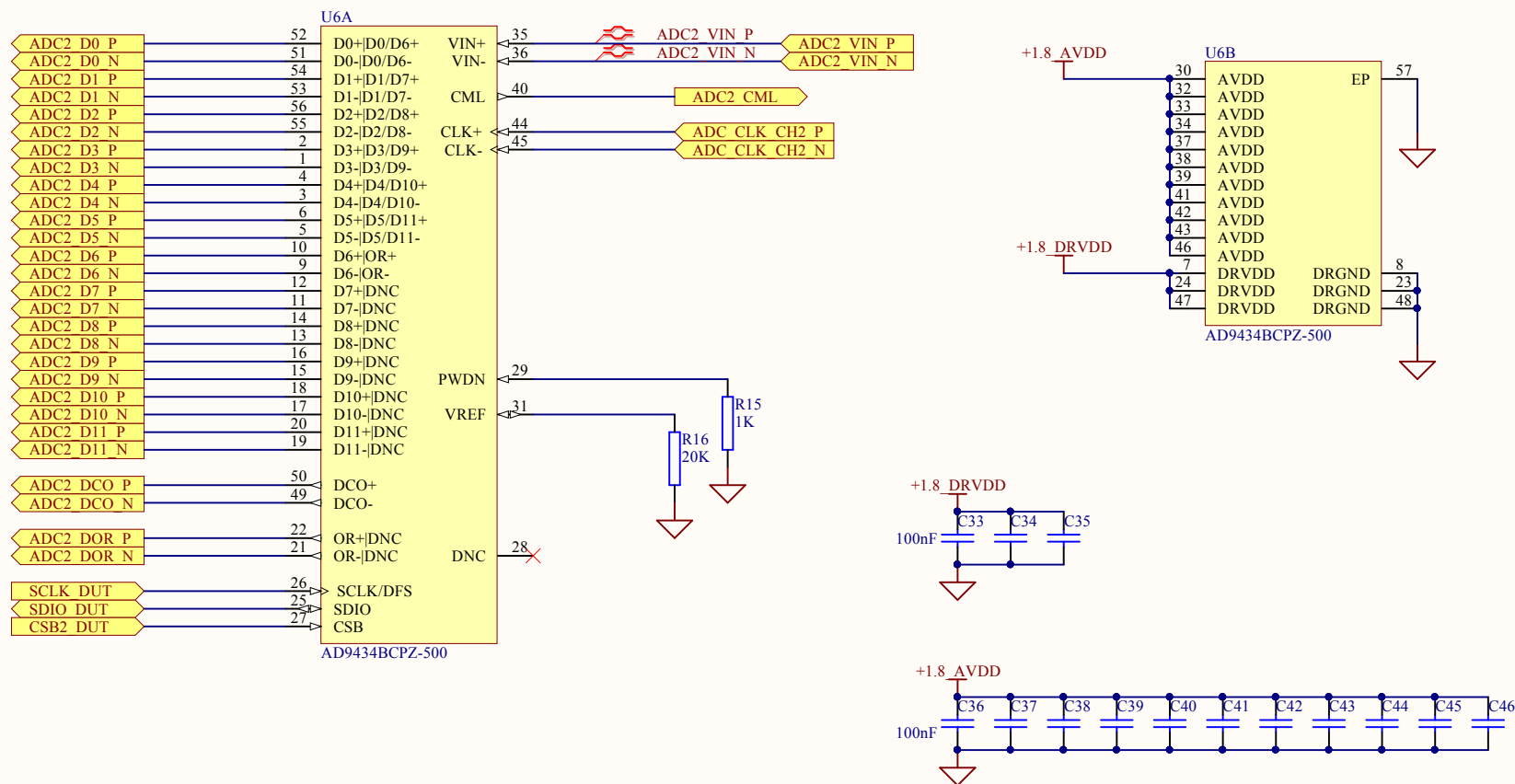
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1

2

3

4




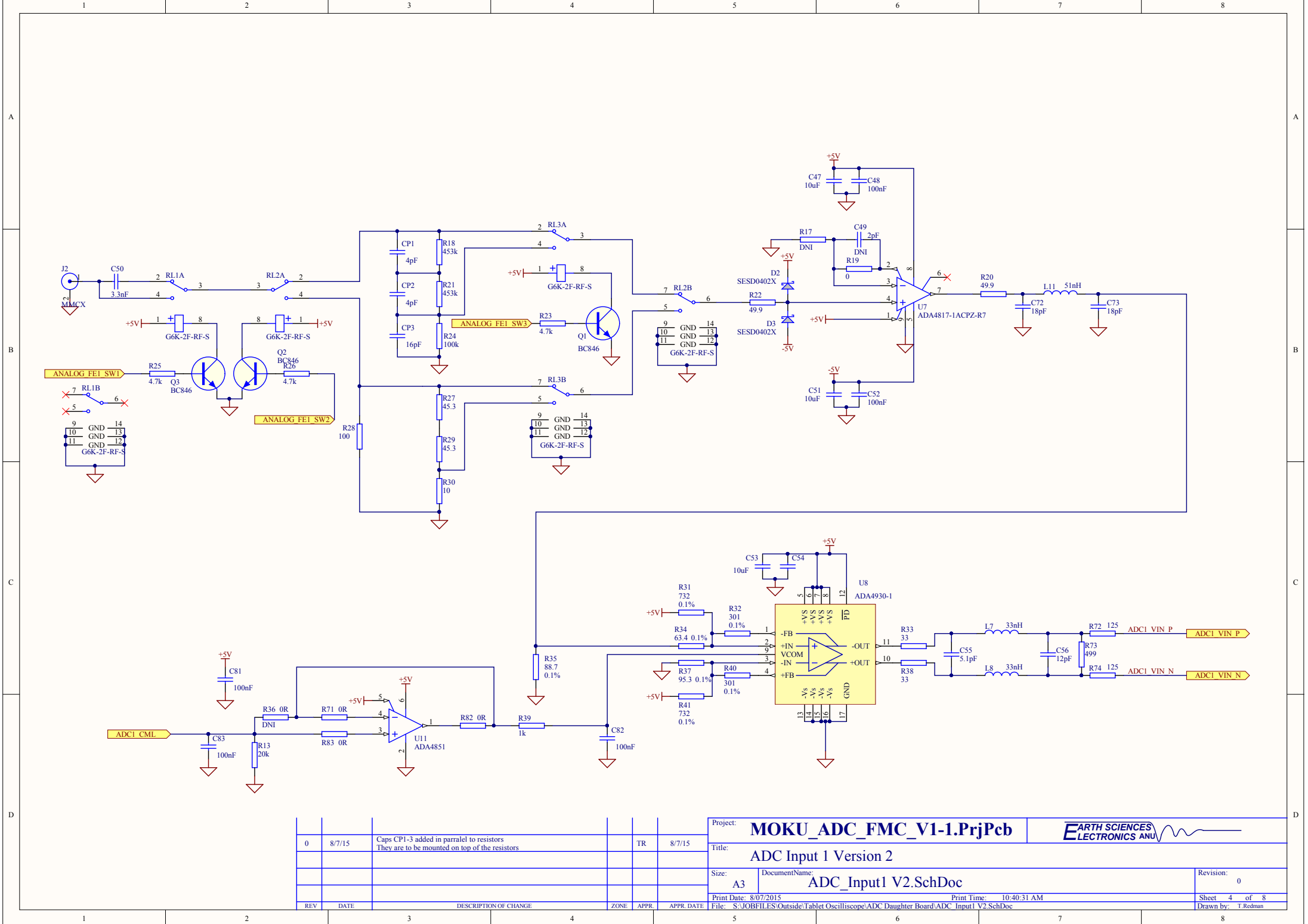
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2


3

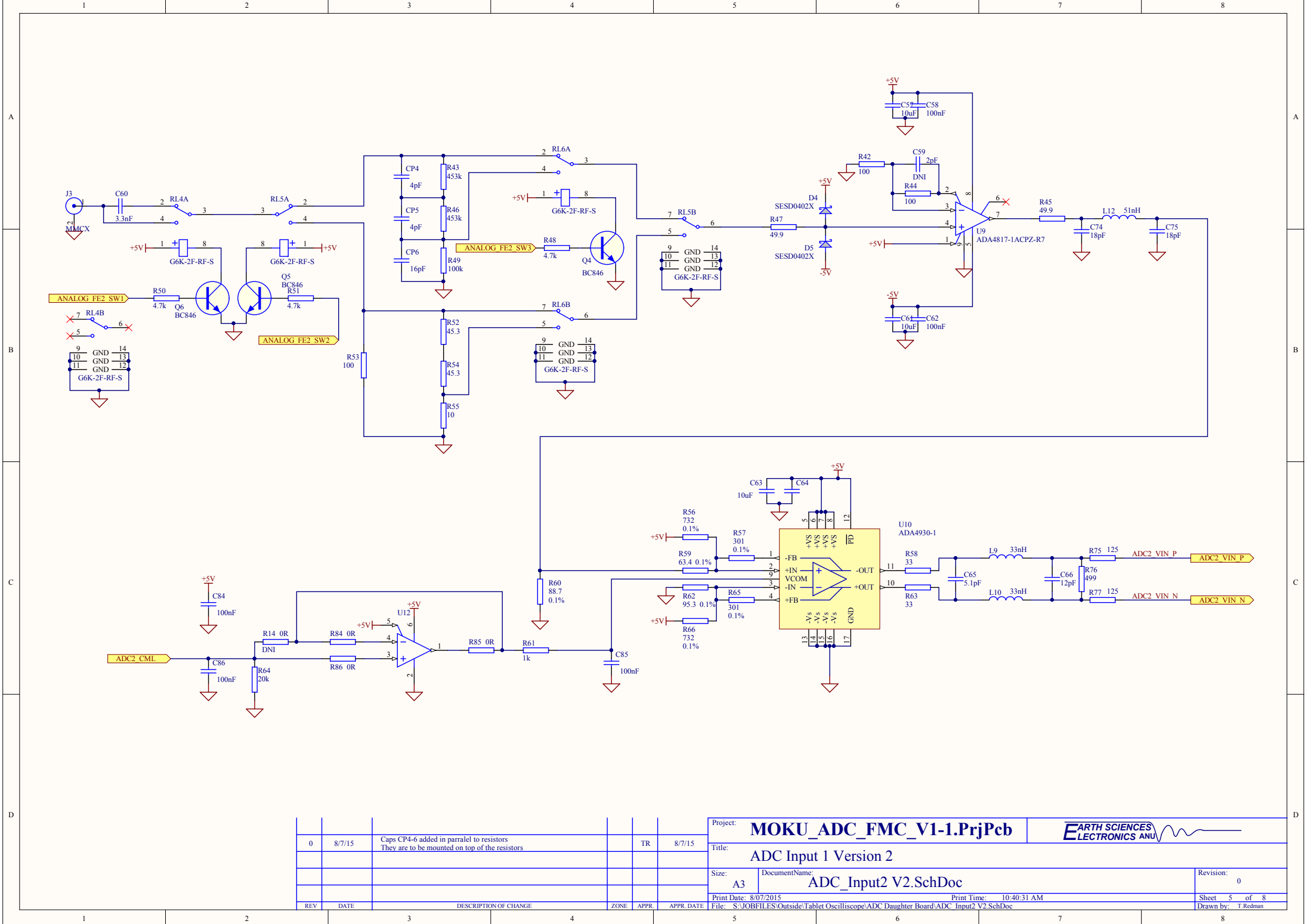
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Size:	DocumentName:			Revision:	
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File: S:\JOBFILES\Outside\Tablet Oscilloscope\ADC Daughter Board\ADC2.SchDoc				Sheet 3 of 8	
				Drawn by: T.Redman	




0	8/7/15	Caps CP1-3 added in parrallel to resistors They are to be mounted on top of the resistors	TR	8/7/15
REV	DATE	DESCRIPTION OF CHANGE	ZONE	APPR. DATE

Project:		MOKU_ADC_FMC_V1-1.PrjPcb			
Title:		ADC Input 1 Version 2			
Size:	A3	DocumentName:		ADC_Input1 V2.SchDoc	
Print Date: 8/07/2015		Print Time: 10:40:31 AM		Revision: 0	
File: S:\JOBFILES\Outside\Tablet Oscilloscope\ADC Daughter Board\ADC_Input1 V2.SchDoc				Sheet 4 of 8	
				Drawn by: T.Redman	



0	8/7/15	Caps CP4-6 added in parrallel to resistors They are to be mounted on top of the resistors	TR	8/7/15
REV	DATE	DESCRIPTION OF CHANGE	ZONE	APPR. DATE

Project:		MOKU_ADC_FMC_V1-1.PrjPcb			
Title:		ADC Input 1 Version 2			
Size:	A3	DocumentName:	ADC_Input2 V2.SchDoc		Revision: 0
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File: S:\JOBFILES\Outside\Tablet Oscilloscope\ADC Daughter Board\ADC_Input2 V2.SchDoc				Drawn by: T.Redman	

1

2

3

4

A

B

C

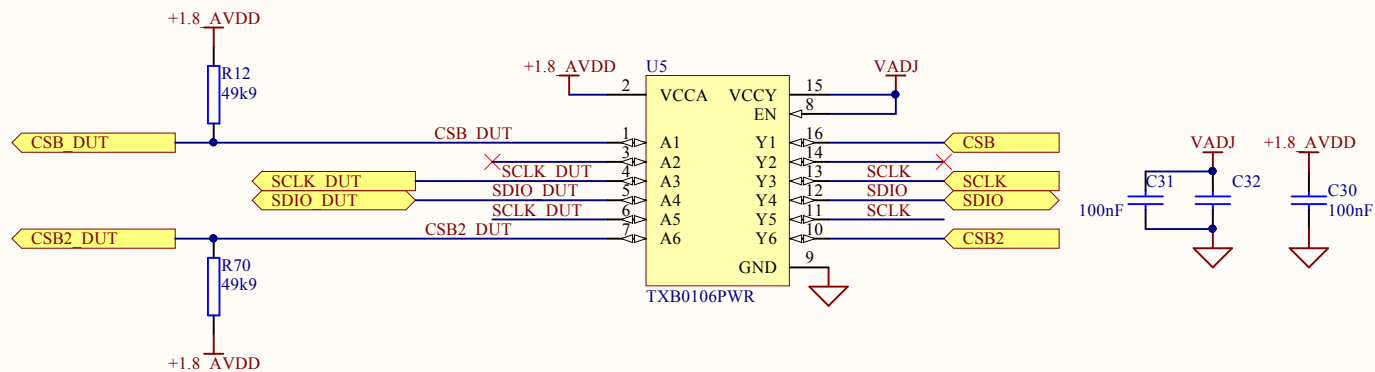
D

A

B

C

D



Project:

MOKU_ADC_FMC_V1-1.PrjPcb

EARTH SCIENCES
ELECTRONICS ANU

Title:

SPI Translator

Size:

A4

DocumentName:

ADC_SPI Translator.SchDoc

Revision:

0

Print Date: 8/07/2015

Print Time: 10:40:32 AM

Sheet 6 of 8

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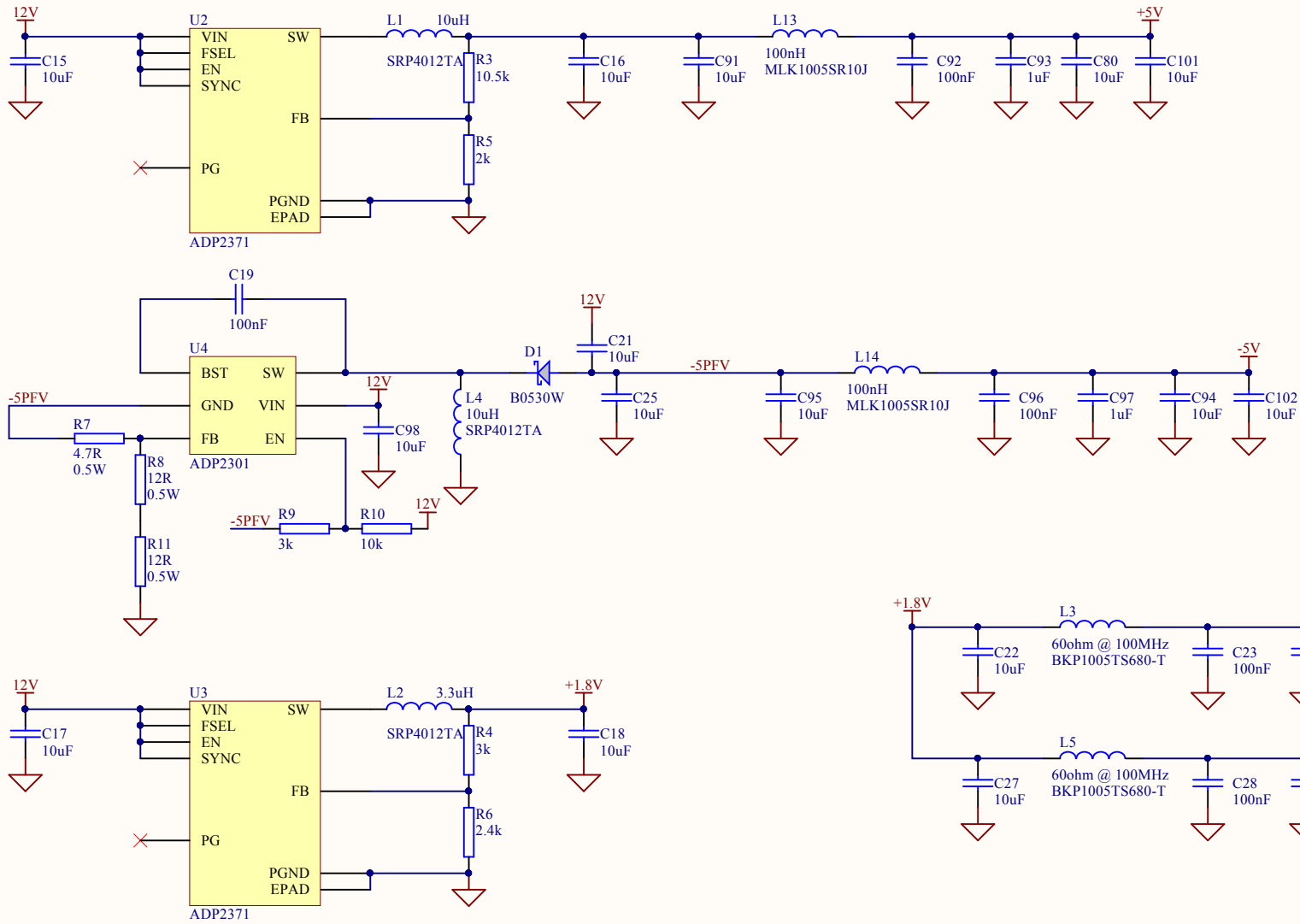
Drawn by: T.Redman


1

2

3

4



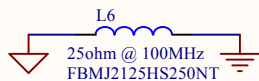
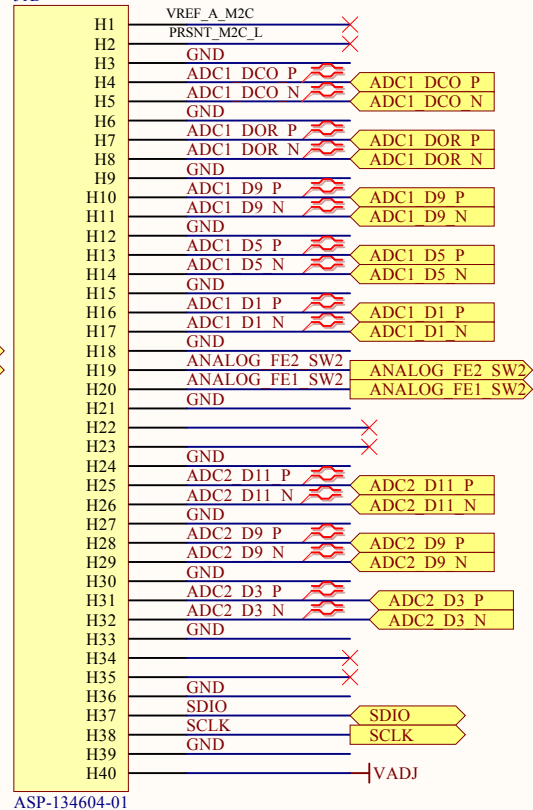
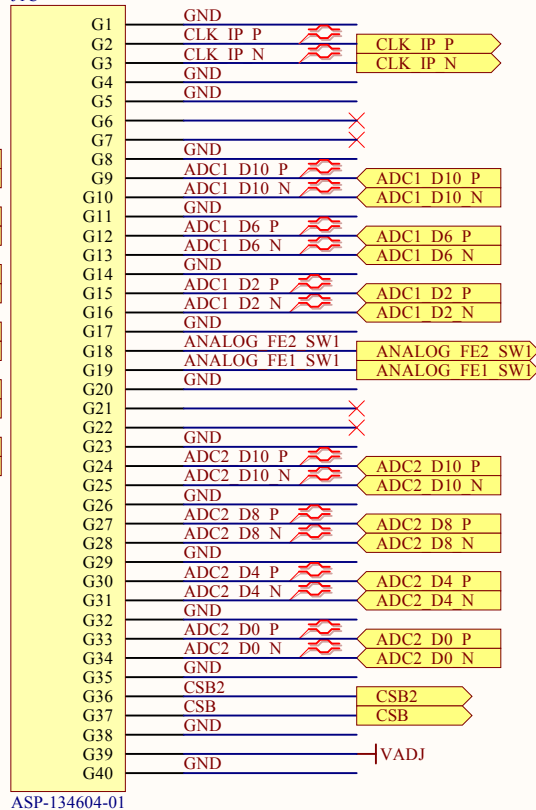
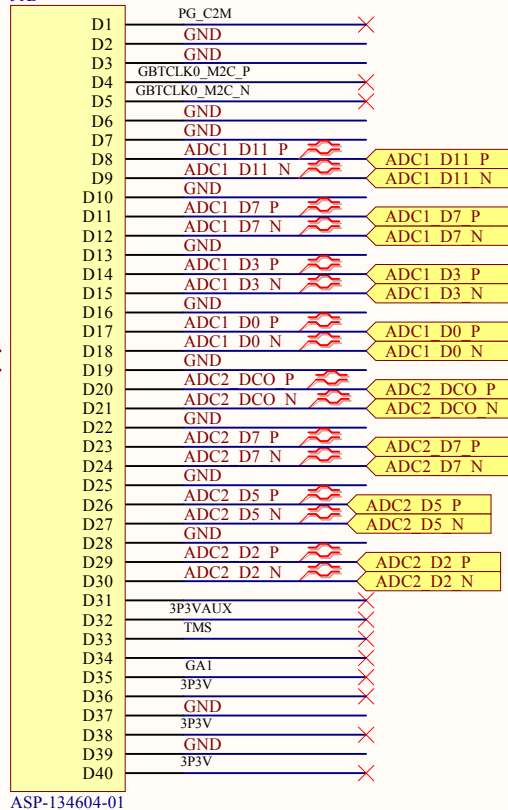
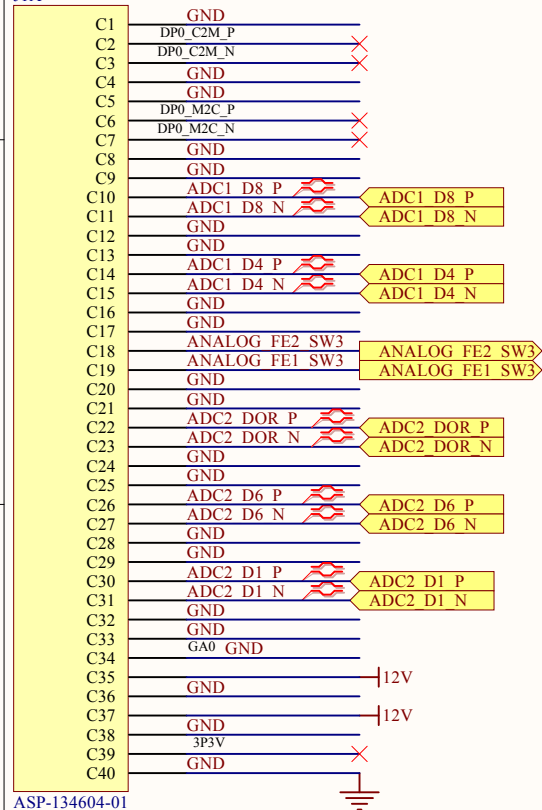
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		Drawn by: T.Redman	

J1A

J1B

J1C

J1D



Project:

MOKU_ADC_FMC_V1-1.PrjPcb

EARTH SCIENCES
ELECTRONICS ANU

Title:

FMC Connector

Size:

A4

DocumentName:

FMC Connector Pin Swapped.SchDoc

Revision:

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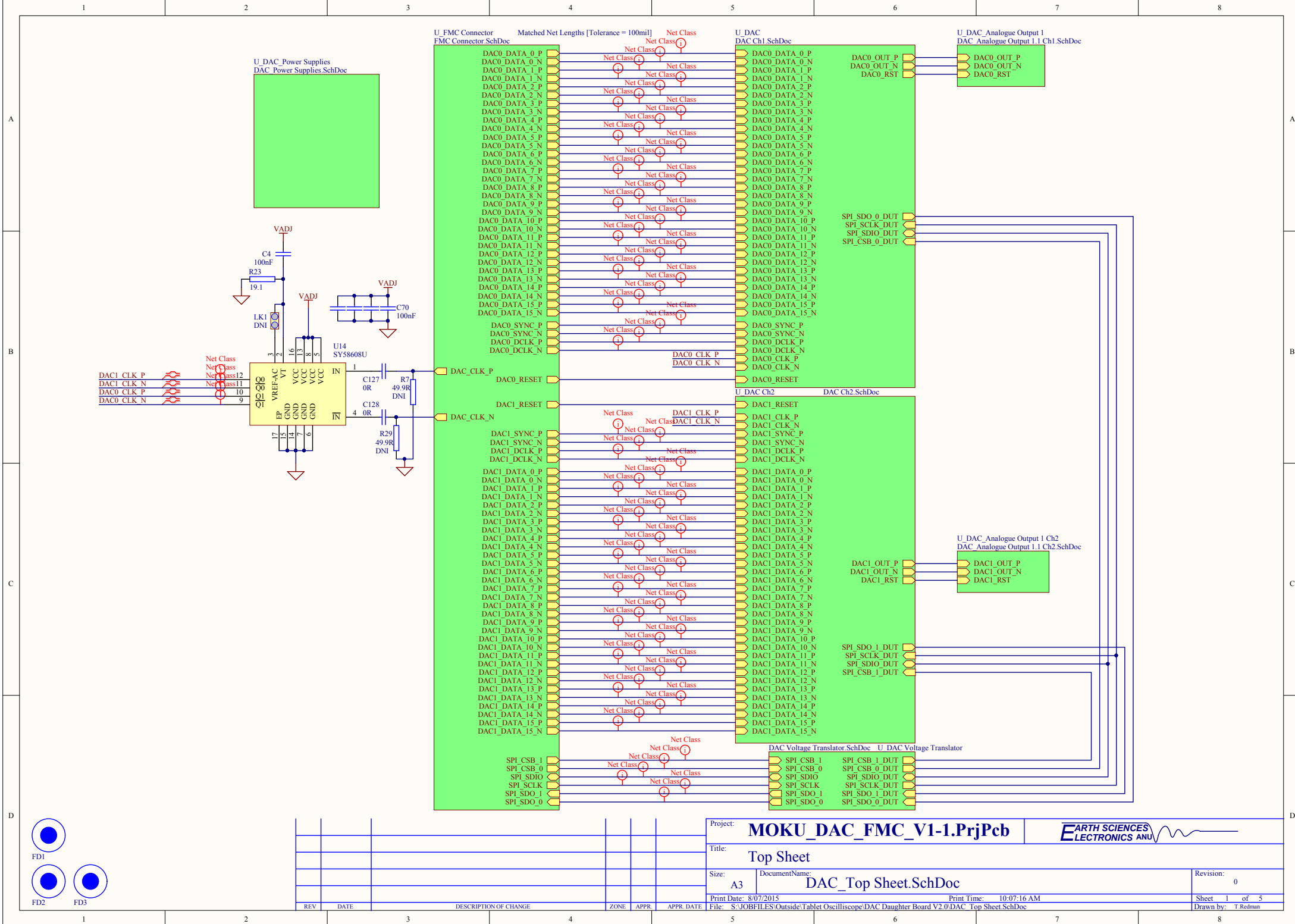
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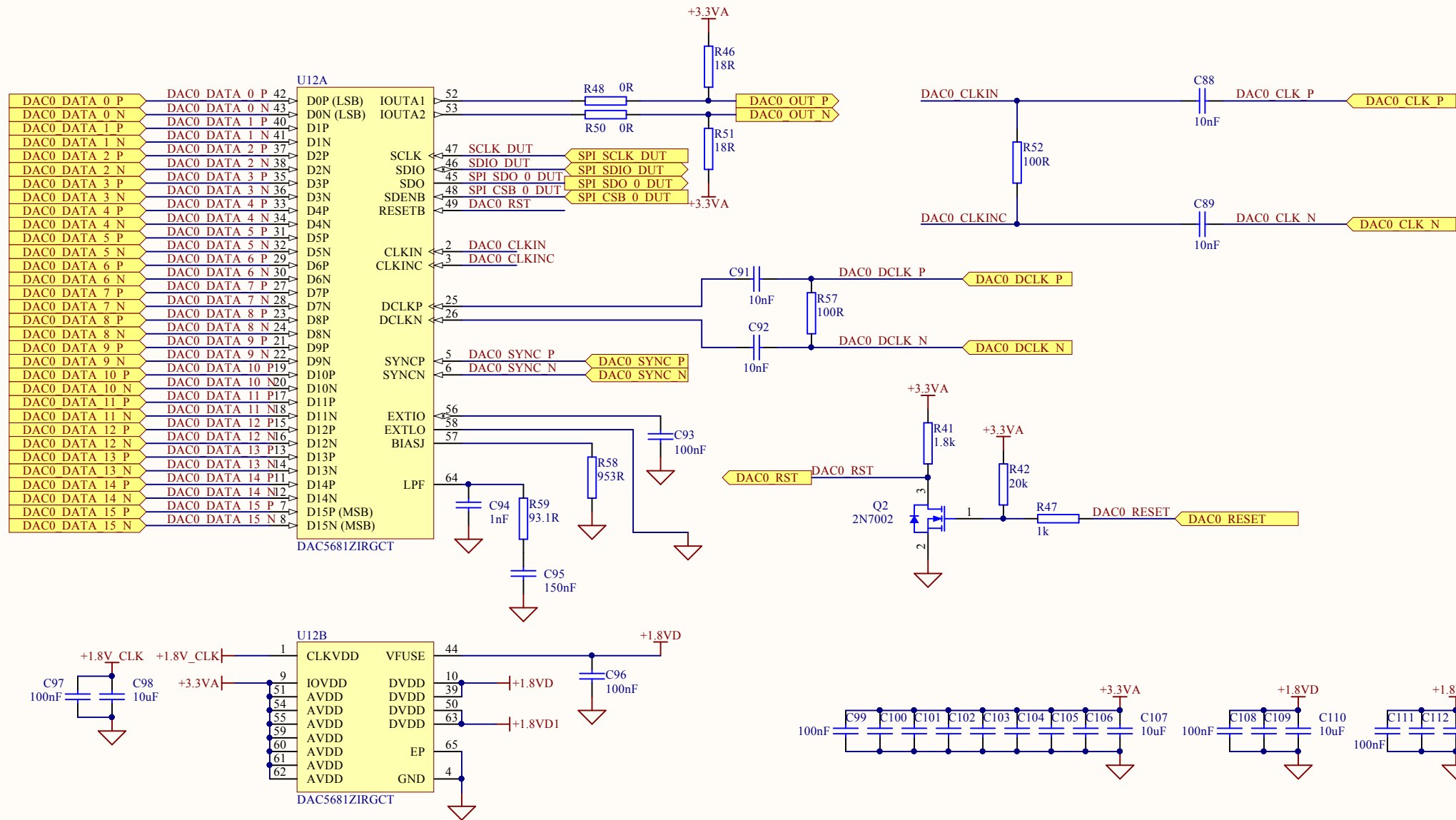
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Sheet 8 of 8

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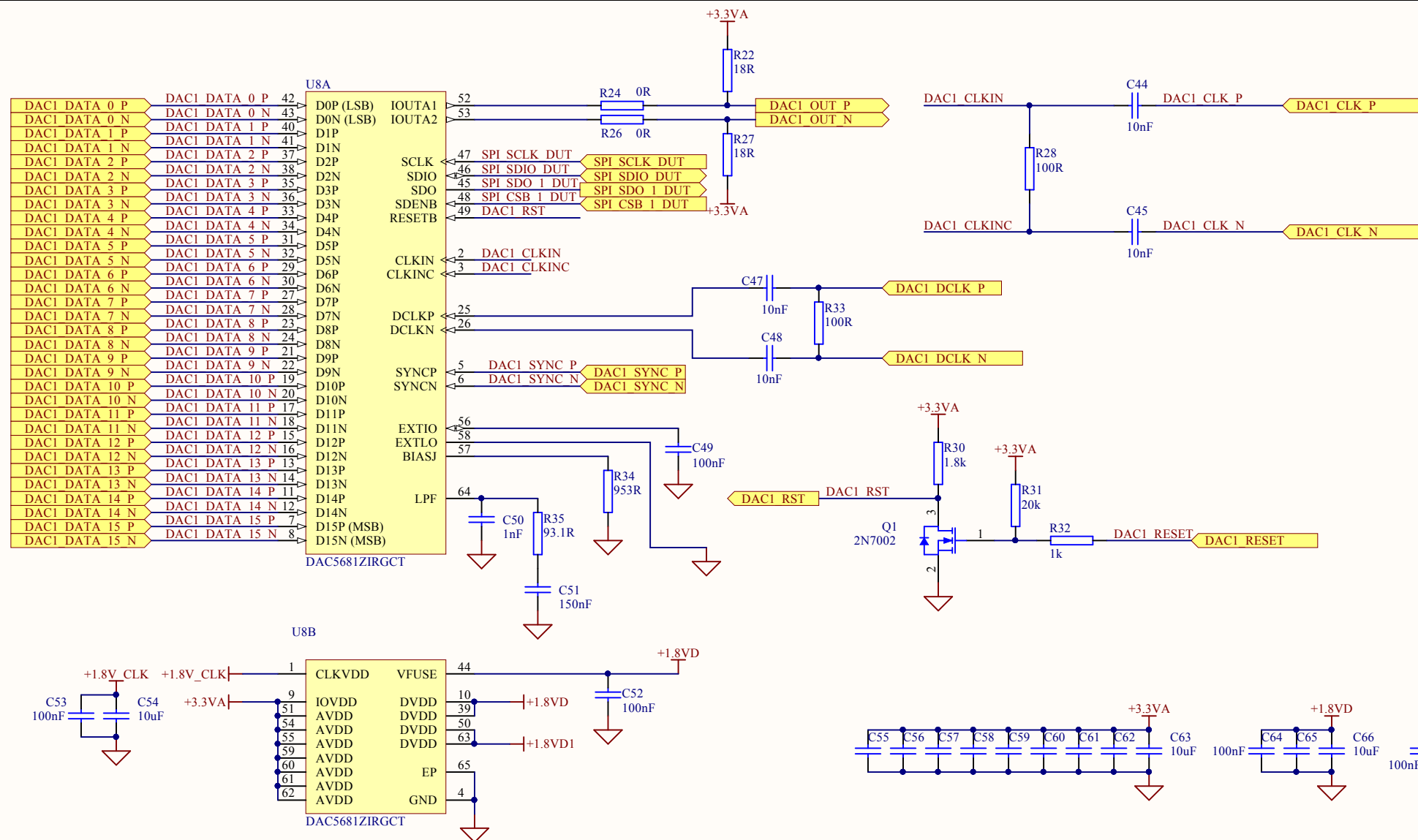
Drawn by: T.Redman




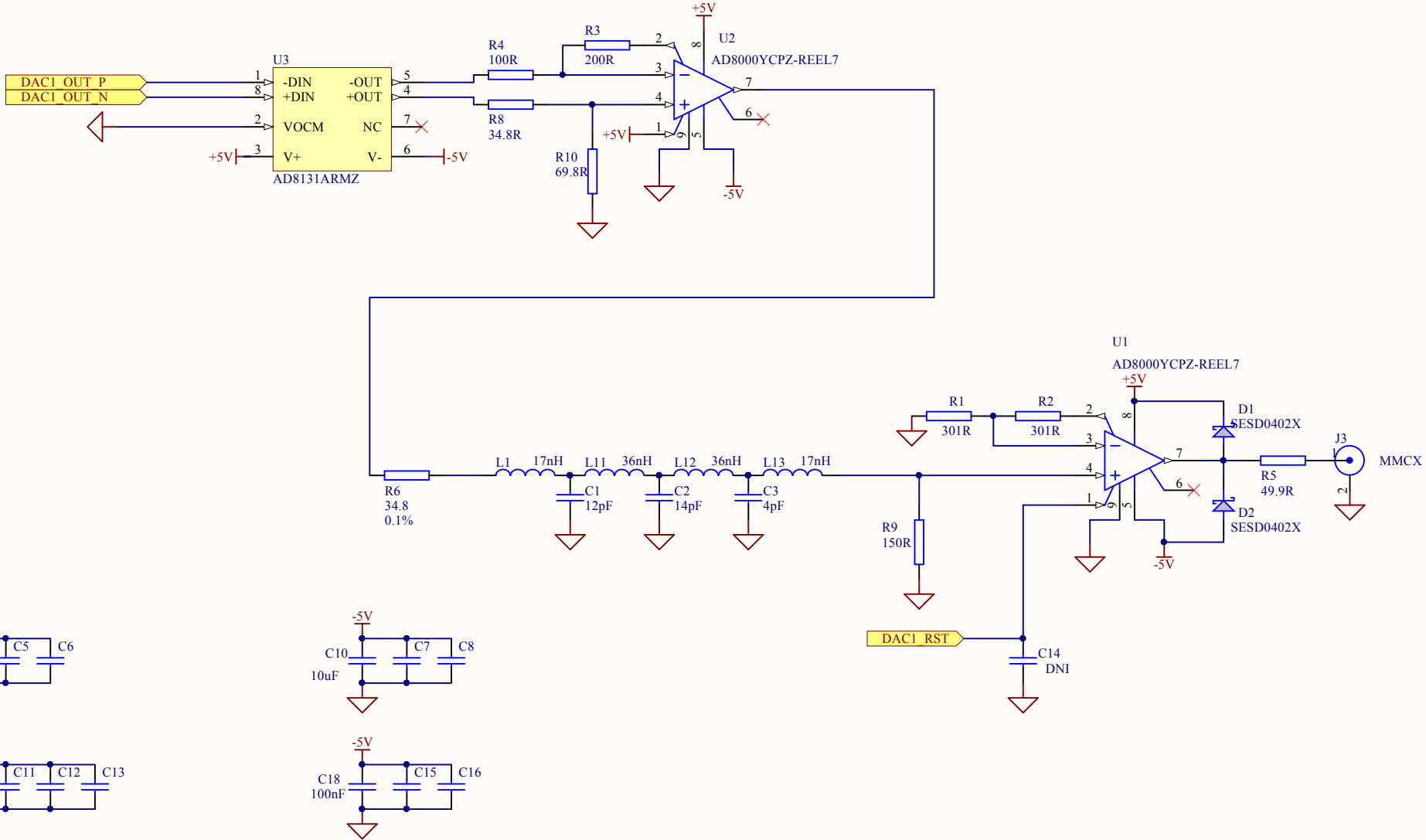


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0	8/7/15	R42 removed from VADJ and changed to +3.3VA Must be done with sky wire		TR	8/7/15	Title: DAC5681z			
0	8/7/15	Add sky wire between DAC0_RST and U9 Pin 1		TR	8/7/15				
						Size: A4	DocumentName: DAC Ch1.SchDoc		Revision: 0
						Print Date: 8/07/2015		Print Time: 10:07:17 AM	
REV	DATE	DESCRIPTION OF CHANGE	ZONE	APPR.	APPR. DATE	File: S:\JOBFILES\Outside\Tablet Oscilloscope\DAC Daughter Board V2.0\DAC Ch1.SchDoc			
						Sheet 2 of 5			
						Drawn by: T.Redman			


REV	DATE	DESCRIPTION OF CHANGE	ZONE	APPR	APPR DATE
0	8/7/15	R42 removed from VADJ and changed to +3.3VA Must be done with sky wire		TR	8/7/15
0	8/7/15	Add sky wire between DAC0_RST and U9 Pin 1		TR	8/7/15

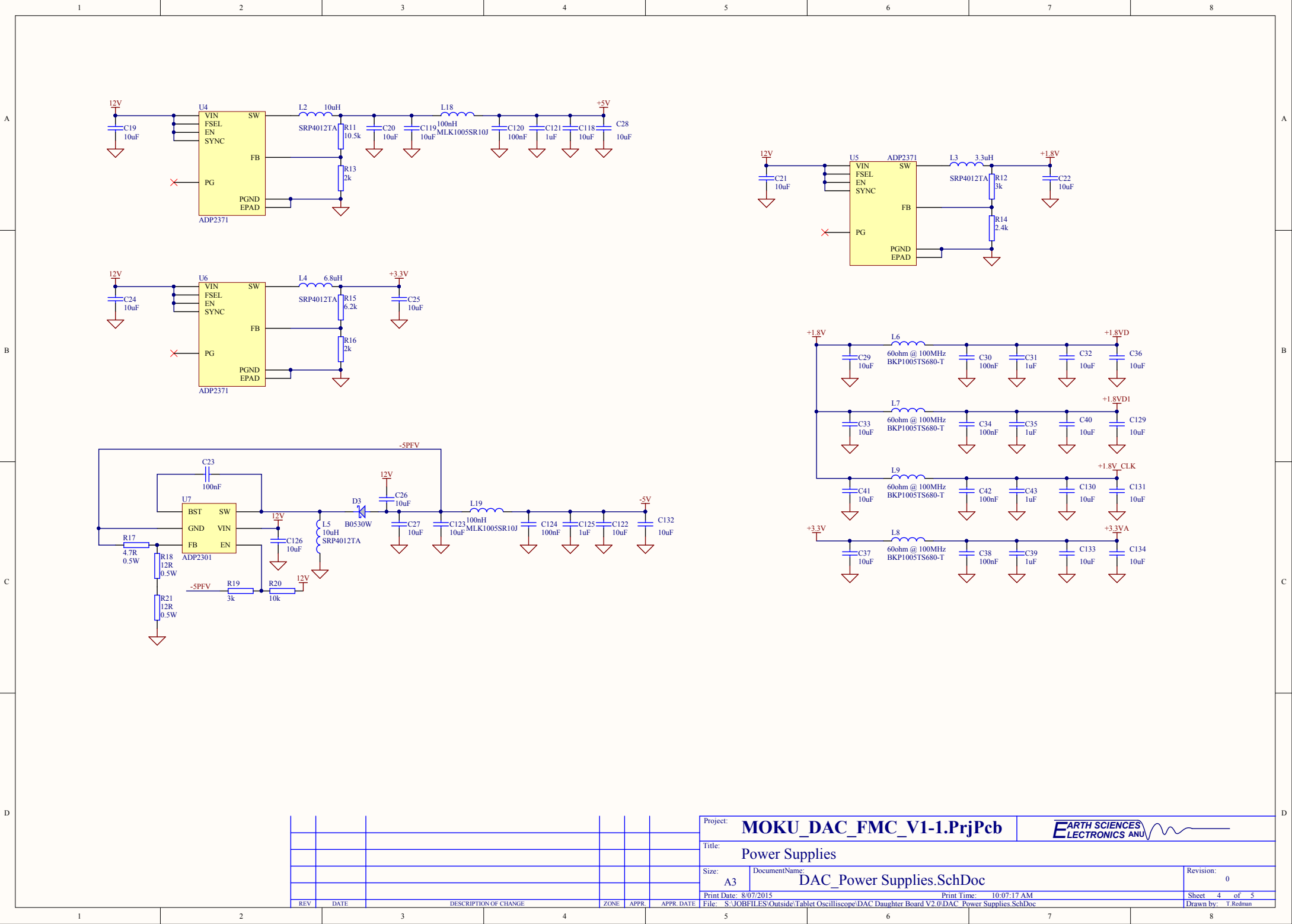



						Project: MOKU_DAC_FMC_V1-1.PrjPcb			
0	8/7/15	R31 removed from VADJ and changed to +3.3VA Must be done with sky wire		TR	8/7/15	Title: DAC5681z			
0	8/7/15	Add sky wire between DAC1_RST and U1 Pin 1		TR	8/7/15				
						Size: A4	DocumentName: DAC Ch2.SchDoc		Revision: 0
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						Sheet 2 of 5 Drawn by: T.Redman			



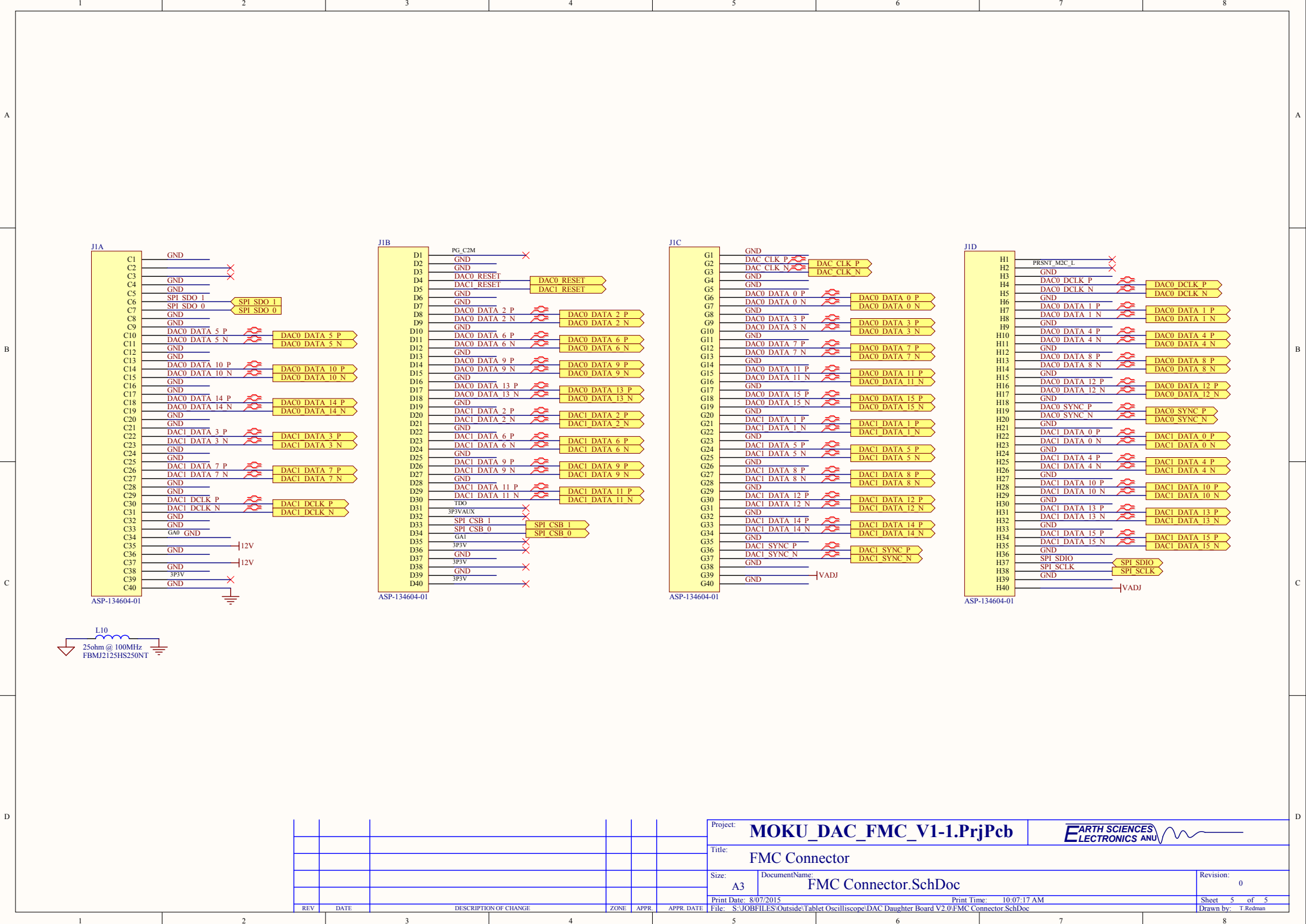
0	8/7/15	C14 Removed and track to 5V cut Sky wire added between U1 pin 1 (C14) and DAC1_RST	TR	8/7/15
REV	DATE	DESCRIPTION OF CHANGE	ZONE	APPR. DATE

Project: MOKU_DAC_FMC_V1-1.PrjPcb			
Title: Analog Output Circuit 1.1			
Size: A4	DocumentName: DAC_Analogue Output 1.1 Ch2.SchDoc		Revision: 0
Print Date: 8/07/2015	Print Time: 10:07:17 AM		Sheet 3 of 5
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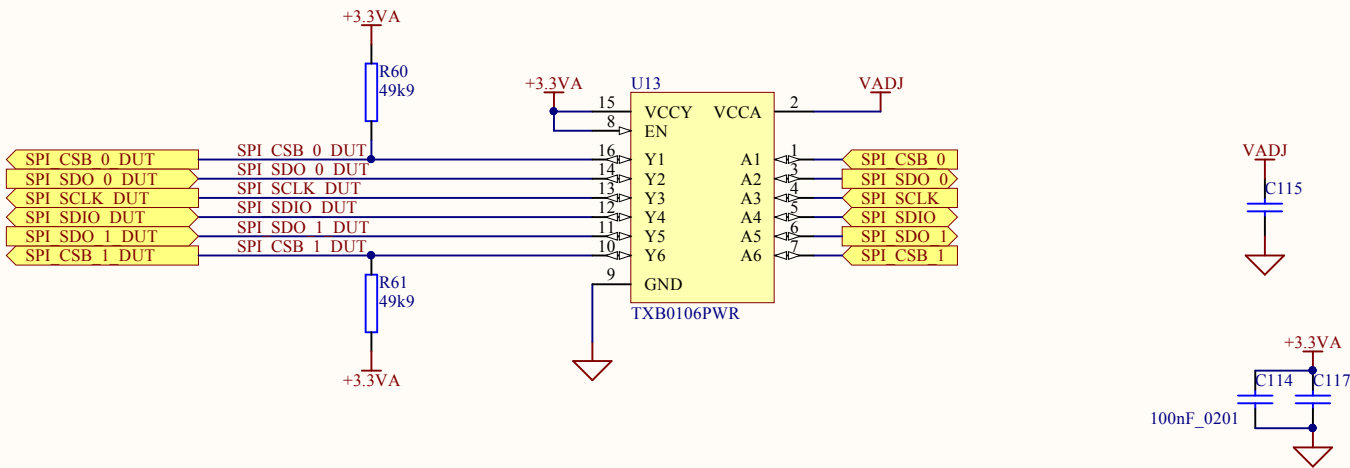
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		Drawn by: T.Redman	


REV	DATE	DESCRIPTION OF CHANGE	ZONE	APPR	APPR. DATE



REV	DATE	DESCRIPTION OF CHANGE	ZONE	APPR	APPR DATE

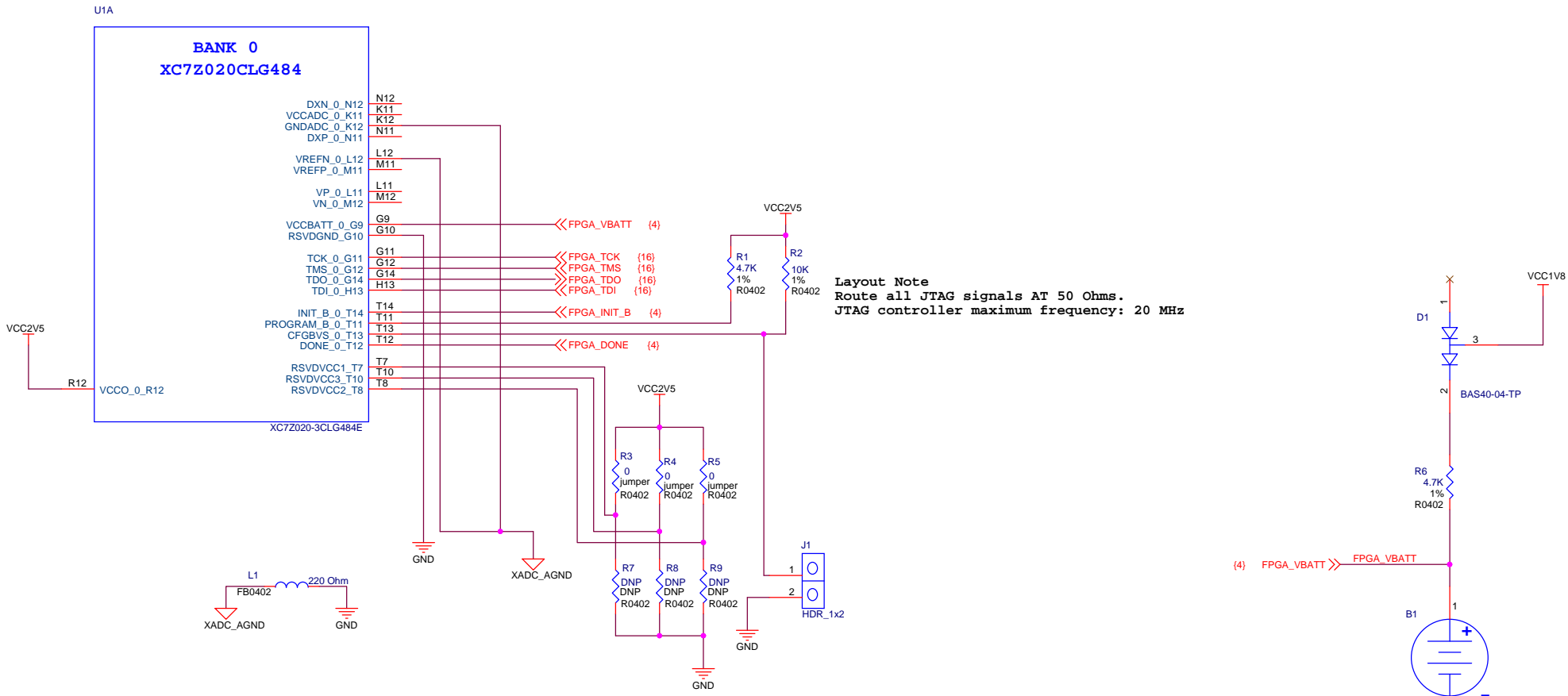
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		Drawn by: T.Redman	



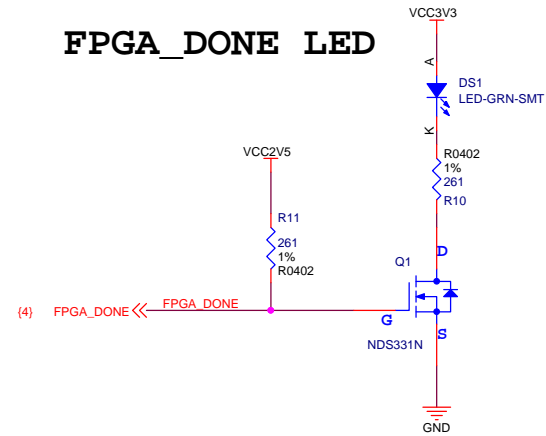
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FPGA ZYNQ-7000 CONFIGURATION BANK 0

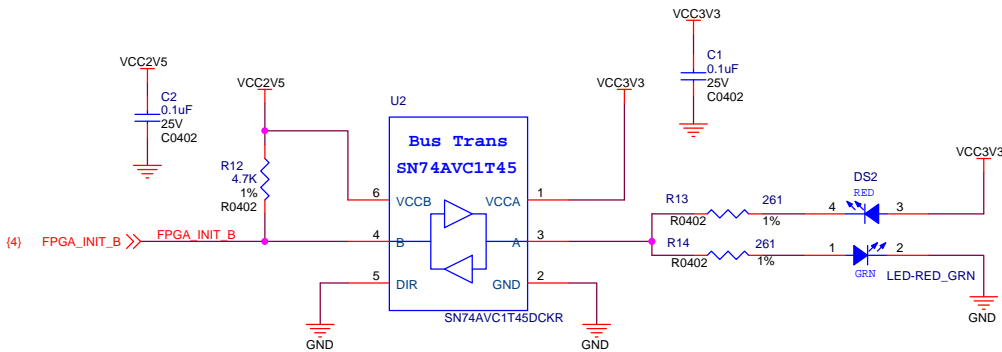
FPGA Maximum CPU clock frequency: 866 MHz
Maximum DDR3 interface performance: 1066 Mb/s



FPGA_DONE LED



FPGA_INIT Bicolour LED



Zynq Bank 0

Proprietary and Confidential



WHIZZ SYSTEMS INC.
3240 Scott Blvd, Santa Clara,
CA 95054, USA
Job # 7490

Client: Liquid Instruments PTY. LTD.

Title: FPGA BANK 0

Sch: 7490 MokuV1.0

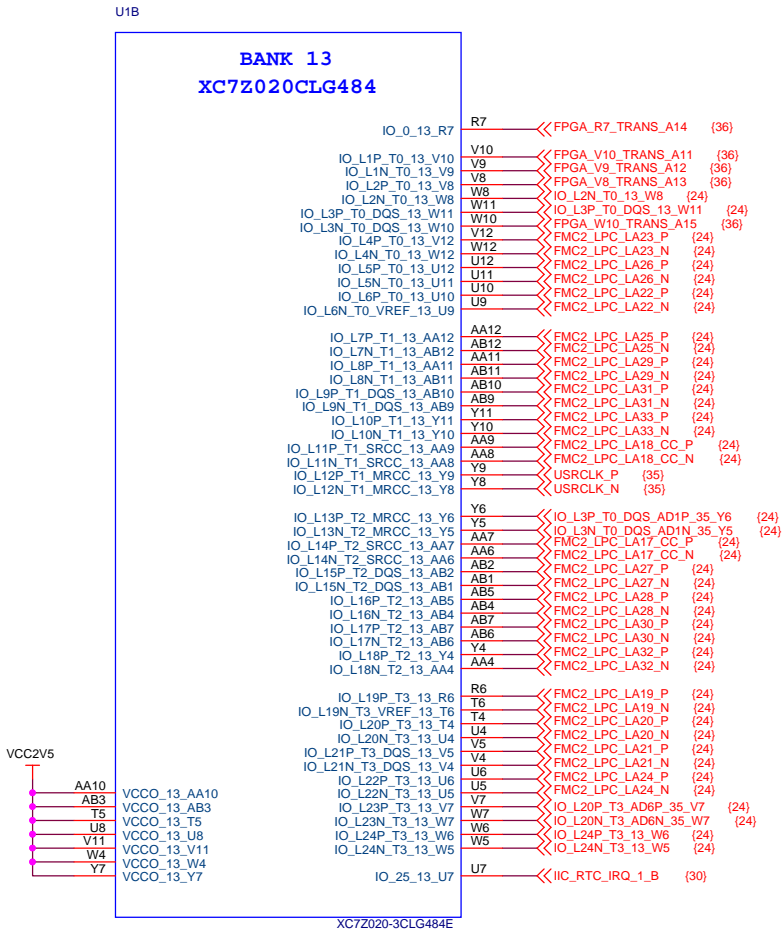
Size: C Engineer: Farooq Bhatti

Rev: A

Date: Thursday, July 09, 2015

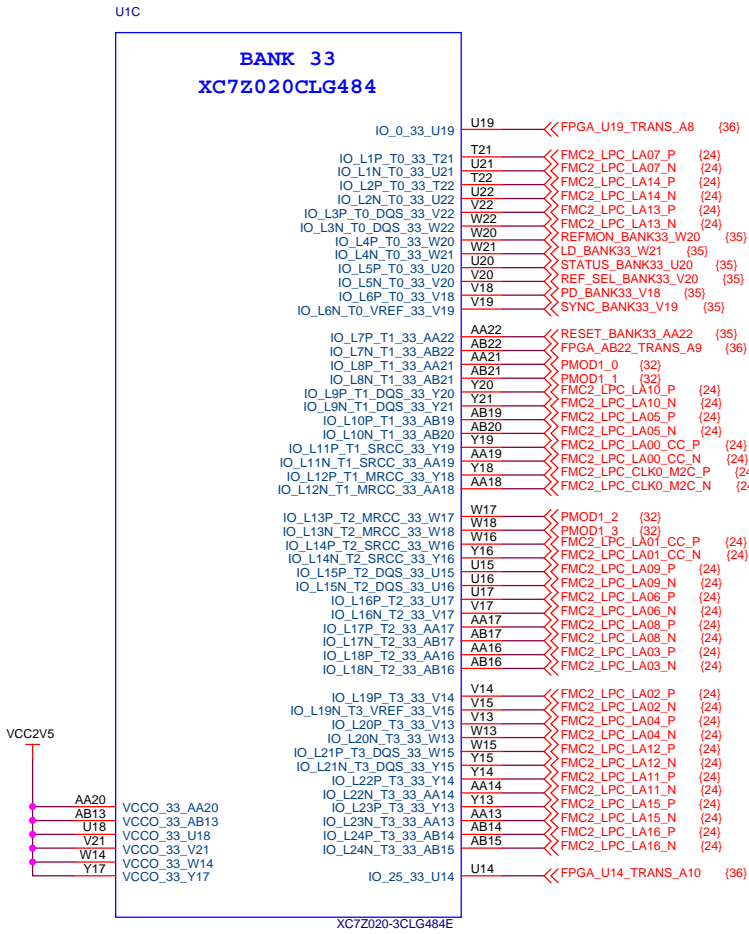
Sheet 4 of 38

FPGA BANK 13 (FPGA-FMC)



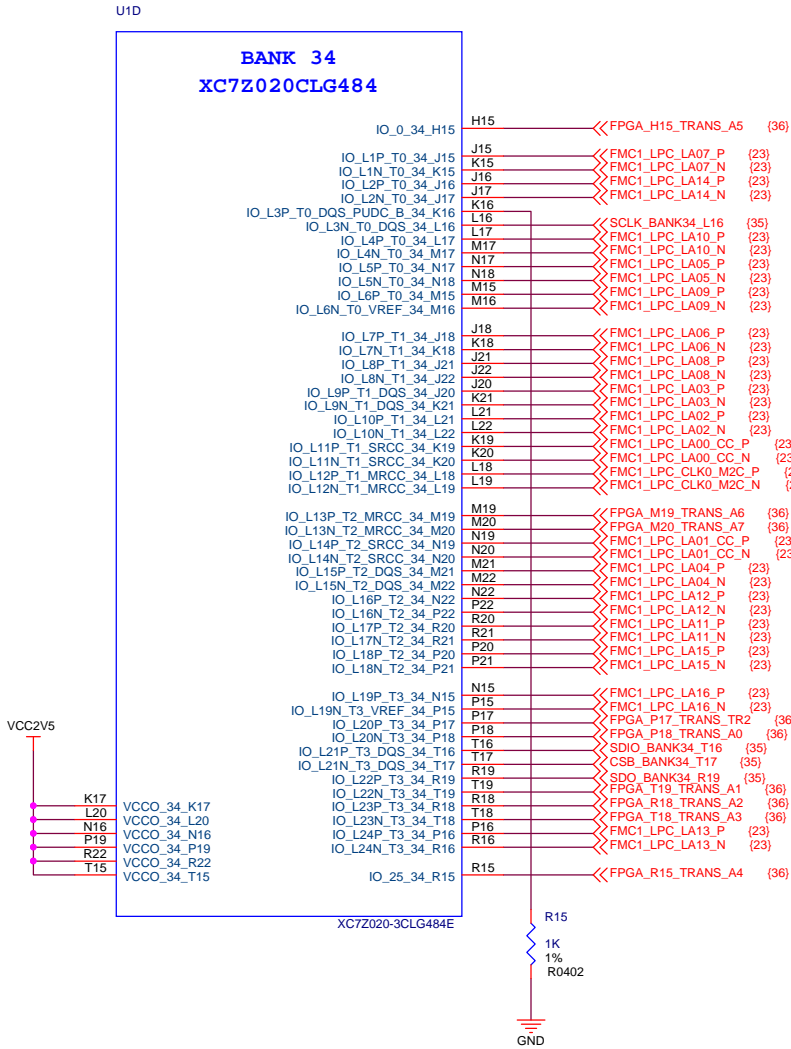
Layout Note
Route all FMC Diff Pairs Signals at 100 Ohms
and Single Ended Signals at 50 Ohms

FPGA BANK 33 (FPGA-FMC)



Layout Note
Route all FMC Diff Pairs Signals at 100 Ohms
and Single Ended Signals at 50 Ohms

FPGA BANK 34 (FPGA-FMC)



Layout Note
Route all FMC Diff Pairs Signals at 100 Ohms
and Single Ended Signals at 50 Ohms

Zynq Bank 34

Proprietary and Confidential

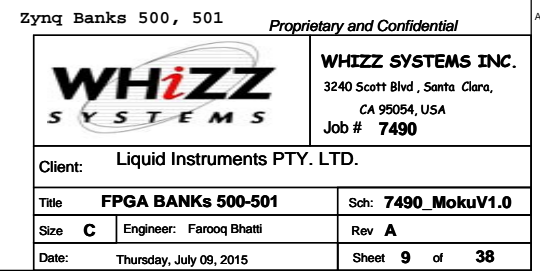


WHIZZ SYSTEMS INC.
3240 Scott Blvd , Santa Clara,
CA 95054, USA
Job # **7490**

Client: Liquid Instruments PTY. LTD.

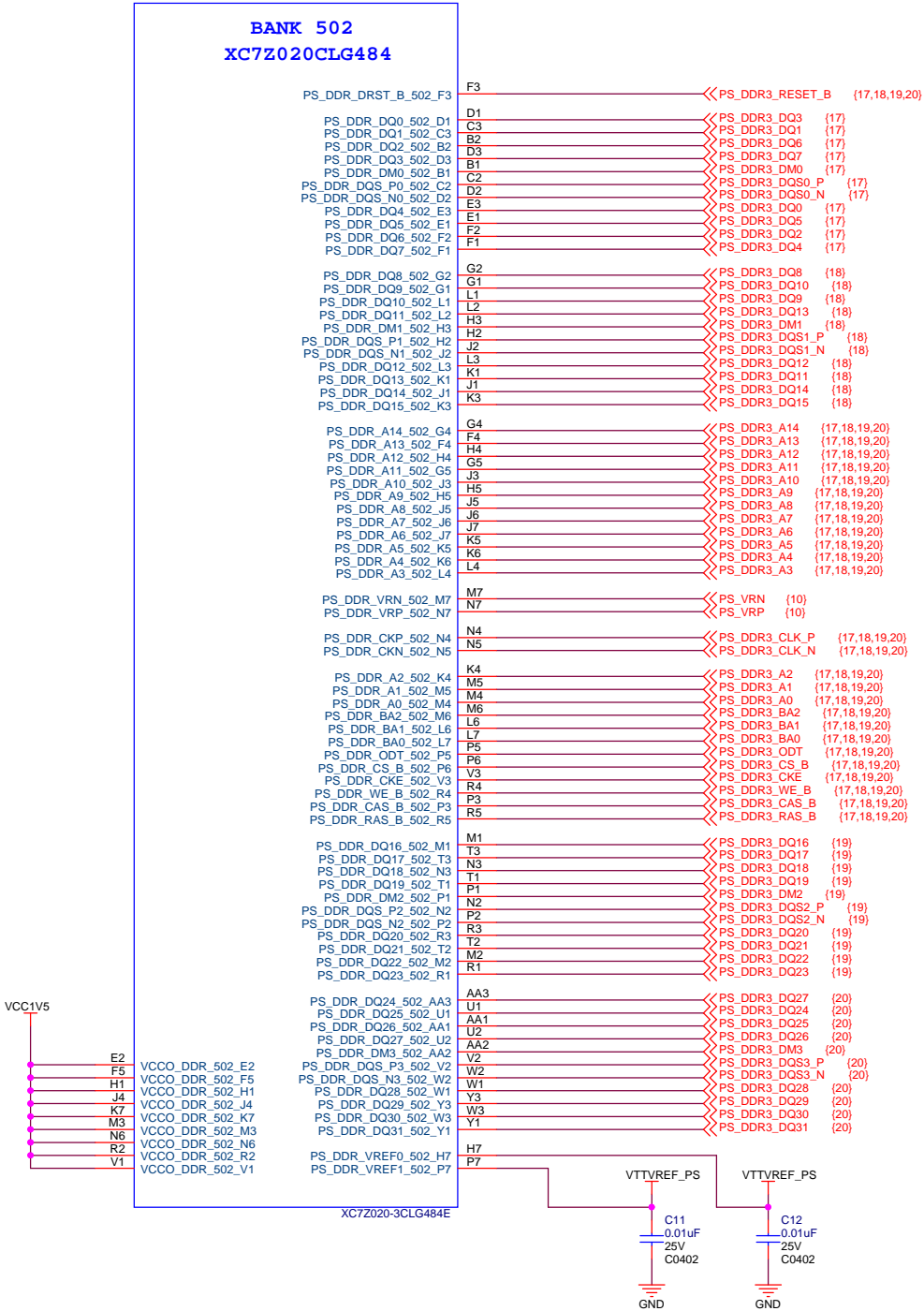
Title	FPGA BANK 34	Sch:	7490_MokuV1.0
Size	C	Engineer:	Farooq Bhatti
Date:	Thursday, July 09, 2015	Rev	A
		Sheet	7 of 38

FPGA BANK 500 (FPGA- WIFI/UART/QSPI)



FPGA BANK 502 (FPGA-DDR3)

U1H



Layout Note

Clock Frequency = 866 MHz DDR
Data Rate = 1600 MTs
Voltage = 1.5V
Single Ended = 40 Ohm
Differential = 80 Ohm
Processor = Xilinx CORTEX-A9 ARTIX-7
SDRAM ICs = DDR3L 1.5V SDRAM

Zynq Bank 502

Proprietary and Confidential



WHIZZ SYSTEMS INC.
3240 Scott Blvd, Santa Clara,
CA 95054, USA
Job # **7490**

Client: Liquid Instruments PTY. LTD.

Title: **FPGA BANK 502**

Sch: **7490_MokuV1.0**

Size: **C** Engineer: Farooq Bhatti

Rev: **A**

Date: Thursday, July 09, 2015

Sheet **10** of **38**

FPGA POWER BANKS

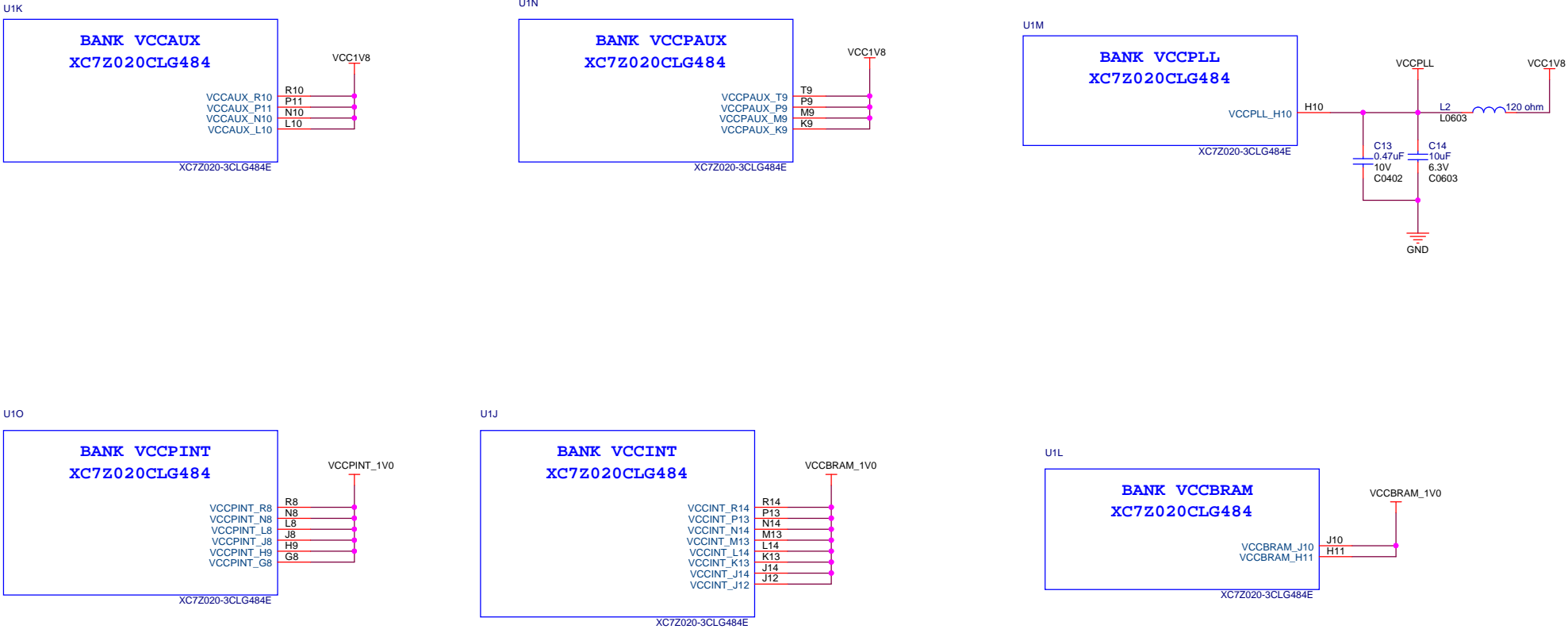
Layout Notes:

Increase width of VCCPLL route to as wide as possible (target is > 20 mils)

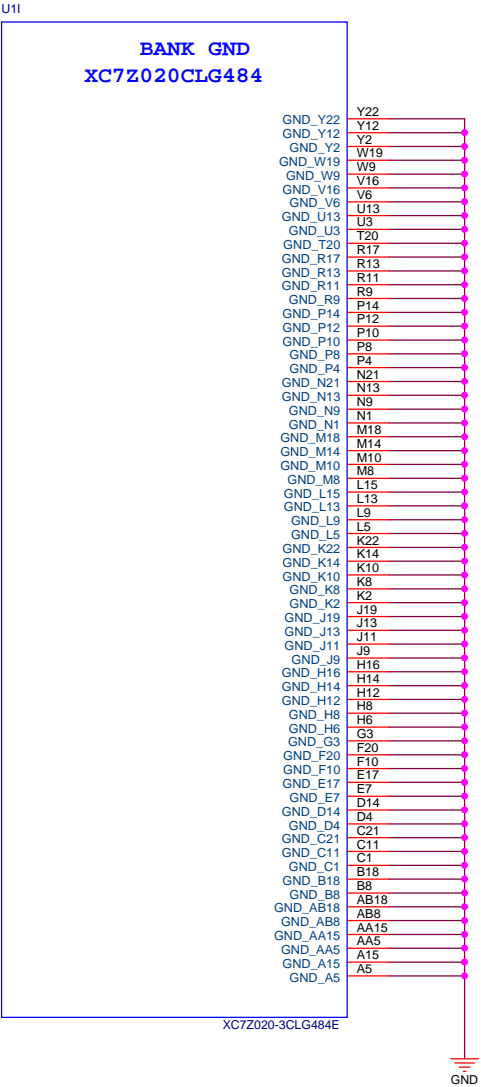
Reduce the length of VCCPLL route as much as possible

Place C538 inside the VIA field to provide as short as possible connection to VCCPLL (H10) and GND

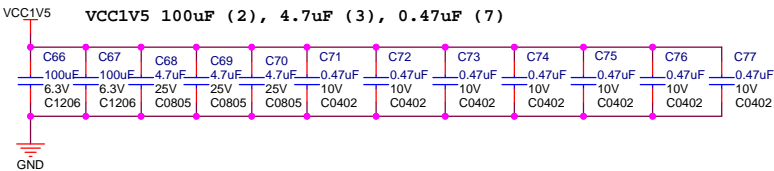
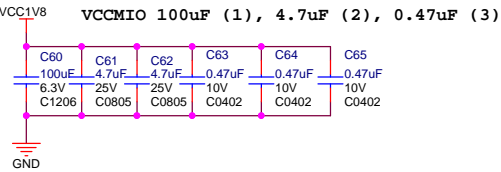
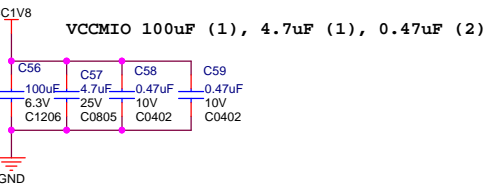
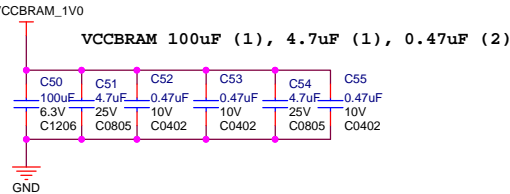
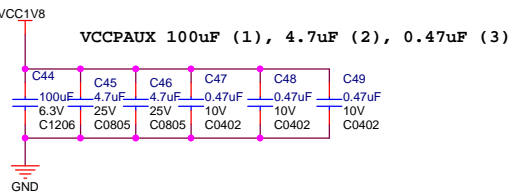
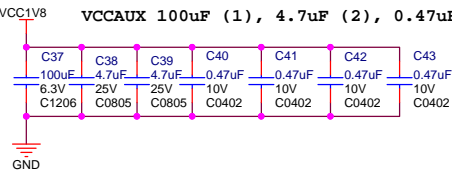
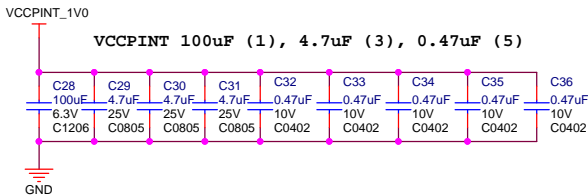
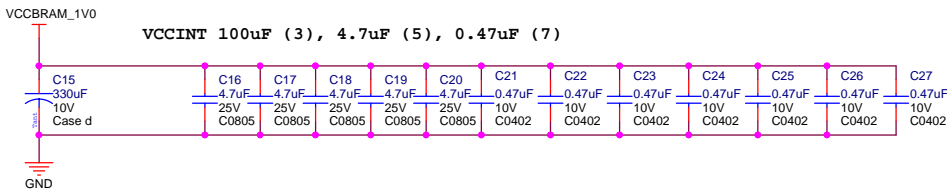
Place C148 inside the open space cross adjacent to H10 for the short possible connection to VCCPLL



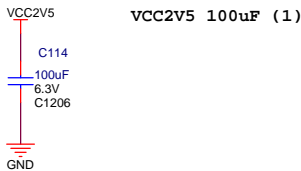
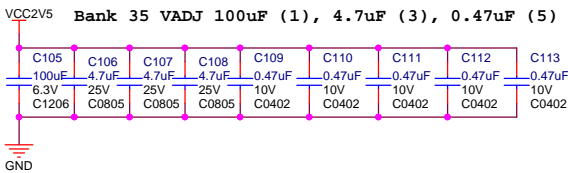
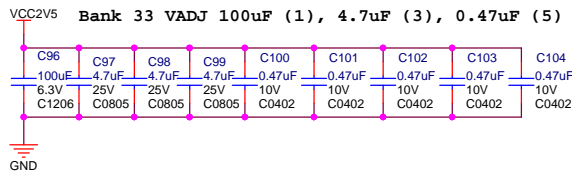
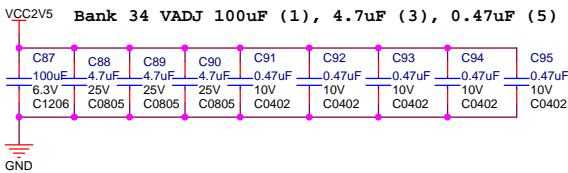
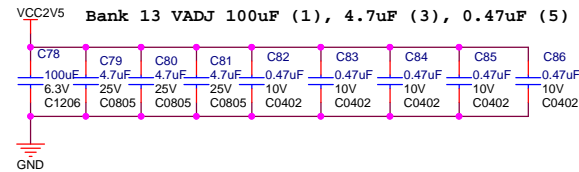
FPGA GND BLOCK



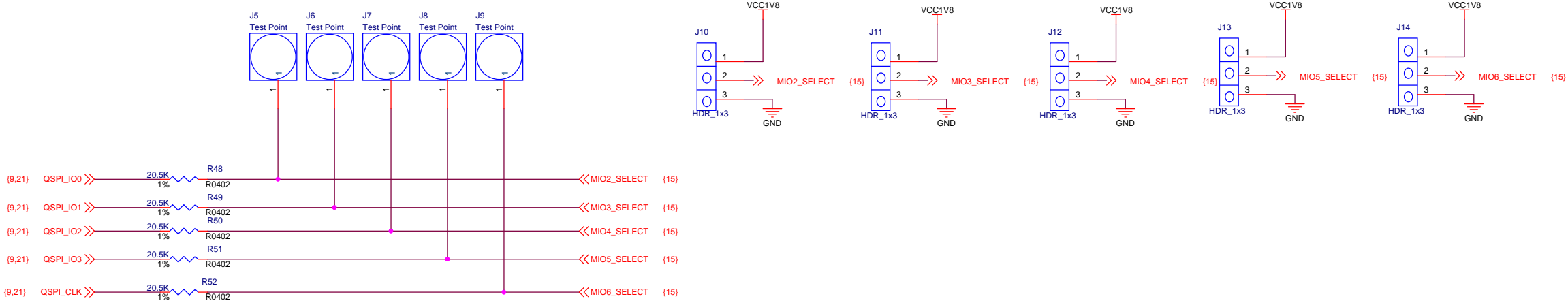
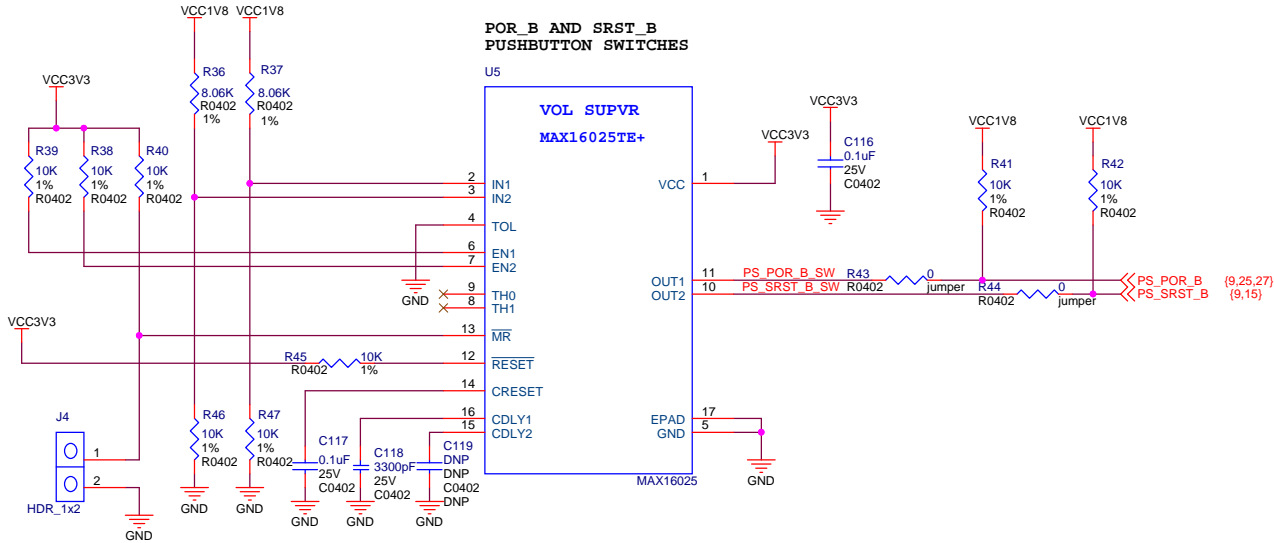
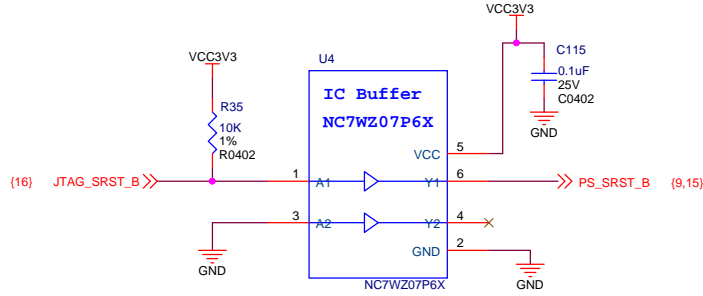
FPGA BYPASS CAPACITORS



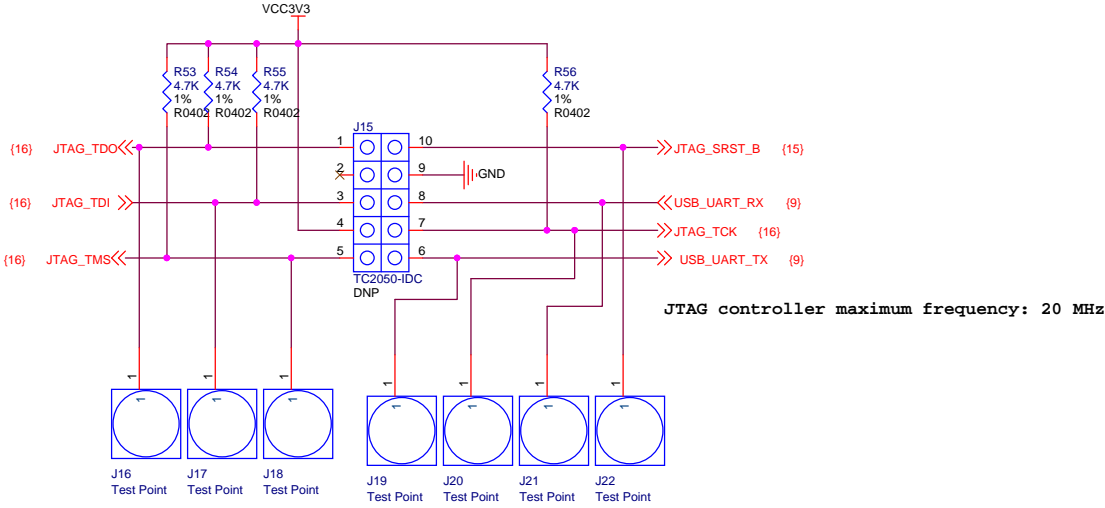
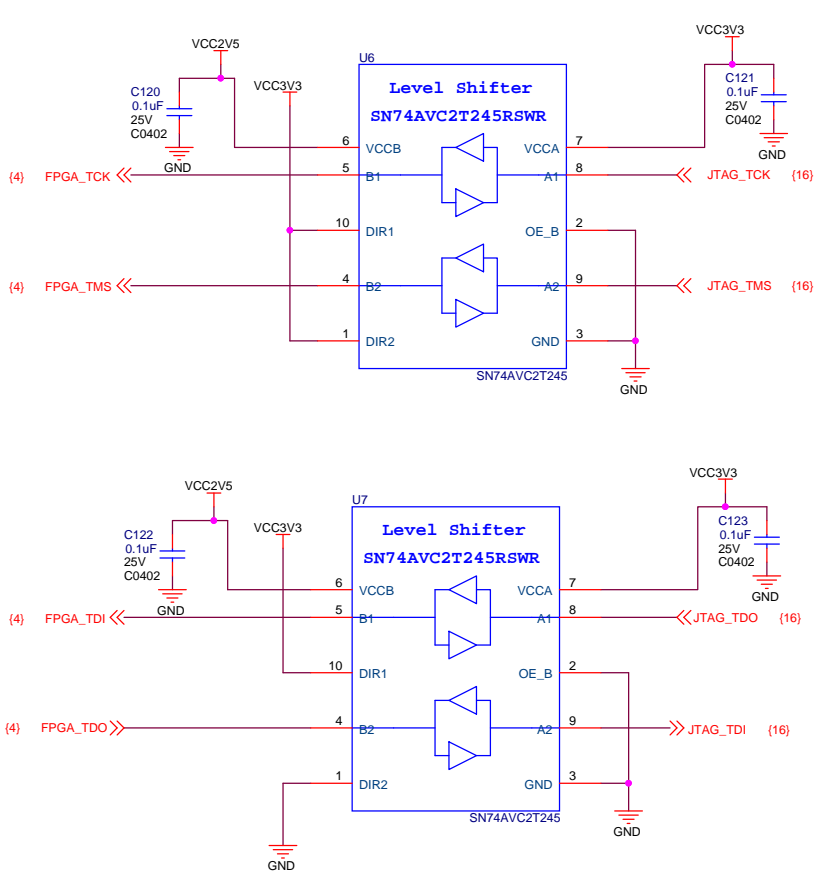
FPGA BYPASS CAPACITORS



VOLTAGE SUPERVISOR & MIO Select Jumpers



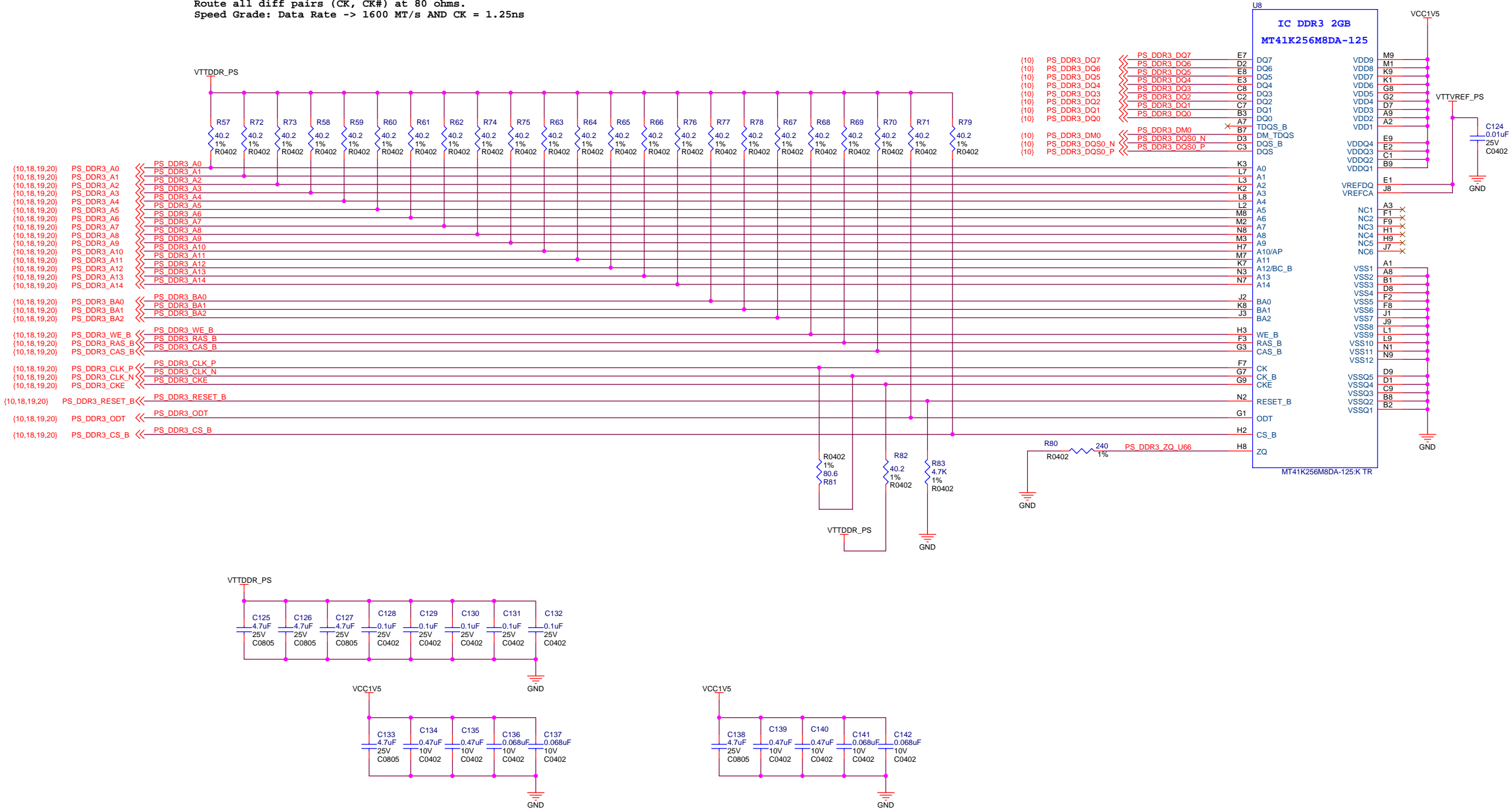
JTAG CONNECTOR



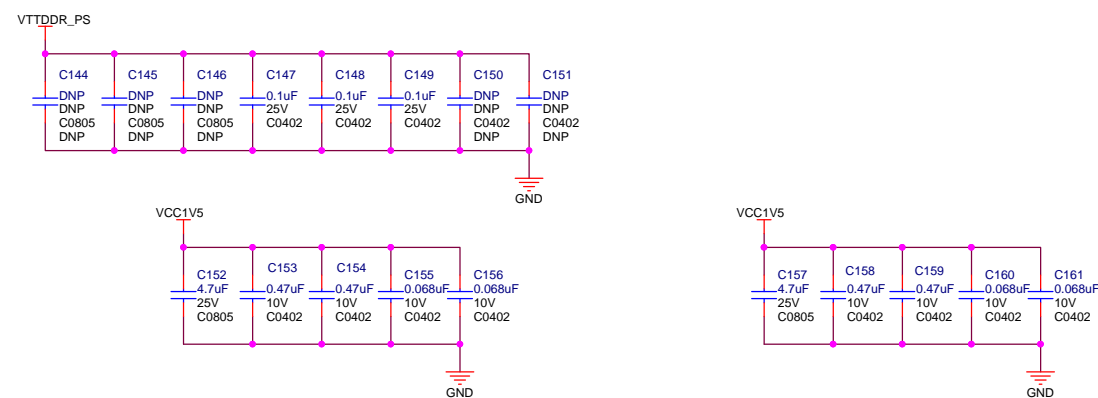
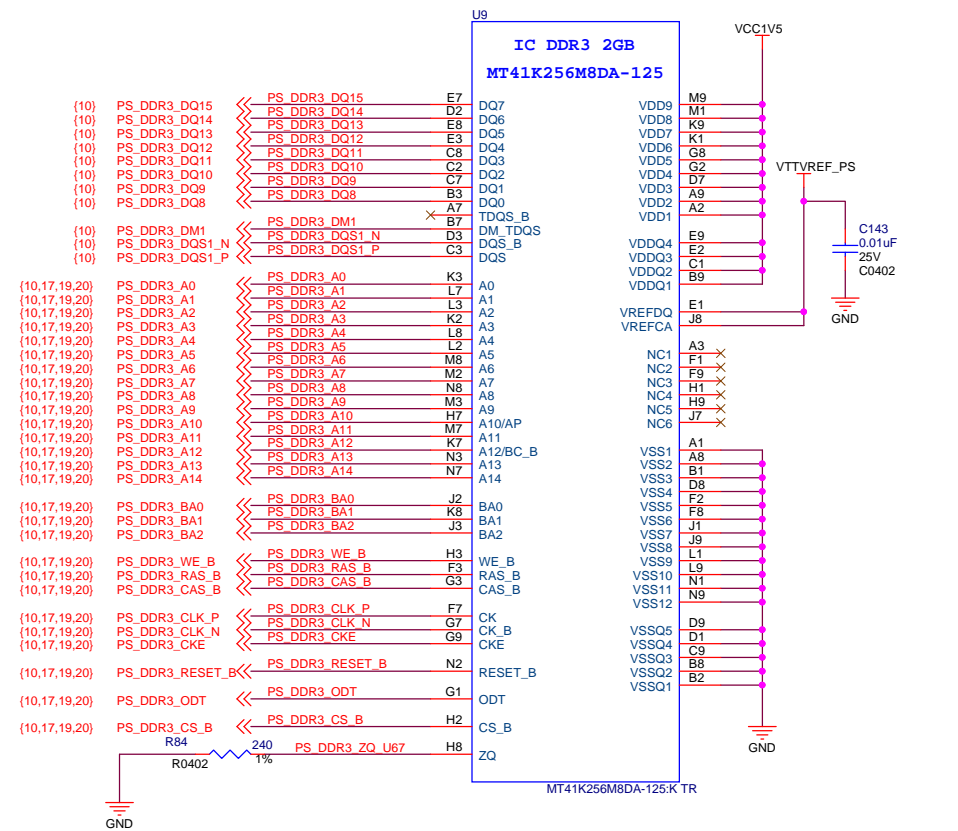
JTAG controller maximum frequency: 20 MHz

DDR3 DEVICE 1

Layout Note
Route all Data, Address and single ended signals of DDR3 at 40 ohms.
Route all diff pairs (CK, CK#) at 80 ohms.
Speed Grade: Data Rate -> 1600 MT/s AND CK = 1.25ns



DDR3 DEVICE 2



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DDR3 PS Device 1
```

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WHIZZ SYSTEMS INC.
3240 Scott Blvd, Santa Clara,
CA 95054, USA
Job # **7490**

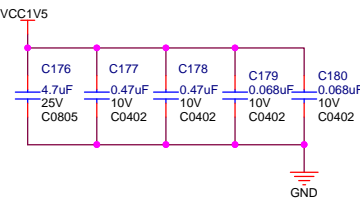
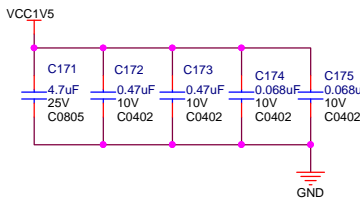
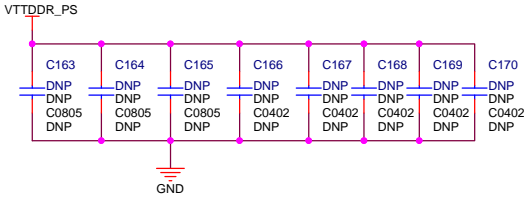
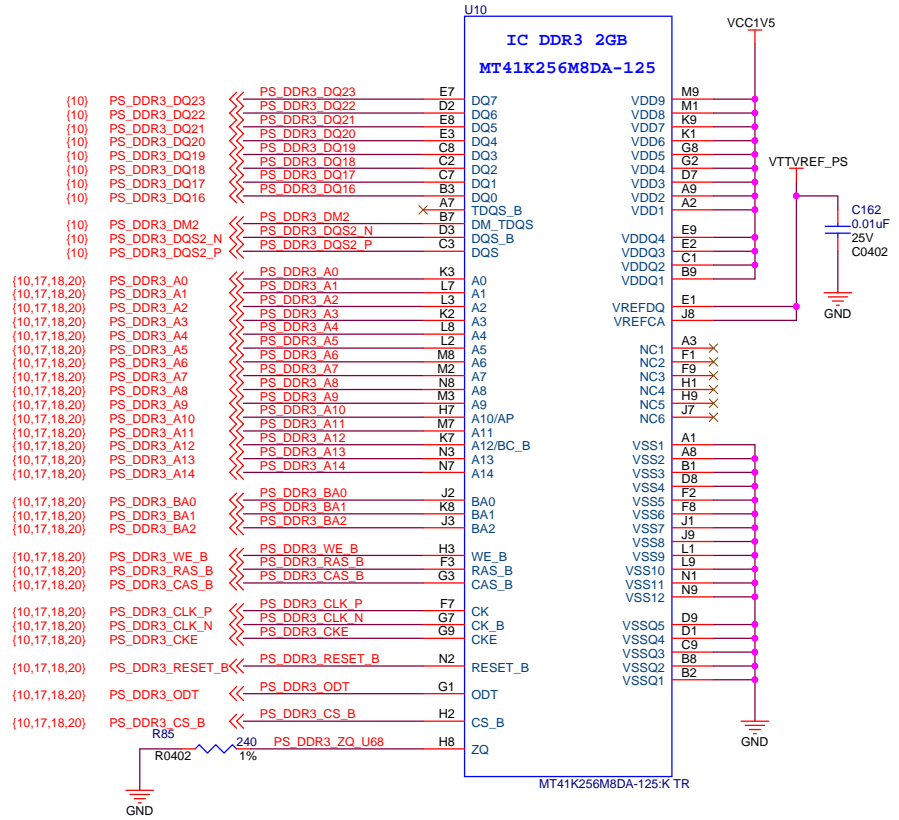
Client:	Liquid Instruments PTY. LTD.
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Title	DDR3 PS Device 1	Sch:	7490_MokuV1.0
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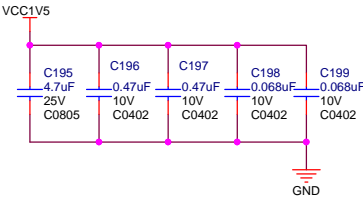
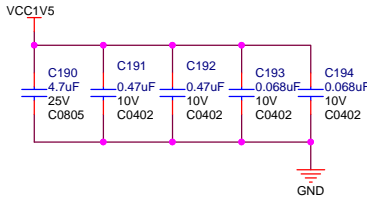
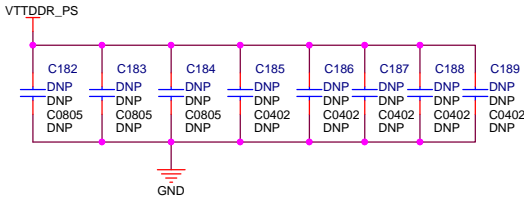
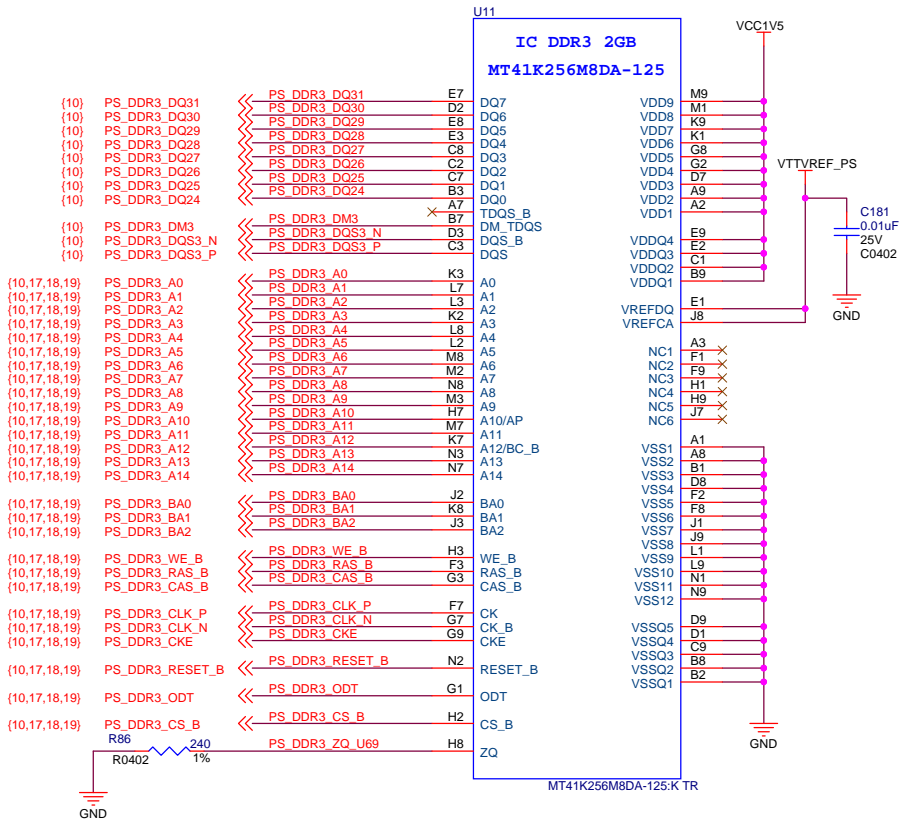
Size C	Engineer: Farooq Bhatti	Rev A
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Date: Thursday, July 09, 2015	Sheet 18 of 38
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DDR3 DEVICE 3



DDR3 DEVICE 4



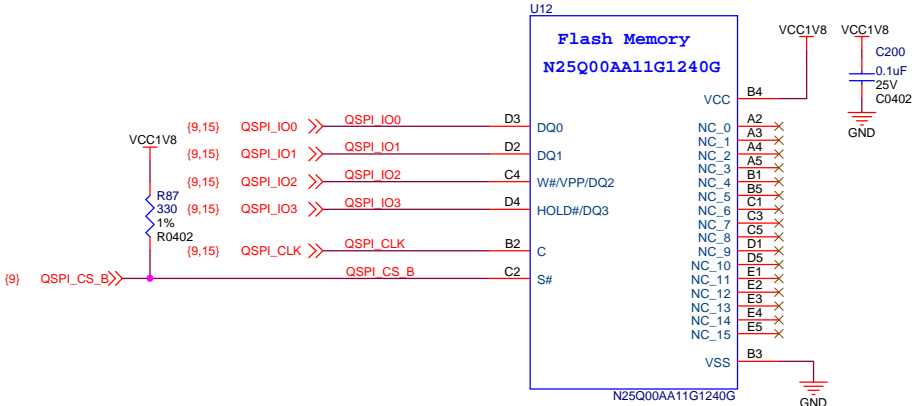
FLASH MEMORY

Layout Note

Route all QSPI signals at 50 Ohms.

Speed: Dual/quad I/O instruction provides increased throughput up to 54 MB/s

Frequency: 108 MHz (MAX) clock frequency supported for all protocols in single transfer rate (STR) mode. 54 MHz (MAX) clock frequency supported for all protocols in DTR mode



Quad SPI

Proprietary and Confidential



WHIZZ SYSTEMS INC.
3240 Scott Blvd , Santa Clara,
CA 95054, USA
Job # 7490

Client: Liquid Instruments PTY. LTD.

Title: QUAD SPI

Sch: 7490_MokuV1.0

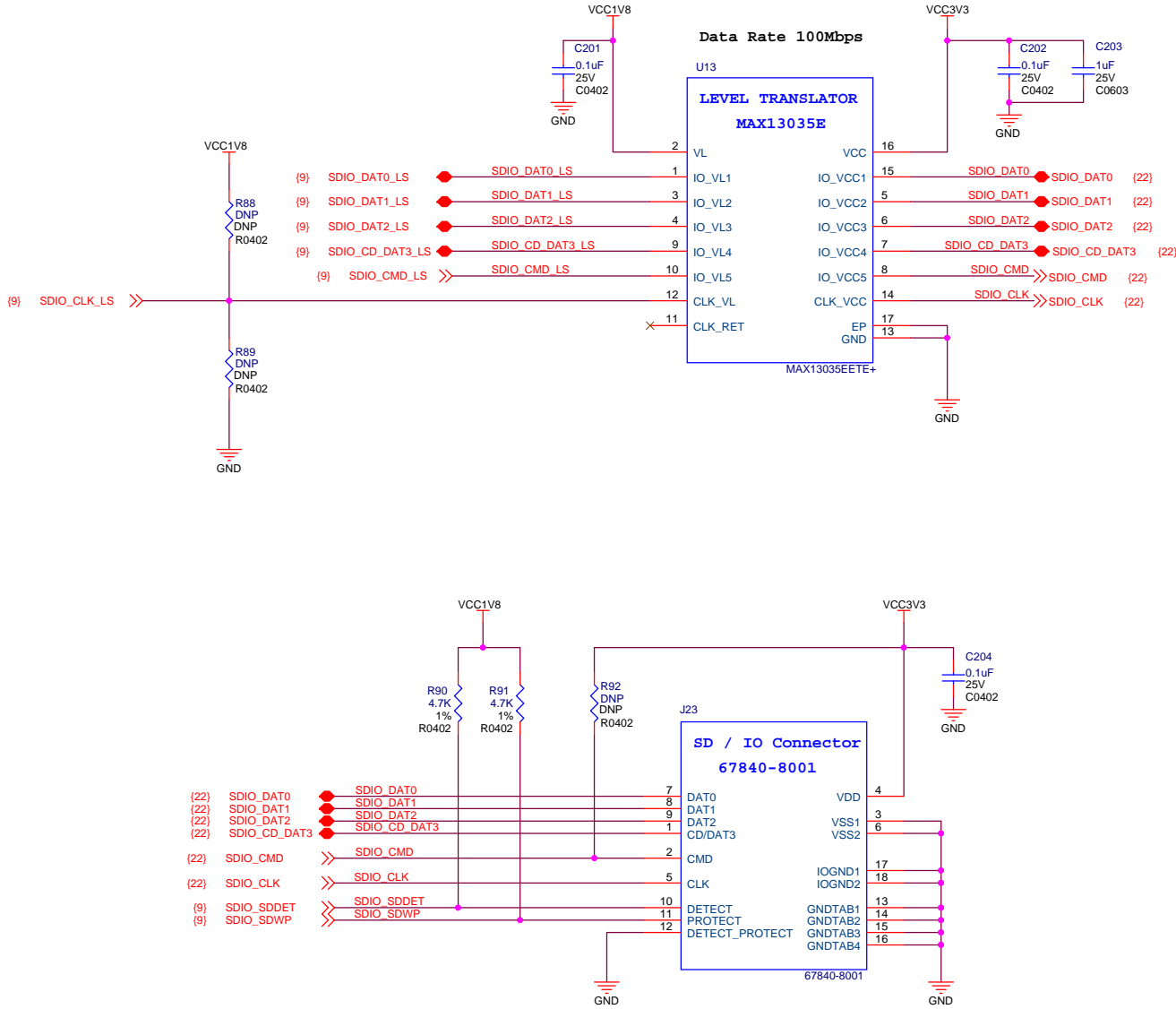
Size: C Engineer: Farooq Bhatti

Rev: A

Date: Thursday, July 09, 2015

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SD CARD



SD Card Connector

Proprietary and Confidential

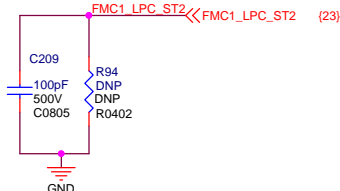
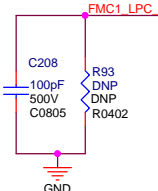
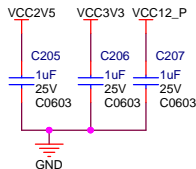
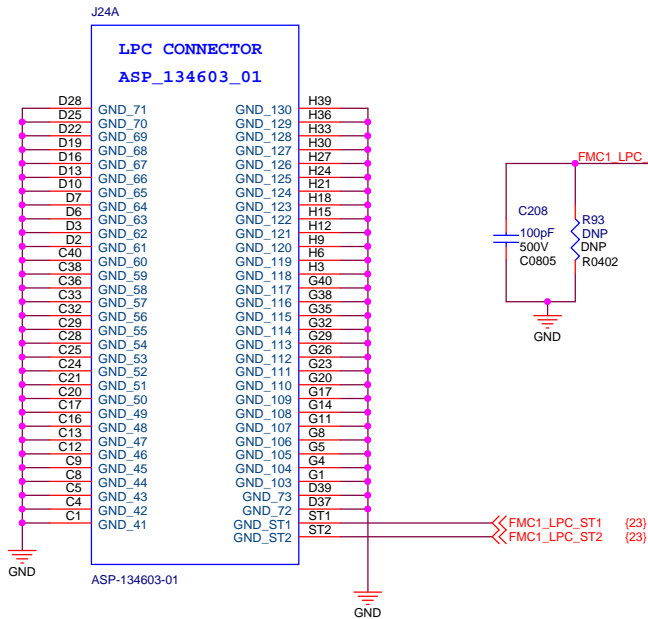
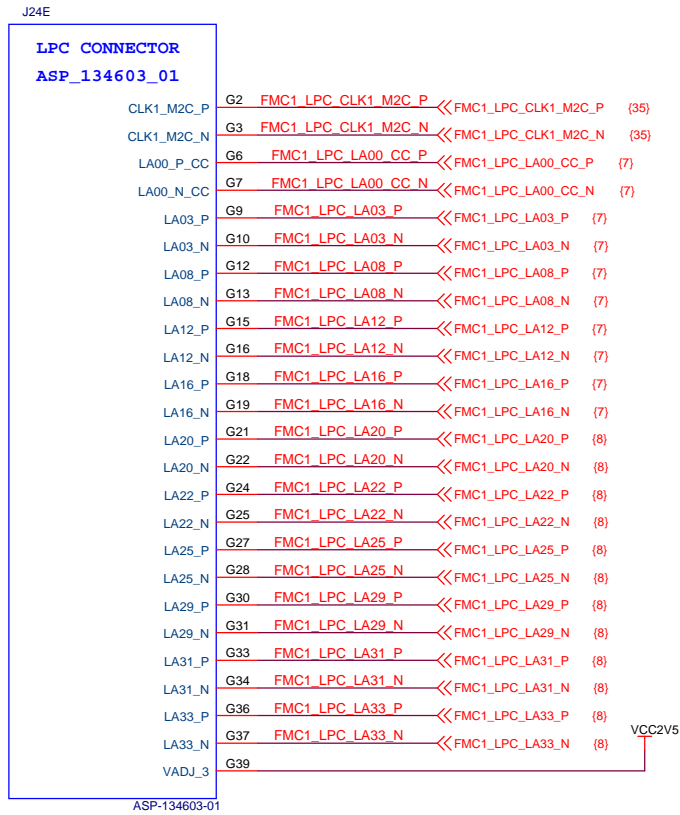
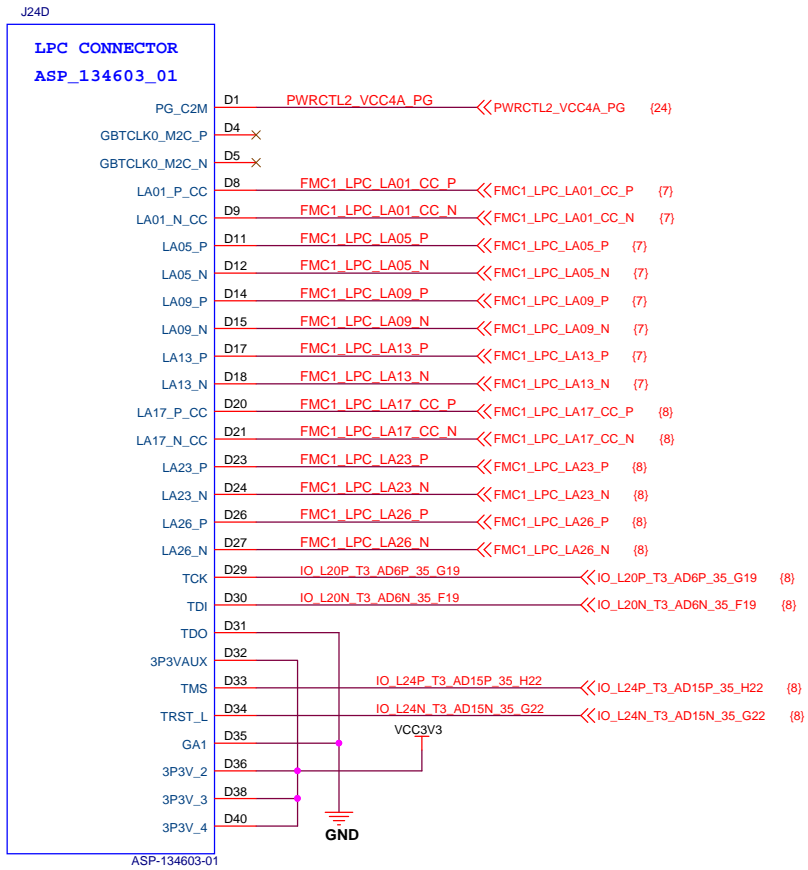
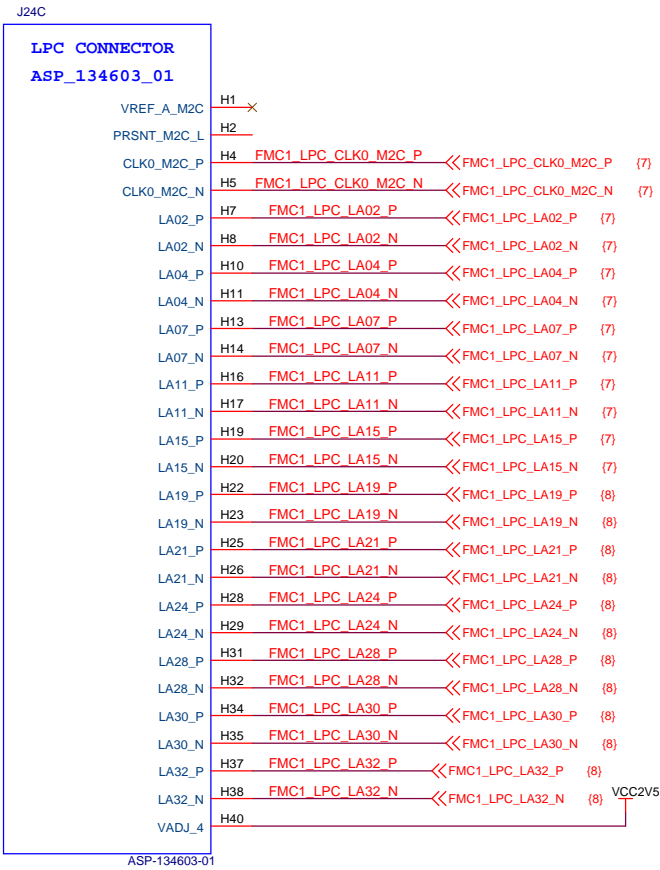
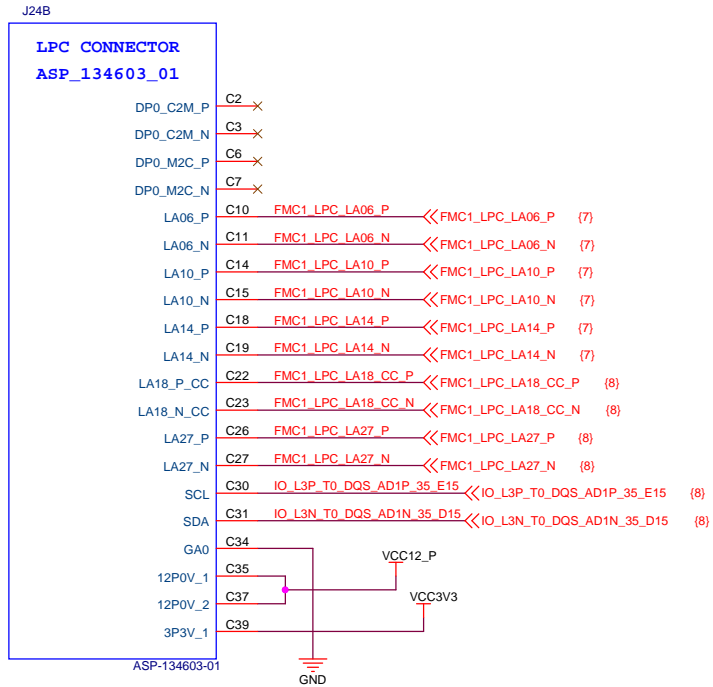



WHIZZ SYSTEMS INC.
3240 Scott Blvd, Santa Clara,
CA 95054, USA
Job # 7490

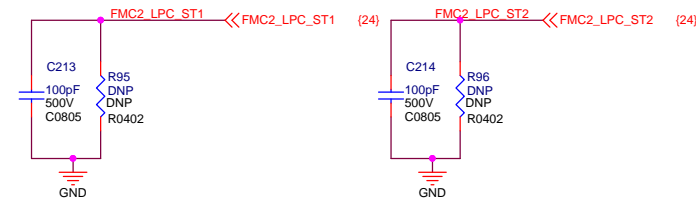
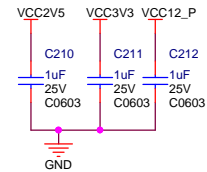
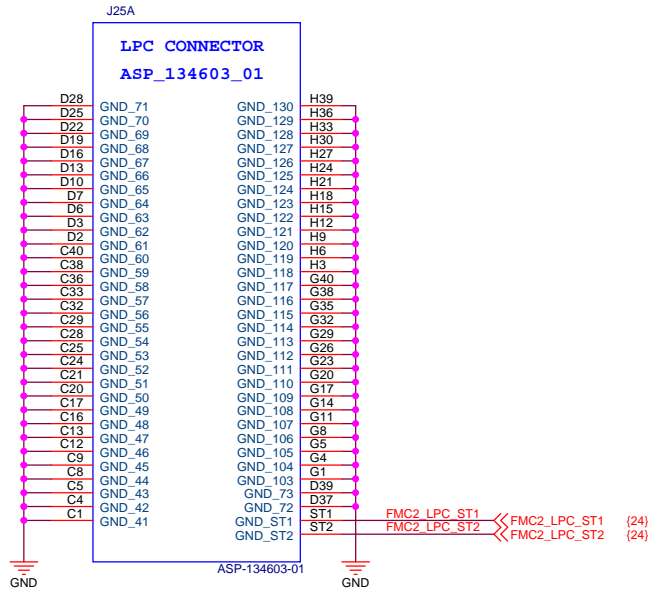
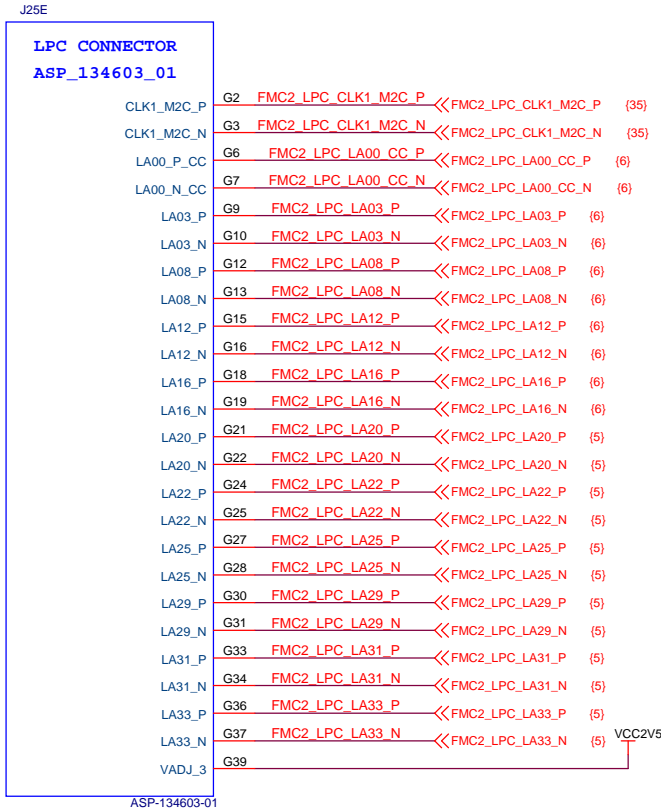
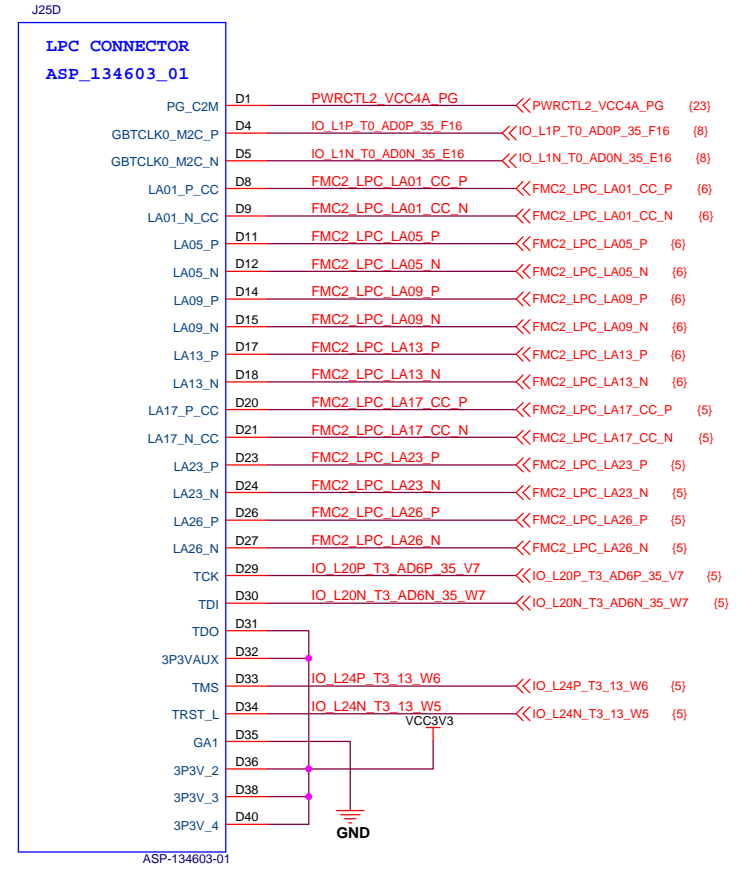
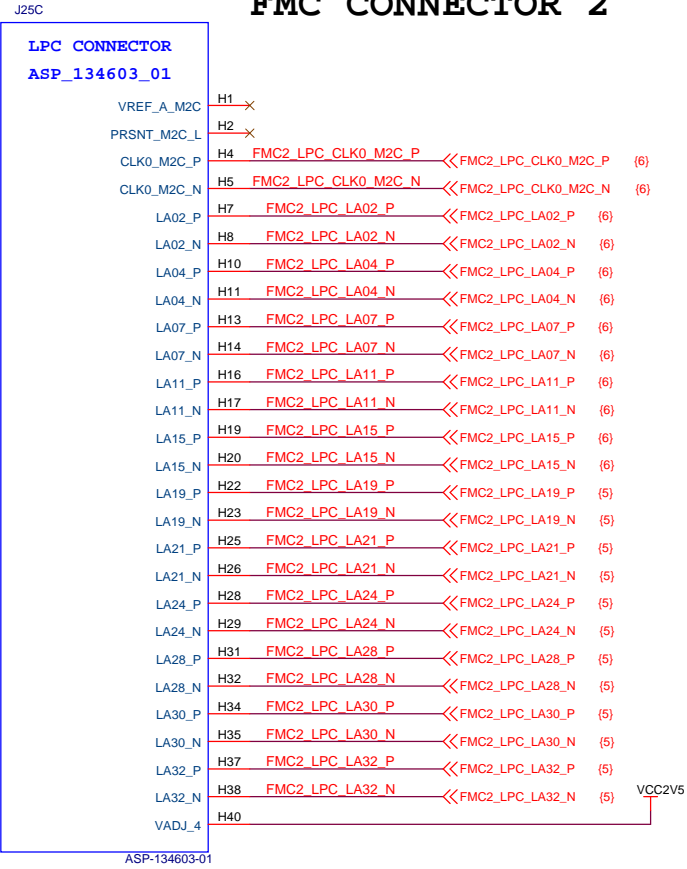
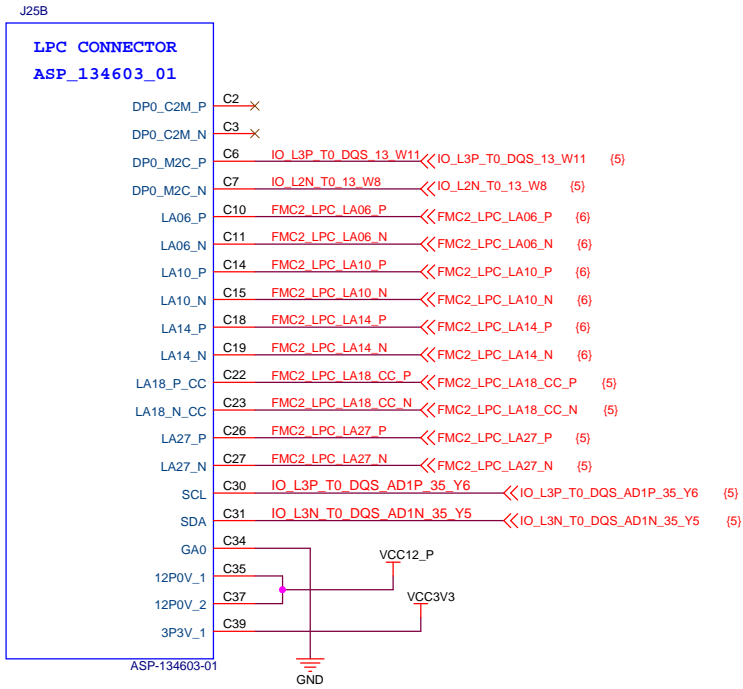
Client: Liquid Instruments PTY. LTD.


Title	SD Card Connector	Sch:	7490_MokuV1.0
Size	C	Engineer:	Farooq Bhatti
Date:	Thursday, July 09, 2015	Rev	A
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FMC CONNECTOR 1



FMC1 LPC Connector		Proprietary and Confidential	
		WHIZZ SYSTEMS INC. 3240 Scott Blvd, Santa Clara, CA 95054, USA Job # 7490	
Client: Liquid Instruments PTY. LTD.			
Title FMC1 LPC Connector		Sch: 7490_MokuV1.0	
Size C Engineer: Farooq Bhatti		Rev A	
Date: Thursday, July 09, 2015		Sheet 23 of 38	



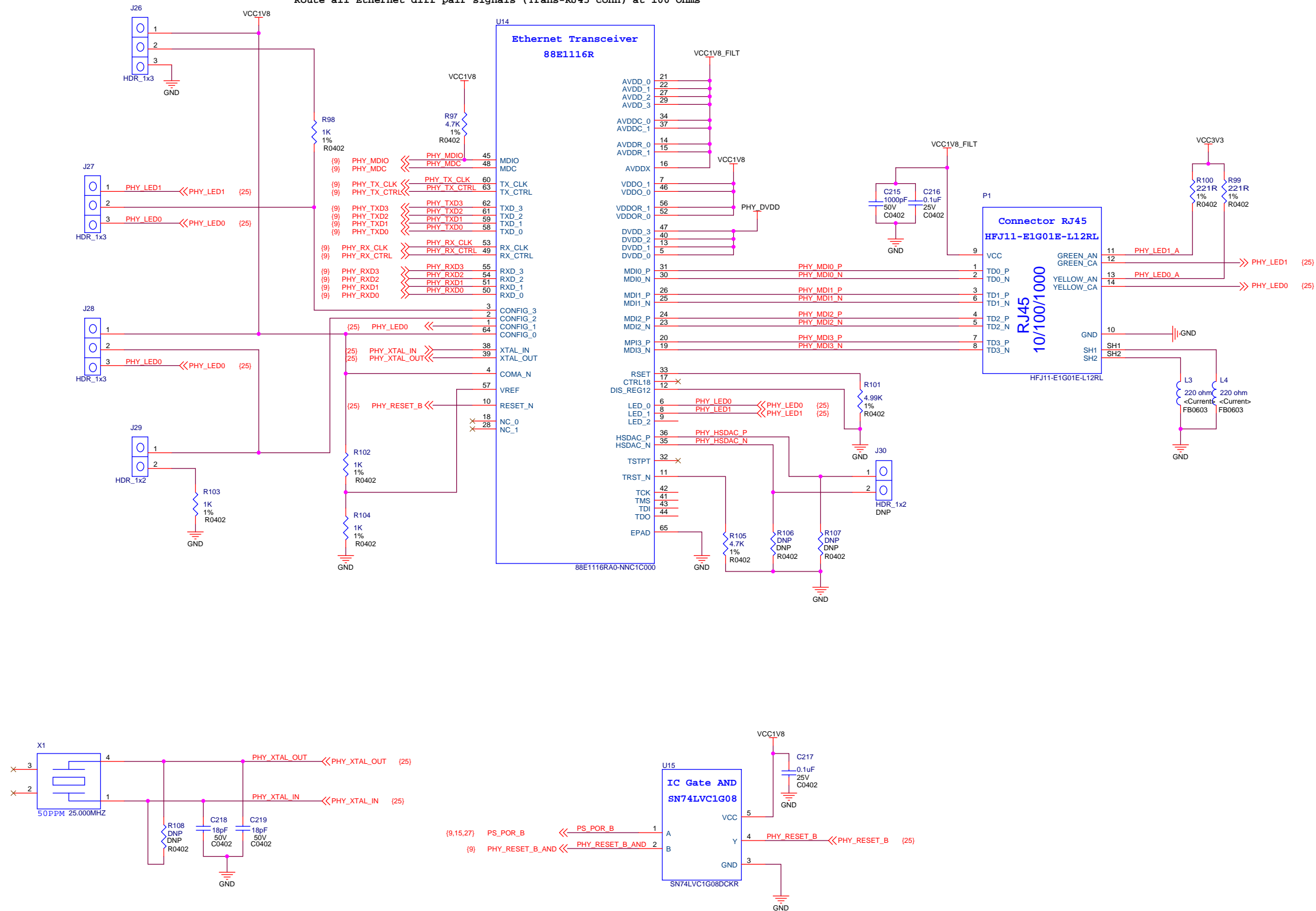
FMC2 LPC Connector			Proprietary and Confidential		
			WHIZZ SYSTEMS INC. 3240 Scott Blvd., Santa Clara, CA 95054, USA Job # 7490		
Client:			Liquid Instruments PTY. LTD.		
Title	FMC2 LPC Connector		Sch:	7490 MokuV1.0	
Size	C	Engineer:	Farooq Bhatti		Rev A
Date:	Thursday, July 09, 2015		Sheet	24 of 38	

ETHERNET TRANSCEIVER & RJ45 CONN

Layout Note

Route all Ethernet single ended signals (FPGA-Trans) at 50 Ohms

Route all Ethernet diff pair signals (Trans-RJ45 conn) at 100 Ohms



GEM / MDIO

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WHIZZ SYSTEMS INC.
3240 Scott Blvd , Santa Clara,
CA 95054, USA
Job # **7490**

Client: Liquid Instruments PTY. LTD.

Title	GEM / MDIO	Sch:	7490 MokuV1.0
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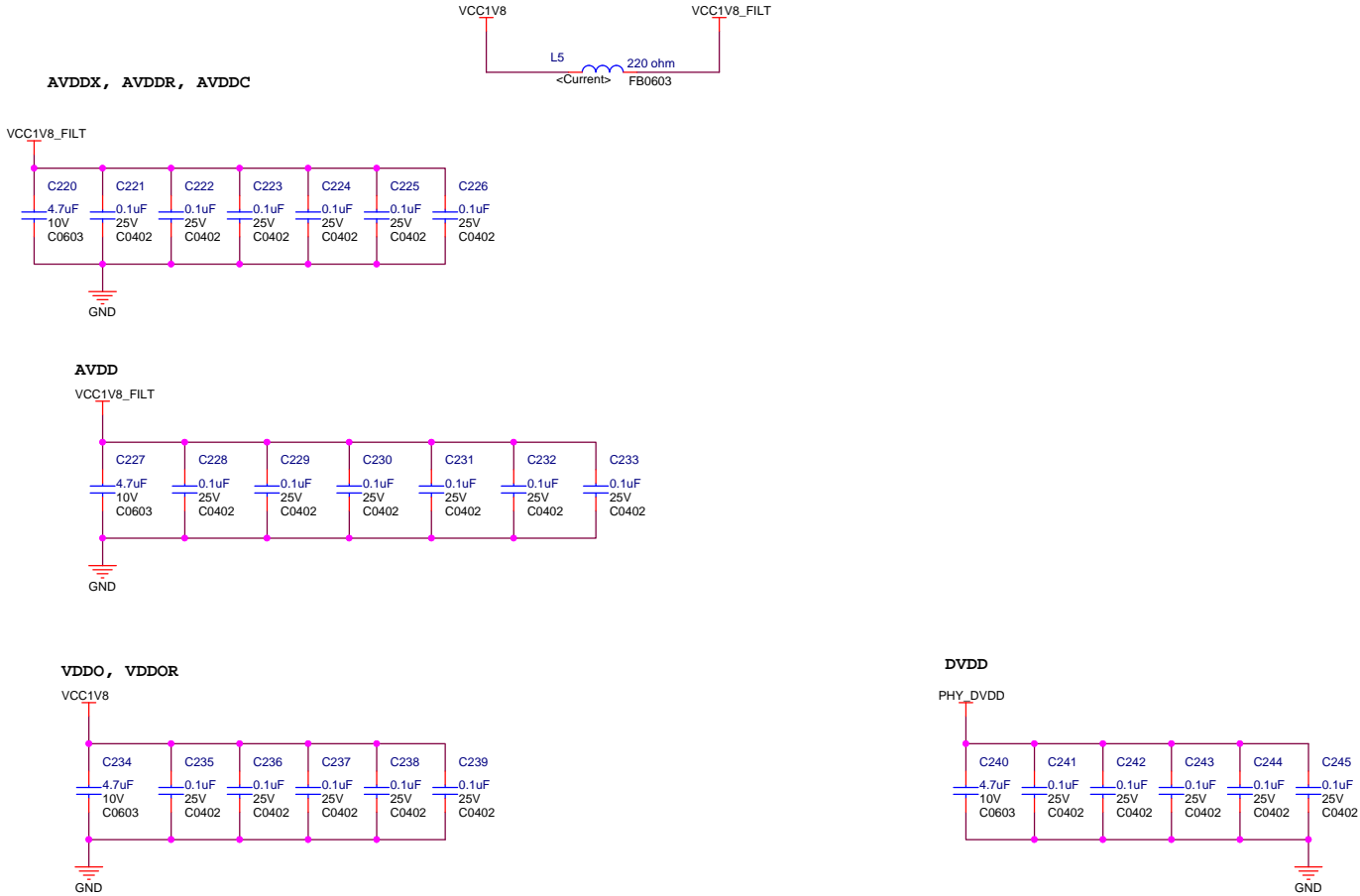
Size	C	Engineer: Farooq Bhatti
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Date: Thursday, July 09, 2015

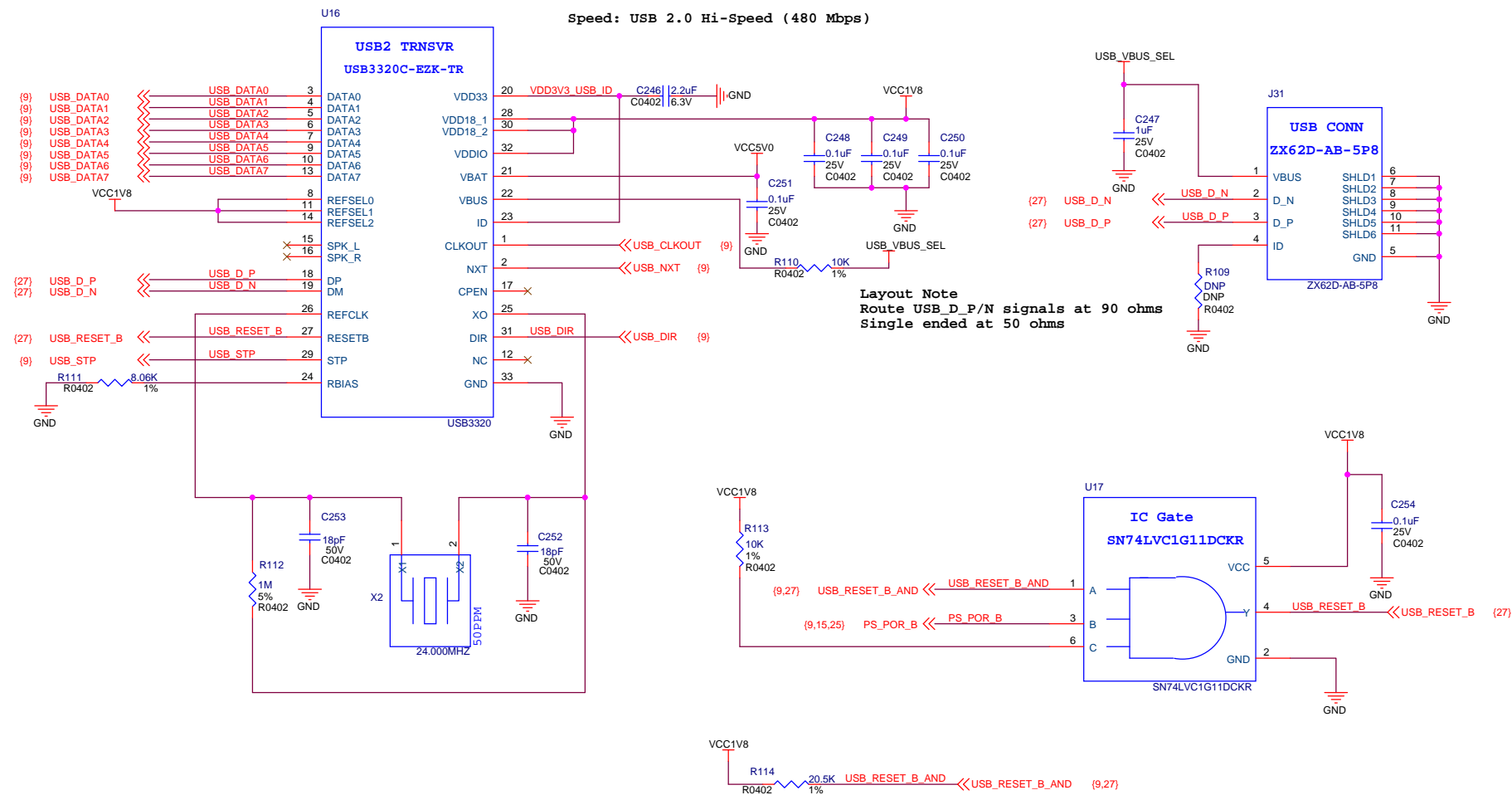
Rev **A**

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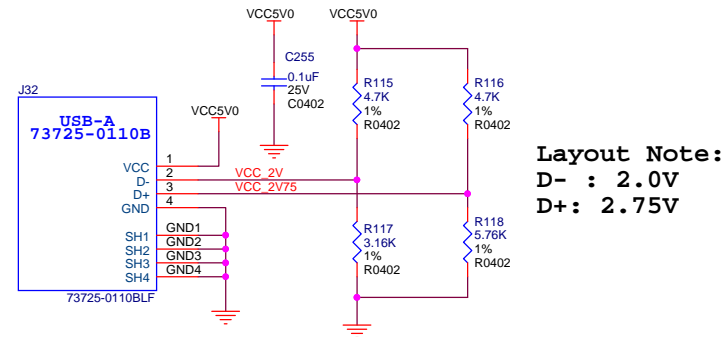
ETHERNET BYPASS CAPACITOR



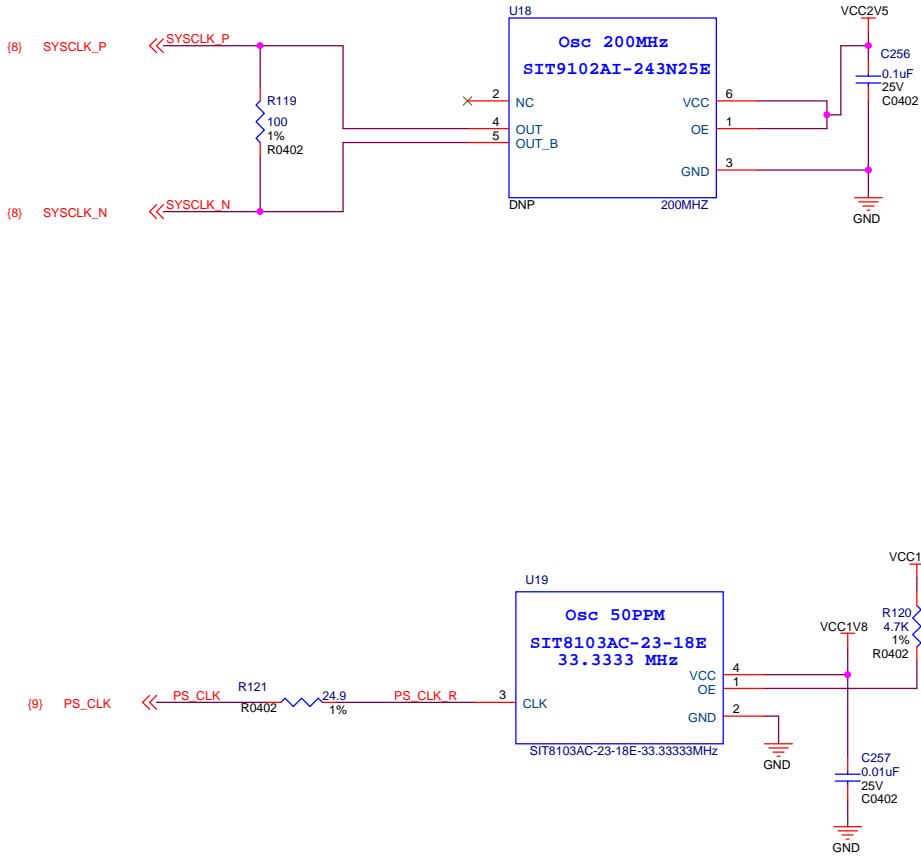
USB 2.0 TRANSEIVER & USB micro AB CONNECTOR



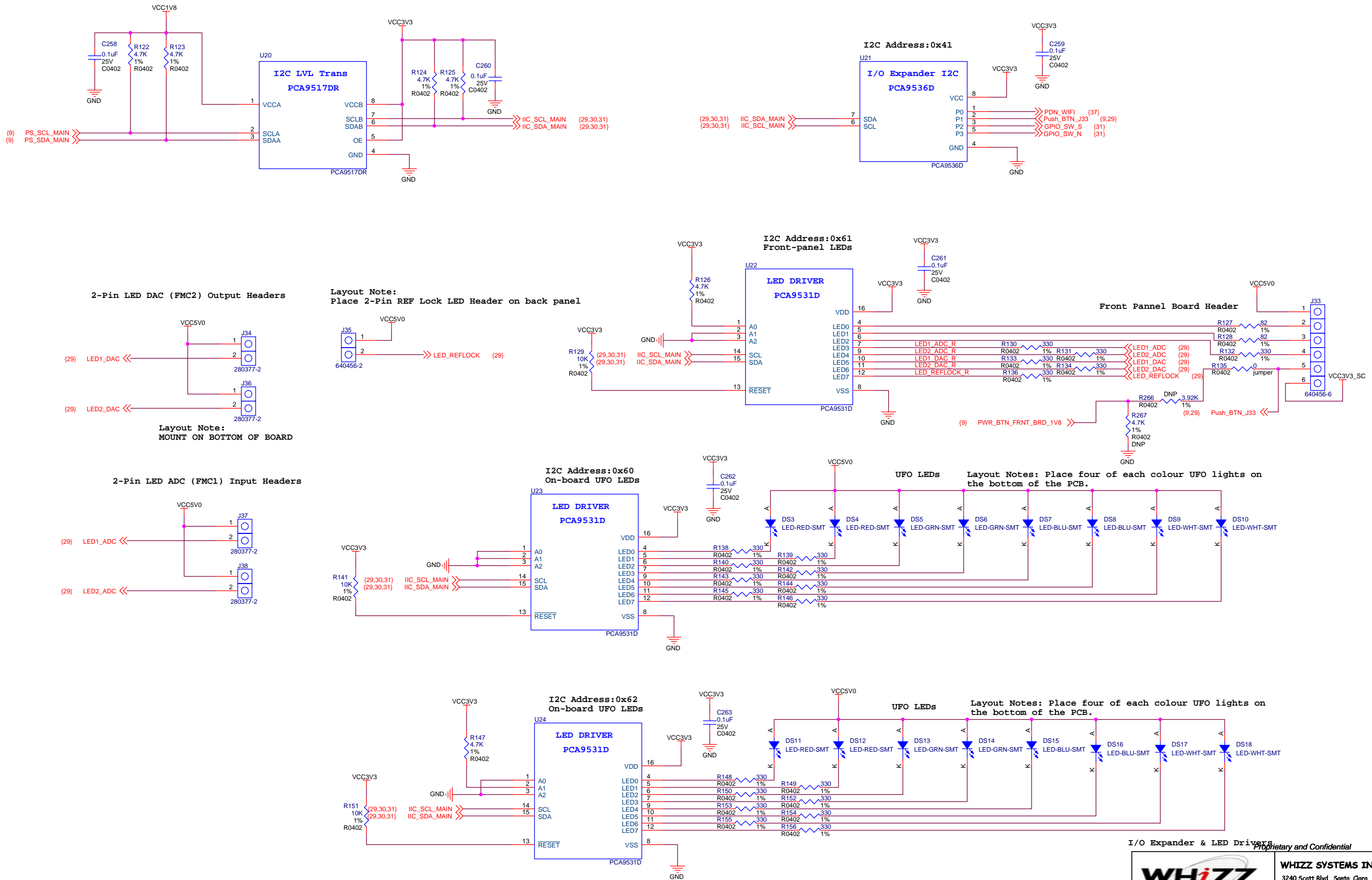
USB-A for Charging at 2000 mA



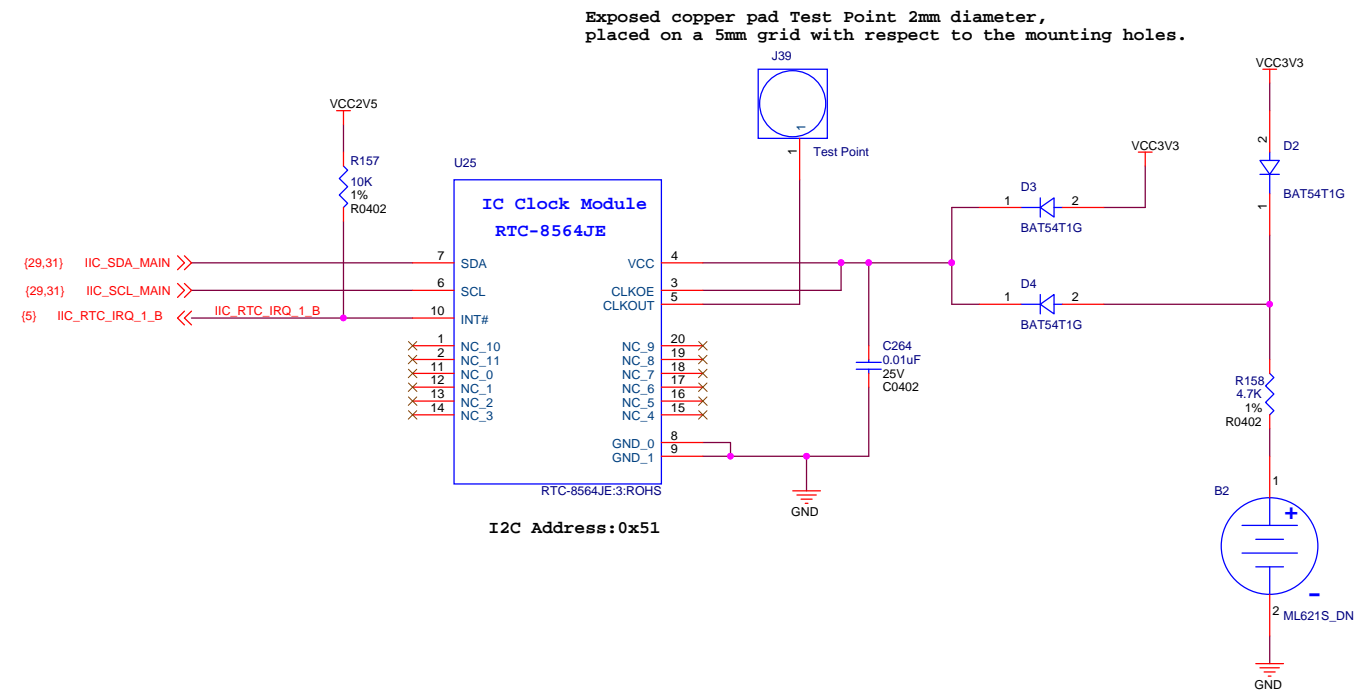
OSCILLATORS



I/O EXPANDER AND LED DRIVERS



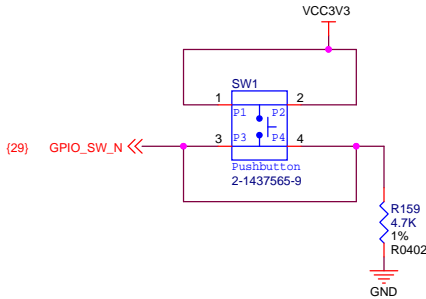
RTC CLOCK MODULE



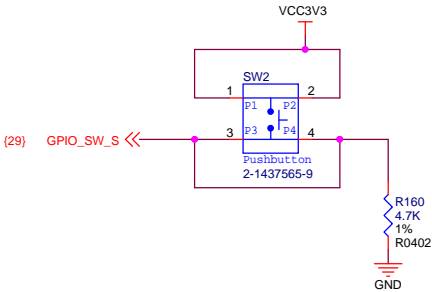
GPIO SWITCHES

Layout Note:
Place tactile switches on bottom of the board

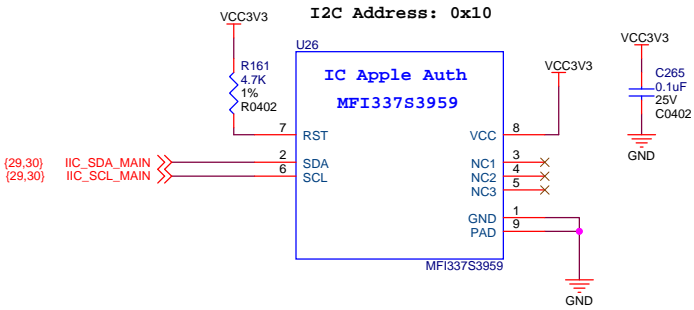
Factory Reset Button



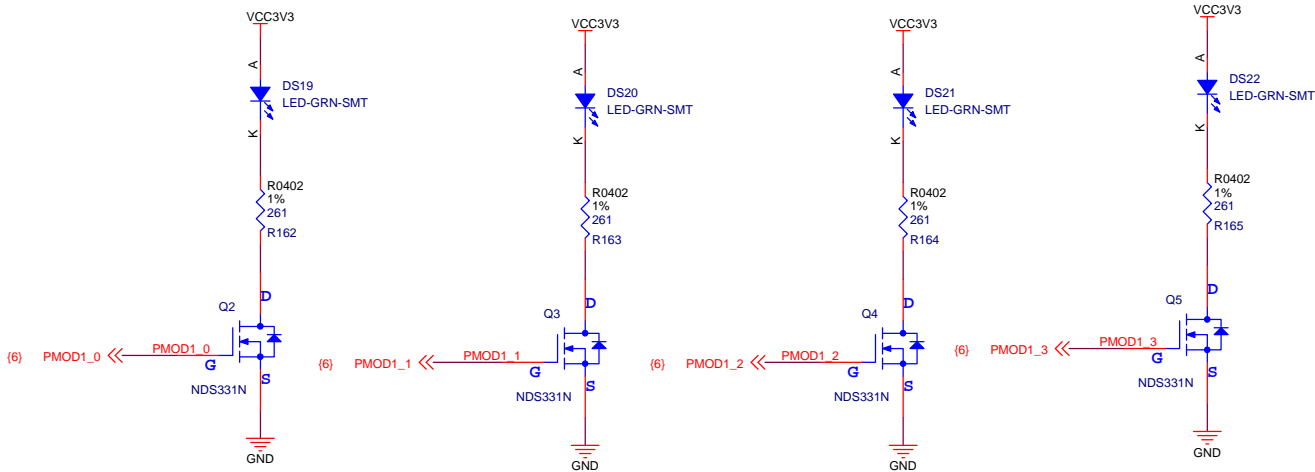
Wifi On/Off Button



Apple Auth Coprocessor

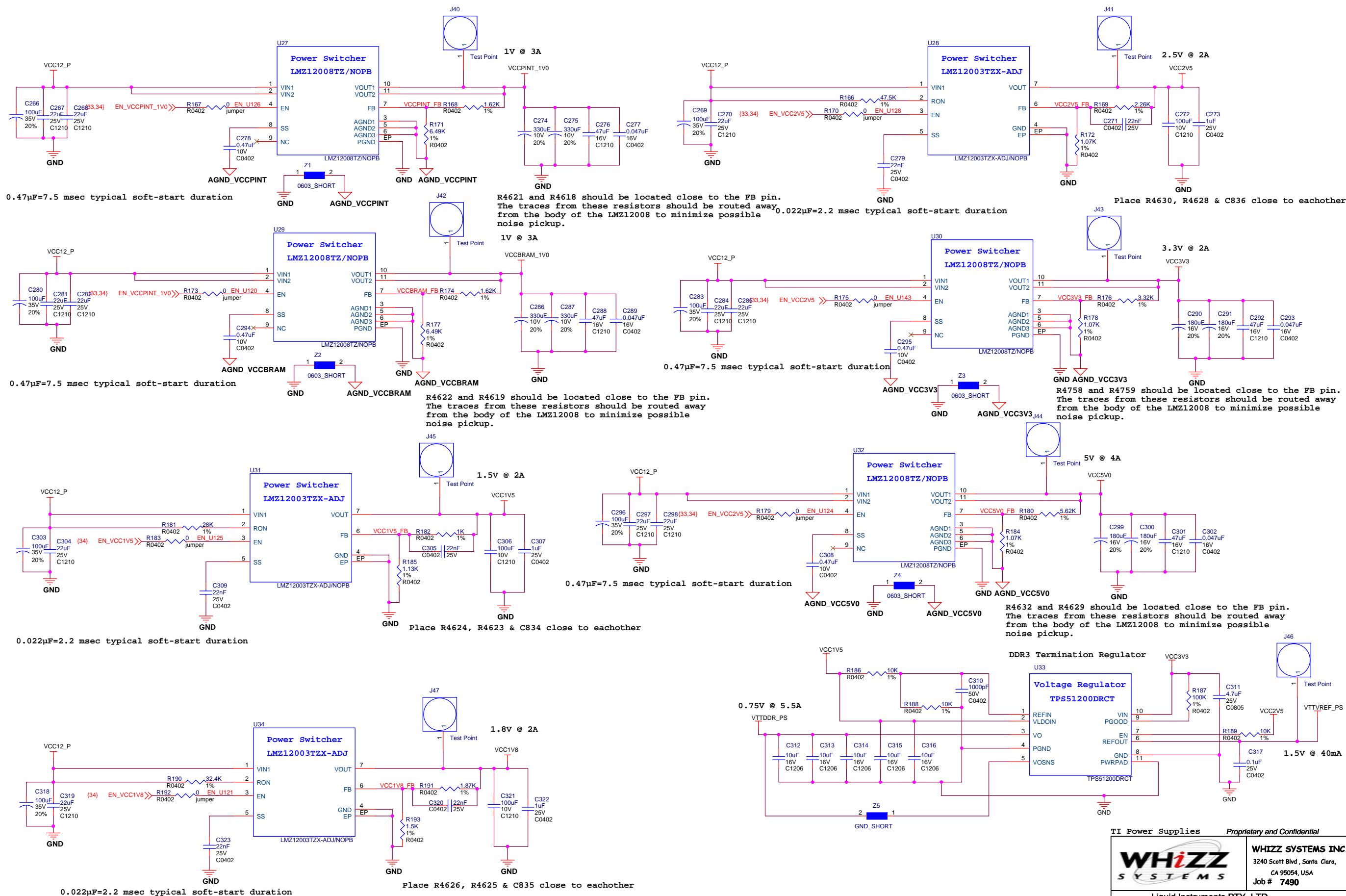


PMOD LEDS



- Have a single point ground.
- Minimize trace length to the FB pin.
- Make input and output bus connections as wide as possible.
- Provide adequate device heat-sinking.

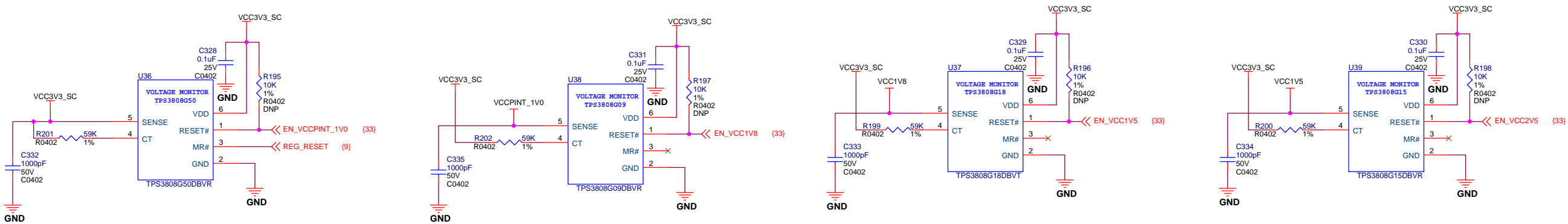
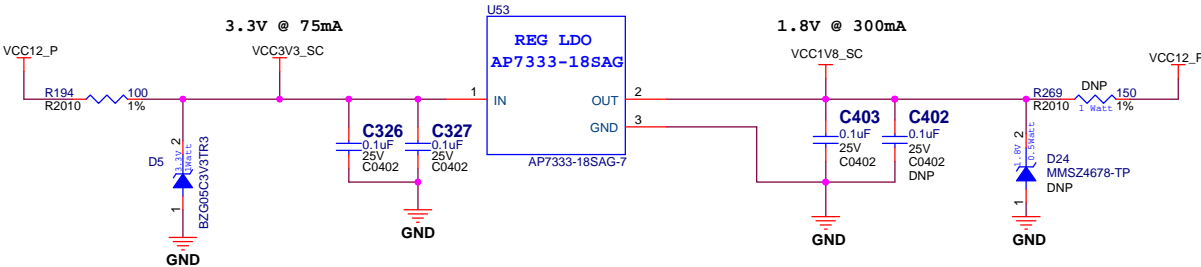
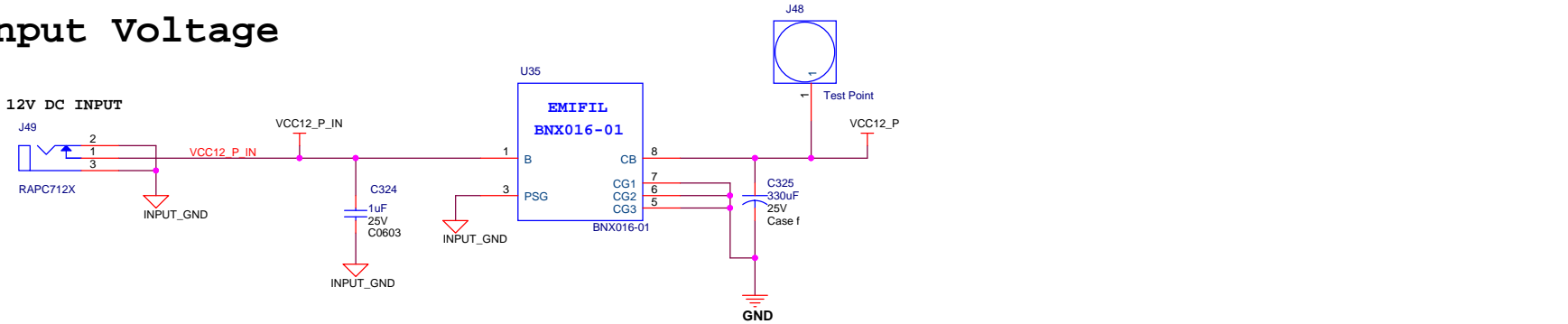
Power Regulators



Power Management/Sequencing System

Exposed copper pad Test Point 2mm diameter, placed on a 5mm grid with respect to the mounting holes.

Input Voltage



Power Sequencing
VCCPINT(VCCPINT_1V0), VCCINT/VCCBRAM(VCCBRAM_1V0) -> VCCAUX, VCCPAUX, VCCPLL(VCC1V8) -> VCCO(VCC1V5) -> VADJ(VCC2V5), VCC3V3, VCC5V0

Voltage New	Name in Design	Voltage Value	Maximum Current measured	New DC-DC design will support
VCCPINT	VCCPINT_1V0	1.0V	1.3	3
VCCO_DDR	VCC1V5	1.5V	0.6	2
VCCINT, VCCBRAM	VCCBRAM_1V0	1.0V	1.506	3
VCCMIO, VCCAUX, VCCPAUX	VCC1V8	1.8V	0.615	2
VCC3V3	VCC3V3	3.3V	0.5	2
VCC2V5, VADJ	VCC2V5	2.5V	0.35	2
VCC5V0	VCC5V0	5.0V	2.5	4

Power Connector and switch

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WHIZZ SYSTEMS INC.
3240 Scott Blvd, Santa Clara,
CA 95054, USA
Job # **7490**

Client: Liquid Instruments PTY. LTD.

Title **Power Connector and switch**

Sch: **7490_MokuV1.0**

Size **C**

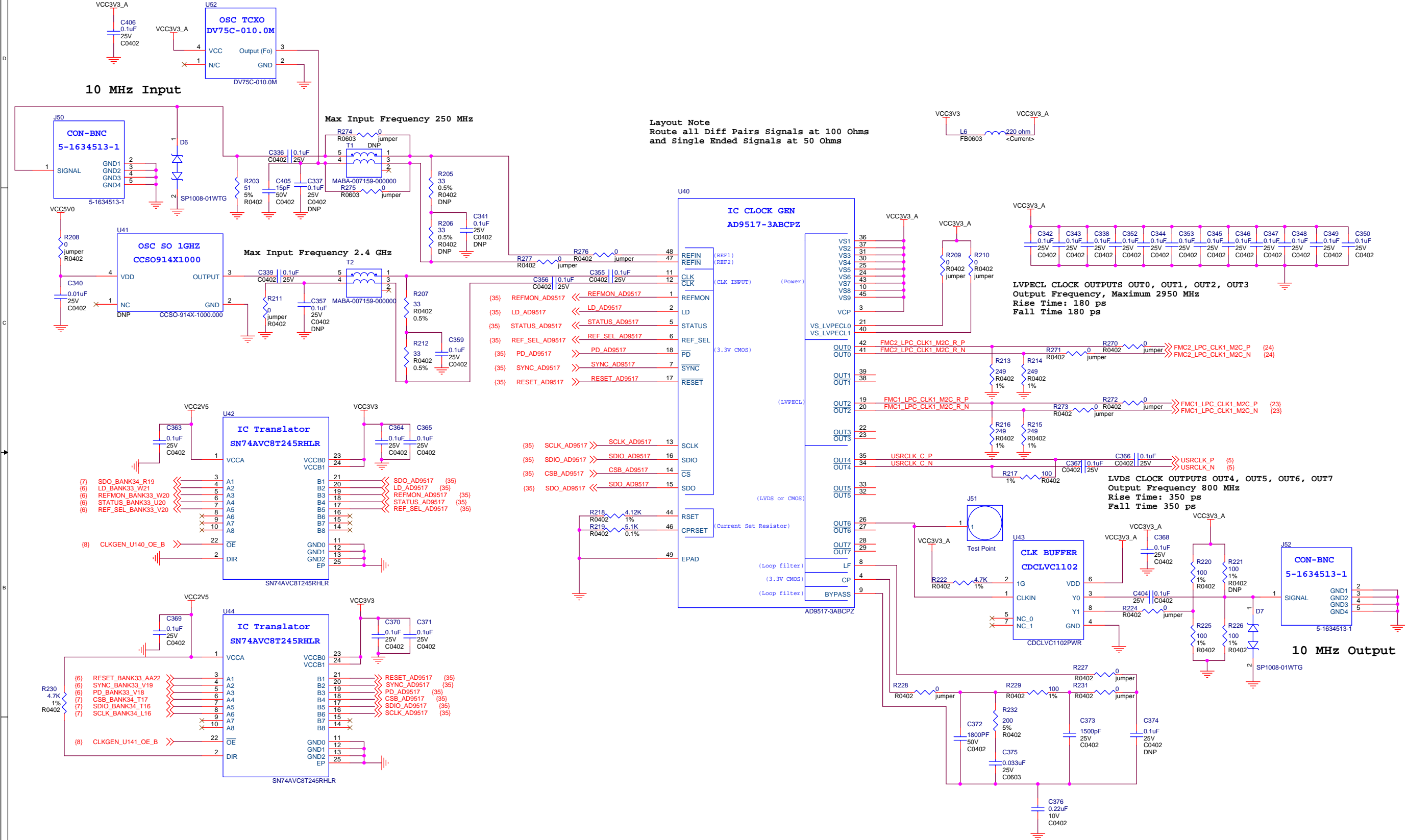
Engineer: Farooq Bhatti

Rev **A**

Date: Thursday, July 09, 2015

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CLOCK GENERATOR BUFFER CIRCUIT



Clock Generator

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WHIZZ SYSTEMS INC.
3240 Scott Blvd., Santa Clara,
CA 95054, USA
Job # 7490

Client: Liquid Instruments PTY. LTD.

Title: Clock Gen

Sch: 7490 MokuV1.0

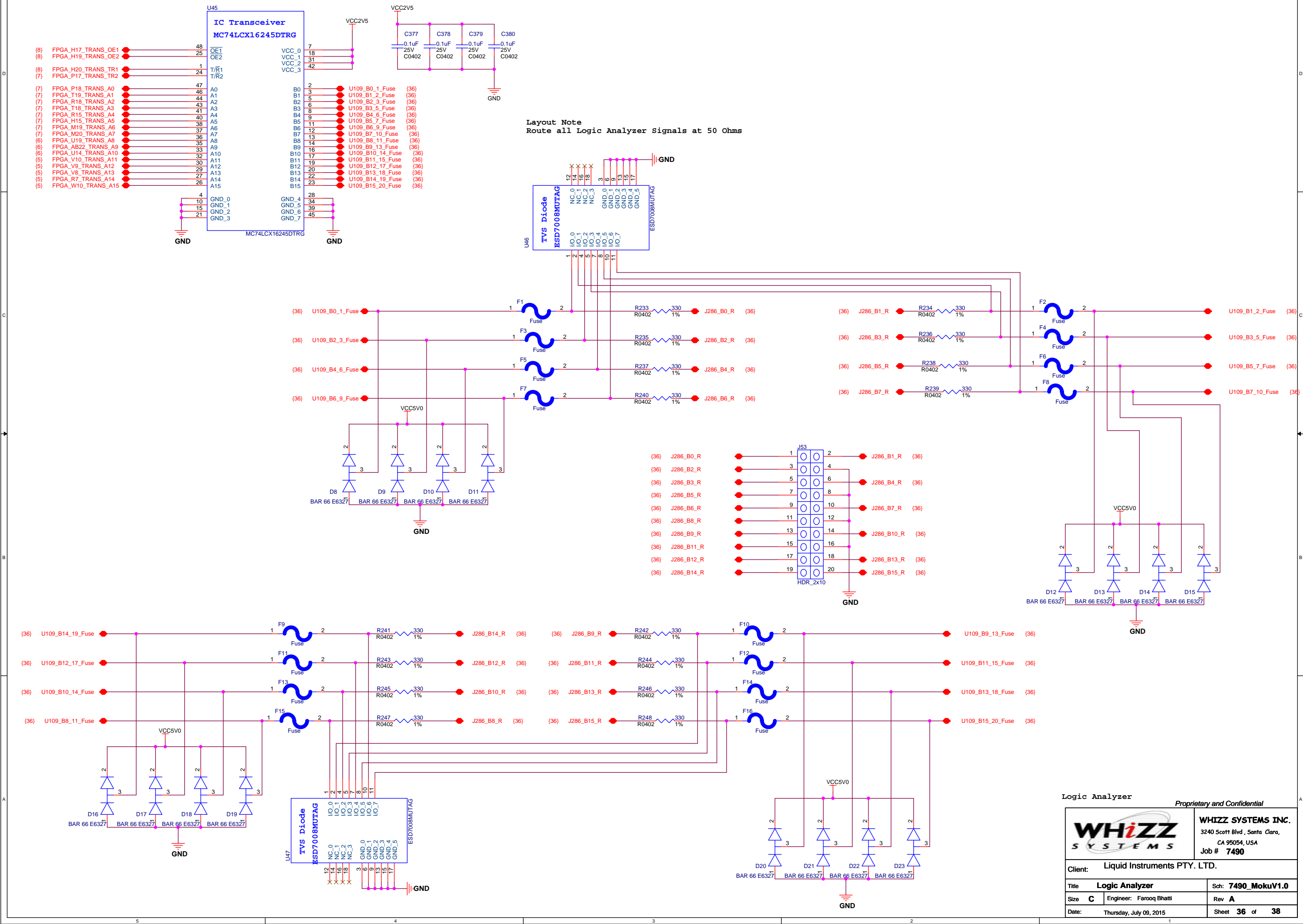
Size: C Engineer: Farooq Bhatti

Rev: A

Date: Thursday, July 09, 2015

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LOGIC ANALYZER



Logic Analyzer

WHIZZ SYSTEMS INC.
3240 Scott Blvd , Santa Clara,
CA 95054, USA
Job # **7490**

Client: Liquid Instruments PTY. LTD.

Title **Logic Analyzer**

Sch: **7490_MokuV1.0**

Size **C** Engineer: Farooq Bhatti

Rev **A**

Date: Thursday, July 09, 2015

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WiFi/Bluetooth Module

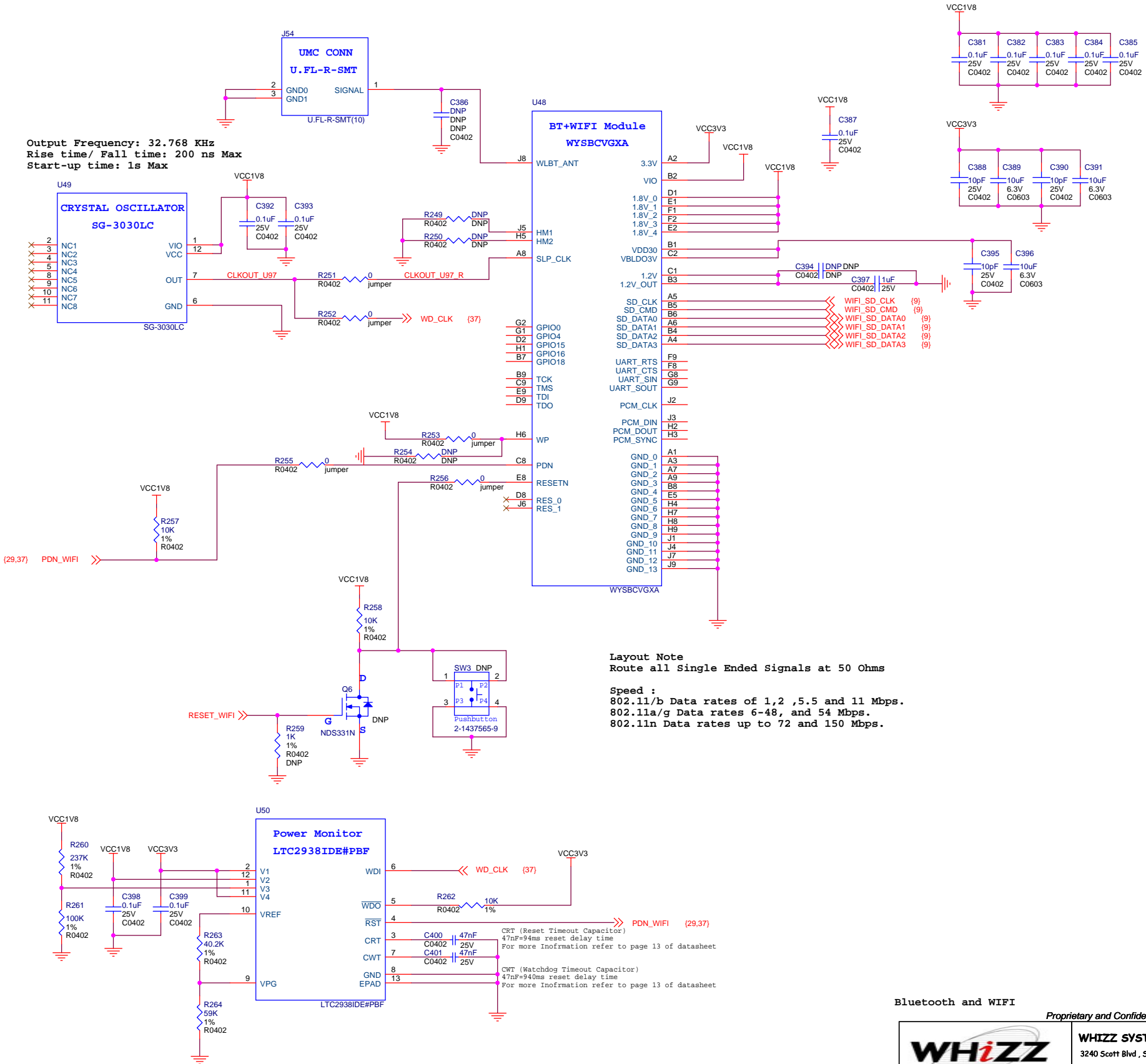


Table 1. Voltage Threshold Modes

MODE	V1 (V)	V2 (V)	V3 (V)	V4 (V)	R1 (kΩ)	R2 (kΩ)	V _{PD} /V _{REF}
0	5	3.3	3.3	Open	Short	0	
1	5	3.3	ADJ	-ADJ	93.1	9.53	0.094
2	3.3	2.5	ADJ	ADJ	86.6	16.2	0.156
3	3.3	2.5	ADJ	-ADJ	78.7	22.1	0.219
4	3.3	1.8	1.5	ADJ	71.5	28	0.281
5	5	3.3	2.5	ADJ	66.5	34.8	0.344
6	5	3.3	2.5	1.8	59	40.2	0.406
7	3.3	1.8	1.5	1.2	53.6	47.5	0.469
8	3.3	1.8	1.2	ADJ	47.5	53.6	0.531
9	3.3	1.8	ADJ	ADJ	40.2	59	0.594
10	3.3	2.5	1.8	1.5	34.8	66.5	0.656
11	3.3	2.5	1.8	ADJ	28	71.5	0.719
12	3.3	1.8	ADJ	-ADJ	22.1	78.7	0.781
13	3.3	1.5	ADJ	ADJ	16.2	86.6	0.844
14	5	3.3	1.8	ADJ	9.53	93.1	0.906
15	3.3	1.2	ADJ	ADJ	Short	Open	1

Bluetooth and WIFI

Proprietary and Confidential



WHIZZ SYSTEMS INC.
3240 Scott Blvd, Santa Clara,
CA 95054, USA
Job # 7490

Client: Liquid Instruments PTY. LTD.

Title: Bluetooth and wifi

Sch: 7490_MokuV1.0

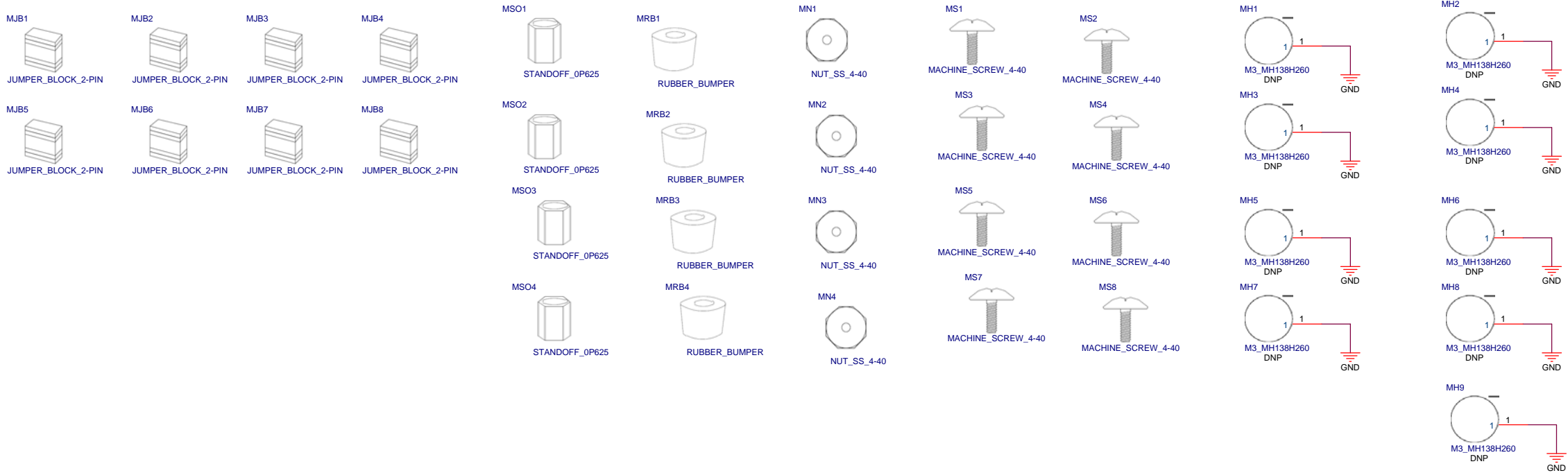
Size: C Engineer: Farooq Bhatti

Rev: A

Date: Thursday, July 09, 2015


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MECHANICAL COMPONENTS



Mechanical

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WHIZZ SYSTEMS INC.
3240 Scott Blvd , Santa Clara,
CA 95054, USA
Job # **7490**

Client: Liquid Instruments PTY. LTD.

Title Mechanical		Sch: 7490_MokuV1.0
Size C	Engineer: Farooq Bhatti	Rev A
Date: Thursday, July 09, 2015	Sheet 38 of 38	