



Aug.2013

BCM20732S Embedded Antenna BLE SIP Module





REVISION HISTORY

Version No.	Revised Date	Revised by	Description
1.0	2013-Aug 2	КМ	Preliminary specification released
	70		
740			
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1. Introduction

1.1 Description

The highly integrated BCM20732S requires minimal external components to make a standalone (ARM CortexTM-M3 built-in) BLE device in a very compact form factor (6.5 mm × 6.5 mm x 1.2 mm Max., 48-LGA package).

This data sheet provides a description of interfaces, pin assignments, and specifications of BCM20732S (Bluetooth Low Energy) Module. This is a document for designers responsible for adding the BCM20732S (Bluetooth Low Energy) Module to wireless input device applications including heart-rate monitors, blood-pressure monitors, proximity sensors, temperature sensors, and battery monitor.

The following profiles are supported in ROM:

- Battery status
- Blood pressure monitor
- Find me
- Heart rate monitor
- Proximity
- Thermometer
- Weight scale
- Time
- BGM (Blood Glucose Monitor)

Additional profiles that can be supported from RAM include:

- Blood glucose monitor
- Temperature alarm
- Location
- Other custom profiles

Features

MCU

Memory capacity

Diverse serial interface

Sensor applications support

On-chip functionality Single-chip

Frequency Band

Network Standard

Operating Temperature

MSL level 3

Certification



32bit Cortex™-M3

Embedded 512Kbits EEPROM

ADC, I2C, GPIO,PWM

MAC/BB/RF

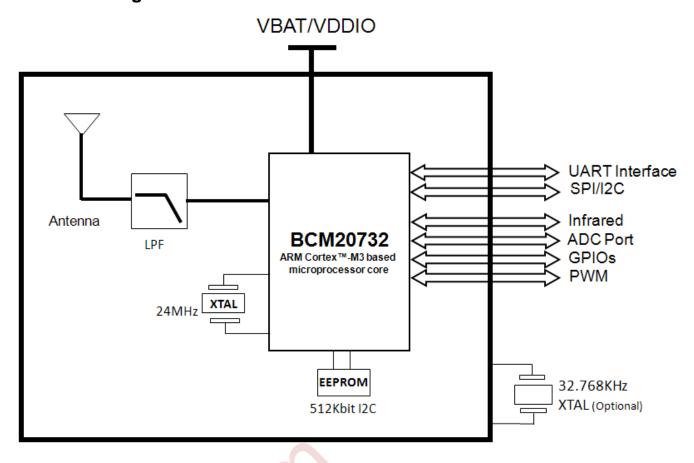
2.4 GHz

Bluetooth low energy

-40°C to 85°C

FCC and **CE** compliant

2. Block Diagram



ADC Analog to Digital Converter

12C Intelligent Interface Controller

SPI Serial Peripheral Interface

UART Universal synchronous/asynchronous receiver transmitters

3. Electrical Specification

3.1 Absolute Maximum Rating

Supply Power Storage Temperature	Max +4 Volt - 40° to 125° Celsius		
Voltage ripple	+/- 2%	Max. Values not exce voltage	eeding Operating
	Power	min	Max
Power Supply Absolute Maximum Ratings	VBAT		3.8

3.2 Recommendable Operation Condition

3.2.1 Temperature, Humidity

The BCM20732S module complies with the operational requirements as listed in the table below.

Operating Temperature	-40° to 85° Celsius	
Humidity range	Max 95%	Non condensing, relative humidity

3.2.2 Voltage

Power supply for the BCM20732S module will be provided by the host via the power pins

Symbol	Parameter	Min	Тур	Max	Unit
VBAT		1.62		3.63	V

3.3 Current Consumption

3.3.1

Condition: Condition: 25deg.C

Item	Condition	Min	Nom	Max	Unit
Receive	Receiver and baseband are both operating, 100%		23		mA
Transmit	Transmitter and baseband are both operating, 100%		20		mA
Deep Sleep	Wakeup on interrupt		1.27		uA
Active idle (average)			30		uA

Note: Current consumption includes that from components (EEPROM. X-tal etc.) on the SIP

4. RF Specification

4.1 wireless Specification

The RF performance of BCM20732S is given as follows. The default voltage is 3.3V.

Parameter	Mode and Conditions	Min.	Тур.	Max.	Unit
Receiver Section					
Frequency range		2402	-	2480	MHz
RX sensitivity (standard)	Packets: 200, Payload: PRBS 9, Length: 37 Bytes, Dirty Transmitter: off. PER: 30.8%	-	-94	-	dBm
Maximum input		-10		-	dBm

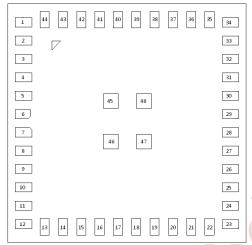
4.2 RF Transmitter Specification

Parameter	Mode and Conditions	Min.	Тур.	Max.	Unit
Transmitter Section					
Frequency range	-	2402	-	2480	MHz
Output power adjustment range	-	-20	-	10	dBm
Output power	-	-	2		dBm
Output power variation	-	-	2.5		dB
LO Performance					
Initial carrier frequency tolerance	-	-	-	±150	KHz
Frequency Drift		•	•	-	
Frequency drift	-	-	-	±50	kHz
Drift rate	-	-	-	20	kHz/50 μs
Frequency Deviation		•	•	-	
Average deviation in payload		225		275	kHz
(sequence used is 00001111)	_	225	_	2/3	KLIZ
Average deviation in payload	_	185	_	_	kHz
(sequence used is 10101010)	_	100			KI IZ
Channel spacing	-	-	2	-	MHz

^{*&}quot; indicates BT4.0 specification
*" Measurement by connected

5. Pin Definition

5.1 Pin Number sequence definition



TOP View

5.2 The detail pin definition information

	Pin Name	I/O Type	Description
Pin#1	GPIO: P27 PWM1		Default Direction: Input After POR State: Input Floating Alternate Function Description: 1- SPI_2: MOSI (master and slave) Current: 16 mA
Pin#2	GND	GND	GND
Pin#3	VBAT		Battery Supply Input.
Pin#4	GND	GND	GND
Pin#5	GND	GND	GND
Pin#6	GND	GND	GND
Pin#7	GND	GND	GND
Pin#8	GND	GND	GND
Pin#9	GND	GND	GND
Pin#10	BT ANT	1/0	Reserved Antenna Port for Bluetooth Tx/Rx, when using external antenna.
Pin#11	GND	GND	GND
Pin#12	GND	GND	GND
Pin#13	GND	GND	GND

	Pin Name	I/O Type	Description
Pin#14	GND	GND	GND
Pin#15	GND	GND	GND
Pin#16	GND	GND	GND
Pin#17	GND	GND	GND
Pin#18	UART_RX	ı	UART_RX, this pin has been pulled down via 10K ohm inside module.
Pin#19	UART_TX	O PU	UART_TX
Pin#20	GND	GND	GND
Pin#21	SCL	I/O PU	Clock signal for an external I2C device
Pin#22	SDA	I/O PU	Data signal for an external I2C device
Pin#23	GND	GND	GND
Pin#24	GND	GND	GND
Pin#25 Pin#26	GPIO: P1	I	Default Direction: Input This pin was tied to WP pin of internal EEPROM inside module. After POR State: Input Floating Alternate Function Description: 1- A/D converter input 2- Peripheral UART: puart_rts 3- SPI_2: MOSO (master and slave) 4- IR_TX Test mode control High: test mode Let it floating if not used. This Pin was connected to GND via 10K internally.
Pin#27	RESET_N	I/O PU	Active-low system reset with open-drain output
Pin#28	GPIO: PO	2	Default Direction: Input After POR State: Input Floating Alternate Function Description: 1- A/D converter input 2- Peripheral UART: puart_tx 3- SPI_2: MOSI (master and slave) 4- IR_RX 5- 60Hz_main
Pin#29	GND	GND	GND

	Pin Name	I/O Type	Description
			Default Direction: Input
			After POR State: Input Floating
Pin#30	GPIO: P3		Alternate Function Description:
			1- Peripheral UART: puart_cts
			2- SPI_2: SPI_CLK (master and slave)
			Default Direction: Input
			After POR State: Input Floating
Pin#31	GPIO: P2		Alternate Function Description:
PIII#31	GPIO. PZ		1- Peripheral UART: puart_rx
			2- SPI_2: SPI_CS (slave only)
			3- SPI_2: SPI_MOSI (master only)
			Default Direction: Input
			After POR State: Input Floating
Pin#32	GPIO: P4	DIO. D4	Alternate Function Description:
FIII#32	GP10. P4		1- Peripheral UART: puart_rx
			2- SPI_2: MOSI (master and slave)
			3- IR_TX
			Default Direction: Input
			After POR State: Input Floating
Pin#33	GPIO: P8		Alternate Function Description:
			1- A/D converter input
			2- External T/R switch control: ~tx_pd
			Default Direction: Input
			After POR State: Input Floating
			Alternate Function Description:
Pin#34	GPIO: P33		1- A/D converter input
			2- SPI_2: MOSI (slave only)
			3- Auxiliary clock output: ACLK1
			4- Peripheral UART: puart_rx

	Pin Name	I/O Type	Description
			Default Direction: Input
			After POR State: Input Floating
			Alternate Function Description:
			1- A/D converter input
Pin#35	GPIO: P32		2- SPI_2: SPI_CS (slave only)
			3- SPI_1: MISO (master only)
			4- Auxiliary clock output: ACLK0
			5- Peripheral UART: puart_tx
			Default Direction: Input
			After POR State: Input Floating
Pin#36	GPIO: P25		Alternate Function Description:
			1- SPI_2: MISO (master and slave)
			2- Peripheral UART: puart_rx
			Default Direction: Input
	GPIO: P24		After POR State: Input Floating
Pin#37			Alternate Function Description:
1 1111137			1- SPI_2: SPI_CLK (master and slave)
			2- SPI_1: MISO (master only)
			3- Peripheral UART: puart_tx
Pin#38	GND	GND	GND
	GPIO: P13		Default Direction: Input
	PWM3		After POR State: Input Floating
			Alternate Function Description:
			1- A/D converter input
GPIO: P28 Default Direction: Input			Default Direction: Input
Pin#39	PWM2		After POR State: Input Floating
	Alternate Function Description:		
			1- A/D converter input
			2- LED1
			3- IR_TX
			Current: 16mA

	Pin Name	I/O Type	Description			
	GPIO: P14		Default Direction: Input			
	PWM2		After POR State: Input Floating			
			Alternate Function Description:			
			1- A/D converter input			
Pin#40			Default Direction: Input			
			After POR State: Input Floating			
	GPIO: P38		Alternate Function Description:			
	GF10. F38		1- A/D converter input			
			2- SPI_2: MOSI (master and slave)			
			3- IR_TX			
			Default Direction: Input			
Pin#41			After POR State: Input Floating			
	GPIO: P15		Alternate Function Description:			
	GPIO: P15		1- A/D converter input			
			2- IR_RX			
			3- 60 Hz_main			
	GPIO: P26		Default Direction: Input			
	PWM0		After POR State: Input Floating			
			Alternate Function Description:			
Pin#42			1- SPI_2: SPI_CS (slave only)			
			2- SPI_1: MISO (master only)			
			Current: 16 mA			
			Default Direction: Input			
			After POR State: Input Floating			
	GPIO: P12		Alternate Function Description:			
			1- A/D converter input			
Pin#43			2- XTALO32K			
			Low-power oscillator (LPO) output.			
	XTALO32K	o	Alternative Function:			
	ATALOGEN	Ĭ	• P12			
			• P26			

	Pin Name	I/O Type	Description
			Default Direction: Input
			After POR State: Input Floating
	GPIO: P11		Alternate Function Description:
			1- A/D converter input
Pin#44			2- XTALI32K
			Low-power oscillator (LPO) input is used.
	V=411001/		Alternative Function:
	XTALI32K		• P11
			• P27
Pin#45	GND	GND	GND
Pin#46	GND	GND	GND
Pin#47	GND	GND	GND
Pin#48	GND	GND	GND

6. Addition Information

6.1 ADC Specification

Table 9: ADC Specification

Parameter	Symbol	Conditions	Min	Тур	Max	Unit
Number of Input Channels	-	-	-	9	-	-
Channel switching rate	fch	-	-	-	133.33	Kch/s
Input signal range	Vinp	-	0	-	3.63	V
Reference settling time	-	Charging refsel	7.5	-	-	us
Input resistance	Rinp	Effective, single end	-	500	-	kΩ
Input capacitance	Cinp				5	pF
Conversion rate	Fc		5.859		187	kHz
Conversion time	Tc		5.35		170.7	us
Resolution	R			16		bits
Absolute voltage measurement error	-	Using on-chip ADC firmware driver		±2	-	%
Current	1	lavdd1p2 + lavdd3p3	-	-	1	mA
Power	Р	-	-	1.5	-	wm
Leakage Current	Ileakage	T = 25°C	_	-	100	nA
Power-up time	Tpowerup		-	-	200	us
Integral nonlinearity	INL	In guaranteed performance range	-1	-	1	LSB
Differential nonlinearity	DNL	In guaranteed performance range	-1	-	1	LSB

Note: LSBs are expressed at the 10-bit level.

6.2 External Reset

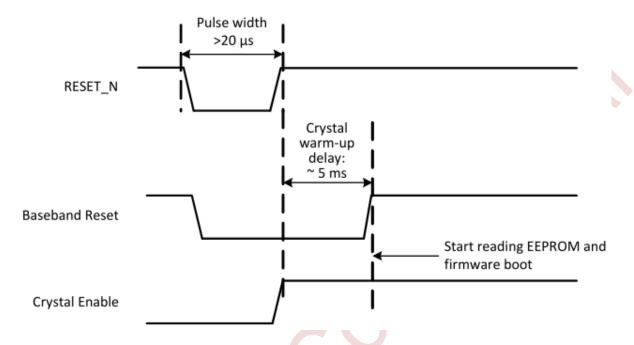


Figure 3 - External Reset Timing

6.3 32.768 kHz Oscillator

It is a standard Pierce oscillator using a comparator with hysteresis on the output to create a single-ended digital output. The hysteresis was added to eliminate any chatter when the input is around the threshold of the comparator and is $^{\sim}100$ mV. This circuit can be operated with a 32 kHz or 32.768 kHz crystal oscillator or be driven with a clock input at similar frequency.

Table 10: 32K XTAL Oscillator Characteristics

Parameter	Symbol	Conditions	Min	Тур	Max	Unit
Output frequency	Foscout	-	-	32.768	-	KHz
Frequency tolerance		Crystal dependent	-	100		ppm
Start-up time	Tstartup	-	-	-	500	us
XTAL drive level	Pdrv	For crystal selection	0.5	-		μ W
XTAL series resistance	Rseries	For crystal selection	-	Y	70	kΩ
XTAL shunt capacitance	Cshunt	For crystal selection	.	-	1.3	pF

6.4 Timing and AC Characteristics

6.4.1 SPI TIMING

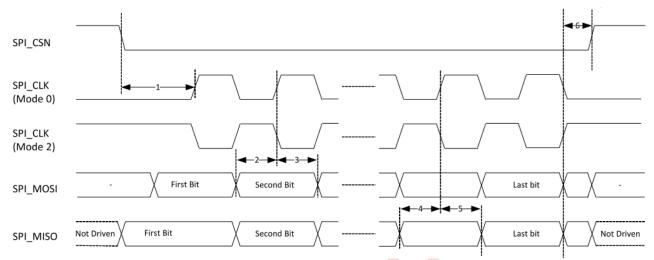


Figure 4 - SPI Timing – Mode 0 and 2

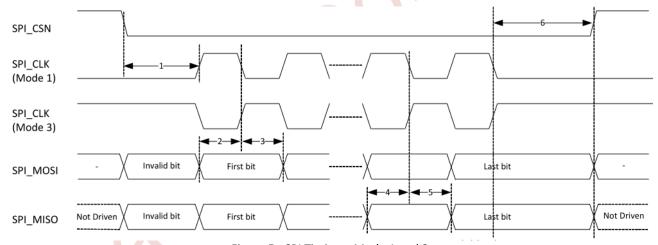


Figure 5 - SPI Timing - Mode 1 and 3

Table 11: SPI Interface Timing Specifications

Reference	Characteristics	Min	Тур	Max
1	Time from CSN asserted to first clock edge	1 SCK	100	∞
2	Master setup time	-	1/2SCK	-
3	Master hold time	1/2SCK	-	-
4	Slave setup time	-	1/2 SCK	-
5	Slave hold time	1/2 SCK	-	-
6	Time from last clock edge to CSN deasserted	SCK	10 SCK	100

6.4.2 BSC INTERFACE TIMING

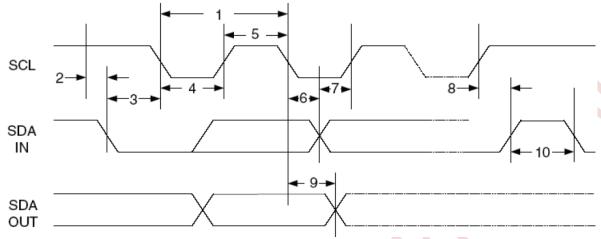


Figure 6 - BSC INTERFACE TIMING

Table 12: BSC INTERFACE Timing Specifications

Reference	Characteristics	Min	Max	Unit
1	Clock frequency		100 400 800 1000	KHz
2	START condition setup time	650	-	ns
3	START condition hold time	280	-	ns
4	Clock low time	650	-	ns
5	Clock high time	280	-	ns
6	Data input hold time	0	-	ns
7	Data input setup time	100	-	ns
8	STOP condition setup time	280	-	ns
9	Output valid from clock	-	400	ns
10	Bus free time	650		ns

6.4.3 UART Timing

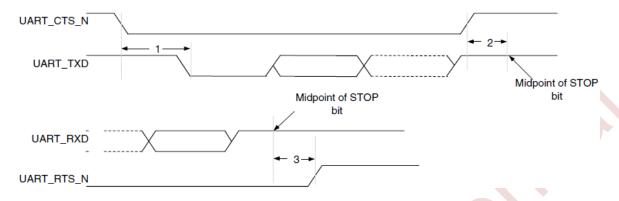


Figure 7 - UART Timing

Table 13: UART Timing Specifications

Reference	Characteristics	Min	Max	Unit
1	Delay time, UART_CTS_N low to UART_TXD valid	-	24	Baudout cycles
2	Setup time, UART_CTS_N high before midpoint of stop bit	-	10	ns
3	Delay time, midpoint of stop bit to UART_RTS_N high	-	2	Baudout cycles

7. Mechanical Specification

7.1 Size of the Module

The following paragraphs provide the requirements for the size, weight.

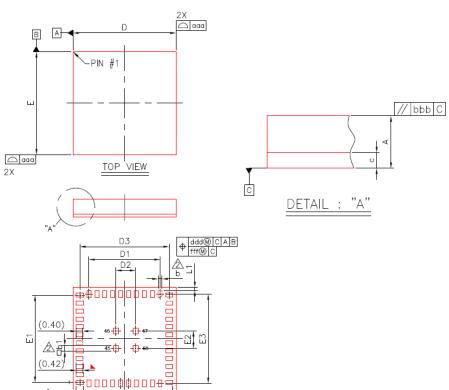
The size and thickness of the BCM20732S module 6.5mm (W) x 6.5mm (L) x 1.18mm (H):

(Tolerance: +/- 0.1mm)

7.2 Mechanical Dimension

Dimension: 6.5 x 6.5 x 1.18 mm³

BOTTOM VIEW



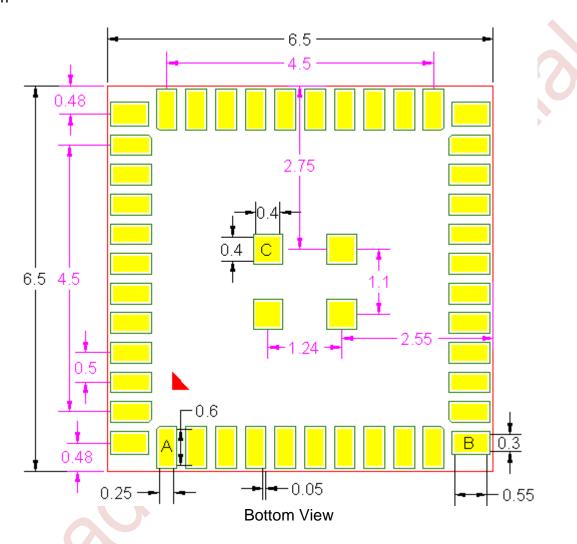
	Dimension in mm			Dimension in inch		
Symbol	MIN	NOM	MAX	MIN	NOM	MAX
Α			1.18			0.046
С	0.17	0.20	0.23	0.007	0.008	0.009
D/E	6.40	6.50	6.60	0.252	0.256	0.260
D1		4.50			0.177	
E1		5.50			0.217	
D2		1.24			0.049	
E2		1.10			0.043	
D3/E3		5.65			0.222	
е		0.50			0.020	
b		0.25			0.010	
L		0.45			0.018	
b1		0.35			0.014	
L1		0.20			0.008	
aaa		0.15			0.006	
bbb		0.10		0.004		
ddd		0.10		0.004		
fff		0.05			0.002	

NOTE:

8. Recommend Footprint

8.1 Module Dimension Measurement

Unit: mm



Note:

- 1. Please use Un-Solder Mask to design the Module Footprint.
- 2. There are two types pad size in the Module.
 - Type A:

Pad size: 0.6 x 0.25 mm & Solder Mask Opening: 0.7 x 0.35mm

Type B

Pad size: 0.55 x 0.3mm & Solder Mask Opening: 0.65 x 0.4mm

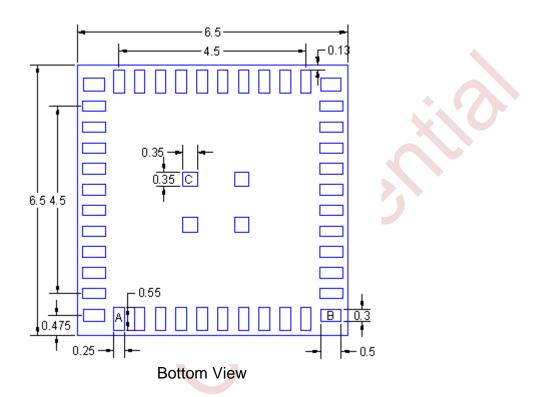
- Type C:

Pad size: 0.4 x 0.4mm & Solder Mask Opening: 0.5 x 0.5 mm

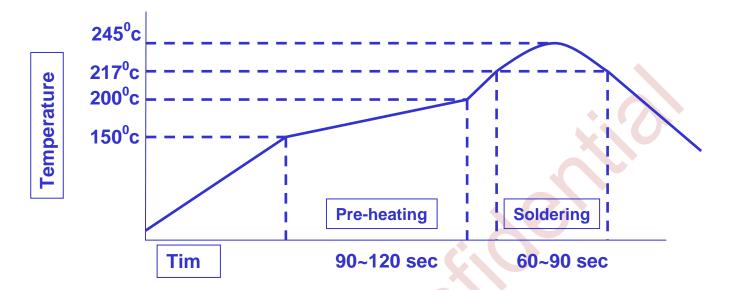
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9. Recommend Stencil

Unit: mm



10. Recommended Reflow Profile



11. Package and Storage Condition

11.1 Package Dimension

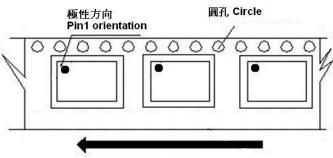


11.2 Laser Mark

TBD

11.3 Pin 1 Location in the Tape/Reel

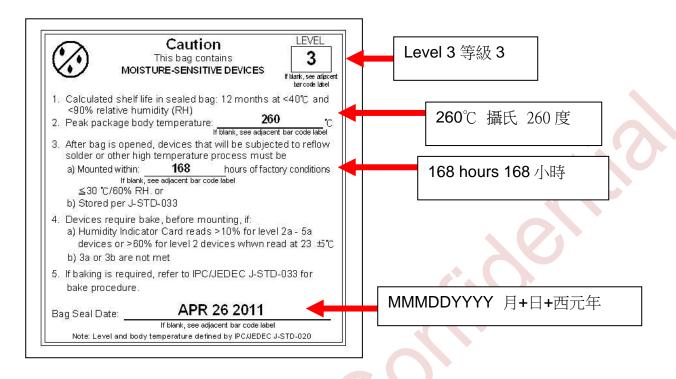
SiP 產品極性方向 SiP Product Pin1 orientation



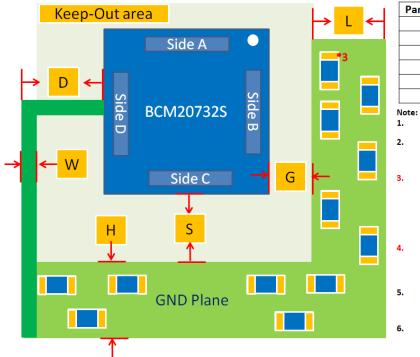
捲帶方向 (進入捲軸)

Feeding Direction (Into Reel)

11.4 MSL & Moisture Sensitive LEVEL



Preliminary Arrangement Guideline for BCM20732S (New Antenna Design)



Parameter	Unit: mm	Antenna Efficiency
L	3 (min.)	
G	3 (typ.)	
S	3 (typ.)	210/ ~410/
Н	3 (typ.)	31% ~41%
W	0.4 (typ.)	
D	4.5 (typ.)	

- Please must Connect "GND" from system to module at side D (#17 pin of the module).
- The L-shape GND plane is required for integrated antenna and please must keep the GND plane continuous, do not cut off the GND shape due to routines.
- A L shape GND plane is required (Green color area). If the L shape GND plane is arranged on top layer of PCB, It's not recommended to place components in this area. If components need to be mounted in this area, the L shape GND plane need to be arranged in inner or bottom layers and avoid a complete GND plane on top layer. (This is to ensure the L shape GND plane for antenna is continuous)
- 4. The measured efficiency is based on the above layout guide. And will support > 50M range using iPhone 5 to test the module (without plastic housing). For real application, the adjustment of the layout may impact the antenna efficiency which will reduce the range.
- Please bring signal traces out of module from Side C (between #27 and #30 of module) or Side D (between #16 and #19 of module) with overlapped routing to minimize metal trace in the keep-out area.
- Please do not bring signal trace from either Side A or Side B.