

Symbol	Description	Conditions	Min	Typ	Max	Unit
IIP3	Input intercept point	$f_1 = f_{LO} + 1 \text{ MHz}$ $f_2 = f_{LO} + 1.945 \text{ MHz}$ Mode A (*1) Mode B (*1)	-36 -21	-33 -18	- -	dBm dBm
BBW	Base band filter bandwidth DSB	Programmable (*2)	- -	200 600	- -	kHz kHz
ACR	Adjacent channel rejection	$f_{unw} = f_{LO} + 650 \text{ kHz}$ $P_w = -108 \text{ dBm}$ , mode A (*1)	45	48	-	dBc
BR	Bit rate	Programmable	1.2		152.3	kbit/s
RFOP	RF output power	Programmable      RFOP1 RFOP2 RFOP3 RFOP4	-3 +2 +7 +12	0 +5 +10 +15	- - - -	dBm dBm dBm dBm
FR	Synthesizer frequency range	Programmable Each range with its own external components	433 868 902	- - -	435 870 928	MHz MHz MHz
TS_TR	Transmitter wake-up time	From oscillator enabled	-	150	250	us
TS_RE	Receiver Baseband wake-up time	From oscillator enabled	-	0.5	0.8	ms
TS_RSSI	RSSI wake-up time	From receiver enabled	-	-	1	ms
TS_RSSIM	RSSI measurement time			0.5		ms
TS_OS	Crystal oscillator wake-up time	Fundamental 3 <sup>rd</sup> overtone	- -	0.3 2.5	0.5	ms ms
TS_FEI	FEI wake-up time		-	-	2/BR	ms
TS_SYNC_AQ	Time for synchronization of the barker decoder	Input power of -106 dBm Data rate = 1154 bits/s Chip rate = 12.7 kcps From Rx enabled	-	5	-	ms
XTAL	Crystal oscillator frequency	Fundamental or 3 <sup>rd</sup> overtone	-	39	-	MHz
FSTEP	Frequency synthesizer step	Exact step is XTAL / 77 824	-	500	-	Hz
VTNR	RSSI equivalent input thresholds	Mode A (*1) Low range: VTNR1 VTNR2 VTNR3 High range: VTNR1 VTNR2 VTNR3	- - - - - - -	-100 -95 -90 -85 -80 -75	- - - - - -	dBm dBm dBm dBm dBm dBm dBm
SPR	Spurious emissions in Rx mode	(*4)	-	-65	-	dBm
VIH	Digital input level high (*3)	% VDD	75	-	-	%
VIL	Digital input level low (*3)	% VDD	-	-	25	%
VOH	Digital output level high	% VDD	75	-	-	%
VOL	Digital output level low	% VDD	-	-	25	%

Table 3: Electrical Specifications

- Notes: (\*1) Mode A: High sensitivity mode; Mode B: High Linearity mode. As defined in Paragraph 4.1.1.  
 (\*2) An intermediate bandwidth of 300 kHz can also be selected by using additional settings described in section 5.2.8.  
 (\*3) Throughout this document, digital signal levels are named "high" or "1", and "low" or "0".  
 (\*4) SPR strongly depends on the design of the application board and the choice of the external components.  
 Values down to -70 dBm can be achieved with careful design.