



1 Features

The AW24MxxL is a 2.4-GHz Direct Sequence Spread Spectrum (DSSS) complete radio module which includes the Cypress radio integrated circuit CyFi™ CYRF7936, integrated Antenna, and all external components

Operates in the unlicensed worldwide Industrial, Scientific and Medical (ISM) band (2.400 GHz–2.483 GHz)

21mA operating current (Transmit @ –5 dBm)

Transmit power up to +4 dBm

Receive sensitivity up to –97 dBm

Sleep Current <1 µA

Operating range of up to 20m indoor or 40m LOS.

DSSS data rates up to 250 kbps, GFSK data rate of 1 Mbps

Auto Transaction Sequencer (ATS) - no micro controller intervention

Framing, Length, CRC16, and Auto ACK

Fast Startup and Fast Channel Changes

Separate 16-byte Transmit and Receive FIFOs

AutoRate™ - dynamic data rate reception

Receive Signal Strength Indication (RSSI)

4-MHz SPI microcontroller interface

No proprietary software required

Serial Peripheral Interface (SPI) control while in sleep mode

Vertical or horizontal mounting

Operating voltage from 2.4 to 3.6 volts

Operating temperature from 0 to 70°C

Size: 16 mm x 13.5 mm (~0.6" x 0.5") with Chip Antenna

Size: 19 mm x 13.5 mm (~0.75" x 0.5") with PCB Antenna

Weight: 2 grams

FCC Modular Approval Grant to meet FCC Part 15, EN 300 328-1, EN 301 489-1, EN 301 489-7 and Industry Canada RSS-210 standards In Progress.

An FCC Module Approval (MA) Grant provides customers significant cost savings, by allowing customers to adopt the AW24MXXL FCC ID into their own products

2 Functional Description

The Artaflex AW24MXXL Wireless Radio Module offers a complete radio module solution for integration into existing or new 2.4-GHz products.

The AW24MXXL is tested for functional operation and is FCC/ETSI (EU)/Industry Canada certified. The module is supplied with two different integrated antenna versions.

The AW24MxxL is available in a small PCB design and can be mounted horizontally or vertically to the device PCB via a 12-pin header. The pin-out of the header is shown in the Connector Footprint section.

3 Applications

PC Human Interface Devices (HID)

Wireless Keyboards and Mice

VOIP and Wireless Headsets

Wireless Gamepads

Remote Control

White Goods (Smart Appliances)

Window unit air conditioners

Kitchen compactors

Dishwashers

Washers

Dryers

Consumer

Sports and Leisure Equipment

Remote Controls

Audio Subwoofer

Presenter Tools

Locator Alarms

Toys

Building/Home Automation

Automatic Meter Readers (AMR)

On-Site Paging Systems

Garage door opener

Alarm and Security

Lighting Control

Climate Control

Fan Control

Industrial Control

Active RFID and asset tracking systems

Inventory Management

Point-of-sale systems

Factory Automation

Data Acquisition

Transportation

Remote Keyless Entry with acknowledgement (RKE)

Airline Baggage Tracking

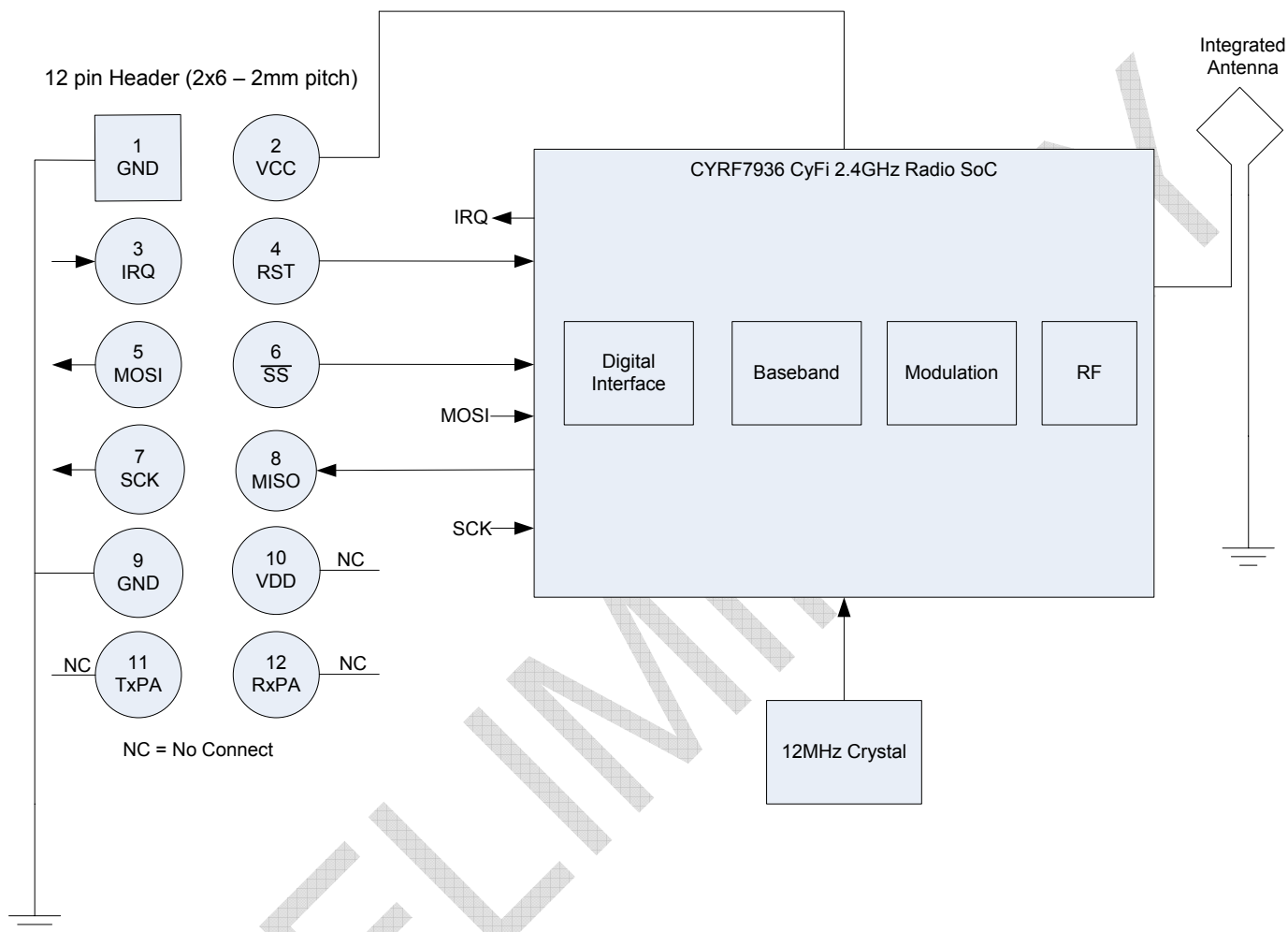
Diagnostics



Compliant



***Figure 1 – Module Schematic (Header version)**



* SMT Module pin out is different and is shown in Table 5.

3.1 Reference Documentation

For information on technical details of the Cypress Semiconductor, CYRF7936 CyFi™, 2.4-GHz DSSS Radio system on chip such as register settings, timing, application interfaces, and clocking, refer to the device data sheet CYFI7936 available on the Cypress Web Site at:- www.cypress.com

- The following is the link location known at the time of publication that accompany this data sheet:

http://download.cypress.com.edgesuite.net/design_resources/datasheets/contents/cyrf7936_8.pdf?key=1229340511568



4 Functional Overview

The AW24MXXL Module provides a complete SPI to RF antenna wireless MODEM. The module is designed to implement wireless device links operating in the worldwide 2.4-GHz ISM frequency band. It is intended for systems compliant with world-wide regulations covered by Europe ETSI EN 301 489-1, ETSI EN 301 489-7, & ETSI EN 300 328-1, USA FCC Part 15 and Industry Canada RSS-210 standards.

The module contains a 2.4-GHz 1-Mbps GFSK radio transceiver, packet data buffering, packet framer, DSSS baseband controller, Received Signal Strength Indication (RSSI), and SPI interface for data transfer and device configuration.

The radio supports 80 discrete 1-MHz channels (regulations may limit the use of some of these channels in certain jurisdictions). In DSSS modes the baseband performs DSSS spreading/de-spreading, while in GFSK Mode (1 Mb/s - GFSK) the baseband performs Start of Frame (SOF), End of Frame (EOF) detection and CRC16 generation and checking. The baseband may also be configured to automatically transmit Acknowledge (ACK) handshake packets whenever a valid packet is received.

When in receive mode, with packet framing enabled, the device is always ready to receive data transmitted at any of the supported bit rates, except SDR, enabling the implementation of mixed-rate systems in which different devices use different data rates. This also enables the implementation of dynamic data rate systems, which use high data rates at shorter distances and/or in a low-moderate interference environment, and change to lower data rates at longer distances and/or in high interference environments.

4.1 Link Layer Modes

The AW24MXXL module supports the following data packet framing features:

SOP – Packets begin with a 2-symbol Start of Packet (SOP) marker. This is required in GFSK and 8DR modes, but is optional in DDR mode and is not supported in SDR mode; if framing is disabled then an SOP event is inferred whenever two successive correlations are detected. The SOP_CODE_ADR code used for the SOP is different from that used for the “body” of the packet and if desired may be a different length. SOP must be configured to be the same length on both sides of the link.

EOP – There are two options for detecting the end of a packet. If SOP is enabled, then a packet length field may be enabled. GFSK and 8DR must enable the length field. This is the first 8-bits after the SOP symbol, and is transmitted at the payload data rate. If the length field is enabled, an End of Packet (EOP) condition is inferred after reception of the number of bytes defined in the length field, plus two bytes for the CRC16 (if enabled—see below). The alternative to using the length field is to infer an EOP condition from a configurable number of successive non-correlations; this option is not available in GFSK mode and is only recommended to enable when using SDR mode.

CRC16 – The device may be configured to append a 16-bit CRC16 to each packet. The CRC16 uses the USB CRC polynomial with the added programmability of the seed. If enabled, the receiver will verify the calculated CRC16 for the payload data against the received value in the CRC16 field. The starting value for the CRC16 calculation is configurable, and the CRC16 transmitted may be calculated using either the loaded seed value or a zero seed; the received data CRC16 will be checked against both the configured and zero CRC16 seeds.

CRC16 detects the following errors:

Any one bit in error

Any two bits in error (no matter how far apart, which column, and so on)

Any odd number of bits in error (no matter where they are)

An error burst as wide as the checksum itself

4.2 Packet Buffers

All data transmission and reception utilizes the 16-byte packet buffers—one for transmission and one for reception.

The transmit buffer allows a complete packet of up to 16-bytes of payload data to be loaded in one burst SPI transaction, and then transmitted with no further micro controller intervention. Similarly, the receive buffer allows an entire packet of payload data up to 16 bytes to be received with no firmware intervention required until packet reception is complete.

The AW24MXXL module supports packet length of up to 40 bytes; interrupts are provided to allow a micro controller to use the transmit and receive buffers as FIFOs. When transmitting a packet longer than 16 bytes, the micro controller can load 16-bytes initially, and add further bytes to the transmit buffer as transmission of data creates space in the buffer. Similarly, when receiving packets longer than 16 bytes, the micro controller must fetch received data from the FIFO periodically during packet reception to prevent it from overflowing.

4.3 Auto Transaction Sequencer (ATS)

The AW24MXXL module provides automated support for transmission and reception of acknowledged data packets.

When transmitting a data packet, the device automatically starts the crystal and synthesizer, enters transmit mode, transmits the packet in the transmit buffer, and then automatically switches to receive mode and waits for a handshake packet and then automatically reverts to sleep mode or idle mode when either an ACK packet is received, or a timeout period expires.

Similarly, when receiving in transaction mode, the device waits in receive mode for a valid packet to be received, and then automatically transitions to transmit mode, transmits an ACK packet, and then switches back to receive mode to await the next packet. The contents of the packet buffers are not affected by the transmission or reception of ACK packets.

In each case, the entire packet transaction takes place without any need for micro controller firmware action; to transmit data the micro controller simply needs to load the data packet to be transmitted, set the length, and set the TX GO bit. Similarly, when receiving packets in transaction mode, firmware simply needs to retrieve the fully received packet in response to an interrupt request indicating reception of a packet.

4.4 Data Rates

By combining the DATA_CODE_ADR code lengths and data transmission modes described above, the AW24MXXL supports the following modes and data rates.

Table 1 - Data Rates

RF Transmission Mode	Raw Data Rate kbps
GFSK	1,000.00
32-Chip 8DR	250.00
64-chip 8DR ^[2]	125.00
32-chip DDR ^[3]	62.50
64-chip DDR ^[3]	31.25
64-chip SDR ^[2,3]	15.63

5 SPI Communication

The AW24MXXL has an SPI interface supporting communications between an application MCU and one or more slave devices (including the AW24MXXL). The SPI interface supports single-byte and multi-byte serial transfers using either 4-pin or 3-pin interfacing. The SPI communications interface consists of Slave Select (\overline{SS}), Serial Clock (SCK), and Master Out-Slave In (MOSI), Master In-Slave Out (MISO), or Serial Data (SDAT).

The SPI communications is as follows:

- Command Direction (bit 7) = "1" enables SPI write transaction. A "0" enables SPI read transactions.
- Command Increment (bit 6) = "1" enables SPI auto address increment. When set, the address field automatically increments at the end of each data byte in a burst access, otherwise the same address is accessed.
- Six bits of address.
- Eight bits of data.

The device receives SCK from an application MCU on the SCK pin. Data from the application MCU is shifted in on the MOSI pin. Data to the application MCU is shifted out on the MISO pin. The active-low Slave Select (\overline{SS}) pin must be asserted to initiate an SPI transfer.

The application MCU can initiate SPI data transfers via a multi byte transaction. The first byte is the Command/Address byte, and the following bytes are the data bytes as shown in Figure 2 through Figure 5.

The SPI communications interface has a burst mechanism, where the first byte can be followed by as many data bytes as desired. A burst transaction is terminated by deasserting the slave select (\overline{SS} = 1).

The SPI communications interface single read and burst read sequences are shown in Figure 3 and Figure 4, respectively.

The SPI communications interface single write and burst write sequences are shown in Figure 5 and Figure 6, respectively.

This interface may optionally be operated in a 3-pin mode with the MISO and MOSI functions combined in a single bidirectional data pin (SDAT). When using 3-pin mode, user firmware should ensure that the MOSI pin on the MCU is in a high impedance state except when MOSI is actively transmitting data.

The device registers may be written to or read from 1 byte at a time, or several sequential register locations may be written/read in a single SPI transaction using incrementing burst mode. In addition to single byte configuration registers, the device includes register files; register files are FIFOs written to and read from using non-incrementing burst SPI transactions.

The IRQ pin function may optionally be multiplexed onto the MOSI pin; when this option is enabled the IRQ function is not available while the \overline{SS} pin is low. When using this configuration, user firmware should ensure that the MOSI pin on the AW24MXXL is in a high impedance state whenever the \overline{SS} pin is high.

The SPI interface is not dependent on the internal 12-MHz clock, and registers may therefore be read from or written to while the device is in sleep mode, and the 12-MHz oscillator disabled.

Figure 2 – SPI Transaction Format

Bit #	Byte 1			Byte 1+N
	7	6	[5:0]	
Bit Name	DIR	INC	Address	Data

Figure 3 - SPI Single Read Sequence

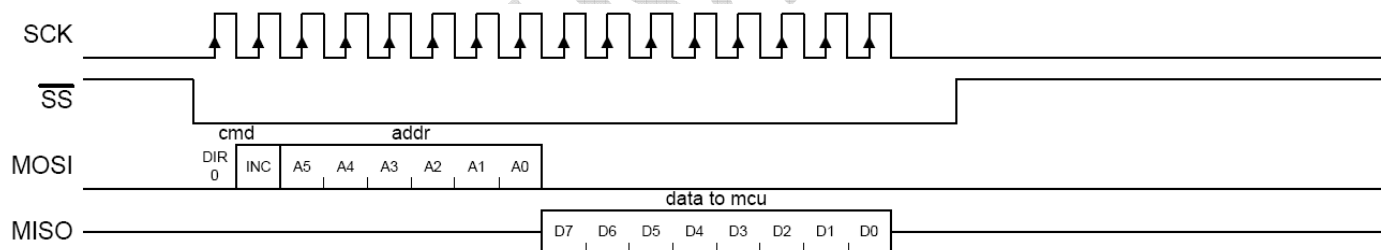


Figure 4 - SPI Incrementing Burst Read Sequence

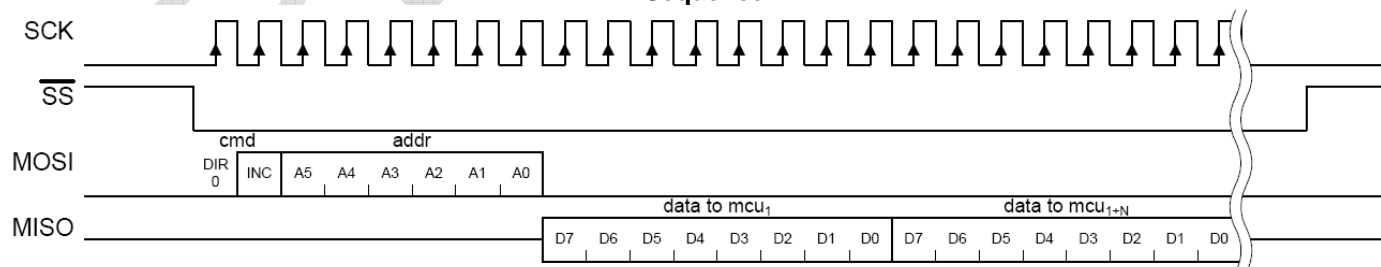


Figure 5 - SPI Single Write Sequence

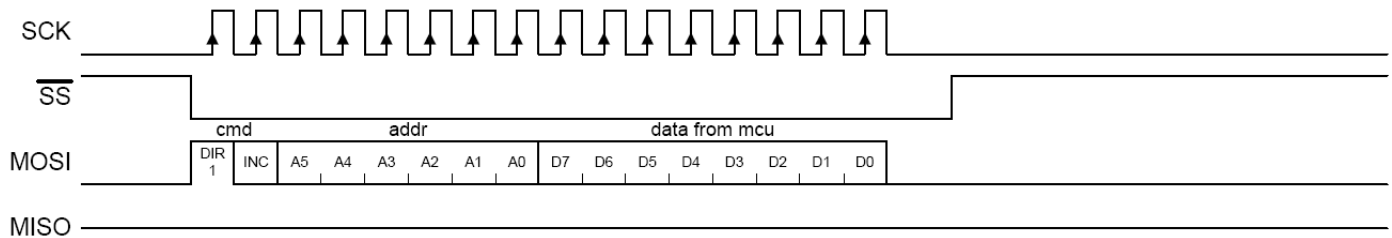
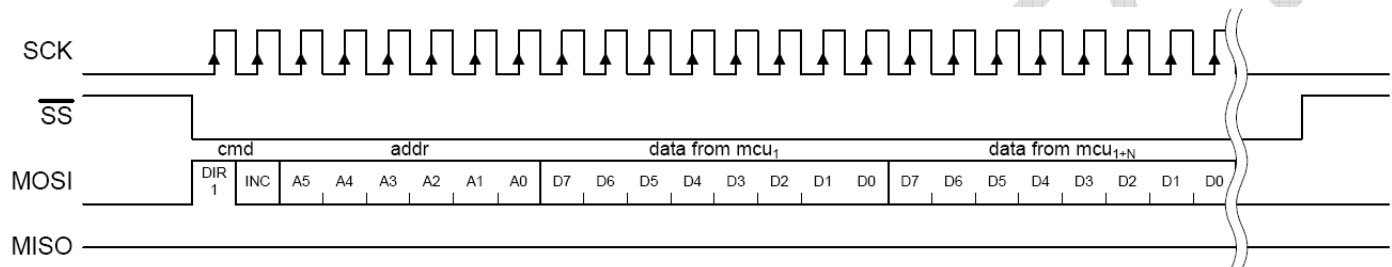


Figure 6 - SPI Incrementing Burst Write Sequence



6 Power Management

The operating voltage of the module is 2.4V to 3.6V DC, which is applied to the V_{cc} pin 2 of the connector. The device can be shutdown to a fully static sleep mode by writing to the FRC END = 1 and END STATE = 000 bits in the XACT_CFG_ADR register over the SPI interface. The module will enter sleep mode within 35- μ s after the last SCK positive edge at the end of this SPI transaction. Alternatively, the module may be configured to automatically enter sleep mode after completing packet transmission or reception. When in sleep mode, the on-chip oscillator is stopped, but the SPI interface remains functional. The module will wake from sleep mode automatically when the module is commanded to enter transmit or receive mode. When resuming from sleep mode, there is a short delay while the oscillator restarts. The module may be configured to assert the IRQ pin when the oscillator has stabilized.

7 Low Noise Amplifier (LNA) and Received Signal Strength Indication (RSSI)

The gain of the receiver may be controlled directly by clearing the AGC EN bit and writing to the Low Noise Amplifier (LNA) bit of the RX_CFG_ADR register. When the LNA bit is cleared, the receiver gain is reduced by approximately 20 dB, allowing accurate reception of very strong received signals (for example when operating a receiver very close to the transmitter). Approximately 30 dB of receiver attenuation can be added by setting the Attenuation (ATT) bit; this allows data reception to be limited to devices at very short ranges. Disabling AGC and enabling LNA is recommended unless receiving from a device using external PA.

When the module is in receive mode the RSSI_ADR register returns the relative signal strength of the on-channel signal power.

When receiving, the module will automatically measure and store the relative strength of the signal being received as a 5-bit value. An RSSI reading is taken automatically when the SOP is detected. In addition, a new RSSI reading is taken every time the previous reading is read from the RSSI_ADR register, allowing the background RF energy level on any given channel to be easily measured when RSSI is read when no signal is being received. A new reading can occur as fast as once every 12 μ s.

8 Absolute Maximum Ratings

Storage Temperature.....	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage on any power supply pin relative to	V_{SS} –0.3V to +3.9V
DC Voltage to Logic Inputs ^[3]	–0.3V to V_{IO} +0.3V
DC Voltage applied to Outputs in High-Z State	–0.3V to V_{IO} +0.3V
Static Discharge Voltage (Digital) ^[4]	>2000V
Static Discharge Voltage (RF) ^[4]	1100V
Latch-up Current.....	+200 mA, –200 mA

9 Operating Conditions

V_{CC}	2.4V to 3.6V
T_A (Ambient Temperature under Bias).....	0°C to +70°C
Ground Voltage.....	0V
F_{OSC} (Crystal Frequency).....	12 MHz \pm 30 ppm

Notes

- [1]. Typically data modes with high chip encoding which provides a higher process gain and lower data rates provide longer range and / or a more robust wireless link.
- [2]. This mode is compatible with Cypress Generation 1 RF CyFi transceiver devices, CYWUSB6934 and CYWUSB6935.
- [3]. It is permissible to connect voltages above V_{IO} to inputs through a series resistor limiting input current to 1 mA. AC timing not guaranteed.
- [4]. Human Body Model (HBM).

10 DC Characteristics (T = 25°C, V_{CC} = 2.4V, f_{OSC} = 12.000 MHz)

Table 2 - DC Characteristics

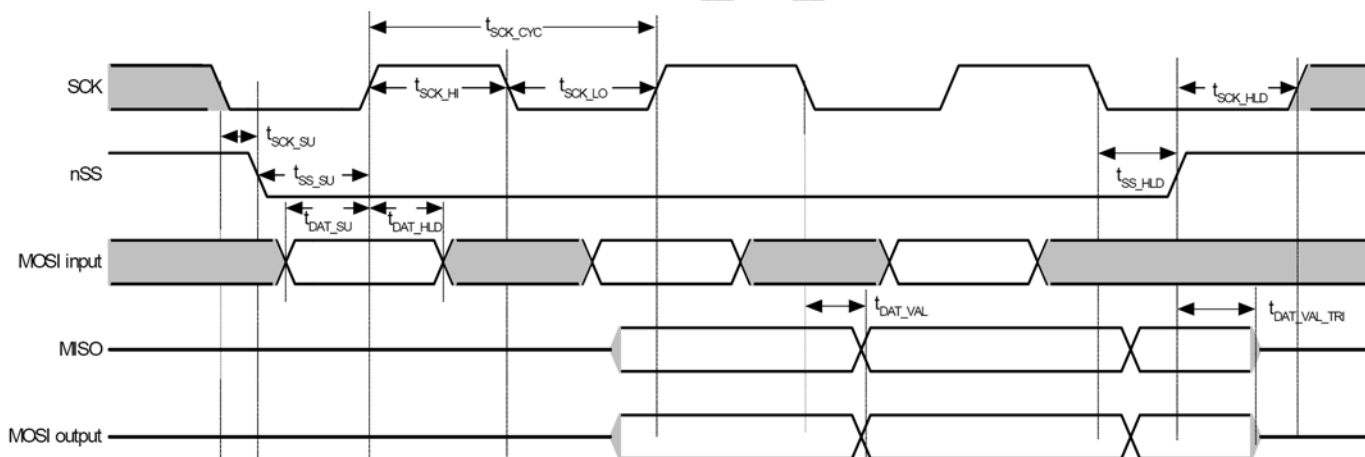
Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Power Supply Voltage	0 to 70°C	2.4		3.6	V
V_{IO}	Voltage applied to I/O				$V_{CC} + 0.7$	V
I_{synth}	I_{CC} during Synth Start			8.4		mA
TX I_{CC5}	I_{CC} during Transmit	PA = 5 (–5dBm)		20.8		mA
TX I_{CC6}	I_{CC} during Transmit	PA = 6 (0dBm)		26.2		mA
TX I_{CC7}	I_{CC} during Transmit	PA = 7 (+4dBm)		34.1		mA
RX I_{CCoff}	I_{CC} during Receive	LNA off, ATT on		18.4		mA
RX I_{CCon}	I_{CC} during Receive	LNA on, ATT off		21.2		mA
I_{SB}	Sleep Mode Current I_{CC}			0.8	10.0	μ A

11 AC Characteristics^[5]

Table 3 – SPI Interface^[6]

Parameter	Description	Min.	Typ.	Max.	Unit
t_{SCK_CYC}	SPI Clock Period	238.1			nS
t_{SCK_HI}	SPI Clock High Time	100			nS
t_{SCK_LO}	SPI Clock Low Time	100			nS
t_{DAT_SU}	SPI Input Data Set-up Time	25			nS
t_{DAT_HLD}	SPI Input Data Hold Time	10			nS
t_{DAT_VAL}	SPI Output Data Valid Time	0		50	nS
$t_{DAT_VAL_TRI}$	SPI Output Data Tri-state (MOSI from Slave Select Deassert)			20	nS
t_{SS_SU}	SPI Slave Select Set-up Time before first positive edge of SCK ^[7]	10			nS
t_{SS_HLD}	SPI Slave Select Hold Time after last negative edge of SCK	10			nS
t_{SS_PW}	SPI Slave Select Minimum Pulse Width	20			nS
t_{SCK_SU}	SPI Slave Select Set-up Time	10			nS
t_{SCK_HLD}	SPI SCK Hold Time	10			nS
t_{RESET}	Minimum RST pin pulse width	10			nS

Figure 7 - SPI Timing



Notes

[5] AC values are not guaranteed if voltage on any pin exceeds V_{IO} .

[6] $C_{LOAD} = 30$ pF.

[7] SCK must start low at the time \overline{SS} goes low, otherwise the success of SPI transactions are not guaranteed.

12 RF Characteristics

Table 4 – Radio Parameters

Parameter Description	Conditions	Min.	Typ.	Max.	Unit
RF Frequency Range		2.400		2.483	GHz
Receiver (T=25°C, VCC = 3.0V, f_{osc} = 12.000000MHz, BER < 1E-3)					
Sensitivity 125kbps 64-8DR	BER 1E-3		-97		dBm
Sensitivity 250-kbps 32-8DR	BER 1E-3		-93		dBm
Sensitivity	CER 1E-3	-80	-87		dBm
Sensitivity GFSK	BER 1E-3, ALL SLOW = 1		-84		dBm
LNA gain			22.8		dB
ATT gain			-31.7		dB
Maximum Received Signal	LNA On	-15	-6		dBm
RSSI value for PWR _{in} -60 dBm	LNA On		21		Count
RSSI slope			1.9		dB/Count
Interference Performance (CER 1E-3)					
Co-channel Interference rejection Carrier-to-Interference (C/I)	C = -60dBm		9		dB
Adjacent (± 1 MHz) channel selectivity C/I 1 MHz	C = -60dBm		3		dB
Adjacent (± 2 MHz) channel selectivity C/I 2 MHz	C = -60dBm		-30		dB
Adjacent (> 3 MHz) channel selectivity C/I > 3 MHz	C = -67dBm		-38		dB
Out-of-Band Blocking 30 MHz–12.75 MHz[C = -67dBm		-30		dBm
Intermodulation	C = -64dBm, Δf = 5, 10 MHz		-36		dBm
Receive Spurious Emission					
800 MHz	100-kHz ResBW		-79		dBm
1.6GHz	100-kHz ResBW		-71		dBm
3.2 GHz	100-kHz ResBW		-65		dBm
Transmitter (T = 25°C, VCC = 3.0V)					
Maximum RF Transmit Power	PA = 7	+2	+4	+6	dBm
Maximum RF Transmit Power	PA = 6	-2	0	+2	dBm
Maximum RF Transmit Power	PA = 5	-7	-5	-3	dBm
Maximum RF Transmit Power	PA = 4	-15	-13	-11	dBm
Maximum RF Transmit Power	PA = 3	-20	-18	-16	dBm
Maximum RF Transmit Power	PA = 2	-26	-24	-22	dBm
Maximum RF Transmit Power	PA = 1	-32	-30	-28	dBm
Maximum RF Transmit Power	PA = 0	-37	-35	-33	dBm
RF Power Control Range			39		dB
RF Power Control Range Step Size	seven steps, monotonic		5.6		dB
Frequency Deviation Min	PN Code Pattern 10101010		270		kHz
Frequency Deviation Max	PN Code Pattern 11110000		323		kHz
Error Vector Magnitude (FSK error)	>0 dBm		10		%rms
Occupied Bandwidth	-6 dBc, 100-kHz ResBW	500	876		kHz

Table 4 – Radio Parameters (continued)



Parameter Description	Conditions	Min.	Typ.	Max.	Unit
Transmit Spurious Emission (PA = 7)					
In-band Spurious Second Channel Power (± 2 MHz)			-38		dBm
In-band Spurious Third Channel Power (> 3 MHz)			-44		dBm
Non-Harmonically Related Spurs (800MHz)			-38		dBm
Non-Harmonically Related Spurs (1.6GHz)			-34		dBm
Non-Harmonically Related Spurs (3.2GHz)			-47		dBm
Harmonic Spurs (Second Harmonic)			-43		dBm
Harmonic Spurs (Third Harmonic)			-48		dBm
Fourth and Greater Harmonics			-59		dBm
Power Management (with 30ppm crystal)					
Crystal start to 10ppm			0.7	1.3	ms
Crystal start to IRQ	XSIRQ EN = 1		0.6		ms
Synth Settle	Slow channels			270	μ s
Synth Settle	Medium channels			180	μ s
Synth Settle	Fast channels			100	μ s
Link turn-around time	GFSK			30	μ s
Link turn-around time	250 kbps			62	μ s
Link turn-around time	125 kbps			94	μ s
Link turn-around time	<125 kbps			31	μ s
Max. packet length	<60ppm crystal-to-crystal all modes except 64-DDR			40	bytes
Max. packet length	<60ppm crystal-to-crystal 64-DDR			16	bytes



13 Mechanical Package Description

Size: 16mm x 13.5mm (0.63" x 0.53") with Chip Antenna (AW24MCHL-H2)
19mm x 13.5mm (0.75" x 0.53") with PCB Antenna (AW24MPLL-H2)
15mm x 13.5mm (0.6" x 0.53") with Chip Antenna (AW24MCHL-SM)

Weight: 2 grams

* Check <http://www.artaflexmodules.com/products.html> for detailed mechanical info.

14 Connector

Table 5 – Connector Pin out Information For both Header and SMT Modules

SMT Pin No	Header Pin No	Name	Type	Default	Description
12	1	GND	Power	GND	Ground
11	2	VCC	Power	VCC	Main Supply 2.4 to 3.6 volts
5	3	IRQ	I/O	-	Interrupt output (configurable active high or low), or GPIO
9	4	RST	Input	Input	Module Reset. Internal on Chip 10k-ohm pull-down resistor. Active HIGH
3	5	MOSI	I/O	Input	SPI data input, or SDAT
4	6	\overline{SS}	Input	Pull Up	SPI Interface enable, Active LOW
2	7	SCK	Input	Input	SPI Clock
6	8	MISO	I/O	Hi Z	SPI data output pin or GPIO in 3-pin SPI mode.
13	9	GND	Power	GND	Ground
10	10	L/D	Power	GND	Connect to GND.
	11	TXPA	I	I	No Connect – Leave Open Circuit ^[8]
	12	RXPA	I	I	No Connect – Leave Open Circuit ^[8]
7		XOUT	I/O	O	Buffered 0.75, 1.5, 3, 6, or 12 MHz clock, PACTL, or GPIO. Tri-states in sleep mode (configure as GPIO drive LOW).
8		PACTL	I/O	O	Control signal for external PA, T/R switch, or GPIO.
1,14,15,16					No Connect – Leave Open Circuit ^[8]

Note

[8]. Reserved pin for power amplifier control signals for compatibility with the AWA24S Artaflex module. Pin can be connected to any user I/O on the OEM's Micro Controller Unit (MCU).



14.1 Standard Part Numbers

Table 6 – Standard Part Numbers

Part Number	Description	Temperature
AW24MCHL-H2	Integrated Chip Antenna Radio with Open 12 Pin Header in Commercial Temperature	0 to 70°C

14.2 Optional Part Numbers

For optional configurations please consult with Artaflex for availability.

Table 6 – Standard Part Numbers

Part Number	Description	Temperature
AW24MCHL-HR	Integrated Chip Antenna Radio with 12 Pin Right Angle Header in Commercial Temperature	0 to 70°C
AW24MPLL- H2	Integrated Print Antenna Radio with 12 Pin Header in Commercial Temperature	0 to 70°C
AW24MPLL-HR	Integrated Print Antenna Radio with 12 Pin Header in Commercial Temperature	0 to 70°C
AW24MCHL-SM	Integrated Chip Antenna Radio in SMT Package, Commercial Temperature	0 to 70°C

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