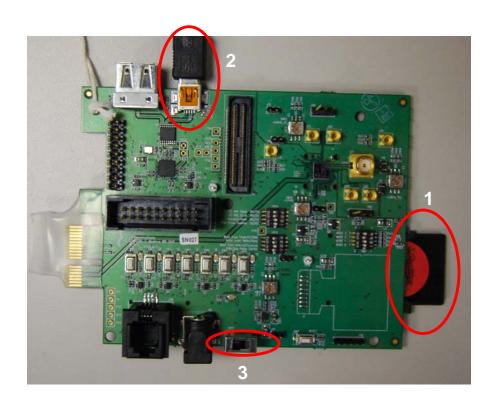
SC4113-D - RIPCORD2 UWB IC DVK User Guide

©2008 Staccato Communications, Inc. All rights reserved.

Abstract: This guide functions as a user guide for the installation and operation of the SC4113-D with regards to regulatory testing





- ☐ Make sure the appropriate flash card is inserted in the slot shown '1'
- ☐ Plug in USB cable into DUT as shown '2'
- ☐ Plug the other end of the USB cable into Laptop.
- ☐ Toggle the power switch to power on the DUT '3'. NOTE:
 - ☐ The switch position shown in figure is the 'OFF' state
 - ☐ The DUT will be powered by the laptop via USB

Hardware set up is done, please proceed to software set up

SOFTWARE INSTALLATION

- ☐ IF USING THE LAPTOP PROVIDED WITH EUT, PLEASE IGNORE THE SOFTWARE INSTALLATION STEPS IN STEP 3
- ☐ Install the following software from the CD/memory stick provided:
 - ☐ Devpak1.1.11_Setup.exe
- ☐ During installation If a XP warning window pops up, hit 'Continue Anyway' button and finish installation
- ☐ Continue instructions on following pages













□ Launch UWB PHY Diagonostics Start → Programs →
>Staccato Developers Pak → Scripts



☐ Enter '0' for connection via USB and press return



☐ 'tk' window should launch as shown above





TESTING TX EMISSIONS



7% tk

-TX-

1000

Length Bytes

C 106.7

C 160

200

C 320

C 400

Num Bursts (or single frames)

Num Frames per Burst

7% tk

-CONFIG 2-

Get Temp

Memory Address (Hex)

Memory Value (Hex)

Mem Read

N∨M

-CONFIG 1-

RTI: ??

DRV: ??

GUI: 50

IC Version: ??

Band Group

Re-cal Hop Gen

@ BG1

BG3

C BG6

● TFC1

C TFC2

C TFC3

C TFC4

C TFC5

-RX-

Start RX

Stop RX

Log Results

Good Frames:

HCS Frames:

FCS Frames:

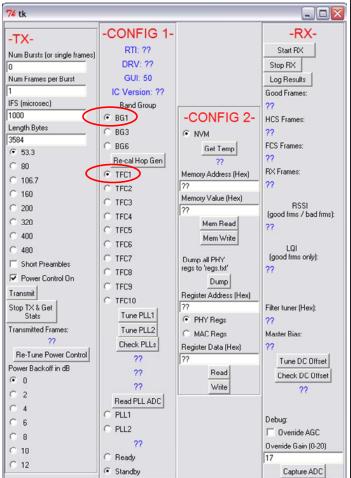
RX Frames:

RSSI

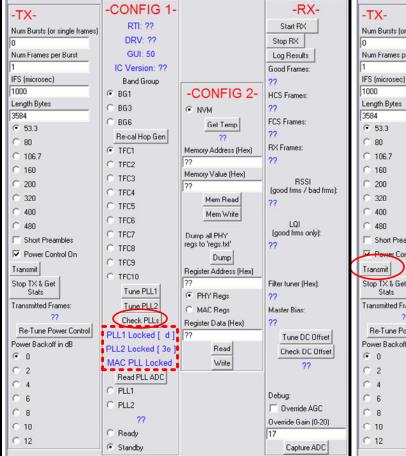
(good frms / bad frms):

??

22



- \square Select the appropriate BG(1/3/6)
- ☐ Select TFC(1-10)



- ☐ Hit 'Check PLLs' button
- ☐ At this point you should see the display indicated in the red block. PLL1, PLL2 and MAC PLL must indicate 'Locked' in order to proceed.
- Mem Write C TFC6 LQI 480 (good frms only): C TFC7 Dump all PHY Short Preambles regs to 'regs.txt' C TFC8 Power Control On Dump C TFC9 Transmit Register Address (Hex) C TFC10 Stop TX & Get Filter tuner (Hex): Tune PLL1 PHY Regs Transmitted Frames: Tune PLL2 C MAC Regs Master Bias Check PLLs Register Data (Hex) Re-Tune Power Control PLL1 Locked [d] Tune DC Offset Power Backoff in dB PLL2 Locked [3e] Read Check DC Offset @ O MAC PLL Locked Write Read PLL ADC C PLL1 Debug: C PLL2 Override AGC Override Gain (0-20) Ready C 12 Standby Capture ADC

☐ At this point the DUT is ready to transmit

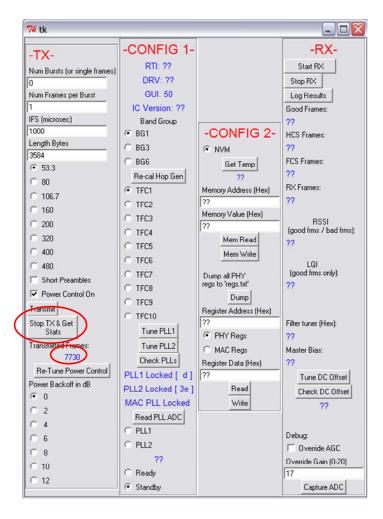
☐ Hit Transmit to start continuous

6195 Lusk Blvd, Suite 200 San Diego, CA 92121 858-812-1000

transmission



10



- When finished with testing, hit 'Stop TX and Get Stats' button to stop transmitter
- ☐ At this point you can change TFC / BG setting and repeat steps 7-10

End of Document

