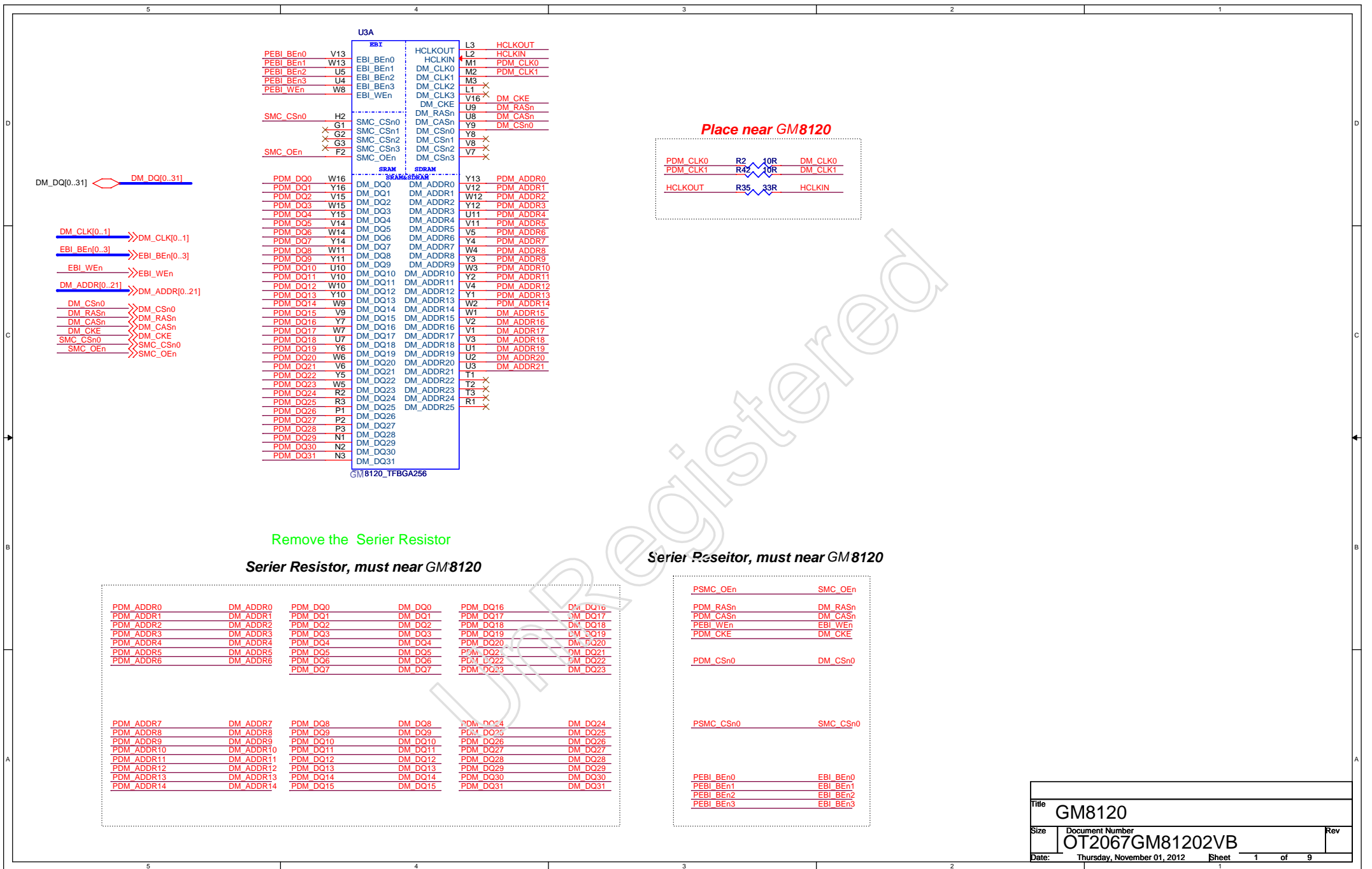


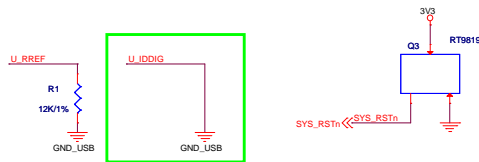
| Data code/<br>Version | Modification   |
|-----------------------|----------------|
| 1.0                   | -First release |
|                       |                |
|                       |                |
|                       |                |
|                       |                |
|                       |                |
|                       |                |

# Change log:

1. USB Connector
2. IRLED Board Connector

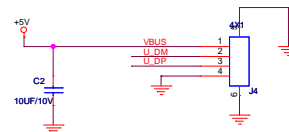
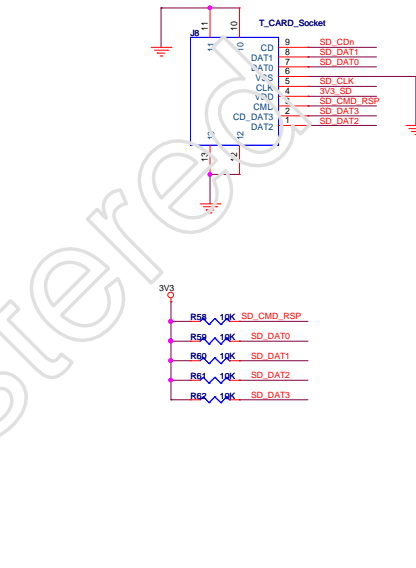
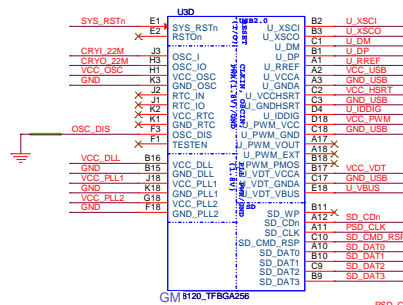
|       |                             |              |
|-------|-----------------------------|--------------|
| Title |                             |              |
| Note  |                             |              |
| Size  | Document Number             | Rev          |
|       | OT2067GM81202VB             |              |
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The diagrams illustrate the placement of decoupling capacitors for various power rails:

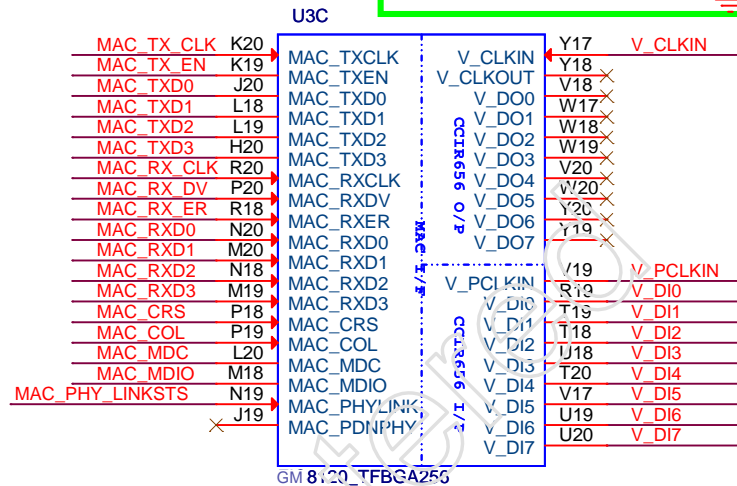
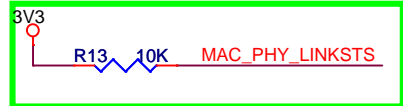
- VCC\_USB:** A 3V3 input is connected to a 1A, 120ohm @ 100MHz inductor (L10). A 10uF/10V capacitor (C6) is connected to the input, and a 0.01uF capacitor (C37) is connected to the output of L10, which is also connected to GND\_USB.
- VCC\_PWM:** A 3V3 input is connected to a 0.1uF capacitor (C62), which is then connected to GND\_USB.
- VCC\_HSRT:** A 3V3 input is connected to a 1A, 120ohm @ 100MHz inductor (L11). A 0.01uF capacitor (C36) is connected to the output of L11, which is also connected to GND\_USB.
- VCC\_VDT:** A 3V3 input is connected to a 0.1uF capacitor (C65), which is then connected to GND\_USB.



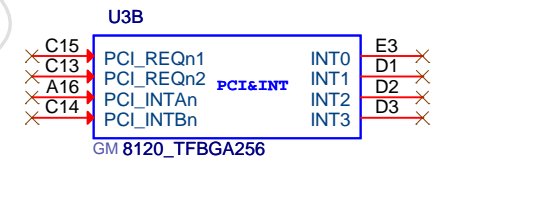


MAC\_TX\_CLK >> MAC\_TX\_CLK  
MAC\_TX\_EN >> MAC\_TX\_EN  
MAC\_TXD[0..3] >> MAC\_TXD[0..3]

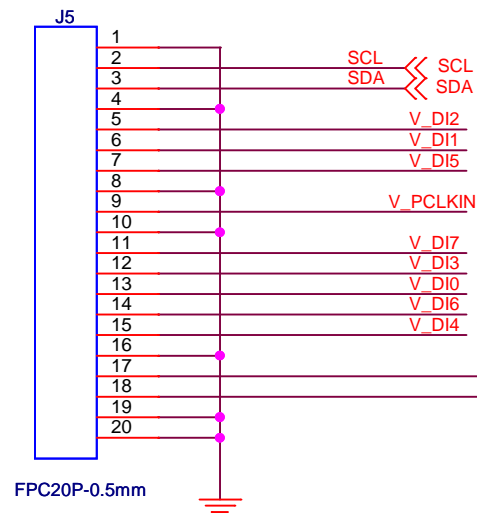
MAC\_RX\_CLK >> MAC\_RX\_CLK  
MAC\_RX\_DV >> MAC\_RX\_DV  
MAC\_RX\_ER >> MAC\_RX\_ER  
MAC\_RXD[0..3] >> MAC\_RXD[0..3]  
MAC\_CRS >> MAC\_CRS  
MAC\_COL >> MAC\_COL  
MAC\_MDC >> MAC\_MDC  
MAC\_MDIO >> MAC\_MDIO



External devices interrupt input. Active high.  
(internal pull-down)



Master requests to use PCI bus. (active low)

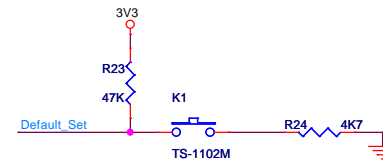
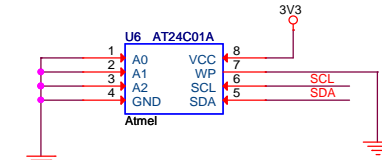
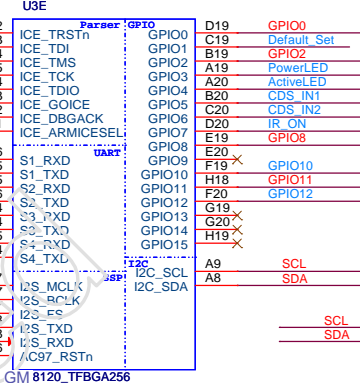
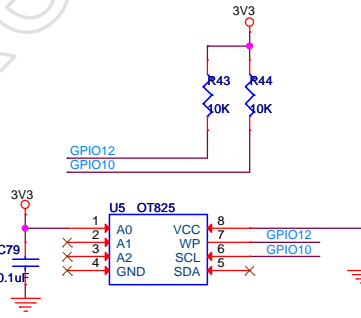
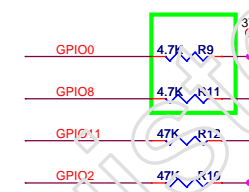
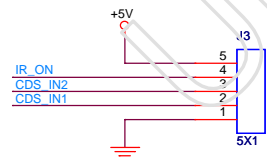
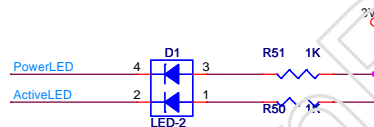
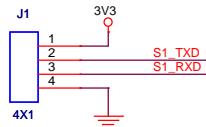
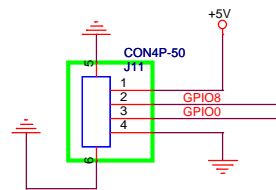


Title  
GM8120

Size  
Document Number  
OT2067GM81202VB

Rev

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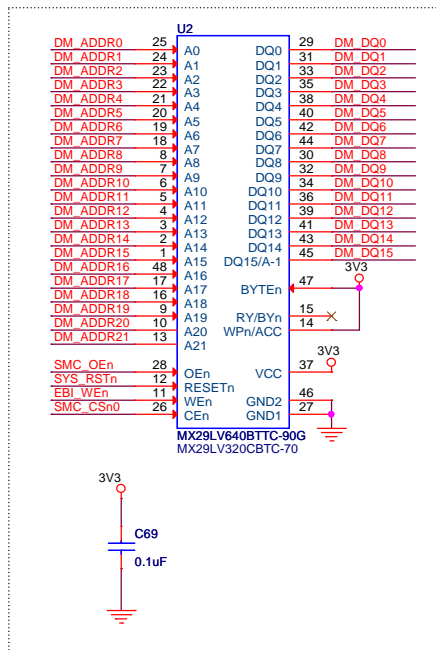
GPIO[11] Timer test. Should be pull-low in normal use.  
 GPIO[8] CPU operating mode. 0=sync mode, 1=async mode  
 At-speed testing use sync mode, but normal operation use asyn mode.  
 Should be pull-high in normal use.  
 GPIO[2] Bypass PLL or not. IC Tester use this jumper setting.  
 Should be pull-low in normal use.  
 GPIO[0] Define 8-bit or 16-bit booting.  
 pull-low: 8-bit booting pull-high: 16-bit booting

|       |  |  |                             |
|-------|--|--|-----------------------------|
| Title |  |  | GM8120                      |
| Size  |  |  | Document Number             |
|       |  |  | OT2067GM81202VB             |
| Date: |  |  | Thursday, November 01, 2012 |
| Sheet |  |  | 2 of 9                      |

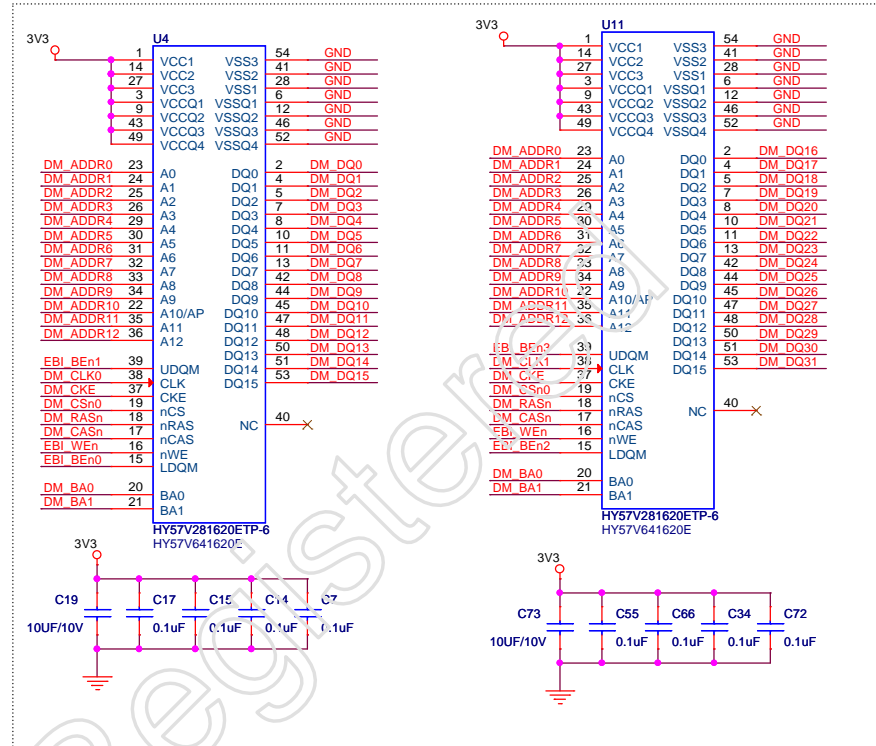
DM\_ADDR[0..21] >> DM\_ADDR[0..21]  
 DM\_DQ[0..31] << DM\_DQ[0..31]  
 EBI\_BE[0..3] >> EBI\_BE[0..3]  
 EBI\_WE >> EBI\_WE  
 DM\_CS[0] >> DM\_CS[0]  
 DM\_RAS >> DM\_RAS  
 DM\_CAS >> DM\_CAS  
 DM\_CLK[0..1] >> DM\_CLK[0..1]  
 DM\_CKE >> DM\_CKE  
 SMC\_CS[0] >> SMC\_CS[0]  
 SMC\_OE >> SMC\_OE  
 SYS\_RST >> SYS\_RST

DM\_ADDR13 DM\_BA0  
 DM\_ADDR14 DM\_BA1

### On Board Flash (4Mx16 or 2Mx16)



### On Board SDRAM(8Mx16)x2



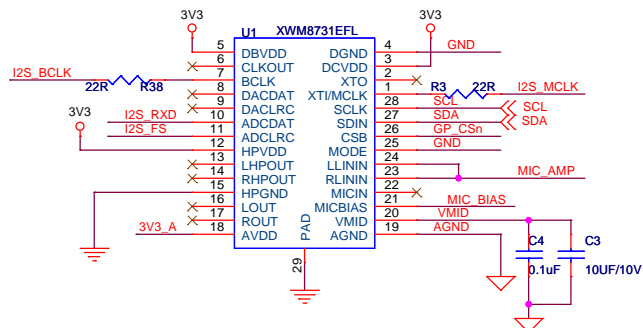
HY57V281620ETP-6  
 HY57V641620E

|        |                             |              |
|--------|-----------------------------|--------------|
| Title  |                             |              |
| Memory |                             |              |
| Size   | Document Number             | Rev          |
|        | OT2067GM81202VB             |              |
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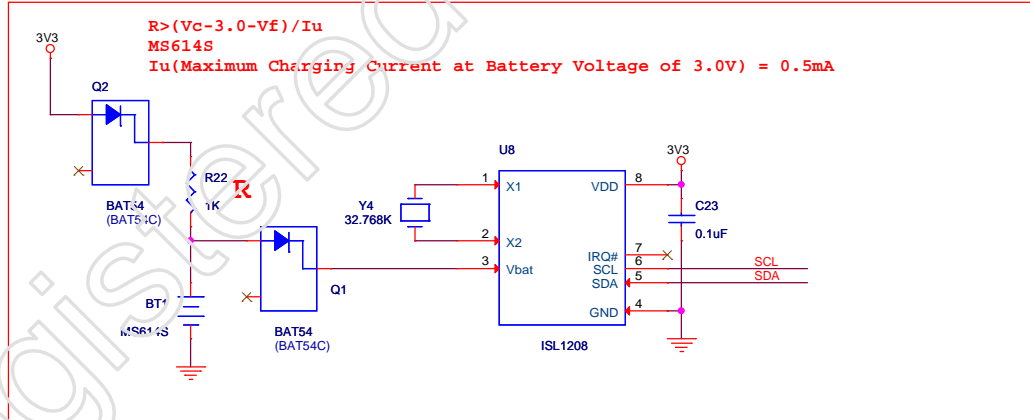
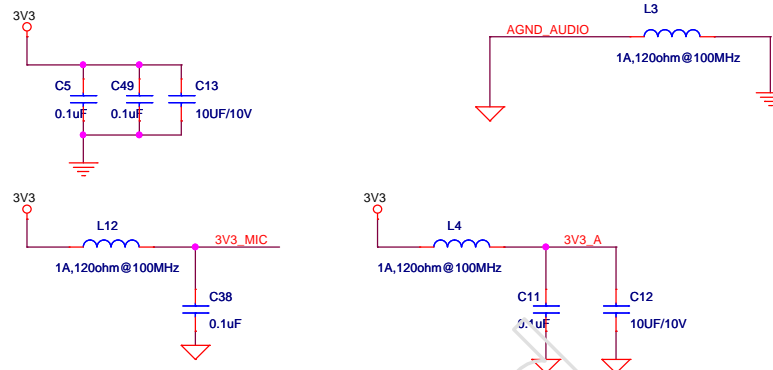




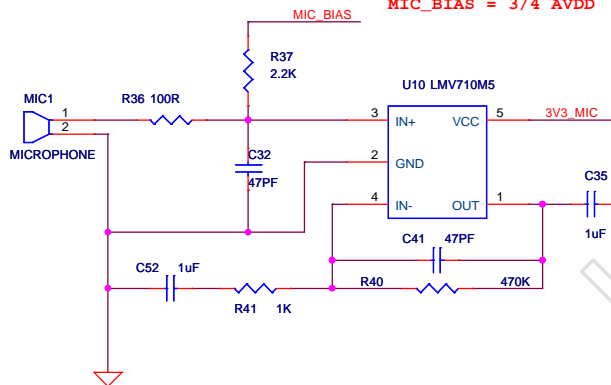
I2S\_MCLK <-> I2S\_MCLK  
I2S\_BCLK <-> I2S\_BCLK  
I2S\_FS <-> I2S\_FS  
I2S\_RXD <-> I2S\_RXD



2-Wire mode address setting  
GP\_CS: 'H': 0xC4, 'L': 0xC6



MIC\_BIAS = 3/4 AVDD



Normal Mode (VDD) to Battery Backup Mode  
To transition from the VDD to VBAT mode, both of the following conditions must be met:

Condition 1:  
 $VDD < VBAT - VBATHYS$

where  $VBATHYS \approx 50mV$

Condition 2:  
 $VDD < VTRIP$

where  $VTRIP \approx 2.2V$

Battery Backup Mode (VBAT) to Normal Mode (VDD)

The ISL1208 device will switch from the VBAT to VDD mode when one of the following conditions occurs:

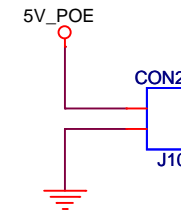
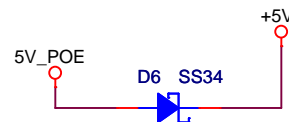
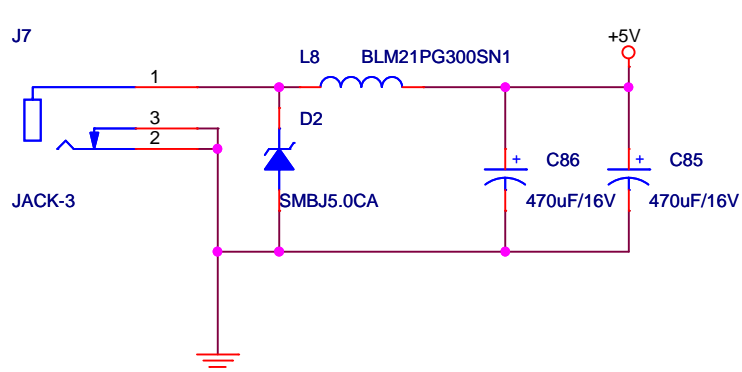
Condition 1:  
 $VDD > VBAT + VBATHYS$

where  $VBATHYS \approx 50mV$

Condition 2:  
 $VDD > VTRIP + VTRIPHYS$

where  $VTRIPHYS \approx 30mV$

|            |                             |              |
|------------|-----------------------------|--------------|
| Title      |                             |              |
| Audio, RTC |                             |              |
| Size       | Document Number             | Rev          |
|            | OT2067GM81202VB             |              |
| Date:      | Thursday, November 01, 2012 | Sheet 7 of 9 |

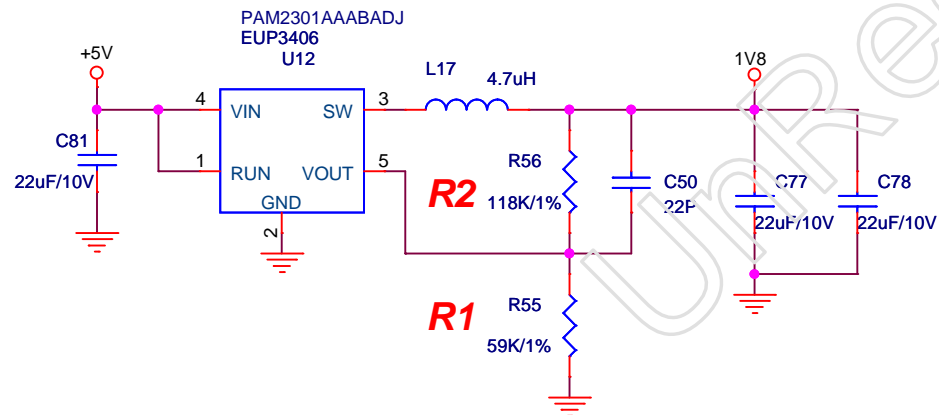
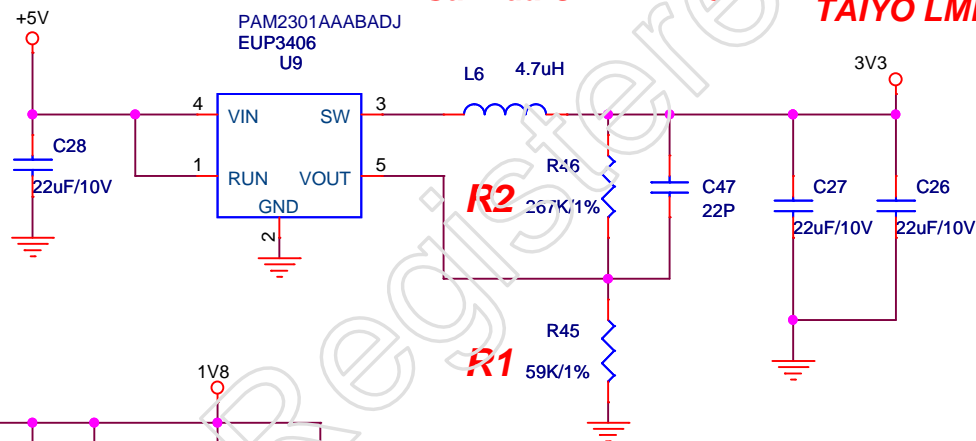


**C4-K2.5L MITSUMI**  
**Sumida CDRH4D18**

**22uF/10V Capacitor use**

**TDK C3216Y5V1C226MT**

**TAIYO LMK316BJ226ML-T**



$$V_{out} = 0.6V \times (1 + R2/R1)$$

$$3.3V = 0.6V \times (1 + 267K/59K)$$

$$1.8V = 0.6V \times (1 + 118K/59K)$$

|       |                             |              |
|-------|-----------------------------|--------------|
| Title |                             |              |
| Power |                             |              |
| Size  | Document Number             | Rev          |
|       | OT2067GM81202VB             |              |
| Date: | Thursday, November 01, 2012 | Sheet 9 of 9 |





