Block Diagram $V_{DD} = 2.0 - 3.6V$ Connect Vunreg = 4.0 - 30V- See Pin Configuration Table -Pin 21 to Pin 22 Debug** when powering 7 from 4.0 - 30V supply Input 4 - 30V DC **IO Controller Digital Supplies** Isolated **USART** Regulator **USART** ADC On-chip 1.8V Audio / DC Regulator Output 8 Channels Timer 1 (16-bit) 3.3V DC 12-bit resolution Analogue and Timer 3 (8-bit) Batt Temp Radio Supplies Mon. Mon. Timer 4 (8-bit) **MAC** address serial chip Sleep Timer Timer 2 Power-On Watchdog MAC Reset Timer Sleep Mode Controller 802.15.4 Brown-out 32 MHz **FLASH** Debug Hi-Speed DMA 32.000 MHz RC Write Interface Crystal Osc Osc 128kByte FLASH 32.768 kHz 32 kHz 8051 32.768 kHz RC Crystal Osc Osc Core **Memory Arbitrator MCU** Random # Clock Mux & Gen. CRC 8kByte SRAM Calibration CC2431 ONLY 8051 Hi-speed **IRQ** Location Engine Encryption **Enhanced core** Controller Decryption Chip Antenna Radio data interface SMA Jack RP-SMA Jack CSMA / CA Strobe Demodulator Receive Chain Processor **AGC** Frequency Synthesiser ~ Balun Radio Registers FIFO and Frame Control RF_N Modulator **Transmit Chain** CC2420 RF Transceiver **RF Ground Plane** CC2430 / 31 SoC Digital Analogue

**Debug Interface is shared with GPIO Port pins 2_1 and 2_2

Mixed

Block Diagram

