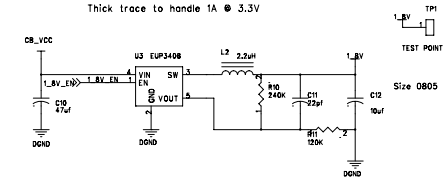
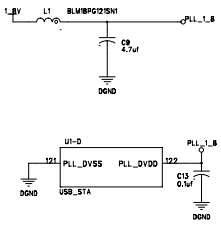
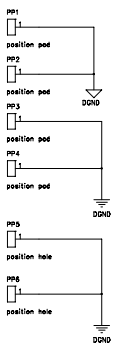
Thick trace to handle 1A @ 3.3V

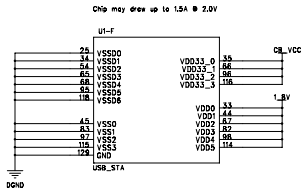


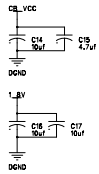
Thick trace to handle 10mA @ 2.0V
Run as a trace not plane



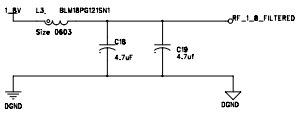


These need to be placed close to power pins
These ones should be on top

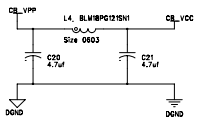


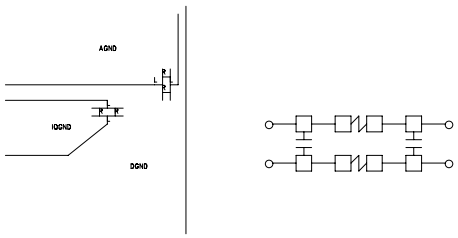


The traces should run through the Caps
Thick trace to handle .3A @ 2.0V

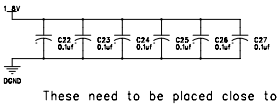


Place between Digital and RF power sections on the board
Thick traces to handle 1A at 3.3V
The traces should run through the Caps

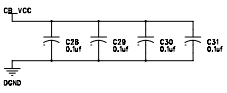




These need to be placed close to power pins



These need to be placed close to power pins



Title	POWER	
Size C	Document Number	Rev ?
Date: Wednesday, April 08, 2009	Sheet 3 of 5	

3DSP-WLAN + AIROHA RF(AL2230) USB

Version B

Page list:

01	Cover	Cover page
02	BUS	USB interface
03	Power	The power supply part
04	RF Interface	The Airoha Transceiver & PA & Antenna
05	GPIO	The digital interface between DSP & RF & other parts

Version Information:

Version	Date	Comment	Designer
Ver 1.0	Feb-27-2008	Initial design, usb interface of MinCard	Aaron HW_Team/Xi'an
Ver 2.0	July-27-2008	Change to two antenna in page4	Aaron HW_Team/Xi'an
Ver 2.4	Jan-15-2009	No change	Isaac HW_Team/Xi'an
Ver 2.5	Jan-21-2009	Add PRST# signal to control the 1.8V power enable	Isaac HW_Team/Xi'an
Ver 2.6	Mar-5-2009	1.Added two capacitors on the antenna circuit 2.Corrected the connection relationship of the components R13,C46 and R15,C59	Isaac HW_Team/Xi'an
Ver 2.7	Mar-19-2009	Added two position holes	Isaac HW_Team/Xi'an
Ver 2.8	Apr-8-2009	Changed the W_disable contoll signal from GPIO7 to GPIO18	Isaac HW_Team/Xi'an

3DSP Corporation

********** NOTICE **********
These are schematics of a design example which is under development.
3DSP Corp. assumes no responsibility for the content and makes no commitment to update any of the information herein.
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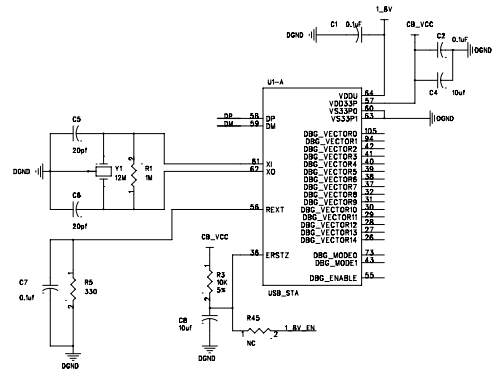
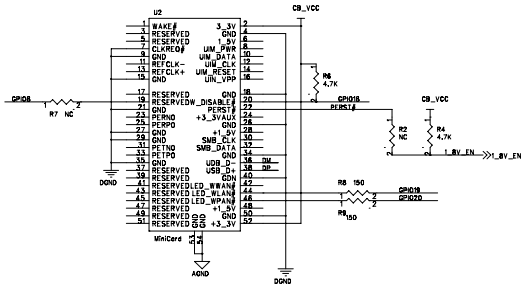
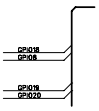
Title	AL2230s Cover Page	
Size: A2	Document Number:	Rev: 1
Date: Wednesday, April 08, 2009	Sheet 1 of 5	

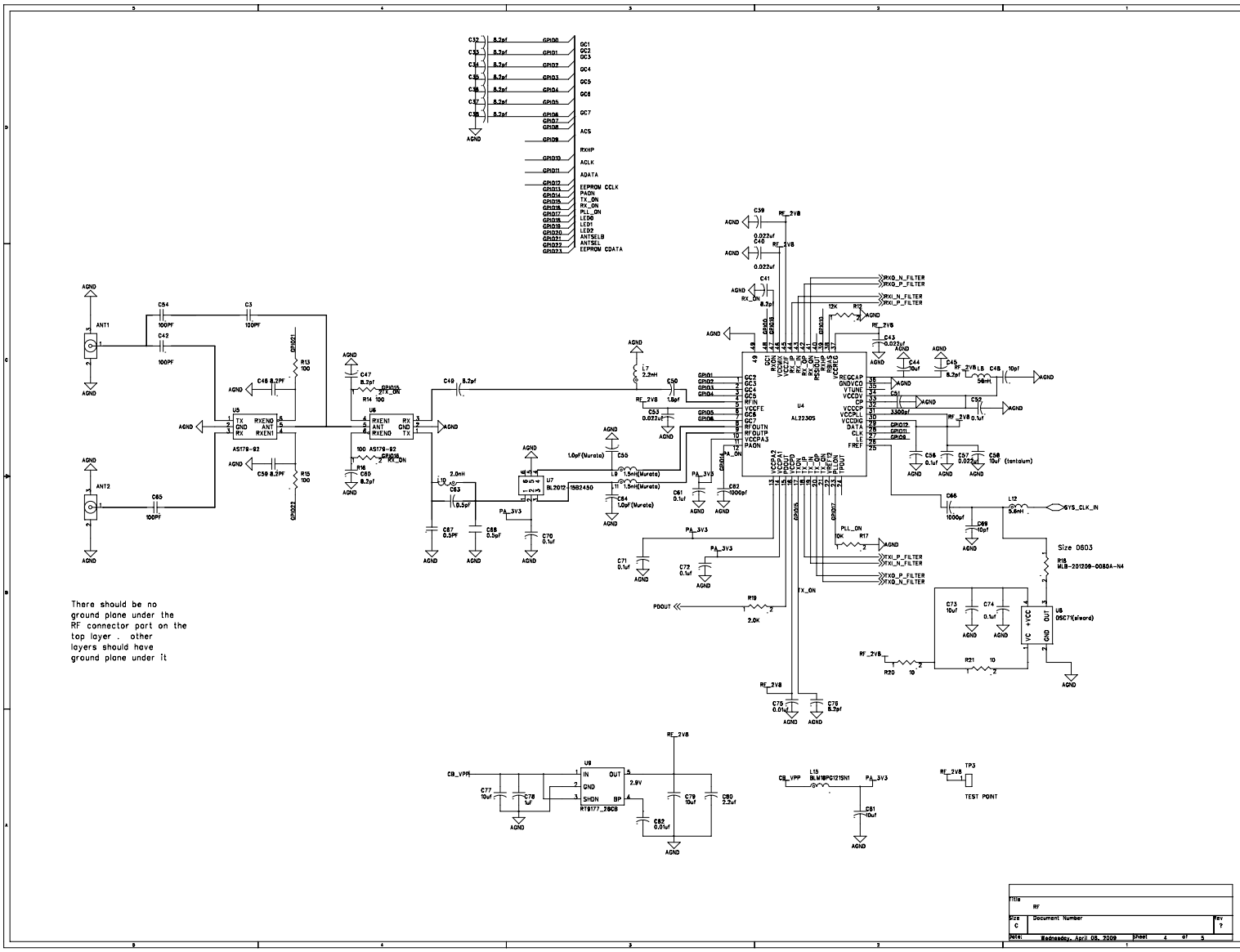
Refer to Layout Reference for placement info







Title	BUS	
Size C	Document Number	Rev ?
Date: Wednesday, April 08, 2009	Sheet 2 of 5	


There should be no ground plane under the RF connector part on the top layer . other layers should have ground plane under it
Size 0603
Title
RF
Size C
Document Number
Rev ?
Date: Wednesday, April 08, 2009
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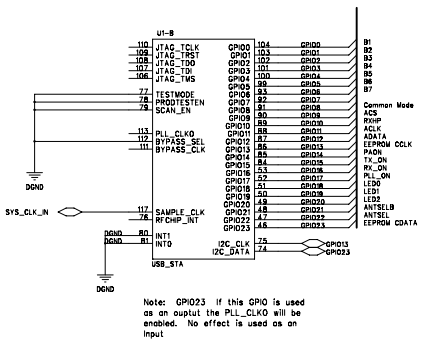
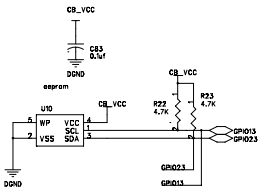


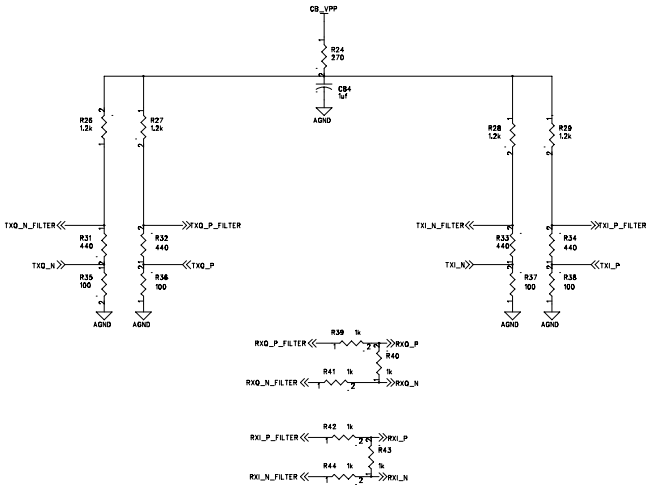
Note: GPIO23 If this GPIO is used as an ouptut the PLL_CLKO will be enabled. No effect is used as an input

DSP Config and GPIOs

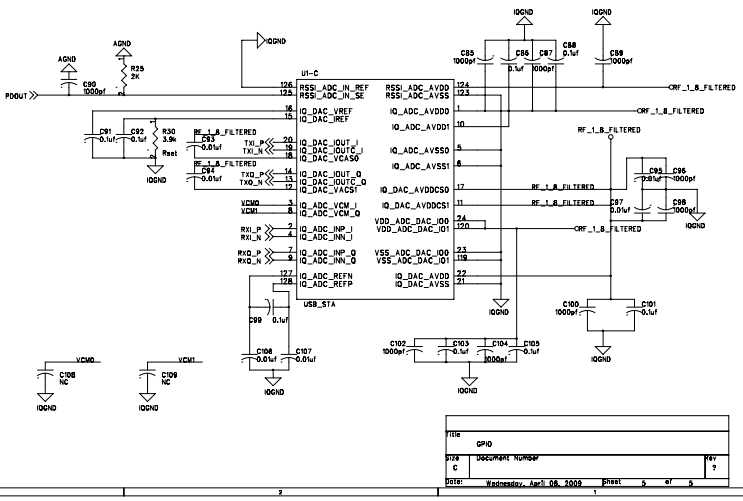


EEPROM

TX/RX RFI



IQ DAC, IQ ADC, RSSI ADC



Title	GPIO		
Size C	Document Number		Rev 7
Date:	Wednesday, April 08, 2009	Sheet 5	of 5