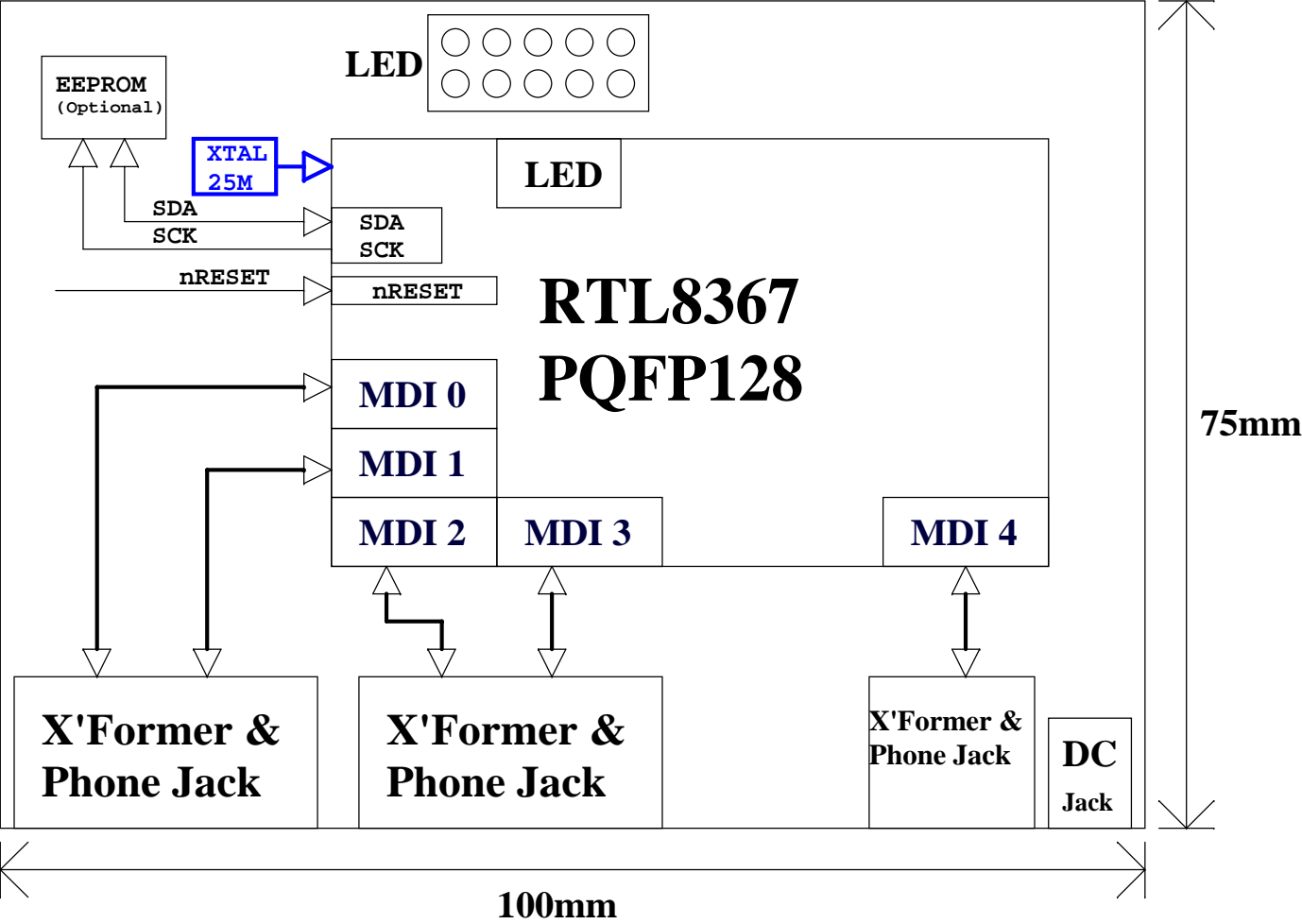


RTL8367 (PQFP128) Demo-Board Block Diagram



REVISION HISTORY

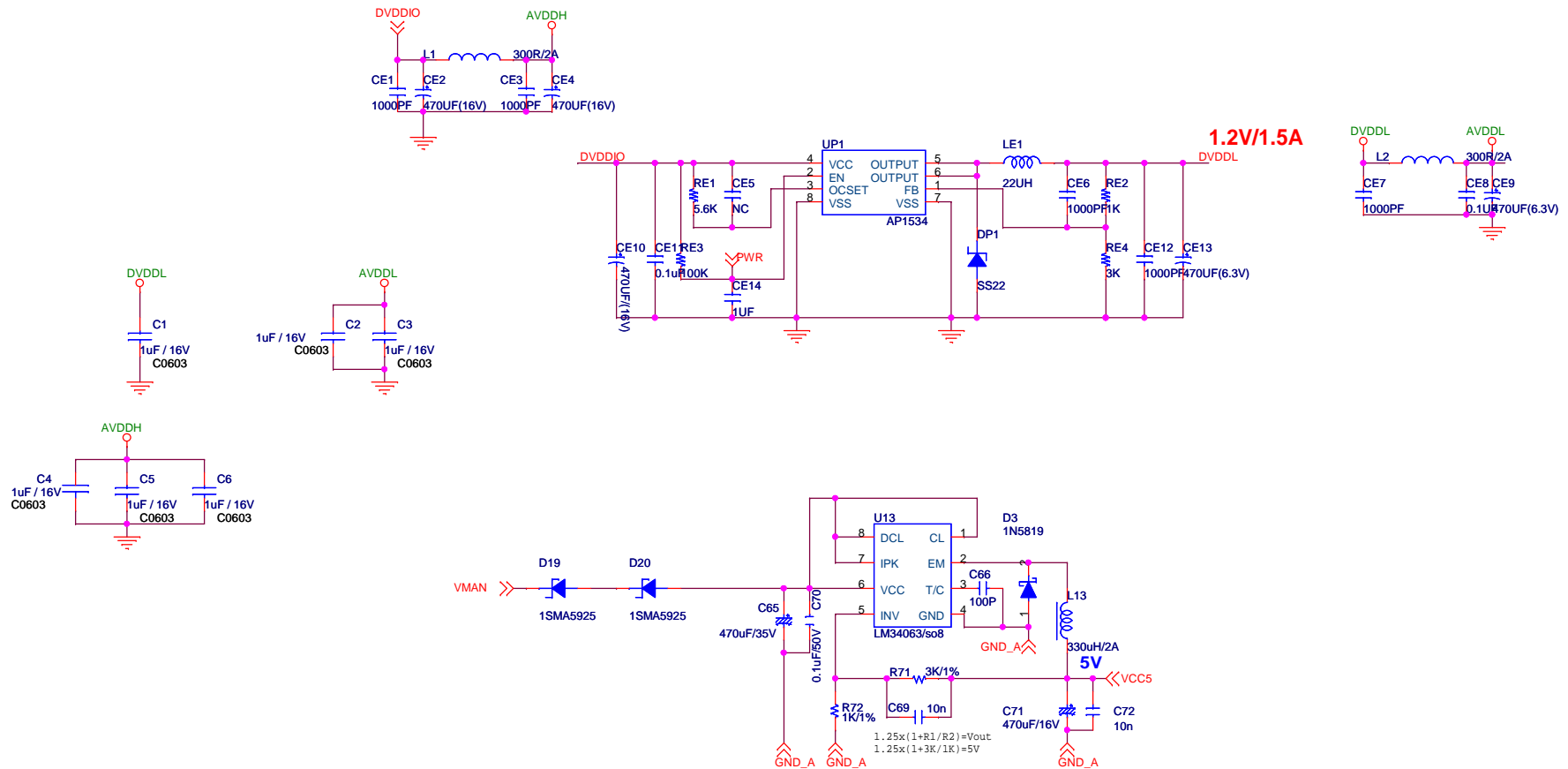
Revision	Release Date	Summary
v.Pre-2.0	2009/09/14	Preliminary Release
v.Pre-2.01	2009/10/16	1. Modify schematic, MDI channel A, B, C, & D's X'Formre central tap at primary side tie with each other, in page 4, X'Former. 2. CAP 0.1uF change to NC: C80, C83, C84, C85, C86, C87, C88, C89, C90, C92, C94, C95, C96, C98, and C99, in page 4, X'Former. 3. CAP 0.1uF change to 0.01uF: C81, C82, C91, C93, and C97, in page 4, X'Former.
v.Pre-2.02	2009/10/29	1. Res 4.7k 5% change to NC: R35, R36, in page 3, RTL8367.

Title		
RTL8367 Demo-Boaard Block Diagram		
Size B	Document Number <Doc>	Rev Pre-2.02
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Max Load: VDDL 1A (continue)

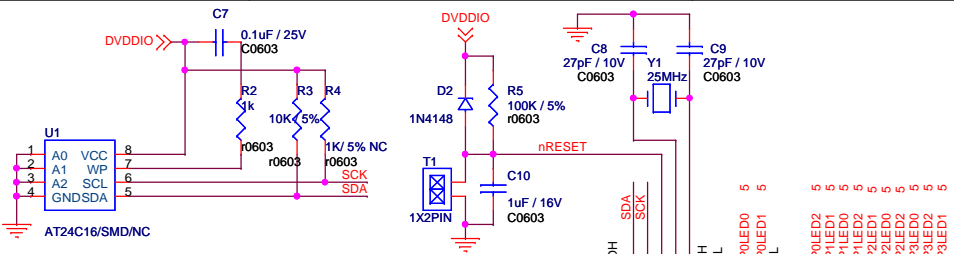
$$1.0V = 0.92V \times (1 + 887 / 10K)$$

Adjust R26, R73 to make sure chip side voltage is 1V
(Due to 2Layer design, need to consider the transmission loss)



Title		
RTL8367 Power Regulator		
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3.3V
SDA
GND
SCK



PIN89 P0LED0: Must Pull High or Floating
PIN84 P0LED2: Must Pull High or Floating
PIN82 P1LED0: Must Pull High or Floating
PIN81 P1LED2: Must Pull High or Floating
PIN77 P3LED0 / Must Pull Low
PIN76 P3LED2 / Must Pull High

PIN79 P2LED0 / DISAUTOLOAD
** Pull Low: Enable Auto load EEPROM
Pull High: Disable Auto load EEPROM
PIN78 P2LED2 / DIS_8051
Pull Low: Enable 8051
Pull High: Disable 8051
PIN73 P4LED0 / EEPROM_MOD
** Pull Low: 24C02~24C16
Pull High: 24C32~

4 P0MDIAP P0MDIAP
4 P0MDIAN P0MDIAN
4 P0MDIBP P0MDIBP
4 P0MDIBN P0MDIBN

4 P0MDICP P0MDICP
4 P0MDICN P0MDICN
4 P0MDIDP P0MDIDP
4 P0MDIDN P0MDIDN

4 P1MDIAP P1MDIAP
4 P1MDIAN P1MDIAN
4 P1MDIBP P1MDIBP
4 P1MDIBN P1MDIBN

4 P1MDICP P1MDICP
4 P1MDICN P1MDICN
4 P1MDIDP P1MDIDP
4 P1MDIDN P1MDIDN

4 P2MDIAP P2MDIAP
4 P2MDIAN P2MDIAN
4 P2MDIBP P2MDIBP
4 P2MDIBN P2MDIBN

4 P2MDICP P2MDICP
4 P2MDICN P2MDICN

AVDDL
AVDDH
PLLVDL0

AVDDL
AVDDH
PLLVDL0

AVDDL
AVDDH
PLLVDL0

AVDDL
AVDDH
PLLVDL0

AVDDL
AVDDH
PLLVDL0

AVDDL
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AVDDH
PLLVDL0

AVDDL
AVDDH
PLLVDL0

AVDDL
AVDDH
PLLVDL0

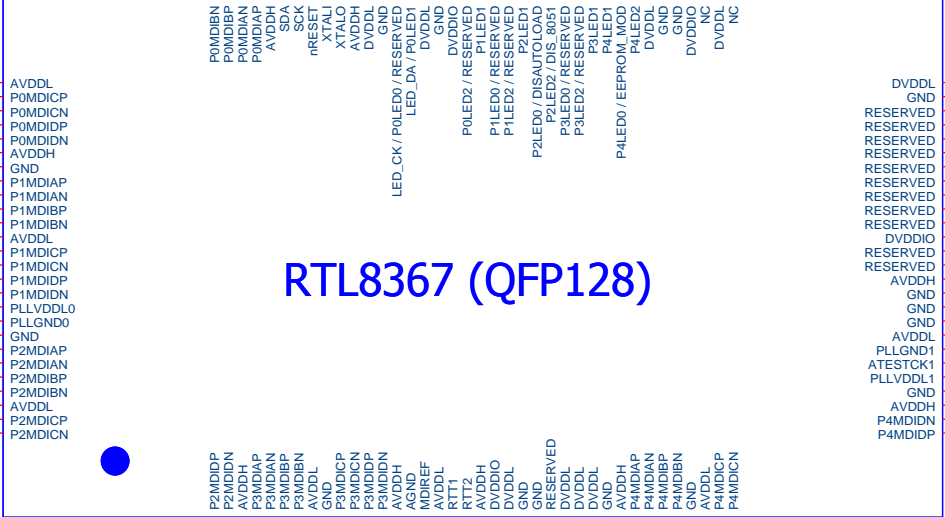
AVDDL
AVDDH
PLLVDL0

AVDDL
AVDDH
PLLVDL0

AVDDL
AVDDH
PLLVDL0

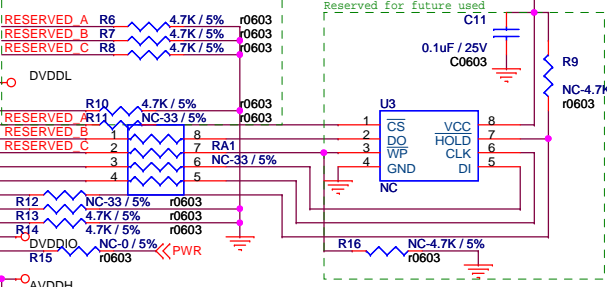
AVDDL
AVDDH
PLLVDL0

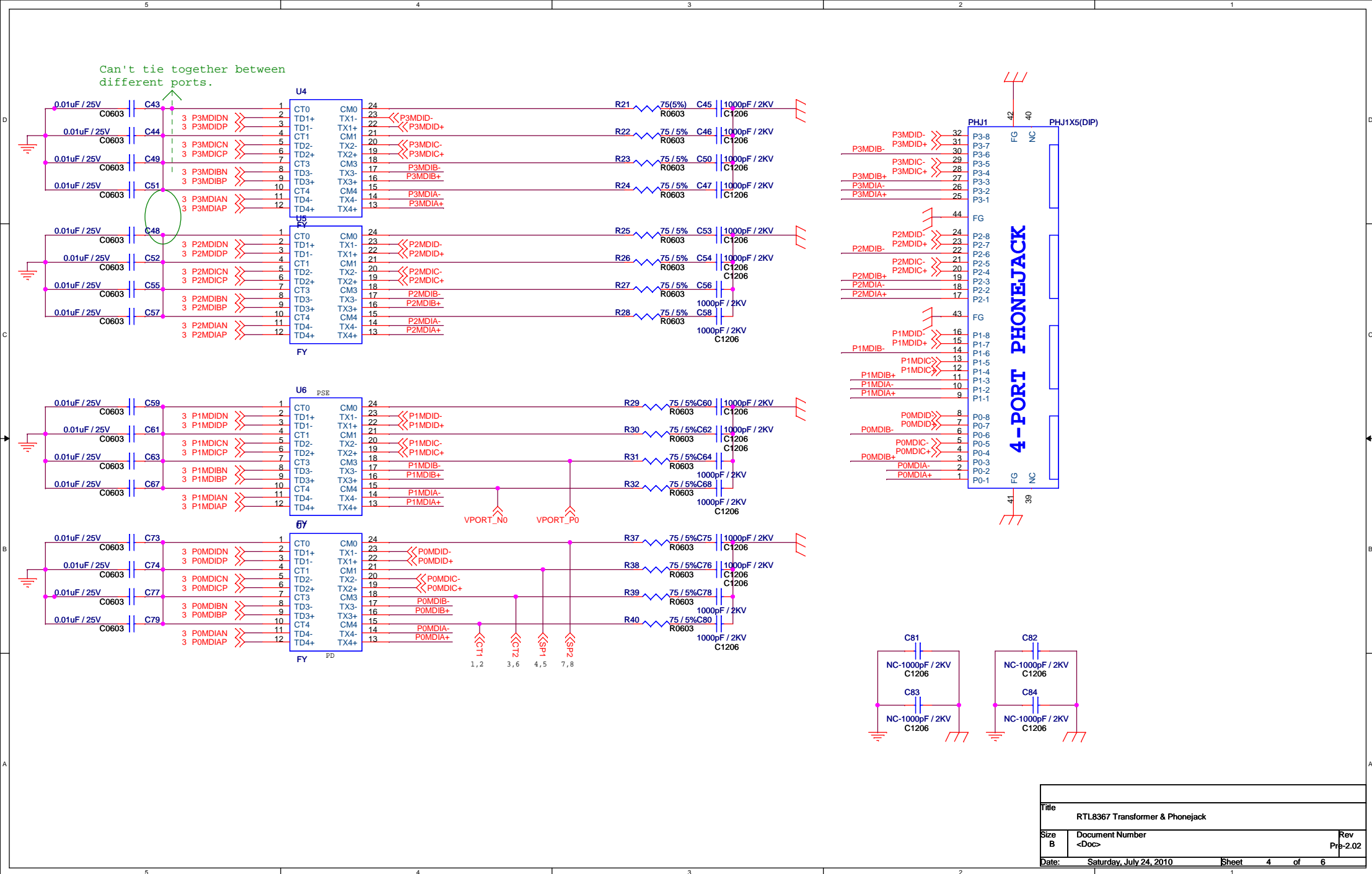
AVDDL
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PLLVDL0

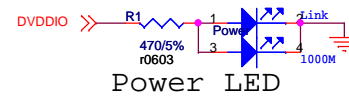
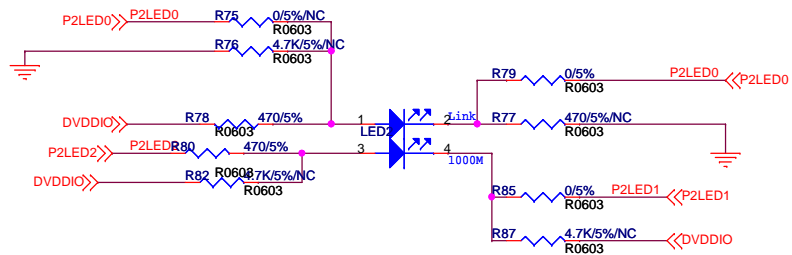
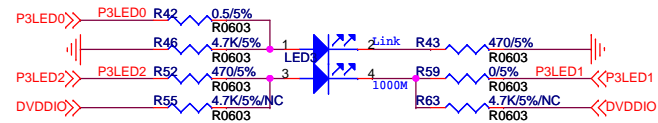
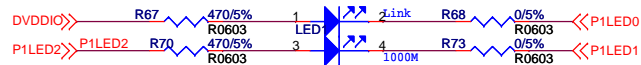
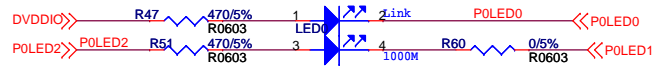


RTL8367 (QFP128)

These pin must connect to GND throught
1k ohm resistor when unused.







P2LED0 / DISAUTOLOAD
** Pull Low: Enable Auto load EEPROM
Pull High: Disable Auto load EEPROM

P2LED2 / DIS_8051
Pull Low: Enable 8051
** Pull High: Disable 8051

Title		
RTL8367 LED		
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B	<Doc>	Pre-2.02
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