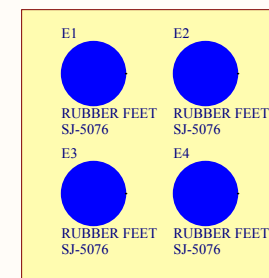


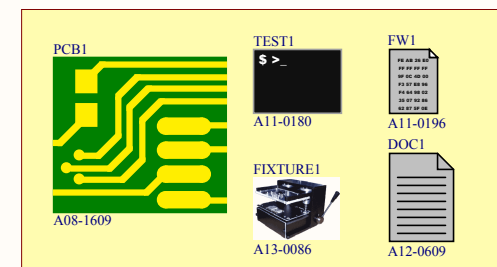
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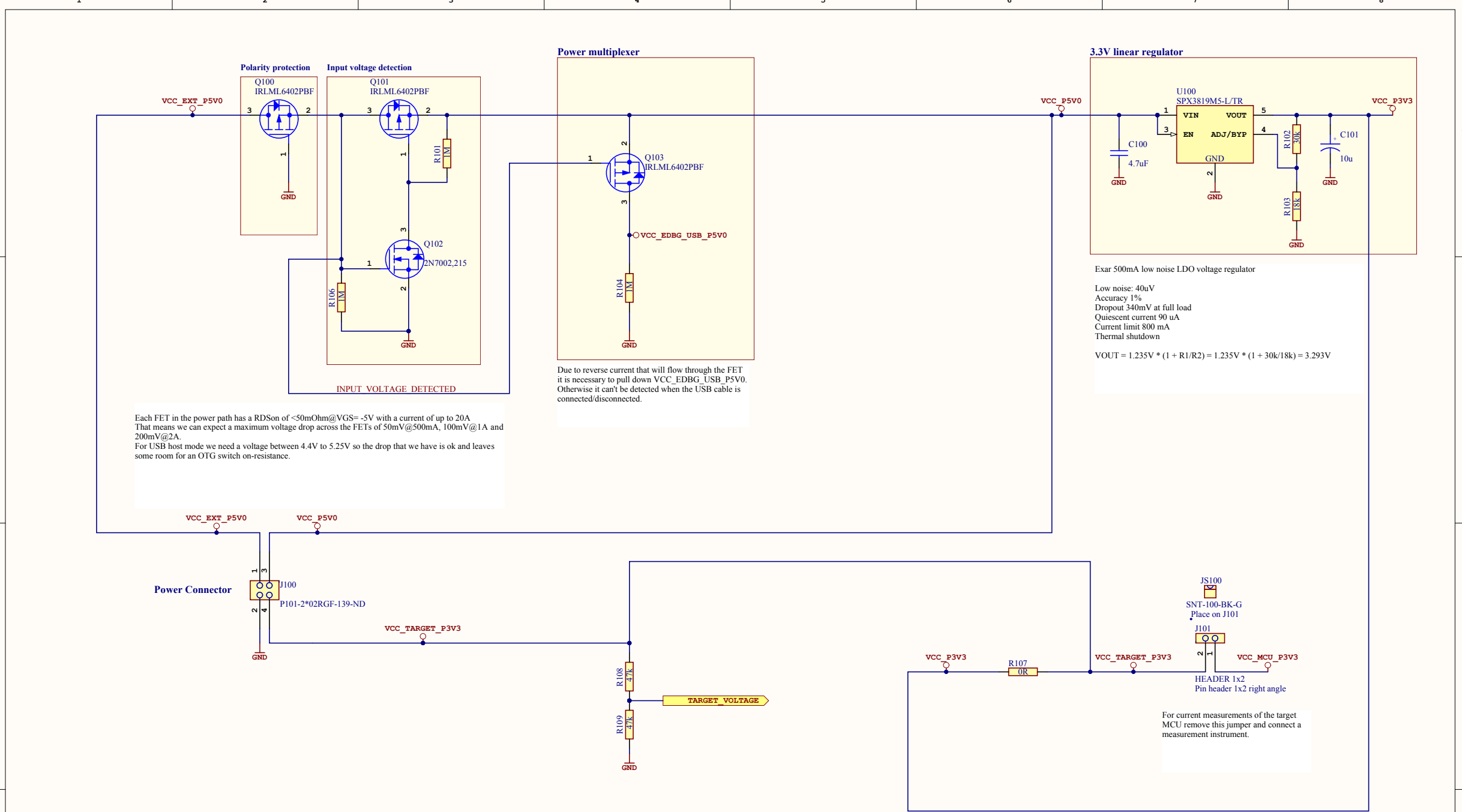
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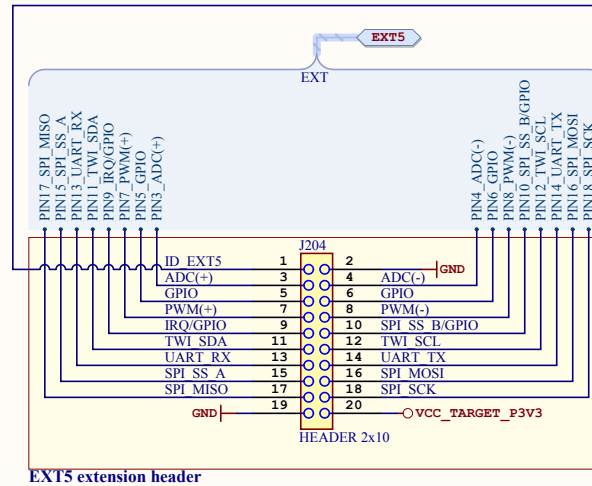
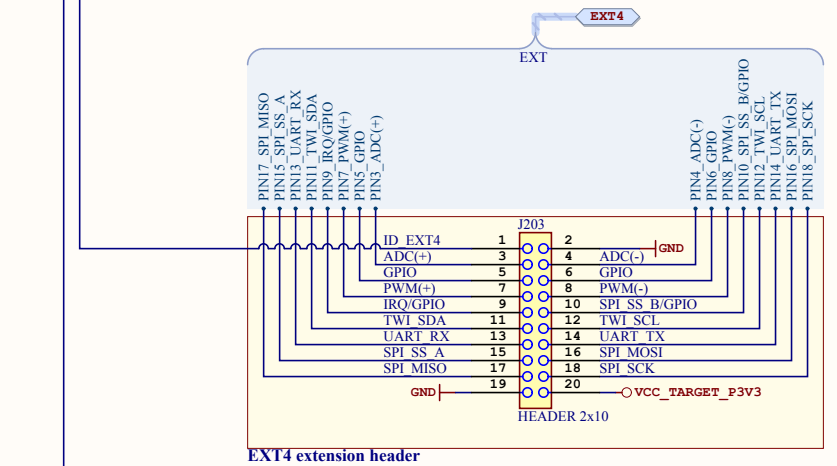
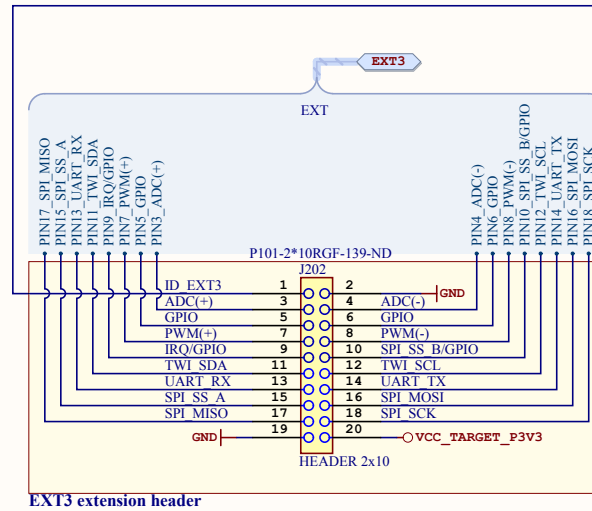
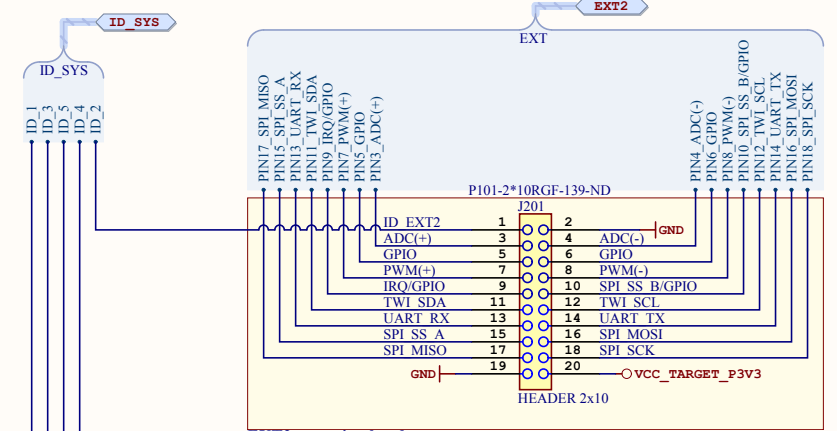
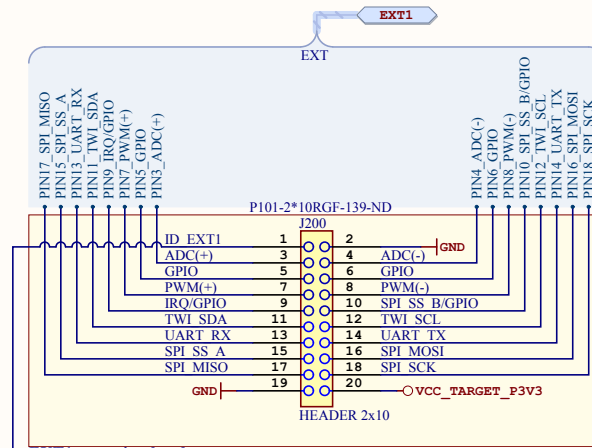
Product number/revision
Serial number


Label PCBA with MAC64 and FCC ID

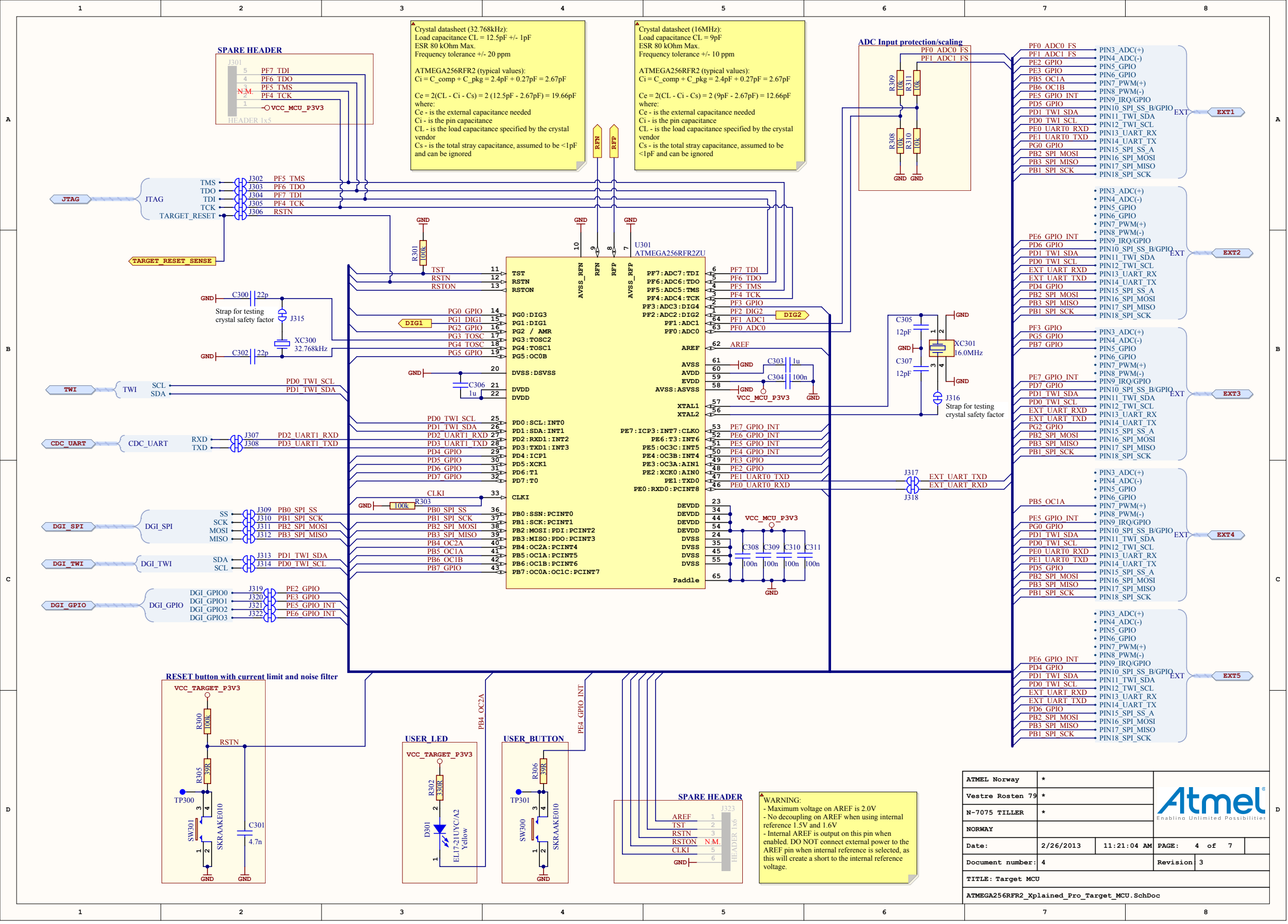


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Crystal datasheet (32.768kHz):
Load capacitance CL = 12.5pF +/- 1pF
ESR 80 kOhm Max.
Frequency tolerance +/- 20 ppm

ATMEGA256RFR2 (typical values):
 $C_i = C_{comp} + C_{pkg} = 2.4pF + 0.27pF = 2.67pF$

$C_e = 2(CL - C_i - C_s) = 2(12.5pF - 2.67pF) = 19.66pF$

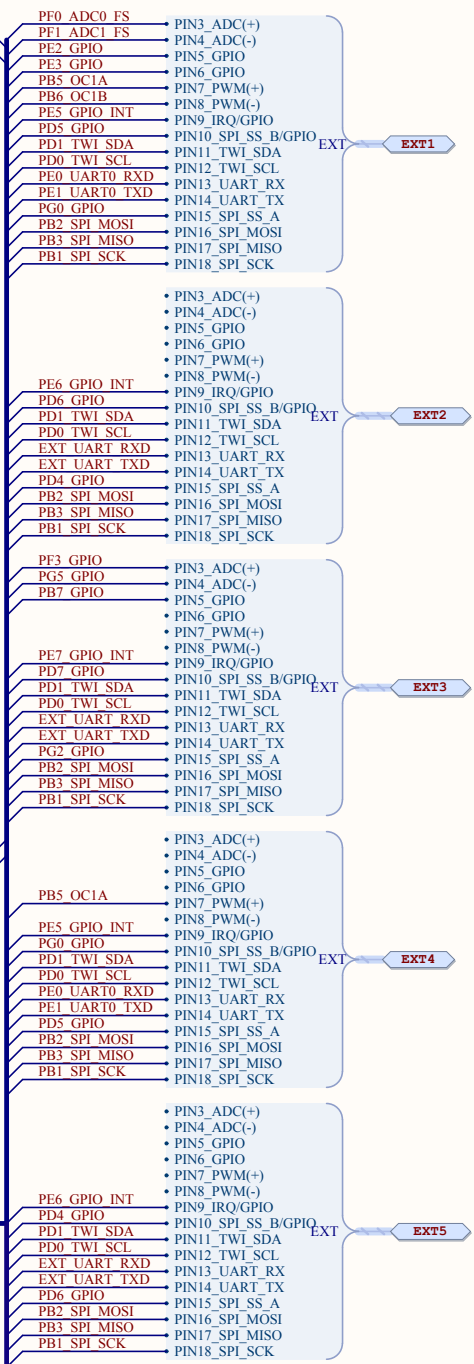
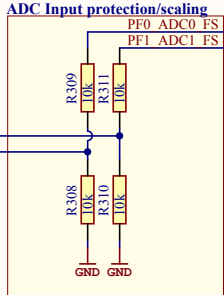
where:
Ce - is the external capacitance needed
Ci - is the pin capacitance
CL - is the load capacitance specified by the crystal vendor
Cs - is the total stray capacitance, assumed to be <1pF and can be ignored

Crystal datasheet (16MHz):
Load capacitance CL = 9pF
ESR 80 kOhm Max.
Frequency tolerance +/- 10 ppm

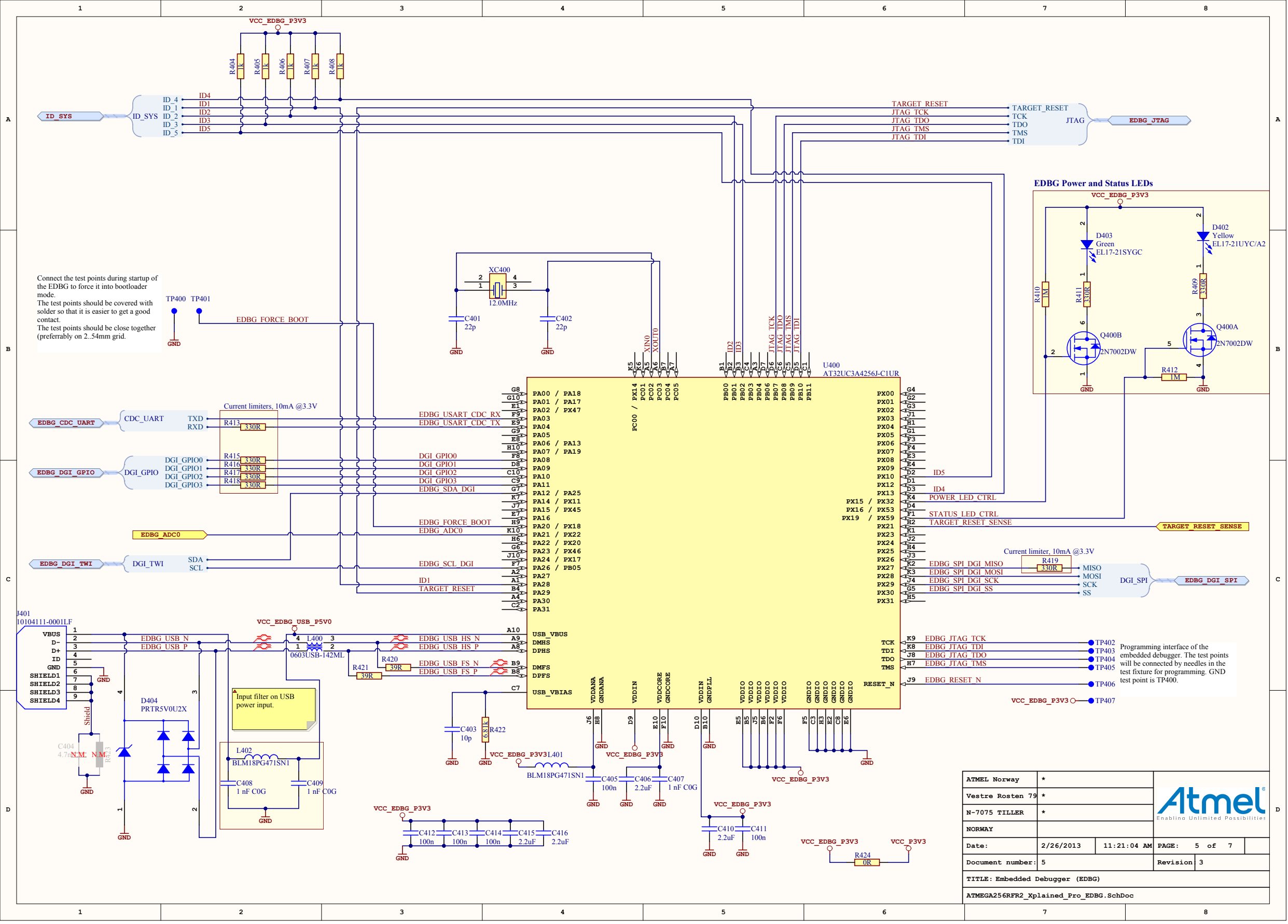
ATMEGA256RFR2 (typical values):
 $C_i = C_{comp} + C_{pkg} = 2.4pF + 0.27pF = 2.67pF$

$C_e = 2(CL - C_i - C_s) = 2(9pF - 2.67pF) = 12.66pF$


where:
Ce - is the external capacitance needed
Ci - is the pin capacitance
CL - is the load capacitance specified by the crystal vendor
Cs - is the total stray capacitance, assumed to be <1pF and can be ignored

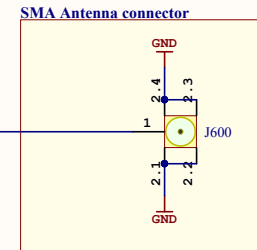



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Connect the test points during startup of the EDBG to force it into bootloader mode. The test points should be covered with solder so that it is easier to get a good contact. The test points should be close together (preferably on 2.54mm grid).

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