3 2 REVISION RECORD LTR ECO NO: APPROVED: \*\*\* Top \*\*\* Revision History Table Of Content Revision Changes Page Content Aug 30, 2011 V1.0.0 Preliminary release. V2.0.0 Nov 28, 2011 Changed LAN jack. P. 1 Тор May 2, 2013 Changed RF front end circuit. Added U2, U6. V3.1.0 D D P. 2 CPU\_1 Added C20 (5.6pF), L3 (39nH). Changed value of R206, C501, R33~R37, R207, C1. P. 3 CPU\_2, RF V4.0.0 Jun 7, 2013 Added capacitor C55~58, ferrite bead L4. P. 4 CPU\_3, DDR I/F Jun 11, 2013 V4.1.0 No change of schematic. V4.1.1 Jul 4, 2013 Changed R3, R8 to 196R for FCC. P. 5 CPU\_4 P. 6 CPU\_5, USB I/F P. 7 CPU\_6, LAN I/F P. 8 CPU\_7 P. 9 CPU\_8, DC/DC P. 10 CPU\_9 (Blank Page) P. 11 MEMORY\_1, SPI Flash P. 12 MEMORY\_2, DDR P. 13 MEMORY\_3, Boot Option P. 14 WLAN\_1 (Blank Page) С P. 15 WLAN\_2 (Blank Page) P. 16 WLAN\_3 P. 17 ETHERNET\_1 P. 18 ETHERNET\_2 (Blank Pgae) P. 19 LED P. 20 POWER P. 21 Connector В PCB requirements Unless otherwise specified: Dimension: 50\*51.5mm Resistors are SMD(0402), +/-5%, 1/16W Resistors specified as SMD(0603) are +/-5%, 1/10W Thickness: 1.6mm Resistors specified as SMD(0805) are +/-5%, 1/8W Number of layers: 6 Copper thickness: 1oz top & bottom; 0.5~1oz all internal layers. Ceramic capacitors >= 10uF are SMD(0805) Ceramic capacitors >= 0.22uF, <10uF, are SMD(0603) Surface treatment: immersion gold plated. Ceramic capacitors <= 0.1uF are SMD(0402) Minimum wire width: 3.5mil (Layer\_2, Layer\_5), 5mil other layers Ceramic and Electrolytic capacitors are 6.3V or higher Minimum wire spacing: 5mil Ferrite beads are SMD(0603). Minimum via hole diameter: 8mil PCB stack-up for fabrication Layer Name Assignment Components, CPU, DDR GND1 Ground SIG1 Signal SUGA ELECTRONICS LTD. SIG2 Signal GND2 Ground RT3352 Wifi Module Components Bottom DATED: Jul 4, 2013 (Model SWP23MA-2) QQ Pei DATED: Jul 4, 2013 CODE: SIZE: TONY TSANG QUALITY CONTROL: DATED: <CONFIDENTIAL> A2 V4.1.1 RELEASED: DATED: SCALE: SHEET: 1 OF 21

SHEET: 13bF 21

SCALE: