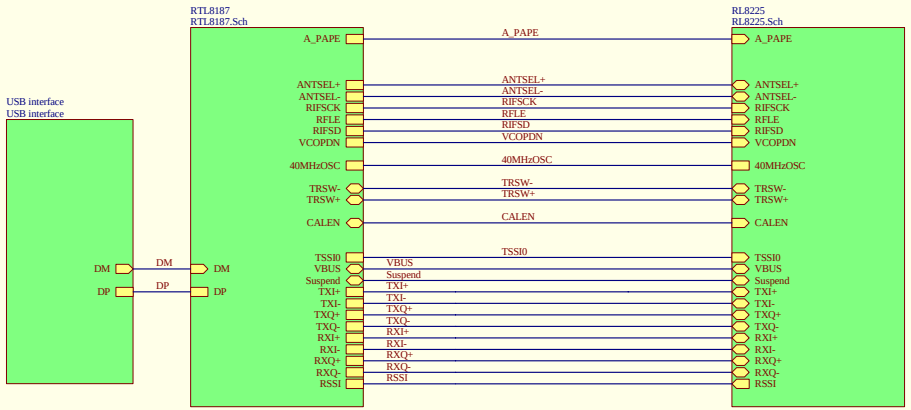
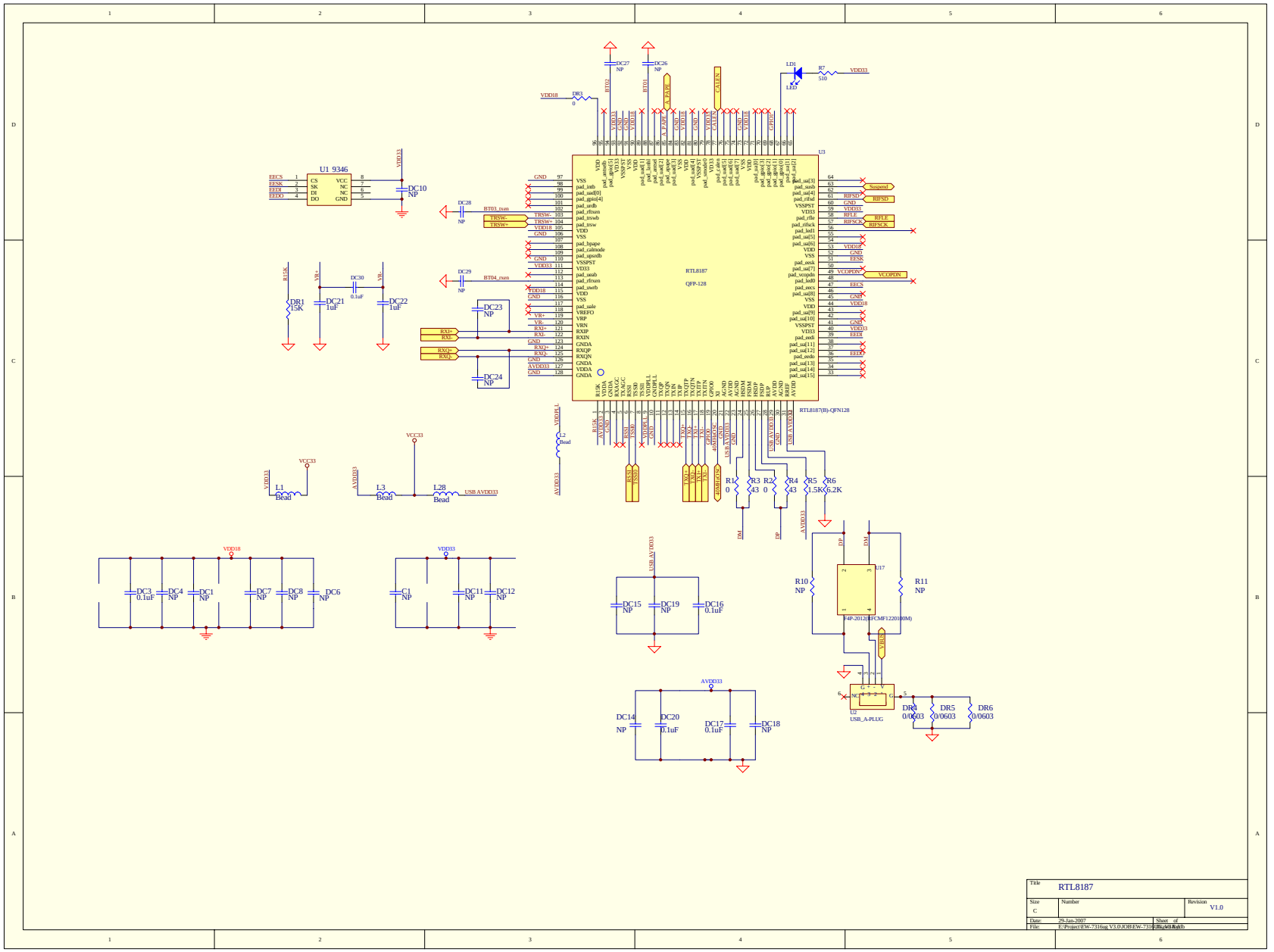
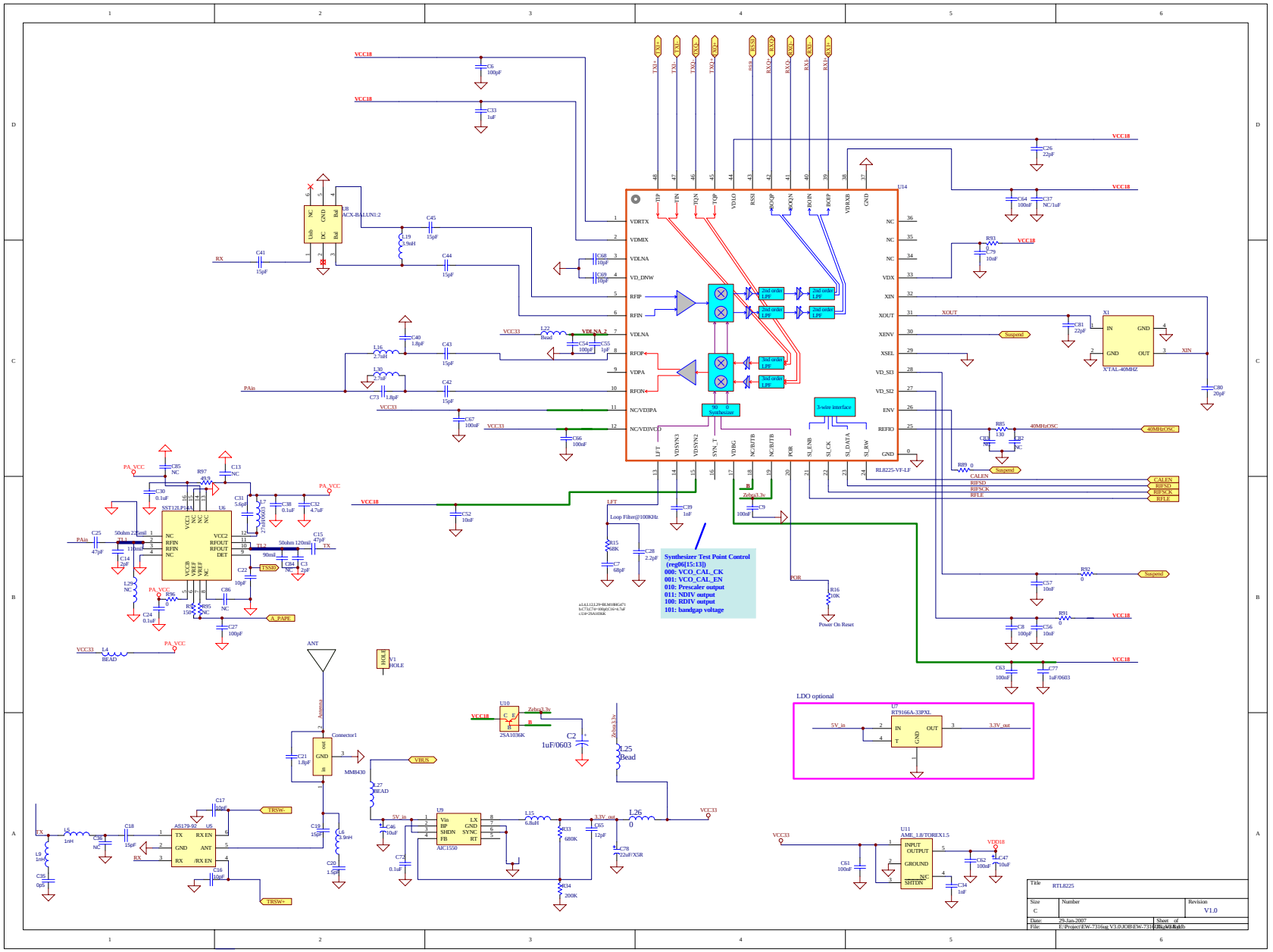
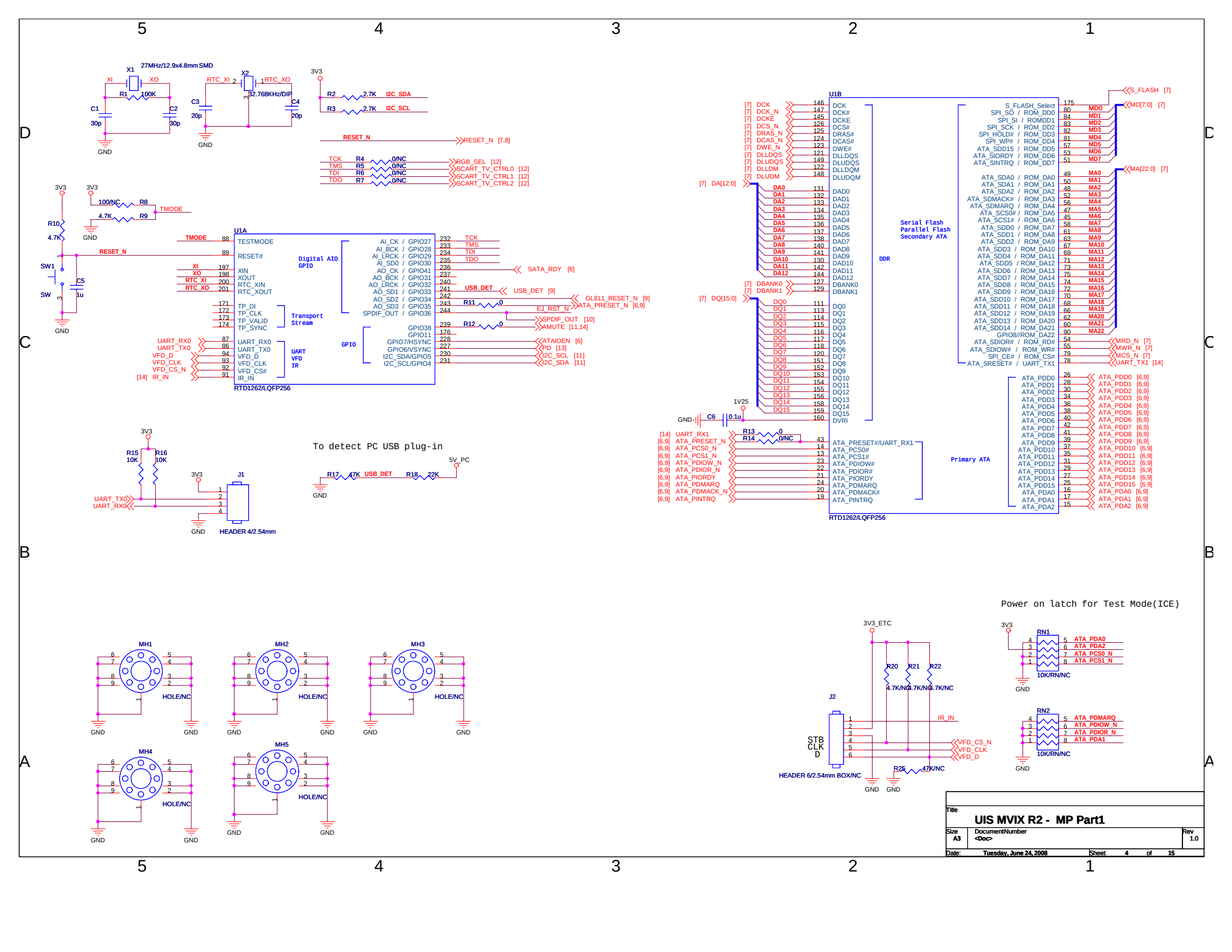
V1.0	add DC26,DC27,DC28,DC29,DC30,C20	ed 2006/05/15
V1.0	add DR3,DR4,DR5,DR6	ed 2006/05/15
V1.0	delete DR2,DC2,DC13,C53,C49,1.8V reg 2V5	ed 2006/05/15
V1.0	update C2,C47,C76,C77	ed 2006/05/15
V3.1	Replace PA by SST 1214A, remove BPF	ed 2006/07/27
V3.2	Co-lay LDO	ed 2006/09/06
V3.2	PCB 0ohm through:L1,L3,L28,R91,R92,R93	

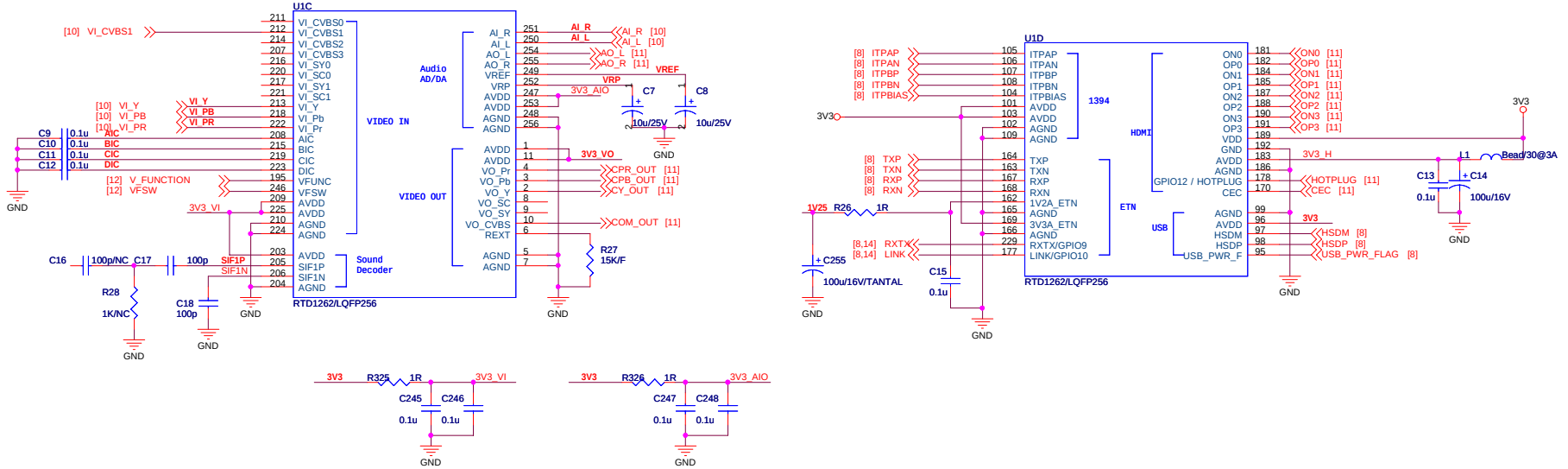


Title			
Size: B	Number:	Revision: V1.0	
Date: 29-Jan-2007	Sheet of		
File: E:\Project\EW-7316ug V3.0\JOB\EW-7316UG V3.0.ddb	Drawn By:		


U1 9346
U3
RTL8187
QFP-128
RTL8187(B)-QFN128
U17
F4P-2012(LFCMF1220100M)
U2
USB_A-PLUG
DC27 NP
DC26 NP
LD1
LED
R7 510
VDD33
VDD18
DR3 0
DC10 NP
DC28 NP
DC29 NP
DC30 0.1uF
DR1 15K
DC21 1uF
DC22 1uF
DC23 NP
DC24 NP
L1 Bead
L3 Bead
L28 Bead
VCC33
USB AVDD33
AVDD33
DC3 0.1uF
DC4 NP
DC1 NP
DC7 NP
DC8 NP
DC6 NP
C1 NP
DC11 NP
DC12 NP
DC15 NP
DC19 NP
DC16 0.1uF
DC14 NP
DC20 0.1uF
DC17 0.1uF
DC18 NP
R1 0
R3 43
R2 0
R4 43
R5 1.5K
R6 6.2K
R10 NP
R11 NP
DR4 0/0603
DR5 0/0603
DR6 0/0603
Suspend
RIFSD
RIFLE
RIFSCK
VCOPDN
VDD18
VDD33
Title
RTL8187
Size
C
Number
Revision
V1.0
Date:
29-Jan-2007
File:
E:\Project\EW-7316ug V3.0\JOB\EW-7316ug V3.0.ddb


Synthesizer Test Point Control (reg06[15:13])
000: VCO_CAL_CK
001: VCO_CAL_EN
010: Prescaler output
011: NDIV output
100: RDIV output
101: bandgap voltage
LDO optional
Title RTL8225
Size C
Number
Revision V1.0
Date: 29-Jun-2007
File: E:\Project\EW-7316ug V3.0\JOB\EW-7316ug V3.0.ddb


27MHz/12.9x4.8mm SMD
X1
XI
XO
R1 100K
C1 30p
C2 30p
GND
X2
RTC_XI
RTC_XO
32.768KHz/DIP
C3 20p
C4 20p
3V3
R2 2.7K I2C_SDA
R3 2.7K I2C_SCL
RESET_N
RESET_N [7,8]
TCK R4 0/NC RGB_SEL [12]
TMS R5 0/NC SCART_TV_CTRL0 [12]
TDI R6 0/NC SCART_TV_CTRL1 [12]
TDO R7 0/NC SCART_TV_CTRL2 [12]
100/NC R8
4.7K R9
TMODE
R10 4.7K
SW1
SW
C5 1u
U1A
TESTMODE
RESET#
XIN
XOUT
RTC_XIN
RTC_XOUT
TP_DI
TP_CLK
TP_VALID
TP_SYNC
UART_RX0
UART_TX0
VFD_D
VFD_CLK
VFD_CS#
IR_IN
Digital AIO GPIO
Transport Stream
UART VFD IR
GPIO
AI_CK / GPIO27
AI_BCK / GPIO28
AI_LRCK / GPIO29
AI_SD0 / GPIO30
AO_CK / GPIO41
AO_BCK / GPIO31
AO_LRCK / GPIO32
AO_SD1 / GPIO33
AO_SD2 / GPIO34
AO_SD3 / GPIO35
SPDIF_OUT / GPIO36
GPIO38
GPIO11
GPIO7/HSYNC
GPIO6/VSYNC
I2C_SDA/GPIO5
I2C_SCL/GPIO4
SATA_RDY [6]
USB_DET
USB_DET [9]
GL811_RESET_N [9]
ATA_PRESET_N [6,9]
EJ_RST_N
SPDIF_OUT [10]
AMUTE [11,14]
ATAIOEN [6]
PD [13]
I2C_SCL [11]
I2C_SDA [11]
RTD1262/LQFP256
R11 0
R12 0
R15 10K
R16 10K
J1
HEADER 4/2.54mm
To detect PC USB plug-in
5V_PC
R17 47K USB_DET R18 22K
U1B
DCK
DCK#
DCKE
DCS#
DRAS#
DCAS#
DWE#
DLLDQS
DLLDQS
DLLDM
DLLDQM
DA[12:0]
DBANK0
DBANK1
DQ[15:0]
DDR
Serial Flash
Parallel Flash
Secondary ATA
S_FLASH_Select
SPI_SO / ROM_DD0
SPI_SI / ROMDD1
SPI_SCK / ROM_DD2
SPI_HOLD# / ROM_DD3
SPI_WP# / ROM_DD4
ATA_SDD15 / ROM_DD5
ATA_SIORDY / ROM_DD6
ATA_SINTRQ / ROM_DD7
ATA_SDA0 / ROM_DA0
ATA_SDA1 / ROM_DA1
ATA_SDA2 / ROM_DA2
ATA_SDMACK# / ROM_DA3
ATA_SDMARQ / ROM_DA4
ATA_SCS0# / ROM_DA5
ATA_SCS1# / ROM_DA6
ATA_SDD0 / ROM_DA7
ATA_SDD1 / ROM_DA8
ATA_SDD2 / ROM_DA9
ATA_SDD3 / ROM_DA10
ATA_SDD4 / ROM_DA11
ATA_SDD5 / ROM_DA12
ATA_SDD6 / ROM_DA13
ATA_SDD7 / ROM_DA14
ATA_SDD8 / ROM_DA15
ATA_SDD9 / ROM_DA16
ATA_SDD10 / ROM_DA17
ATA_SDD11 / ROM_DA18
ATA_SDD12 / ROM_DA19
ATA_SDD13 / ROM_DA20
ATA_SDD14 / ROM_DA21
GPIO8//ROM_DA22
ATA_SDIOR# / ROM_RD#
ATA_SDIOW# / ROM_WR#
SPI_CE# / ROM_CS#
ATA_SRESET# / UART_TX1
S_FLASH [7]
MD[7:0] [7]
MA[22:0] [7]
MRD_N [7]
MWR_N [7]
MCS_N [7]
UART_TX1 [14]
ATA_PDD0 [6,9]
ATA_PDD1 [6,9]
ATA_PDD2 [6,9]
ATA_PDD3 [6,9]
ATA_PDD4 [6,9]
ATA_PDD5 [6,9]
ATA_PDD6 [6,9]
ATA_PDD7 [6,9]
ATA_PDD8 [6,9]
ATA_PDD9 [6,9]
ATA_PDD10 [6,9]
ATA_PDD11 [6,9]
ATA_PDD12 [6,9]
ATA_PDD13 [6,9]
ATA_PDD14 [6,9]
ATA_PDD15 [6,9]
ATA_PDA0 [6,9]
ATA_PDA1 [6,9]
ATA_PDA2 [6,9]
Primary ATA
ATA_PRESET#/UART_RX1
ATA_PCS0#
ATA_PCS1#
ATA_PDIOW#
ATA_PDIOR#
ATA_PIORDY
ATA_PDMARQ
ATA_PDMACK#
ATA_PINTRQ
UART_RX1 [14]
ATA_PRESET_N [6,9]
ATA_PCS0_N [6,9]
ATA_PCS1_N [6,9]
ATA_PDIOW_N [6,9]
ATA_PDIOR_N [6,9]
ATA_PIORDY [6,9]
ATA_PDMARQ [6,9]
ATA_PDMACK_N [6,9]
ATA_PINTRQ [6,9]
1V25
C6 0.1u
R13 0
R14 0/NC
RTD1262/LQFP256
Power on latch for Test Mode(ICE)
3V3_ETC
R20 4.7K/NC
R21 4.7K/NC
R22 4.7K/NC
J2
STB
CLK
D
IR_IN
VFD_CS_N
VFD_CLK
VFD_D
R25 47K/NC
HEADER 6/2.54mm BOX/NC
RN1
10K/RN/NC
RN2
10K/RN/NC
ATA_PDA0
ATA_PDA2
ATA_PCS0_N
ATA_PCS1_N
ATA_PDMARQ
ATA_PDIOW_N
ATA_PDIOR_N
ATA_PDA1
MH1
MH2
MH3
MH4
MH5
HOLE/NC
Title
UIS MVIX R2 - MP Part1
Size A3
DocumentNumber <Doc>
Rev 1.0
Date: Tuesday, June 24, 2008
Sheet 4 of 15



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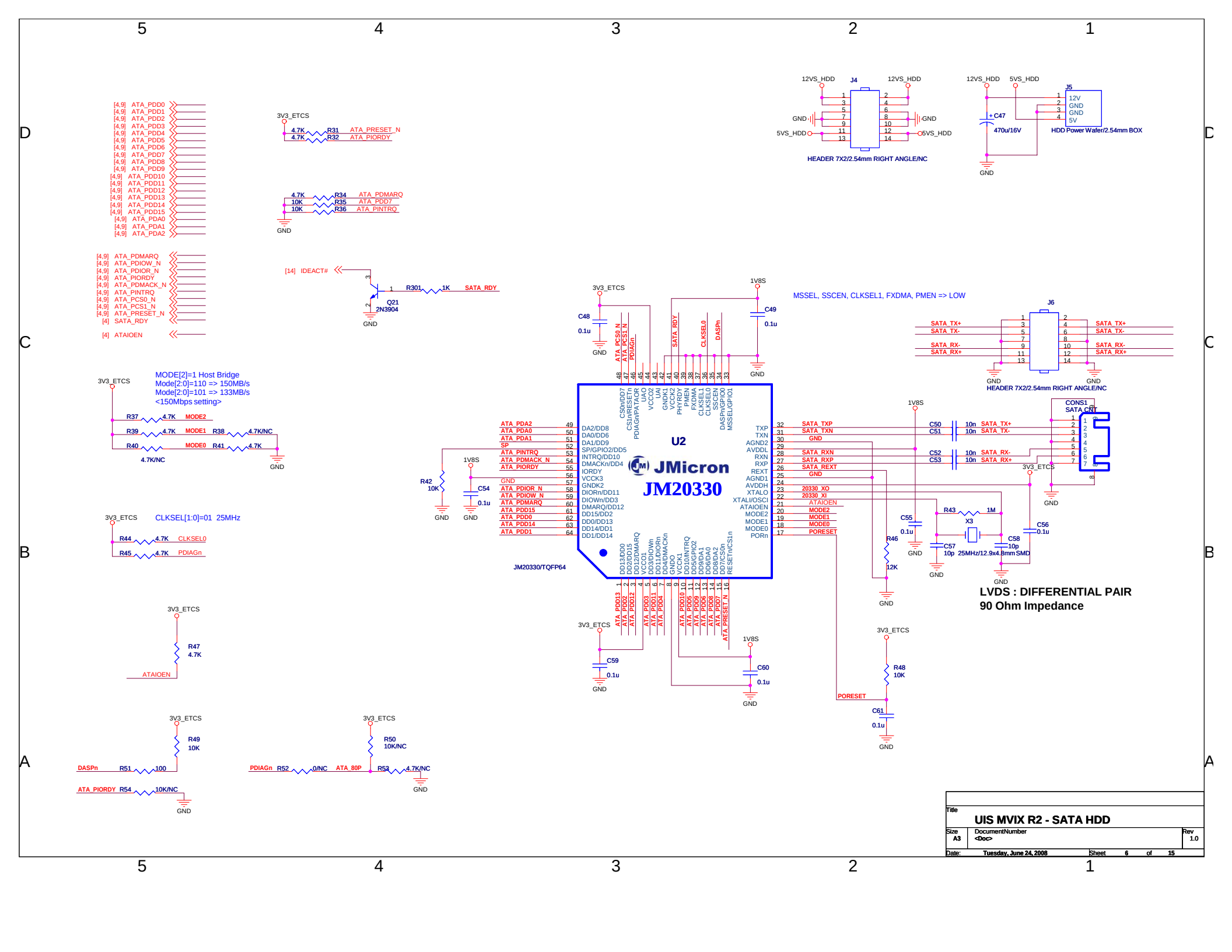
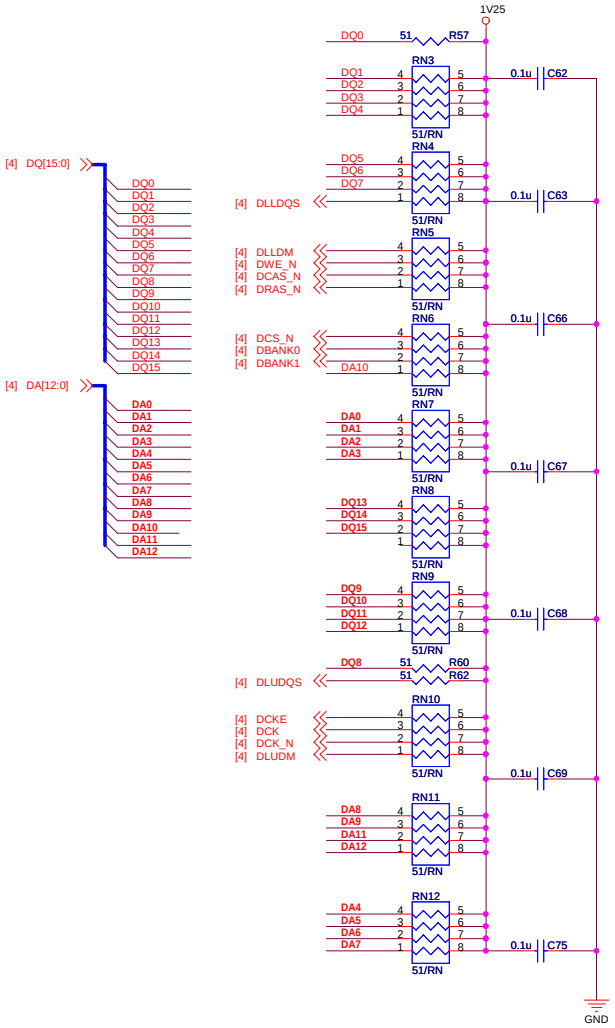
Size A3	DocumentNumber <Doc>		Rev 1.0
Date: Thursday, November 13, 2008	Sheet 5 of 15		


[4,9] ATA_PDD0
[4,9] ATA_PDD1
[4,9] ATA_PDD2
[4,9] ATA_PDD3
[4,9] ATA_PDD4
[4,9] ATA_PDD5
[4,9] ATA_PDD6
[4,9] ATA_PDD7
[4,9] ATA_PDD8
[4,9] ATA_PDD9
[4,9] ATA_PDD10
[4,9] ATA_PDD11
[4,9] ATA_PDD12
[4,9] ATA_PDD13
[4,9] ATA_PDD14
[4,9] ATA_PDD15
[4,9] ATA_PDA0
[4,9] ATA_PDA1
[4,9] ATA_PDA2
[4,9] ATA_PDMARQ
[4,9] ATA_PDIOW_N
[4,9] ATA_PDIOR_N
[4,9] ATA_PIORDY
[4,9] ATA_PDMACK_N
[4,9] ATA_PINTRQ
[4,9] ATA_PCS0_N
[4,9] ATA_PCS1_N
[4,9] ATA_PRESET_N
[4] SATA_RDY
[4] ATAIOEN
[14] IDEACT#
3V3_ETCS
4.7K R31 ATA_PRESET_N
4.7K R32 ATA_PIORDY
4.7K R34 ATA_PDMARQ
10K R35 ATA_PDD7
10K R36 ATA_PINTRQ
GND
Q21 2N3904
R301 1K SATA_RDY
12VS_HDD
5VS_HDD
J4
HEADER 7X2/2.54mm RIGHT ANGLE/NC
C47 470u/16V
J5
12V
GND
GND
5V
HDD Power Wafer/2.54mm BOX
MSSEL, SSCEN, CLKSEL1, FXDMA, PMEN => LOW
J6
SATA_TX+
SATA_TX-
SATA_RX-
SATA_RX+
HEADER 7X2/2.54mm RIGHT ANGLE/NC
MODE[2]=1 Host Bridge
Mode[2:0]=110 => 150MB/s
Mode[2:0]=101 => 133MB/s
<150Mbps setting>
R37 4.7K MODE2
R39 4.7K MODE1
R38 4.7K/NC
R40 MODE0
R41 4.7K
4.7K/NC
CLKSEL[1:0]=01 25MHz
R44 4.7K CLKSEL0
R45 4.7K PDIAGn
R47 4.7K ATAIOEN
R49 10K
DASPn R51 100
ATA_PIORDY R54 10K/NC
R50 10K/NC
PDIAGn R52 0/NC ATA_80P R53 4.7K/NC
U2
JMicron
JM20330
JM20330/TQFP64
C48 0.1u
C49 0.1u
C54 0.1u
R42 10K
C59 0.1u
C60 0.1u
C61 0.1u
R46 12K
R48 10K
C50 10n SATA_TX+
C51 10n SATA_TX-
C52 10n SATA_RX-
C53 10n SATA_RX+
CONS1
SATA CNT
C55 0.1u
C56 0.1u
C57 10p
R43 1M
X3
C58 10p
25MHz/12.9x4.8mm SMD
LVDS : DIFFERENTIAL PAIR
90 Ohm Impedance
PORESET
SATA_TXP
SATA_TXN
SATA_RXP
SATA_RXN
SATA_REXT
20330_XO
20330_XI
MODE2
MODE1
MODE0
PORESET
Title
UIS MVIX R2 - SATA HDD
Size A3
DocumentNumber <Doc>
Rev 1.0
Date: Tuesday, June 24, 2008
Sheet 6 of 15

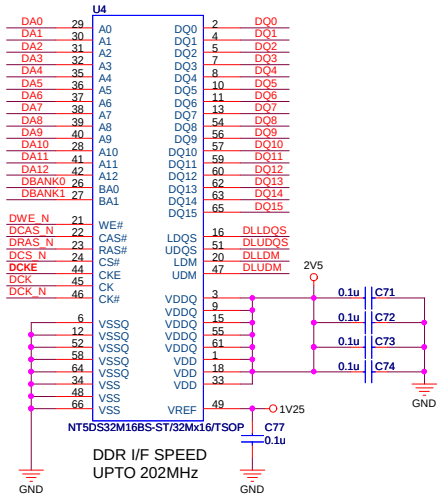
DDR termination resistors should be 100 ohm for 2-layer PCB
or 50 ohm for 4-layer PCB

DDR trace spacing : DQ0~DQ15,DLUDQS,DLLDQS,DLUDM,DLLDM = 7mil
The other DDR trace = 5mil

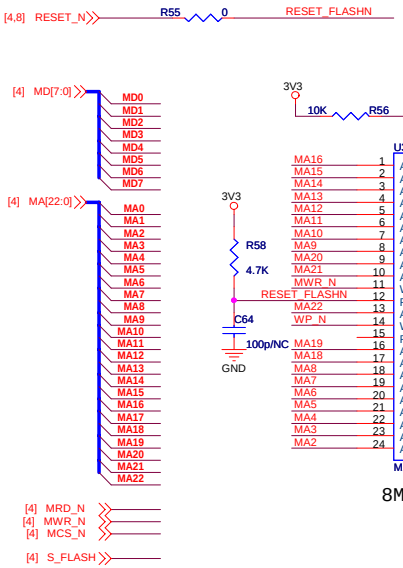


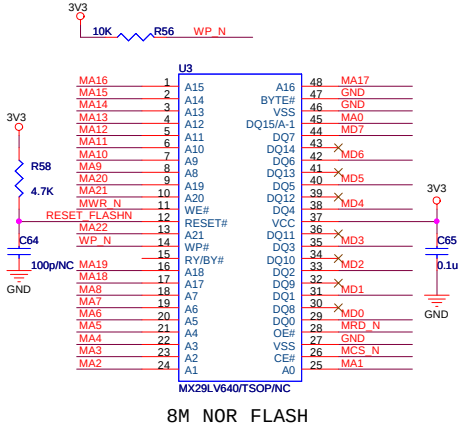
<64MB>
K4H511638-CC(OK)
HY5DU121622-D43
P2S12D40CTP-G5
NT5D32M16-5T(OK)

<32MB>
K4H51638-CC
HY5DU151622-D43
P2S56D40CTP-G5
MT5D16M16-5T



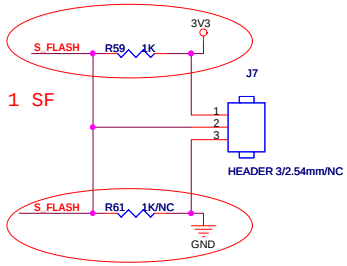
DDR I/F SPEED
UPTO 202MHz



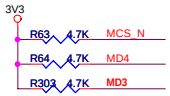


8M NOR FLASH

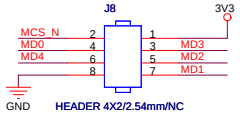
P_S Flash Option : 0 PF, 1 SF
P Flash :R61 Short
S Flash :R59 Short

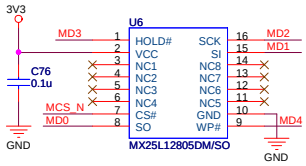


TYPICAL APP NOTE



080121 Part Delete
U5, C70, U6, C76





Title: UIS MVIX R2 - Memory
Size: A3
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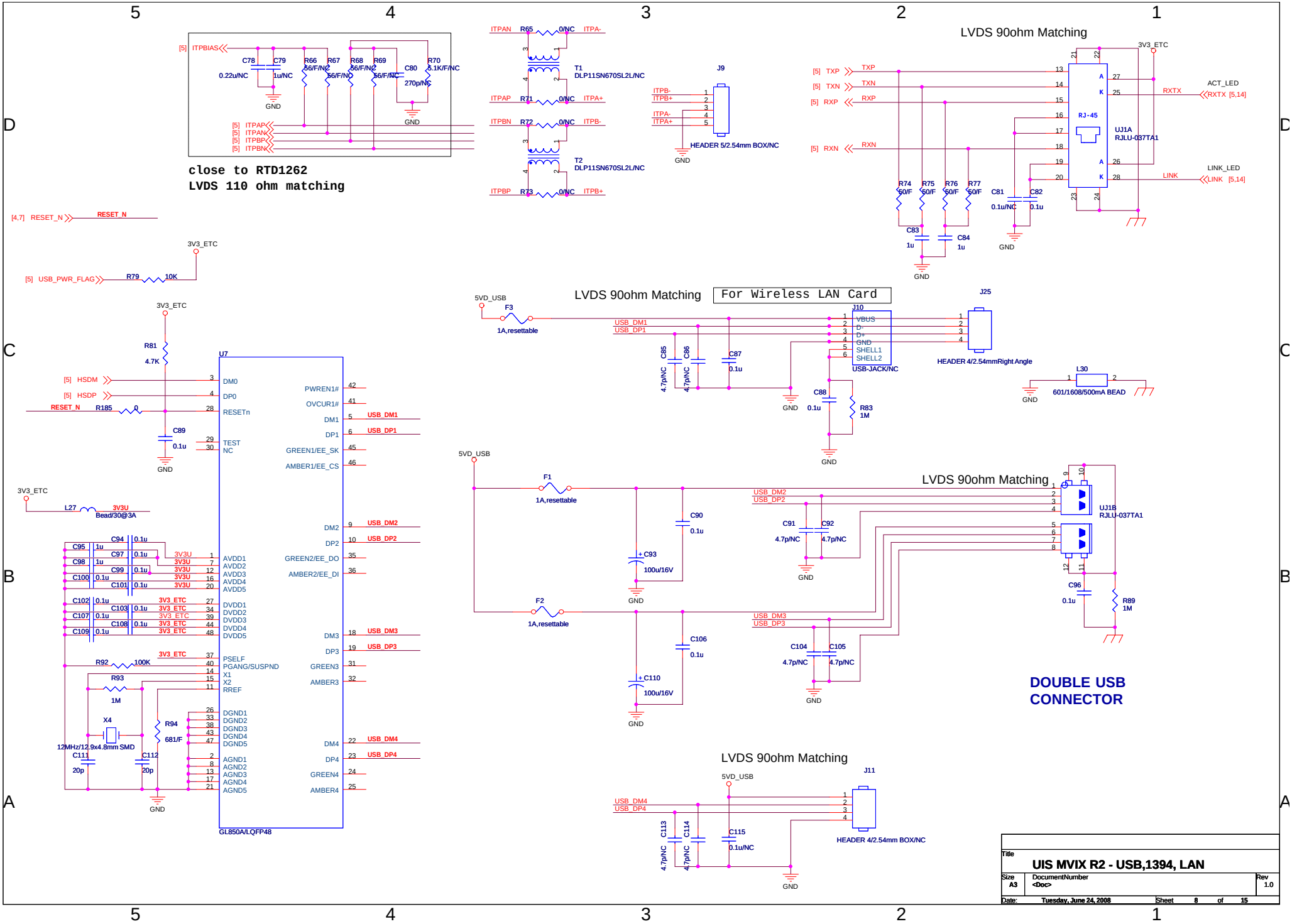
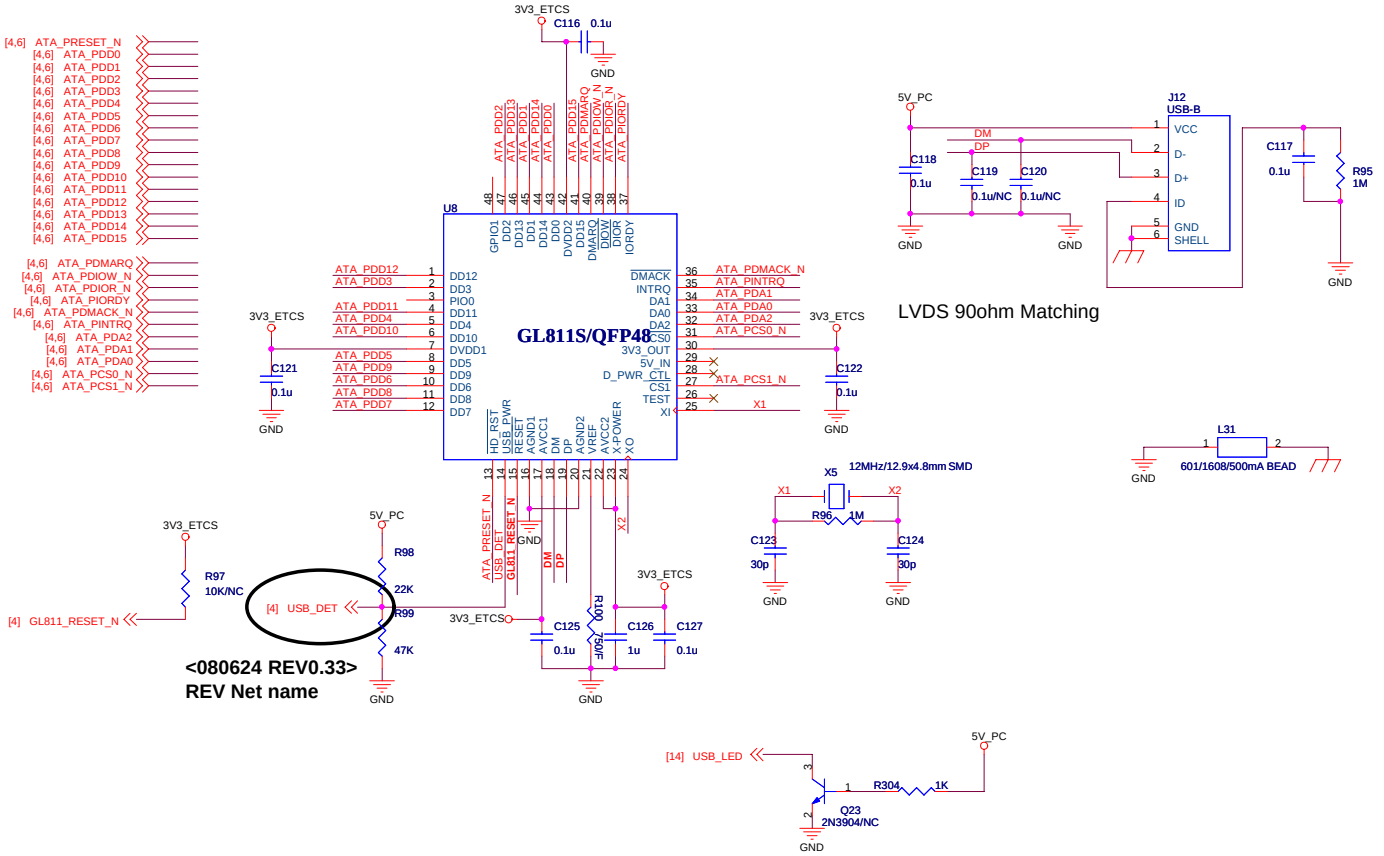
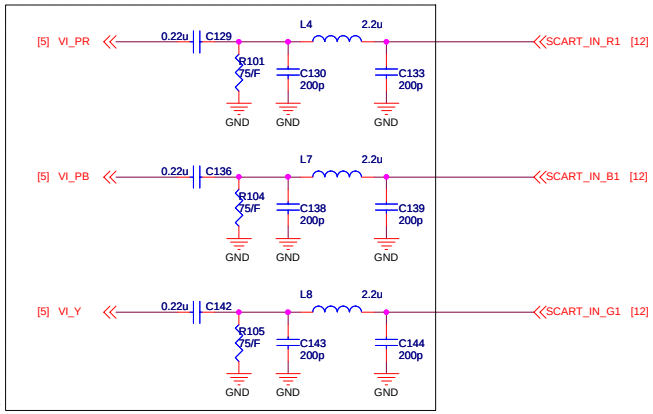

close to RTD1262
LVDS 110 ohm matching
LVDS 90ohm Matching
LVDS 90ohm Matching For Wireless LAN Card
LVDS 90ohm Matching
LVDS 90ohm Matching
DOUBLE USB CONNECTOR
GL850A/LQFP48
UIS MVIX R2 - USB,1394, LAN
Tuesday, June 24, 2008

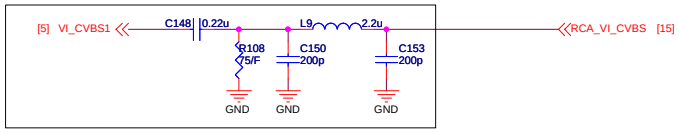


Title	UIS MVIX R2 - USB Device	
Size: A3	DocumentNumber: <Doc>	Rev: 1.0
Date: Tuesday, July 08, 2008	Sheet 9 of 15	

VIDEO IN

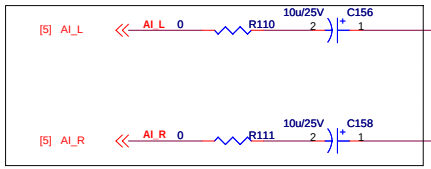


close to RTD1262

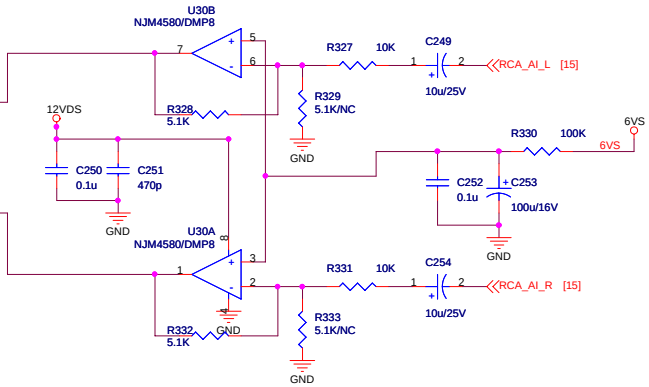


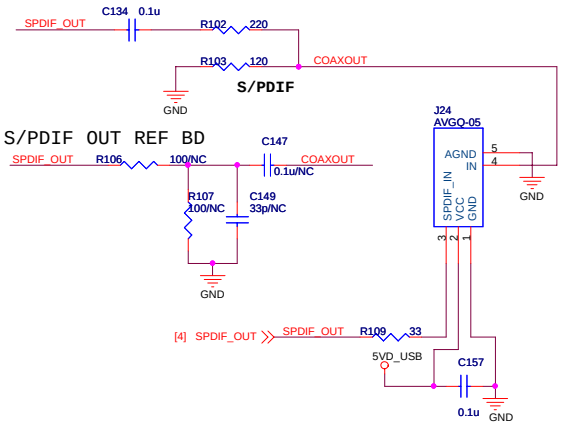
Close to RTD1262

A IN



Close to RTD1262

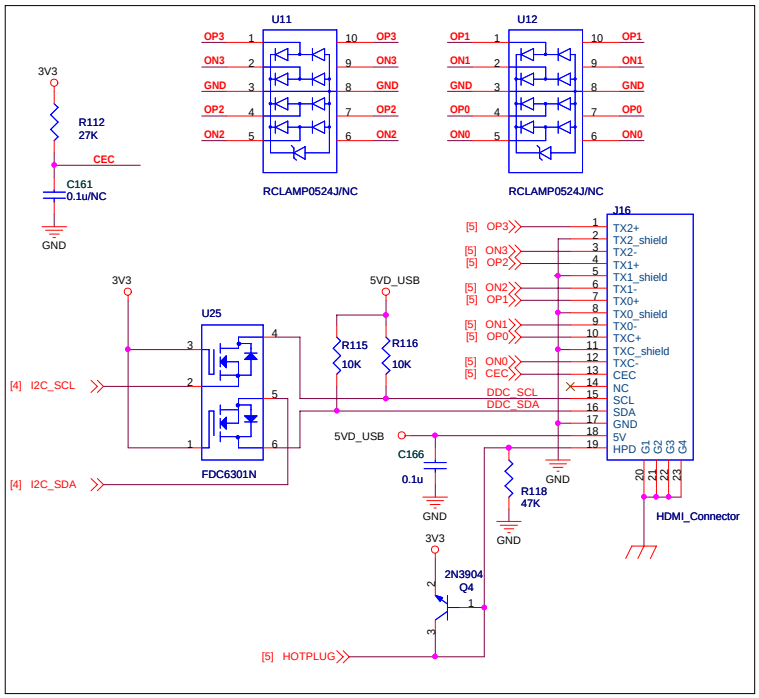


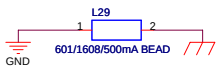


AI

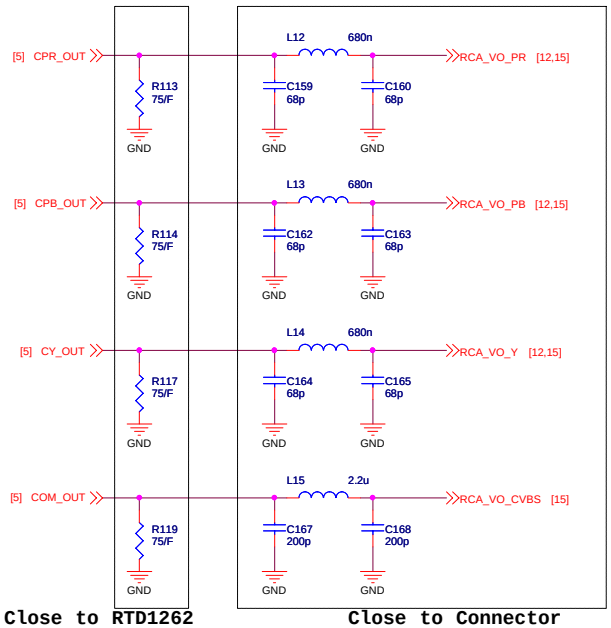
Title	UIS MVIX R2 - AV IN		
Size A3	DocumentNumber <Doc>		Rev 1.0
Date: Tuesday, June 24, 2008		Sheet 10 of 15	

HDMI OUT



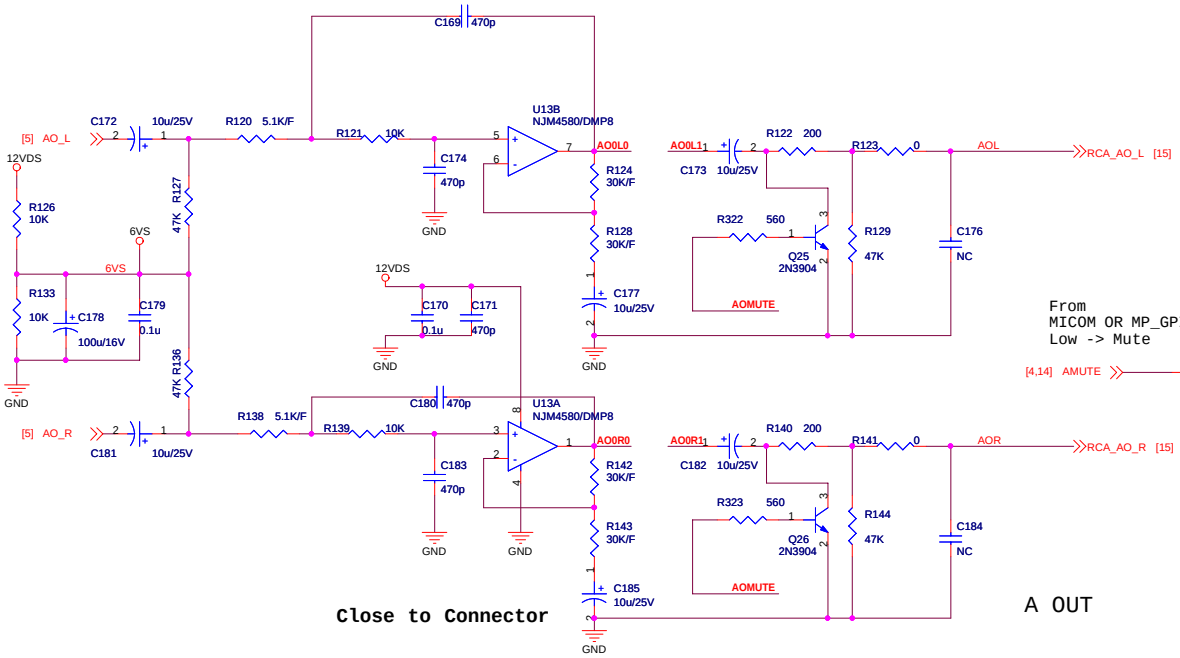


V OUT



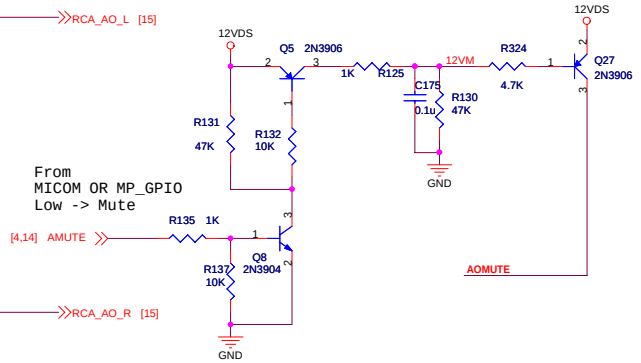
Close to RTD1262

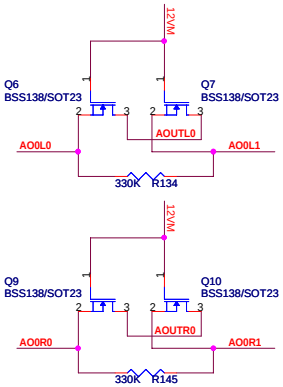
Close to Connector



Close to Connector

From
MICOM OR MP_GPIO
Low -> Mute





A OUT

Title: UIS MVIX R2 - AV OUT

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[4] RGB_SEL
[5] V_FUNCTION
[5] VFSW
[4] SCART_TV_CTRL0
[4] SCART_TV_CTRL1
[4] SCART_TV_CTRL2

For scart

[15] SW_VO_CVBS
[15] SW_AO_L
[15] SW_AO_R

SW_VO_CVBS
SW_AO_L
SW_AO_R

[15] SW_VI_CVBS
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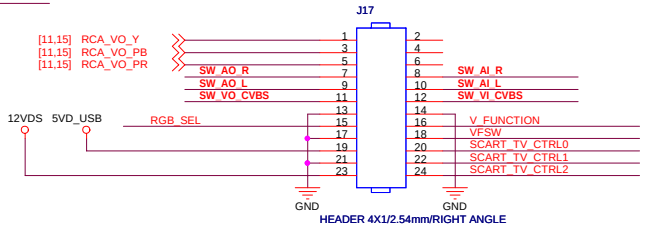
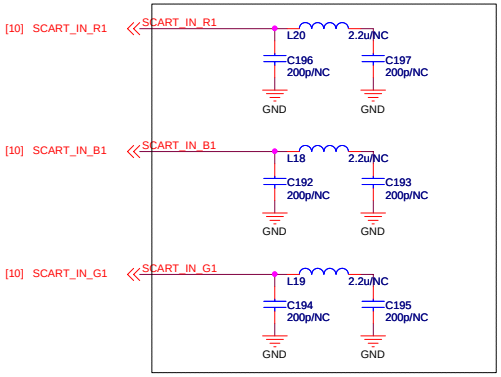
[15] SW_AI_R

SW_VI_CVBS
SW_AI_L
SW_AI_R





Close to CON

Title	UIS MVIX R2 - SCART CTRL	
Size: A3	DocumentNumber: <Doc>	Rev: 1.0
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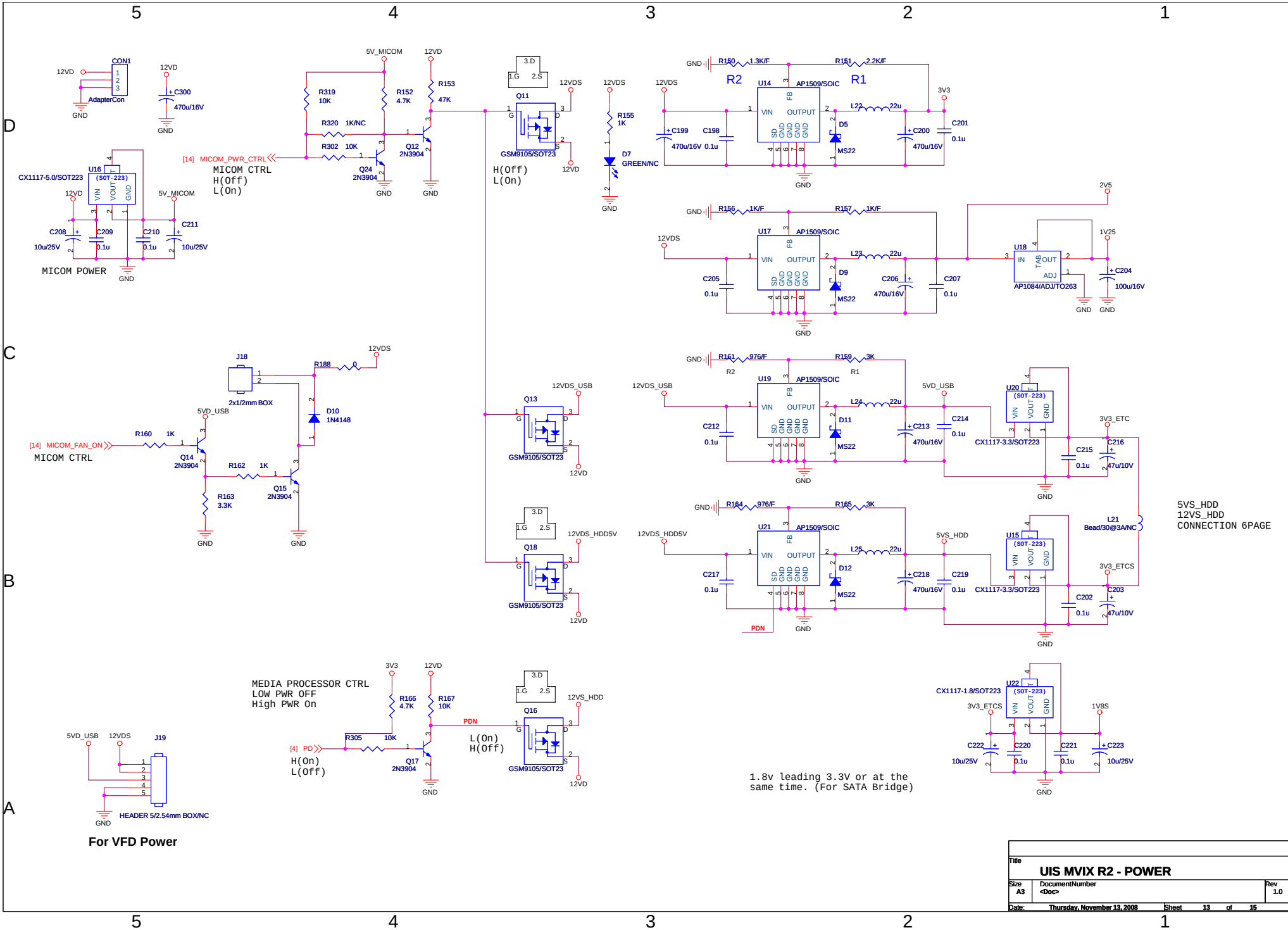

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Size	A3
DocumentNumber	<Doc>
Rev	1.0
Date:	Thursday, November 13, 2008
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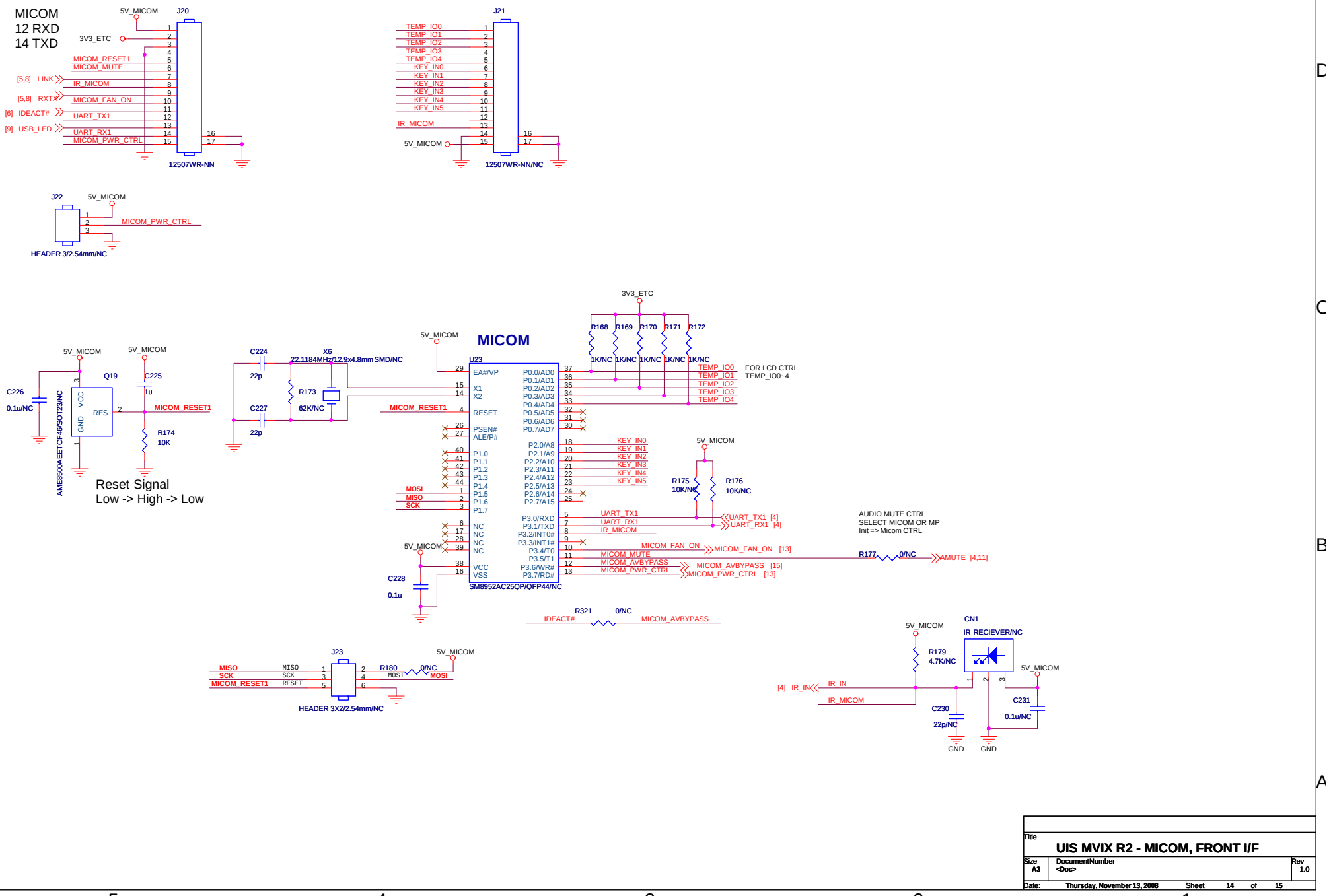

Title	UIS MVIX R2 - MICOM, FRONT I/F	
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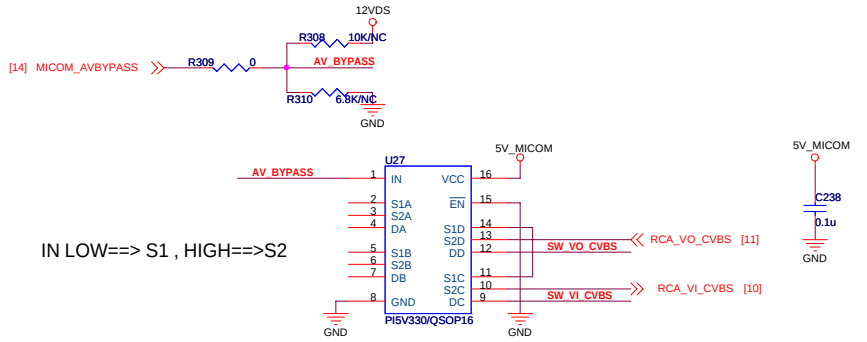

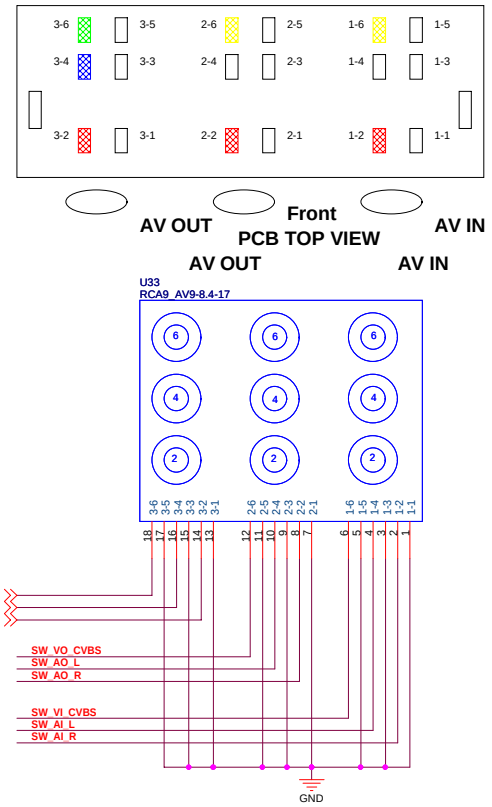

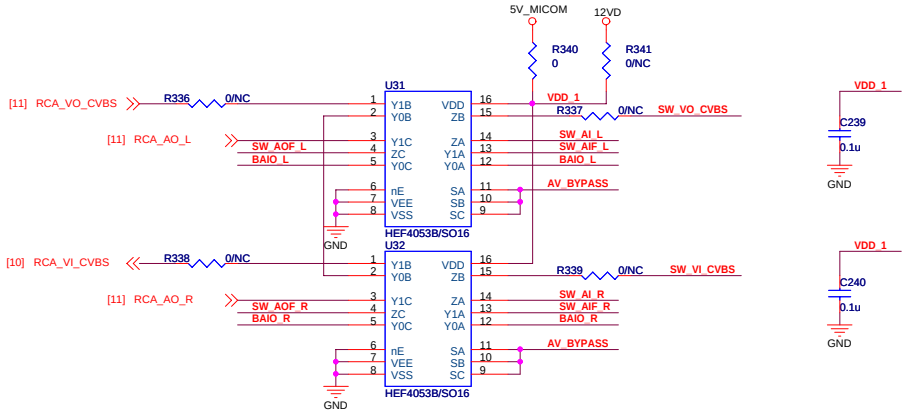

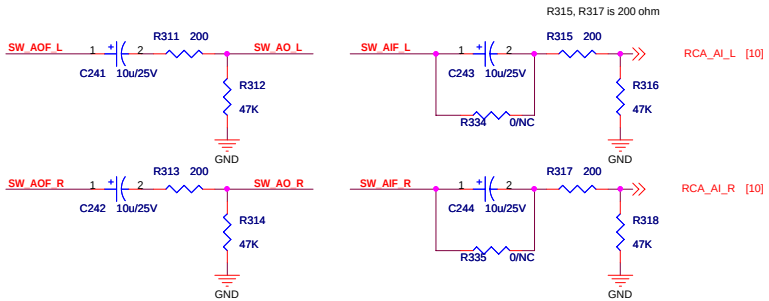

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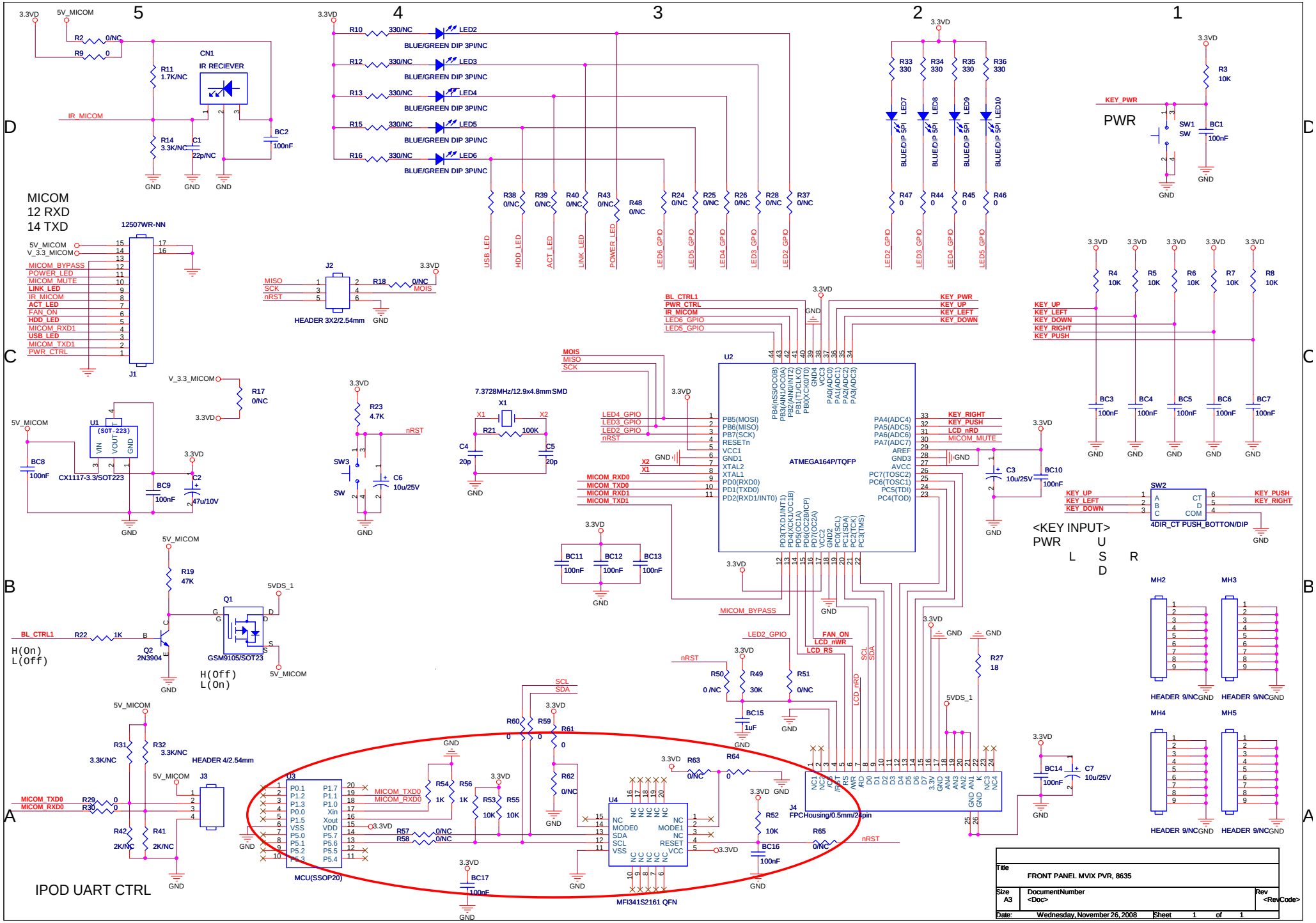
MICOM
12 RXD
14 TXD
IR RECIEVER
CN1
BLUE/GREEN DIP 3PI/NC
BLUE/DIP 5PI
PWR
12507WR-NN
HEADER 3X2/2.54mm
ATMEGA164P/TQFP
7.3728MHz/12.9x4.8mm SMD
CX1117-3.3/SOT223
GSM9105/SOT23
2N3904
4DIR_CT PUSH_BOTTON/DIP
HEADER 4/2.54mm
FPCHousing/0.5mm/24pin
HEADER 9/NC
MCU(SSOP20)
MFI341S2161 QFN
IPOD UART CTRL
H(On)
L(Off)
H(Off)
L(On)
<KEY INPUT>
PWR U
L S R
D
Title
FRONT PANEL MVIX PVR, 8635
Size A3
DocumentNumber <Doc>
Rev <RevCode>
Date: Wednesday, November 26, 2008
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