

## General Description

The CYBLE-2X20XX-X1 is a Bluetooth® Low Energy (BLE) wireless module solution. The CYBLE-2X20XX-X1 is a turnkey solution and includes onboard crystal oscillators, passive components, and the Cypress PRoC™ BLE. Refer to the CYBL1XX7X [datasheet](#) for additional details on the capabilities of the PRoC BLE device used on this module.

The CYBLE-2X20XX-X1 supports a number of peripheral functions (ADC, timers, counters, PWM) and serial communication protocols ( $I^2C$ , UART, SPI) through its programmable architecture. The CYBLE-2X20XX-X1 includes a royalty-free BLE stack compatible with Bluetooth 4.2 and provides up to 19 GPIOs in a  $15.0 \times 23.0 \times 2.0$  mm package.

The CYBLE-2X20XX-X1 is available in two fully certified and qualified versions (CYBLE-212006-01 and CYBLE-202007-01), and an uncertified version (CYBLE-202013-11). The CYBLE-212006-01 includes an integrated trace antenna. The CYBLE-202007-01 supports an external antenna via a u-FL connector, and the CYBLE-202013-11 supports an external antenna through a RF pin. The CYBLE-202013-11 does not include an RF shield and is not certified by Bluetooth SIG or regulatory agencies.

The CYBLE-2X20XX-X1 is a complete solution targeted at applications requiring extended communication range with an optimized cost structure.

## Module Description

- Module size:  $15.00 \text{ mm} \times 23.00 \text{ mm} \times 2.00 \text{ mm}$
- Bluetooth 4.2 single-mode module
- Certified to FCC, IC, MIC, KC, and CE regulations
- Castellated solder pad connections for ease-of-use
- 256-KB flash memory, 32-KB SRAM memory
- Up to 19 GPIOs configurable as open drain high/low, pull-up/pull-down, HI-Z analog, HI-Z digital, or strong output
- Industrial temperature range:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$
- 32-bit processor (0.9 DMIPS/MHz) with single-cycle 32-bit multiply, operating at up to 48 MHz
- Watchdog timer with dedicated internal low-speed oscillator
- Two-pin SWD for programming

## Power Consumption

- TX output power: +1 dbm or +7.5 dbm
- RX Receive Sensitivity:  $-93 \text{ dbm}$
- Received signal strength indicator (RSSI) with 1-dB resolution

## ■ TX current consumption

- BLE silicon: 15.6 mA (radio only, 0 dbm)
- RFX2401C: 27 mA (PA/LNA only, +7.5 dBm)

## ■ RX current consumption of 16.4 mA (radio only)

- BLE silicon: 16.4 mA (radio only, 0 dbm)
- RFX2401C: 7.5 mA (PA/LNA only)

## ■ Cypress CYBL1XX7X silicon low power mode support

- Deep Sleep: 1.3  $\mu\text{A}$  with watch crystal oscillator (WCO) on
- Hibernate: 150 nA with SRAM retention
- Stop: 60 nA with XRES wakeup

## Functional Capabilities

- Up to 18 capacitive sensors for buttons or sliders with best-in-class signal-to-noise ratio (SNR) and liquid tolerance
- 12-bit, 1-MspS SAR ADC with internal reference, sample-and-hold (S/H), and channel sequencer
- Two serial communication blocks (SCBs) supporting  $I^2C$  (master/slave), SPI (master/slave), or UART
- Four dedicated 16-bit timer, counter, or PWM blocks (TCPWMs)
- LCD drive supported on all GPIOs (common or segment)
- Programmable low voltage detect (LVD) from 1.8 V to 4.5 V
- $I^2S$  master interface
- Bluetooth Low Energy protocol stack supporting generic access profile (GAP) Central, Peripheral, Observer, or Broadcaster roles
- Switches between Central and Peripheral roles on-the-go
- Standard Bluetooth Low Energy profiles and services for interoperability
- Custom profile and service for specific use cases

## Benefits

The CYBLE-2X20XX-X1 module is provided as a turnkey solution, including all necessary hardware required to use BLE communication standards.

- Proven hardware design ready to use
- Cost optimized for applications without space constraint
- Reprogrammable architecture
- Fully certified module eliminates the time needed for design, development and certification
- Bluetooth SIG qualified with QDID and Declaration ID
- Flexible communication protocol support
- PSoC Creator™ provides an easy-to-use integrated design environment (IDE) to configure, develop, program, and test a BLE application

## More Information

Cypress provides a wealth of data at [www.cypress.com](http://www.cypress.com) to help you to select the right module for your design, and to help you to quickly and effectively integrate the module into your design.

- Overview: [EZ-BLE Module Portfolio](#), [Module Roadmap](#)
- [EZ-BLE PRoC Product Overview](#)
- [PRoC BLE Silicon Datasheet](#)
- Application notes: Cypress offers a number of BLE application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with EZ-BLE modules are:
  - [AN96841](#) - Getting Started with EZ-BLE Module
  - [AN94020](#) - Getting Started with PRoC BLE
  - [AN97060](#) - PSoC® 4 BLE and PRoC™ BLE - Over-The-Air (OTA) Device Firmware Upgrade (DFU) Guide
  - [AN91162](#) - Creating a BLE Custom Profile
  - [AN91184](#) - PSoC 4 BLE - Designing BLE Applications
  - [AN92584](#) - Designing for Low Power and Estimating Battery Life for BLE Applications
  - [AN85951](#) - PSoC® 4 CapSense® Design Guide
  - [AN95089](#) - PSoC® 4/PRoC™ BLE Crystal Oscillator Selection and Tuning Techniques

### PSoC® Creator™ Integrated Design Environment (IDE)

[PSoC Creator](#) is an Integrated Design Environment (IDE) that enables concurrent hardware and firmware editing, compiling and debugging of PSoC 3, PSoC 4, PSoC 5LP, PSoC 4 BLE, PRoC BLE and EZ-BLE module systems with no code size limitations. PSoC peripherals are designed using schematic capture and simple graphical user interface (GUI) with over 120 pre-verified, production-ready PSoC Components™.

PSoC Components are analog and digital “virtual chips,” represented by an icon that users can drag-and-drop into a design and configure to suit a broad array of application requirements.

### Bluetooth Low Energy Component

The [Bluetooth Low Energy Component](#) inside PSoC Creator provides a comprehensive GUI-based configuration window that lets you quickly design BLE applications. The Component incorporates a Bluetooth Core Specification v4.1 compliant BLE protocol stack and provides API functions to enable user applications to interface with the underlying Bluetooth Low Energy Sub-System (BLESS) hardware via the stack.

### Technical Support

- [Frequently Asked Questions \(FAQs\)](#): Learn more about our BLE ECO System.
- [Forum](#): See if your question is already answered by fellow developers on the PSoC 4 BLE and PRoC BLE forums.
- Visit our [support](#) page and create a [technical support case](#) or contact a [local sales representatives](#). If you are in the United States, you can talk to our technical support team by calling our toll-free number: +1-800-541-4736. Select option 2 at the prompt.

- [AN91445](#) - Antenna Design and RF Layout Guidelines
- Knowledge Base Articles
  - [KBA97095](#) - EZ-BLE™ Module Placement
- Technical Reference Manual (TRM):
  - [PRoC® BLE Technical Reference Manual](#)
- Development Kits:
  - CYBLE-212006-EVAL, CYBLE-212006-01 Evaluation Board
  - CYBLE-202007-EVAL, CYBLE-202007-01 Evaluation Board
  - CYBLE-202013-EVAL, CYBLE-202013-11 Evaluation Board
  - [CY8CKIT-042-BLE](#), Bluetooth® Low Energy (BLE) Pioneer Kit
  - [CY8CKIT-002](#), PSoC® MiniProg3 Program and Debug Kit
- Test and Debug Tools:
  - [CYSmart](#), Bluetooth® LE Test and Debug Tool (Windows)
  - [CYSmart Mobile](#), Bluetooth® LE Test and Debug Tool (Android/iOS Mobile App)



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## Overview

### Module Description

The CYBLE-2X20XX-X1 module is a complete module designed to be soldered to the applications main board.

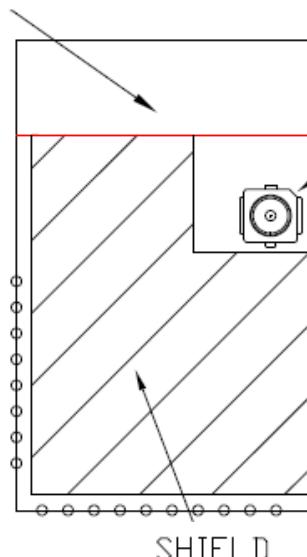
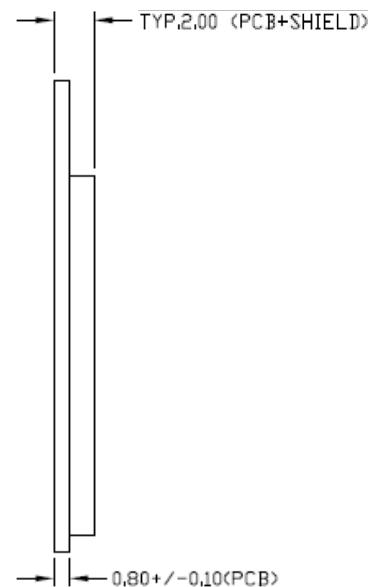
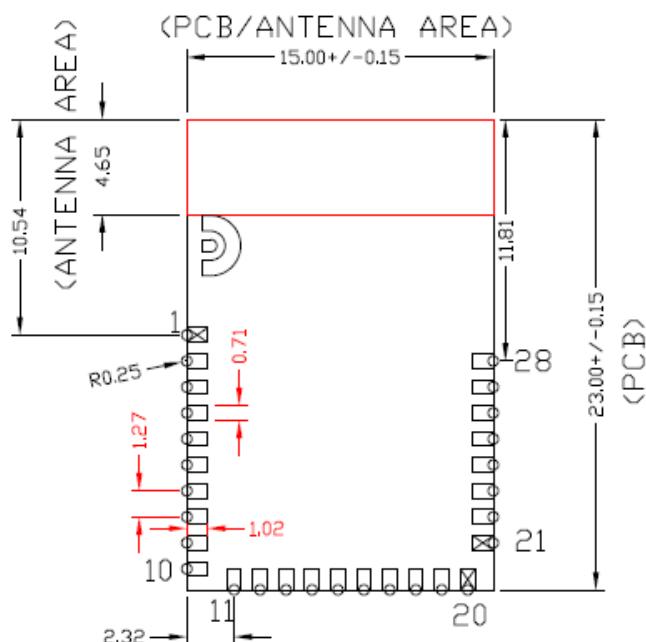
#### *Module Dimensions and Drawing*

Cypress reserves the right to select components (including the appropriate BLE device) from various vendors to achieve the BLE module functionality. Such selections will still guarantee that all height restrictions of the component area are maintained. Designs should be held within the physical dimensions shown in the mechanical drawings in [Figure 1](#). All dimensions are in millimeters (mm).

**Table 1. Module Design Dimensions**

Dimension Item	Specification
Module dimensions	Length (X) 15.00 ± 0.15 mm
	Width (Y) 23.00 ± 0.15 mm
Antenna location dimensions	Length (X) 15.00 ± 0.15 mm
	Width (Y) 4.65 ± 0.15 mm
PCB thickness	Height (H) 0.80 ± 0.10 mm
Shield height	Height (H) 1.20 ± 0.10 mm
Maximum component height	Height (H) 1.20 mm typical (shield) - CYBLE-212006-01 1.25 mm typical (connector) - CYBLE-202007-01 0.75mm typical (crystal) - CYBLE-202013-11
Total module thickness (bottom of module to highest component)	Height (H) 2.00 mm typical - CYBLE-212006-01 2.05 mm typical - CYBLE-202007-01 1.55 mm typical - CYBLE-202013-11

See [Figure 1 on page 5](#) for the mechanical reference drawing for CYBLE-2X20XX-X1.

**Figure 1. Module Mechanical Drawing**
**ANTENNA AREA**

**Top View (View from Top)**

**Side View**

**MODULE PAD  
ASSIGNMENT:**

PAD1:GND  
 PAD2:XRES  
 PAD3:P4,0  
 PAD4:P3,7  
 PAD5:P3,6  
 PAD6:P3,5  
 PAD7:P3,4  
 PAD8:VREF  
 PAD9:P2,6  
 PAD10:P2,4  
 PAD11:P2,3  
 PAD12:P2,2  
 PAD13:P2,0  
 PAD14:P1,7  
 PAD15:P1,6  
 PAD16:P1,5  
 PAD17:P1,4  
 PAD18:P0,7  
 PAD19:P1,0  
 PAD20:P0,4  
 PAD21:P0,5  
 PAD22:VDD  
 PAD23:P0,6  
 PAD24:GND  
 PAD25:GND  
 PAD26:GND  
 PAD27:GND  
 PAD28:VDDR

**Bottom View (Seen from Bottom)**
**Note**

- No metal should be located beneath or above the antenna area. Only bare PCB material should be located beneath the antenna area. For more information on recommended host PCB layout, see [Figure 3](#), [Figure 4](#), [Figure 5](#), and [Figure 6](#) and [Table 3](#).

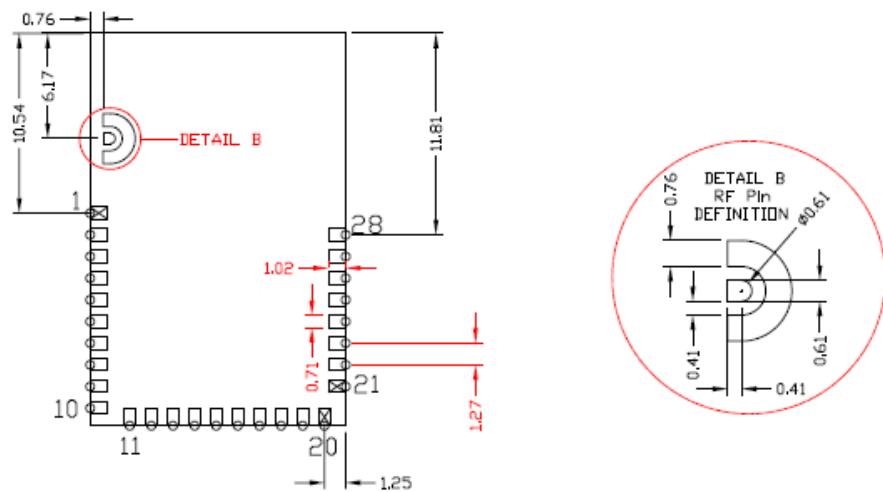
## Pad Connection Interface

As shown in the bottom view of [Figure 1 on page 5](#), the CYBLE-2X20XX-X1 connects to the host board via solder pads on the backside of the module. [Table 2](#) and [Figure 2](#) detail the solder pad length, width, and pitch dimensions of the CYBLE-2X20XX-X1 module.

**Table 2. Solder Pad Connection Description**

Name	Connections	Connection Type	Pad Length Dimension	Pad Width Dimension	Pad Pitch
SP	30	Solder Pads	1.02 mm	0.71 mm	1.27 mm

**Figure 2. Solder Pad Dimensions (Seen from Bottom)**

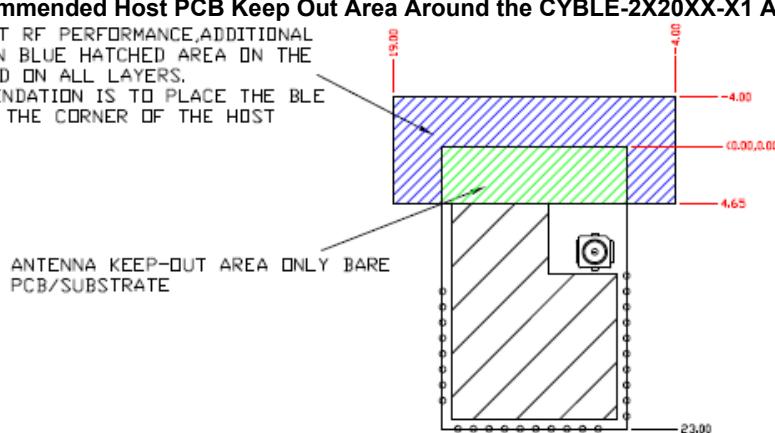


To maximize RF performance, the host layout should follow these recommendations:

1. The ideal placement of the Cypress BLE module is in a corner of the host board with the trace antenna located at the far corner. This placement minimizes the additional recommended keep out area stated in item 2. Please refer to [AN96841](#) for module placement best practices.
2. To maximize RF performance, the area immediately around the Cypress BLE module trace antenna should contain an additional keep out area, where no grounding or signal trace are contained. The keep out area applies to all layers of the host board. The recommended dimensions of the host PCB keep out area are shown in [Figure 3](#) (dimensions are in mm).

**Figure 3. Recommended Host PCB Keep Out Area Around the CYBLE-2X20XX-X1 Antenna**

1. FOR BEST RF PERFORMANCE, ADDITIONAL KEEPOUT IN BLUE HATCHED AREA ON THE HOST BOARD ON ALL LAYERS.
2. RECOMMENDATION IS TO PLACE THE BLE MODULE IN THE CORNER OF THE HOST BOARD,

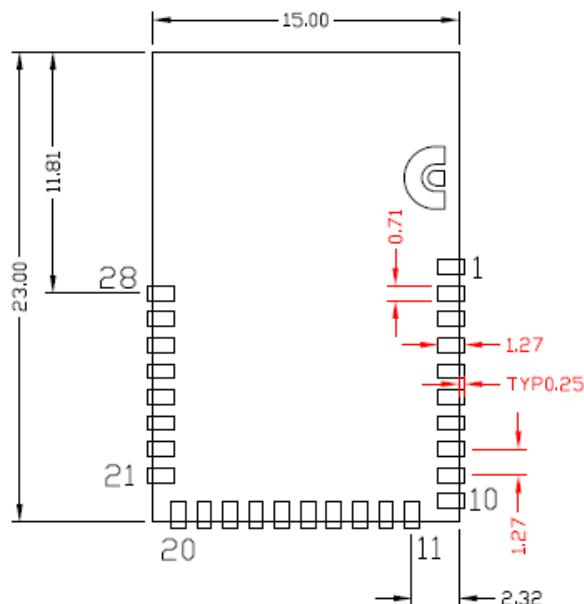


**Host PCB Keep Out Area Around Trace Antenna**

## Recommended Host PCB Layout

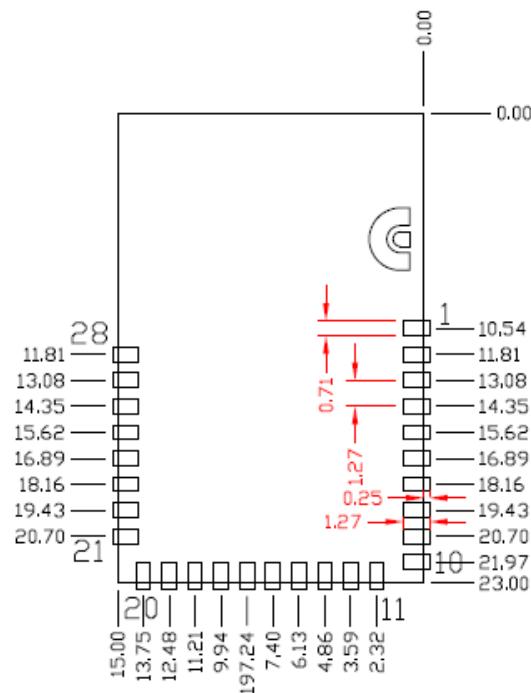
Figure 4, Figure 5, Figure 6, and Table 3 provide details that can be used for the recommended host PCB layout pattern for the CYBLE-212006-01. Dimensions are in millimeters unless otherwise noted. Pad length of 1.27 mm (0.635 mm from center of the pad on either side) shown in Figure 6 is the minimum recommended host pad length. The host PCB layout pattern can be completed using either Figure 4, Figure 5, or Figure 6. It is not necessary to use all figures to complete the host PCB layout pattern.

**Figure 4. Host Layout Pattern for CYBLE-2X20XX-X1**



**Top View (On Host PCB)**

**Figure 5. Module Pad Location from Origin**



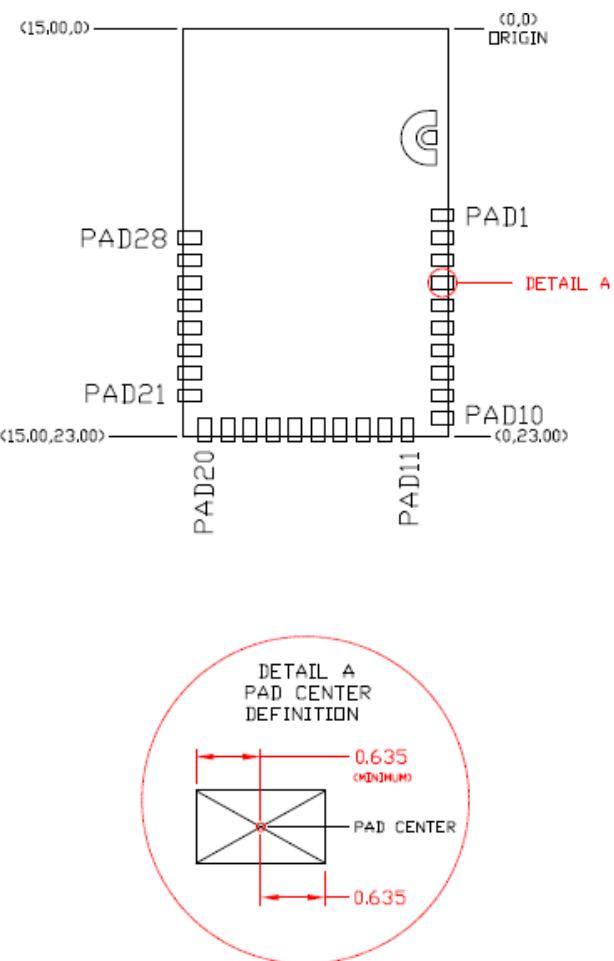
**Top View (On Host PCB)**

**Table 3** provides the center location for each solder pad on the CYBLE-2X20XX-X1. All dimensions reference the to the center of the solder pad. Refer to [Figure 6](#) for the location of each module solder pad.

**Table 3. Module Solder Pad Location**

Solder Pad (Center of Pad)	Location (X,Y) from Origin (mm)	Dimension from Origin (mils)
1	(0.38, 10.54)	(14.96, 414.96)
2	(0.38, 11.81)	(14.96, 464.96)
3	(0.38, 13.08)	(14.96, 514.96)
4	(0.38, 14.35)	(14.96, 564.96)
5	(0.38, 15.62)	(14.96, 614.96)
6	(0.38, 16.89)	(14.96, 664.96)
7	(0.38, 18.16)	(14.96, 714.96)
8	(0.38, 19.43)	(14.96, 764.96)
9	(0.38, 20.70)	(14.96, 814.96)
10	(0.38, 21.97)	(14.96, 864.96)
11	(2.32, 22.62)	(91.34, 890.55)
12	(3.59, 22.62)	(141.34, 890.55)
13	(4.86, 22.62)	(191.34, 890.55)
14	(6.13, 22.62)	(241.34, 890.55)
15	(7.40, 22.62)	(291.34, 890.55)
16	(8.67, 22.62)	(341.34, 890.55)
17	(9.94, 22.62)	(391.34, 890.55)
18	(11.21, 22.62)	(441.34, 890.55)
19	(12.48, 22.62)	(491.34, 890.55)
20	(13.75, 22.62)	(541.34, 890.55)
21	(14.62, 20.70)	(575.59, 814.96)
22	(14.62, 19.43)	(575.59, 764.96)
23	(14.62, 18.16)	(575.59, 714.96)
24	(14.62, 16.89)	(575.59, 664.96)
25	(14.62, 15.62)	(575.59, 614.96)
26	(14.62, 14.35)	(575.59, 564.96)
27	(14.62, 13.08)	(575.59, 514.96)
28	(14.62, 11.81)	(575.59, 464.96)
29	See <a href="#">Figure 2</a>	See <a href="#">Figure 2</a>
30	See <a href="#">Figure 2</a>	See <a href="#">Figure 2</a>

**Figure 6. Solder Pad Reference Location**





**Table 4** details the solder pad connection definitions and available functions for each connection pad. **Table 4** lists the solder pads on CYBLE-2X20XX-X1, the BLE device port-pin, and denotes whether the function shown is available for each solder pad. Each connection is configurable for a single option shown with a ✓.

**Table 4. Solder Pad Connection Definitions**

Solder Pad Number	Device Port Pin	UART	SPI	I <sup>2</sup> C	TCPWM <sup>[2]</sup>	Cap-Sense	WCO Out	ECO Out	LCD	SWD	GPIO
1	GND	Ground Connection									
2	XRES	External Reset Hardware Connection Input									
3	P4.0 <sup>[3]</sup>	✓ (SCB1_RTS)	✓ (SCB1_MOSI)		✓ (TCPWM0_P)	✓ (C <sub>MOD</sub> )			✓		✓
4	P3.7	✓ (SCB1_CTS)			✓ (TCPWM3_N)	✓ (Sensor)	✓		✓		✓
5	P3.6	✓ (SCB1_RTS)			✓ (TCPWM3_P)	✓ (Sensor)			✓		✓
6	P3.5	✓ (SCB1_TX)		✓ (SCB1_SCL)	✓ (TCPWM2_N)	✓ (Sensor)			✓		✓
7	P3.4	✓ (SCB1_RX)		✓ (SCB1_SDA)	✓ (TCPWM2_P)	✓ (Sensor)			✓		✓
8	VREF	Reference Voltage Input (Optional)									
9	P2.6					✓ (Sensor)			✓		✓
10	P2.4					✓ (Sensor)			✓		✓
11	P2.3					✓ (Sensor)	✓		✓		✓
12	P2.2		✓ (SCB0_SS3)			✓ (Sensor)			✓		✓
13	P2.0		✓ (SCB0_SS1)			✓ (Sensor)			✓		✓
14	P1.7	✓ (SCB0_CTS)	✓ (SCB0_SCLK)		✓ (TCPWM3_N)	✓ (Sensor)			✓		✓
15	P1.6	✓ (SCB0_RTS)	✓ (SCB0_SS0)		✓ (TCPWM3_P)	✓ (Sensor)			✓		✓
16	P1.5	✓ (SCB0_TX)	✓ (SCB0_MISO)	✓ (SCB0_SCL)	✓ (TCPWM2_N)	✓ (Sensor)			✓		✓
17	P1.4	✓ (SCB0_RX)	✓ (SCB0_MOSI)	✓ (SCB0_SDA)	✓ (TCPWM2_P)	✓ (Sensor)			✓		✓
18	P0.7	✓ (SCB0_CTS)	✓ (SCB0_SCLK)		✓ (TCPWM2_N)	✓ (Sensor)			✓	✓ (SWDCLK)	✓
19	P1.0				✓ (TCPWM0_P)	✓ (Sensor)			✓		✓
20	P0.4	✓ (SCB0_RX)	✓ (SCB0_MOSI)	✓ (SCB0_SDA)	✓ (TCPWM1_P)	✓ (Sensor)		✓	✓		✓
21	P0.5	✓ (SCB0_TX)	✓ (SCB0_MISO)	✓ (SCB0_SCL)	✓ (TCPWM1_N)	✓ (Sensor)			✓		✓
22	V <sub>DD</sub>	Digital Power Supply Input (1.8 to 5.5V)									
23	P0.6	✓ (SCB0_RTS)	✓ (SCB0_SS0)		✓ (TCPWM2_P)	✓ (Sensor)			✓	✓ (SWDIO)	✓
24	GND <sup>[4]</sup>	Ground Connection									
25	GND	Ground Connection									
26	GND	Ground Connection									
27	GND	Ground Connection									
28	V <sub>DDR</sub>	Radio Power Supply (2V to 3.6V)									
29	ANT	RF Pin to External Antenna									
30	GND	Ground Connection									

## Notes

- Notes**

  2. TCPWM: Timer, Counter, and Pulse Width Modulator. If supported, the pad can be configured to any of these peripheral functions.
  3. When using the capacitive sensing functionality, Pad 3 (P4.0) must be connected to a  $C_{MOD}$  capacitor (located off of Cypress BLE Module). The value of this capacitor is 2.2 nF and should be placed as close to the module as possible.
  4. The main board needs to connect all GND connections (Pad 24/25/26/27) on the module to the common ground of the system.
  5. If the I<sup>2</sup>S feature is used in the design, the I<sup>2</sup>S pins shall be dynamically routed to the appropriate available GPIO by PSoC Creator.

## Power Supply Connections and Recommended External Components

### Power Connections

The CYBLE-2X20XX-X1 contains two power supply connections, VDD and VDDR. The VDD connection supplies power for both digital and analog device operation. The VDDR connection supplies power for the device radio.

VDD accepts a supply range of 1.71 V to 5.5 V. VDDR accepts a supply range of 2.0V to 3.6V. These specifications can be found in [Table 12](#). The maximum power supply ripple for both power connections on the module is 100 mV, as shown in [Table 10](#).

The power supply ramp rate of VDD must be equal to or greater than that of VDDR.

### Connection Options

Two connection options are available for any application:

1. Single supply: Connect VDD and VDDR to the same supply.
2. Independent supply: Power VDD and VDDR separately.

### External Component Recommendation

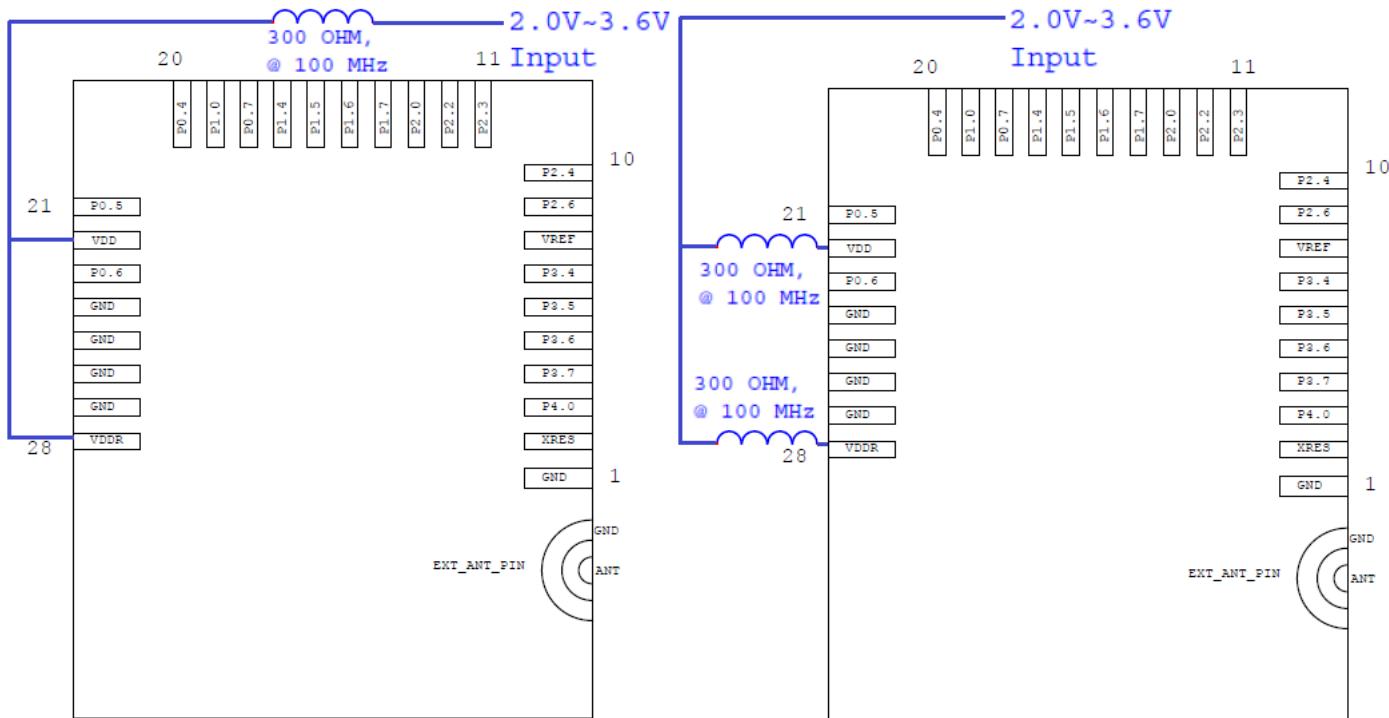
In either connection scenario, it is recommended to place an external ferrite bead between the supply and the module connection. The ferrite bead should be positioned as close as possible to the module pin connection.

[Figure 7](#) details the recommended host schematic options for a single supply scenario. The use of one or two ferrite beads will depend on the specific application and configuration of the CYBLE-2X20XX-X1.

[Figure 8](#) details the recommended host schematic for an independent supply scenario.

The recommended ferrite bead value is  $330 \Omega$ , 100 MHz. (Murata BLM21PG331SN1D).

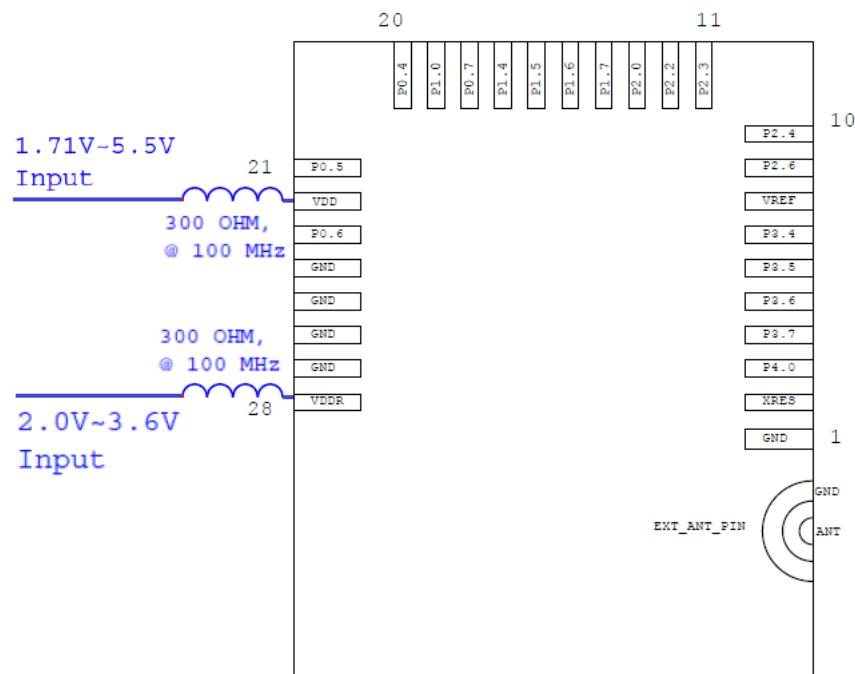
**Figure 7. Recommended Host Schematic Options for a Single Supply Option**



**Single Ferrite Bead Option**

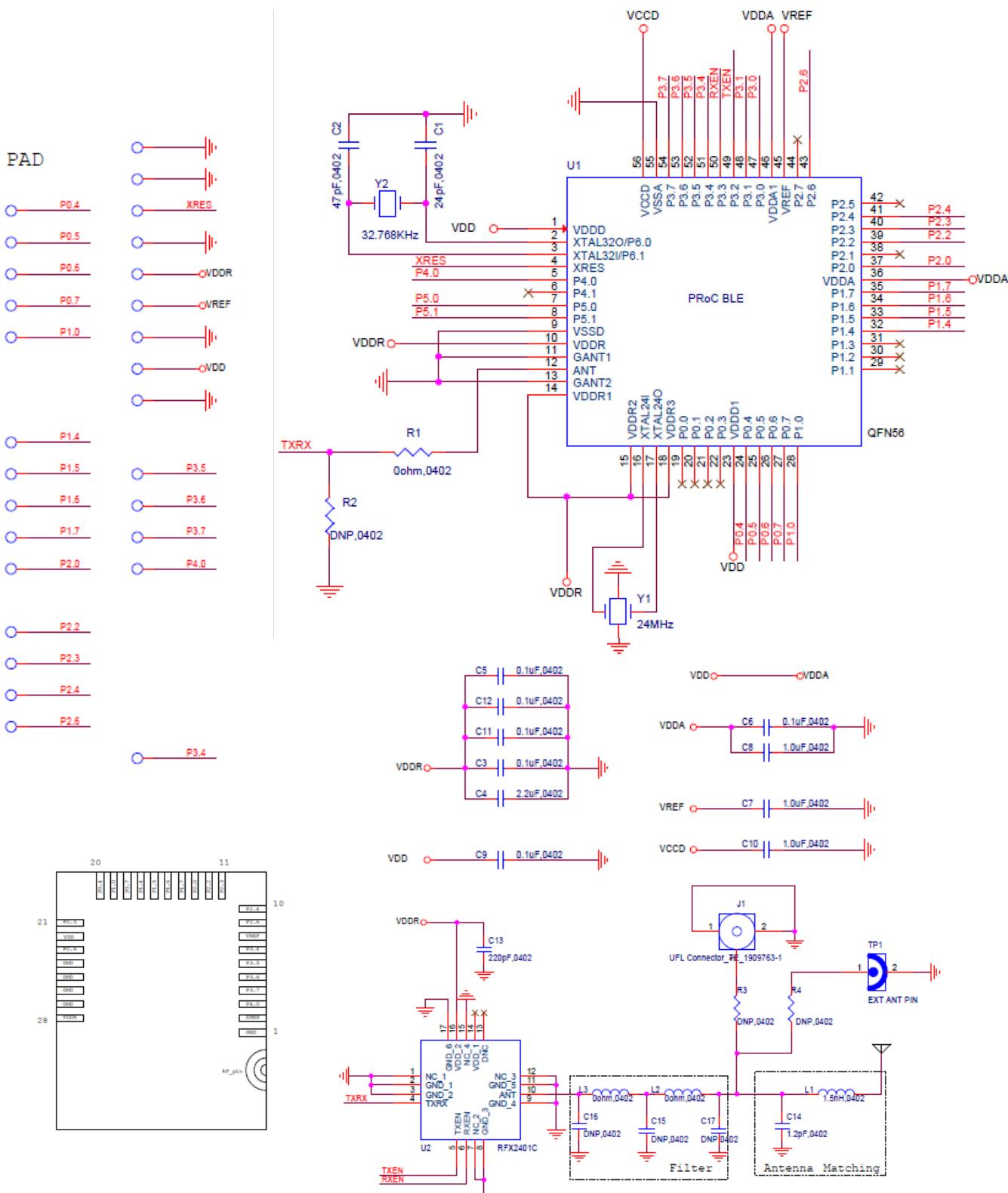
**Two Ferrite Bead Option**

**Figure 8. Recommended Host Schematic for an Independent Supply Option**



The CYBLE-2X20XX-X1 schematic is shown in Figure 9.

**Figure 9. CYBLE-2X20XX-X1 Schematic Diagram**



## Critical Components List

Table 5 details the critical components used in the CYBLE-2X20XX-X1 module.

**Table 5. Critical Component List**

Component	Reference Designator	Description
Silicon	U1	56-pin QFN Programmable Radio-on-Chip (PRoC) with BLE
Crystal	Y1	24.000 MHz, 12PF
Crystal	Y2	32.768 kHz, 12.5PF

## Antenna Design

Table 6 details trace antenna used in the CYBLE-212006-01 module. For more information, see Table 11.

**Table 6. Trace Antenna Specifications**

Item	Description
Frequency Range	2402 – 2480 MHz
Peak Gain	-0.5 dBi
Return Loss	10 dB minimum

## Qualified Antenna for CYBLE-202007-01 and CYBLE-202013-11

The CYBLE-202007-01 and CYBLE-202013-11 modules have been designed to work with a standard 2.2 dBi dipole antenna. Any antenna of equivalent or less gain can be used without additional application and testing for FCC regulations. Table 7 details approved antenna for the CYBLE-202007-01 and CYBLE-202013-11modules antennas for BLE.

**Table 7. Qualified Antenna**

Manufacturer	Part Number	Gain
Antenova	B4844-01	2.2 dBi
RFLink	RF21C01228A	2.0 dBi
Pulse	W1030	2.0 dBi

## Power Amplifier (PA) and Low Noise Amplifier (LNA)

Table 8 details the PA/LNA that is used on the CYBLE-2X20XX-X1 module. For more information, see Table 11.

**Table 8. Power Amplifier/Low Noise Amplifier Details**

Item	Description
PA/LNA Manufacturer	Skyworks Inc.
PA/LNA Part Number	RFX2401C
Power Supply Range	2.0V to 3.6V

Table 9 details the power consumption of the integrated PA/LNA used on the CYBLE-2X20XX-X1 module. Table 9 only details the current consumption of the RFX2401C PA/LNA. VDD= 3.3 V, TA = +25°C, measured on the RFX2401C evaluation board, unless otherwise noted.

**Table 9. Power Amplifier/Low Noise Amplifier Current Consumption Specifications**

Parameter	Test Condition	Min	Typical	Max	Unit
Tx High Power Current	Pout = +20dBm		90		mA
Tx Quiescent Current	No RF applied		17		mA
Rx Quiescent Current	No RF applied		8		mA

## Electrical Specification

**Table 10** details the absolute maximum electrical characteristics for the Cypress BLE module.

**Table 10. CYBLE-2X20XX-X1 Absolute Maximum Ratings**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V <sub>DDD_ABS</sub>	Analog, digital, or radio supply relative to V <sub>SS</sub> (V <sub>SSD</sub> = V <sub>SSA</sub> )	-0.5	—	6	V	Absolute maximum
V <sub>CCD_ABS</sub>	Direct digital core voltage input relative to V <sub>SSD</sub>	-0.5	—	1.95	V	Absolute maximum
V <sub>DD_RIPPLE</sub>	Maximum power supply ripple for V <sub>DD</sub> and V <sub>DDR</sub> input voltage	—	—	100	mV	3.0V supply Ripple frequency of 100 kHz to 750 kHz
V <sub>GPIO_ABS</sub>	GPIO voltage	-0.5	—	V <sub>DD</sub> + 0.5	V	Absolute maximum
I <sub>GPIO_ABS</sub>	Maximum current per GPIO	-25	—	25	mA	Absolute maximum
I <sub>GPIO_injection</sub>	GPIO injection current: Maximum for V <sub>IH</sub> > V <sub>DD</sub> and minimum for V <sub>IL</sub> < V <sub>SS</sub>	-0.5	—	0.5	mA	Absolute maximum current injected per pin
LU	Pin current for latch up	-200	—	200	mA	—

**Table 11** details the RF characteristics for the Cypress BLE module.

**Table 11. CYBLE-2X20XX-X1 RF Performance Characteristics**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
RF <sub>O</sub>	RF output power on ANT	1	—	7.5	dBm	Configurable via register settings (CYBLE-212006-01)
RX <sub>S</sub>	RF receive sensitivity on ANT	—	-93	—	dBm	Measured value (CYBLE-212006-01)
F <sub>R</sub>	Module frequency range	2402	—	2480	MHz	—
G <sub>P</sub>	Peak gain	—	-0.5	—	dBi	—
RL	Return loss	—	-10	—	dB	—

**Table 12** through **Table 51** list the module level electrical characteristics for the CYBLE-2X20XX-X1. All specifications are valid for -40 °C ≤ TA ≤ 85 °C and TJ ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

**Table 12. CYBLE-2X20XX-X1 DC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V <sub>DD1</sub>	Power supply input voltage	1.8	—	5.5	V	With regulator enabled
V <sub>DD2</sub>	Power supply input voltage unregulated	1.71	1.8	1.89	V	Internally unregulated supply
V <sub>DDR1</sub>	Radio supply voltage (radio on)	2.0	—	3.6	V	Restricted by RFX2401C
V <sub>DDR2</sub>	Radio supply voltage (radio off)	2.0	—	3.6	V	—
<b>Active Mode, V<sub>DD</sub> = 1.71 V to 5.5 V</b>						
I <sub>DD3</sub>	Execute from flash; CPU at 3 MHz	—	1.7	—	mA	T = 25 °C, V <sub>DD</sub> = 3.3 V
I <sub>DD4</sub>	Execute from flash; CPU at 3 MHz	—	—	—	mA	T = -40 °C to 85 °C
I <sub>DD5</sub>	Execute from flash; CPU at 6 MHz	—	2.5	—	mA	T = 25 °C, V <sub>DD</sub> = 3.3 V
I <sub>DD6</sub>	Execute from flash; CPU at 6 MHz	—	—	—	mA	T = -40 °C to 85 °C
I <sub>DD7</sub>	Execute from flash; CPU at 12 MHz	—	4	—	mA	T = 25 °C, V <sub>DD</sub> = 3.3 V
I <sub>DD8</sub>	Execute from flash; CPU at 12 MHz	—	—	—	mA	T = -40 °C to 85 °C

**Table 12. CYBLE-2X20XX-X1 DC Specifications (continued)**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I <sub>DD9</sub>	Execute from flash; CPU at 24 MHz	–	7.1	–	mA	T = 25 °C, V <sub>DD</sub> = 3.3 V
I <sub>DD10</sub>	Execute from flash; CPU at 24 MHz	–	–	–	mA	T = –40 °C to 85 °C
I <sub>DD11</sub>	Execute from flash; CPU at 48 MHz	–	13.4	–	mA	T = 25 °C, V <sub>DD</sub> = 3.3 V
I <sub>DD12</sub>	Execute from flash; CPU at 48 MHz	–	–	–	mA	T = –40 °C to 85 °C
<b>Sleep Mode, V<sub>DD</sub> = 1.8 to 5.5 V</b>						
I <sub>DD13</sub>	IMO on	–	–	–	mA	T = 25 °C, V <sub>DD</sub> = 3.3 V, SYSCLK = 3 MHz
<b>Sleep Mode, V<sub>DD</sub> and V<sub>DDR</sub> = 1.9 to 5.5 V</b>						
I <sub>DD14</sub>	ECO on	–	–	–	mA	T = 25 °C, V <sub>DD</sub> = 3.3 V, SYSCLK = 3 MHz
<b>Deep-Sleep Mode, V<sub>DD</sub> = 1.8 to 3.6 V</b>						
I <sub>DD15</sub>	WDT with WCO on	–	1.5	–	μA	T = 25 °C, V <sub>DD</sub> = 3.3 V
I <sub>DD16</sub>	WDT with WCO on	–	–	–	μA	T = –40 °C to 85 °C
I <sub>DD17</sub>	WDT with WCO on	–	–	–	μA	T = 25 °C, V <sub>DD</sub> = 5 V
I <sub>DD18</sub>	WDT with WCO on	–	–	–	μA	T = –40 °C to 85 °C
<b>Deep-Sleep Mode, V<sub>DD</sub> = 1.71 to 1.89 V (Regulator Bypassed)</b>						
I <sub>DD19</sub>	WDT with WCO on	–	–	–	μA	T = 25 °C
I <sub>DD20</sub>	WDT with WCO on	–	–	–	μA	T = –40 °C to 85 °C
<b>Hibernate Mode, V<sub>DD</sub> = 1.8 to 3.6 V</b>						
I <sub>DD27</sub>	GPIO and reset active	–	150	–	nA	T = 25 °C, V <sub>DD</sub> = 3.3 V
I <sub>DD28</sub>	GPIO and reset active	–	–	–	nA	T = –40 °C to 85 °C
<b>Hibernate Mode, V<sub>DD</sub> = 3.6 to 5.5 V</b>						
I <sub>DD29</sub>	GPIO and reset active	–	–	–	nA	T = 25 °C, V <sub>DD</sub> = 5 V
I <sub>DD30</sub>	GPIO and reset active	–	–	–	nA	T = –40 °C to 85 °C
<b>Stop Mode, V<sub>DD</sub> = 1.8 to 3.6 V</b>						
I <sub>DD33</sub>	Stop-mode current (V <sub>DD</sub> )	–	20	–	nA	T = 25 °C, V <sub>DD</sub> = 3.3 V
I <sub>DD34</sub>	Stop-mode current (V <sub>DDR</sub> )	–	40	--	nA	T = 25 °C, V <sub>DDR</sub> = 3.3 V
I <sub>DD35</sub>	Stop-mode current (V <sub>DD</sub> )	–	–	–	nA	T = –40 °C to 85 °C
I <sub>DD36</sub>	Stop-mode current (V <sub>DDR</sub> )	–	–	–	nA	T = –40 °C to 85 °C, V <sub>DDR</sub> = 1.9 V to 3.6 V
<b>Stop Mode, V<sub>DD</sub> = 3.6 to 5.5 V</b>						
I <sub>DD37</sub>	Stop-mode current (V <sub>DD</sub> )	–	–	–	nA	T = 25 °C, V <sub>DD</sub> = 5 V
I <sub>DD38</sub>	Stop-mode current (V <sub>DDR</sub> )	–	–	–	nA	T = 25 °C, V <sub>DDR</sub> = 5 V
I <sub>DD39</sub>	Stop-mode current (V <sub>DD</sub> )	–	–	–	nA	T = –40 °C to 85 °C
I <sub>DD40</sub>	Stop-mode current (V <sub>DDR</sub> )	–	–	–	nA	T = –40 °C to 85 °C

**Table 13. AC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
$F_{CPU}$	CPU frequency	DC	—	48	MHz	$1.71 \text{ V} \leq V_{DD} \leq 5.5 \text{ V}$
$T_{SLEEP}$	Wakeup from Sleep mode	—	0	—	$\mu\text{s}$	Guaranteed by characterization
$T_{DEEPSLEEP}$	Wakeup from Deep-Sleep mode	—	—	25	$\mu\text{s}$	24-MHz IMO. Guaranteed by characterization
$T_{HIBERNATE}$	Wakeup from Hibernate mode	—	—	2	ms	Guaranteed by characterization
$T_{STOP}$	Wakeup from Stop mode	—	—	2	ms	XRES wakeup

## GPIO

**Table 14. GPIO DC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
$V_{IH}^{[6]}$	Input voltage HIGH threshold	$0.7 \times V_{DD}$	—	—	V	CMOS input
	LVTTL input, $V_{DD} < 2.7 \text{ V}$	$0.7 \times V_{DD}$	—	—	V	—
	LVTTL input, $V_{DD} \geq 2.7 \text{ V}$	2.0	—	—	V	—
$V_{IL}$	Input voltage LOW threshold	—	—	$0.3 \times V_{DD}$	V	CMOS input
	LVTTL input, $V_{DD} < 2.7 \text{ V}$	—	—	$0.3 \times V_{DD}$	V	—
	LVTTL input, $V_{DD} \geq 2.7 \text{ V}$	—	—	0.8	V	—
$V_{OH}$	Output voltage HIGH level	$V_{DD} - 0.6$	—	—	V	$I_{OH} = 4 \text{ mA}$ at 3.3-V $V_{DD}$
	Output voltage HIGH level	$V_{DD} - 0.5$	—	—	V	$I_{OH} = 1 \text{ mA}$ at 1.8-V $V_{DD}$
$V_{OL}$	Output voltage LOW level	—	—	0.6	V	$I_{OL} = 8 \text{ mA}$ at 3.3-V $V_{DD}$
	Output voltage LOW level	—	—	0.6	V	$I_{OL} = 4 \text{ mA}$ at 1.8-V $V_{DD}$
	Output voltage LOW level	—	—	0.4	V	$I_{OL} = 3 \text{ mA}$ at 3.3-V $V_{DD}$
$R_{PULLUP}$	Pull-up resistor	3.5	5.6	8.5	k $\Omega$	—
$R_{PULLDOWN}$	Pull-down resistor	3.5	5.6	8.5	k $\Omega$	—
$I_{IL}$	Input leakage current (absolute value)	—	—	2	nA	$25^\circ\text{C}$ , $V_{DD} = 3.3 \text{ V}$
$I_{IL\_CTBM}$	Input leakage on CTBm input pins	—	—	4	nA	—
$C_{IN}$	Input capacitance	—	—	7	pF	—
$V_{HYSTTL}$	Input hysteresis LVTTL	25	40	—	mV	$V_{DD} > 2.7 \text{ V}$
$V_{HYSCMOS}$	Input hysteresis CMOS	$0.05 \times V_{DD}$	—	—	1	—
$I_{DIODE}$	Current through protection diode to $V_{DD}/V_{SS}$	—	—	100	$\mu\text{A}$	—
$I_{TOT\_GPIO}$	Maximum total source or sink chip current	—	—	200	mA	—

**Note**

6.  $V_{IH}$  must not exceed  $V_{DD} + 0.2 \text{ V}$ .

**Table 15. GPIO AC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
$T_{RISEF}$	Rise time in Fast-Strong mode	2	—	12	ns	3.3-V $V_{DDD}$ , $C_{LOAD} = 25 \text{ pF}$
$T_{FALLF}$	Fall time in Fast-Strong mode	2	—	12	ns	3.3-V $V_{DDD}$ , $C_{LOAD} = 25 \text{ pF}$
$T_{RISES}$	Rise time in Slow-Strong mode	10	—	60	ns	3.3-V $V_{DDD}$ , $C_{LOAD} = 25 \text{ pF}$
$T_{FALLS}$	Fall time in Slow-Strong mode	10	—	60	ns	3.3-V $V_{DDD}$ , $C_{LOAD} = 25 \text{ pF}$
$F_{GPIOOUT1}$	GPIO Fout; $3.3 \text{ V} \leq V_{DD} \leq 5.5 \text{ V}$ Fast-Strong mode	—	—	33	MHz	90/10%, 25 pF load, 60/40 duty cycle
$F_{GPIOOUT2}$	GPIO Fout; $1.7 \text{ V} \leq V_{DD} \leq 3.3 \text{ V}$ Fast-Strong mode	—	—	16.7	MHz	90/10%, 25 pF load, 60/40 duty cycle
$F_{GPIOOUT3}$	GPIO Fout; $3.3 \text{ V} \leq V_{DD} \leq 5.5 \text{ V}$ Slow-Strong mode	—	—	7	MHz	90/10%, 25 pF load, 60/40 duty cycle
$F_{GPIOOUT4}$	GPIO Fout; $1.7 \text{ V} \leq V_{DD} \leq 3.3 \text{ V}$ Slow-Strong mode	—	—	3.5	MHz	90/10%, 25 pF load, 60/40 duty cycle
$F_{GPIOIN}$	GPIO input operating frequency $1.71 \text{ V} \leq V_{DD} \leq 5.5 \text{ V}$	—	—	48	MHz	90/10% $V_{IO}$

**Table 16. OVT GPIO DC Specifications (P5\_0 and P5\_1 Only)**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
$I_{IL}$	Input leakage (absolute value). $V_{IH} > V_{DD}$	—	—	10	$\mu\text{A}$	$25^\circ\text{C}$ , $V_{DD} = 0 \text{ V}$ , $V_{IH} = 3.0 \text{ V}$
$V_{OL}$	Output voltage LOW level	—	—	0.4	V	$I_{OL} = 20 \text{ mA}$ , $V_{DD} > 2.9 \text{ V}$

**Table 17. OVT GPIO AC Specifications (P5\_0 and P5\_1 Only)**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
$T_{RISE\_OVFS}$	Output rise time in Fast-Strong mode	1.5	—	12	ns	25-pF load, 10%-90%, $V_{DD} = 3.3 \text{ V}$
$T_{FALL\_OVFS}$	Output fall time in Fast-Strong mode	1.5	—	12	ns	25-pF load, 10%-90%, $V_{DD} = 3.3 \text{ V}$
$T_{RISESS}$	Output rise time in Slow-Strong mode	10	—	60	ns	25 pF load, 10%-90%, $V_{DD} = 3.3 \text{ V}$
$T_{FALLSS}$	Output fall time in Slow-Strong mode	10	—	60	ns	25 pF load, 10%-90%, $V_{DD} = 3.3 \text{ V}$
$F_{GPIOOUT1}$	GPIO $F_{OUT}$ ; $3.3 \text{ V} \leq V_{DD} \leq 5.5 \text{ V}$ Fast-Strong mode	—	—	24	MHz	90/10%, 25 pF load, 60/40 duty cycle
$F_{GPIOOUT2}$	GPIO $F_{OUT}$ ; $1.71 \text{ V} \leq V_{DD} \leq 3.3 \text{ V}$ Fast-Strong mode	—	—	16	MHz	90/10%, 25 pF load, 60/40 duty cycle

## XRES

**Table 18. XRES DC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
$V_{IH}$	Input voltage HIGH threshold	$0.7 \times V_{DDD}$	—	—	V	CMOS input
$V_{IL}$	Input voltage LOW threshold	—	—	$0.3 \times V_{DDD}$	V	CMOS input
$R_{PULLUP}$	Pull-up resistor	3.5	5.6	8.5	k $\Omega$	—
$C_{IN}$	Input capacitance	—	3	—	pF	—
$V_{HYSXRES}$	Input voltage hysteresis	—	100	—	mV	—
$I_{DIODE}$	Current through protection diode to $V_{DD}/V_{SS}$	—	—	100	$\mu\text{A}$	—

**Table 19. XRES AC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T_RESETWIDTH	Reset pulse width	1	–	–	μs	–

*Temperature Sensor*
**Table 20. Temperature Sensor Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T_SENSACC	Temperature-sensor accuracy	–5	±1	5	°C	–40 °C to +85 °C

*SAR ADC*
**Table 21. SAR ADC DC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
A_RES	Resolution	–	–	12	bits	
A_CHNIS_S	Number of channels - single-ended	–	–	8		8 full-speed
A_CHNKS_D	Number of channels - differential	–	–	4		Diff inputs use neighboring I/O
A-MONO	Monotonicity	–	–	–		Yes
A_GAINERR	Gain error	–	–	±0.1	%	With external reference
A_OFFSET	Input offset voltage	–	–	2	mV	Measured with 1-V V <sub>REF</sub>
A_ISAR	Current consumption	–	–	1	mA	
A_VINS	Input voltage range - single-ended	V <sub>SS</sub>	–	V <sub>DDA</sub>	V	
A_VIND	Input voltage range - differential	V <sub>SS</sub>	–	V <sub>DDA</sub>	V	
A_INRES	Input resistance	–	–	2.2	kΩ	
A_INCAP	Input capacitance	–	–	10	pF	
VREFSAR	Trimmed internal reference to SAR	–1	–	1	%	Percentage of Vbg (1.024 V)

**Table 22. SAR ADC AC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
A_PSRR	Power-supply rejection ratio	70	–	–	dB	Measured at 1-V reference
A_CMRR	Common-mode rejection ratio	66	–	–	dB	
A_SAMP	Sample rate	–	–	1	Msp	
Fsarintref	SAR operating speed without external ref. bypass	–	–	100	Ksp	12-bit resolution
A_SNR	Signal-to-noise ratio (SNR)	65	–	–	dB	F <sub>IN</sub> = 10 kHz
A_BW	Input bandwidth without aliasing	–	–	A_SAMP/2	kHz	
A_INL	Integral nonlinearity. V <sub>DD</sub> = 1.71 V to 5.5 V, 1 Msp	–1.7	–	2	LSB	V <sub>REF</sub> = 1 V to V <sub>DD</sub>
A_INL	Integral nonlinearity. V <sub>DD</sub> = 1.71 V to 3.6 V, 1 Msp	–1.5	–	1.7	LSB	V <sub>REF</sub> = 1.71 V to V <sub>DD</sub>
A_INL	Integral nonlinearity. V <sub>DD</sub> = 1.71 V to 5.5 V, 500 Ksp	–1.5	–	1.7	LSB	V <sub>REF</sub> = 1 V to V <sub>DD</sub>
A_dnl	Differential nonlinearity. V <sub>DD</sub> = 1.71 V to 5.5 V, 1 Msp	–1	–	2.2	LSB	V <sub>REF</sub> = 1 V to V <sub>DD</sub>

**Table 22. SAR ADC AC Specifications (continued)**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
A_DNL	Differential nonlinearity. $V_{DD} = 1.71\text{ V}$ to $3.6\text{ V}$ , $1\text{ Msps}$	-1	-	2	LSB	$V_{REF} = 1.71\text{ V}$ to $V_{DD}$
A_DNL	Differential nonlinearity. $V_{DD} = 1.71\text{ V}$ to $5.5\text{ V}$ , $500\text{ Ksps}$	-1	-	2.2	LSB	$V_{REF} = 1\text{ V}$ to $V_{DD}$
A THD	Total harmonic distortion	-	-	-65	dB	$F_{IN} = 10\text{ kHz}$

CSD

**CSD Block Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
$V_{CSD}$	Voltage range of operation	1.71	-	5.5	V	-
IDAC1	DNL for 8-bit resolution	-1	-	1	LSB	-
IDAC1	INL for 8-bit resolution	-3	-	3	LSB	-
IDAC2	DNL for 7-bit resolution	-1	-	1	LSB	-
IDAC2	INL for 7-bit resolution	-3	-	3	LSB	-
SNR	Ratio of counts of finger to noise	5	-	-	Ratio	Capacitance range of $9\text{ pF}$ to $35\text{ pF}$ , $0.1\text{-pF}$ sensitivity. Radio is not operating during the scan
$I_{DAC1\_CRT1}$	Output current of IDAC1 (8 bits) in High range	-	612	-	$\mu\text{A}$	-
$I_{DAC1\_CRT2}$	Output current of IDAC1 (8 bits) in Low range	-	306	-	$\mu\text{A}$	-
$I_{DAC2\_CRT1}$	Output current of IDAC2 (7 bits) in High range	-	305	-	$\mu\text{A}$	-
$I_{DAC2\_CRT2}$	Output current of IDAC2 (7 bits) in Low range	-	153	-	$\mu\text{A}$	-

## Digital Peripherals

### Timer

**Table 23. Timer DC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I <sub>TIM1</sub>	Block current consumption at 3 MHz	–	–	42	µA	16-bit timer
I <sub>TIM2</sub>	Block current consumption at 12 MHz	–	–	130	µA	16-bit timer
I <sub>TIM3</sub>	Block current consumption at 48 MHz	–	–	535	µA	16-bit timer

**Table 24. Timer AC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T <sub>TIMFREQ</sub>	Operating frequency	F <sub>CLK</sub>	–	48	MHz	
T <sub>CAPWINT</sub>	Capture pulse width (internal)	2 × T <sub>CLK</sub>	–	–	ns	
T <sub>CAPWEXT</sub>	Capture pulse width (external)	2 × T <sub>CLK</sub>	–	–	ns	
T <sub>TIMRES</sub>	Timer resolution	T <sub>CLK</sub>	–	–	ns	
T <sub>TENWIDINT</sub>	Enable pulse width (internal)	2 × T <sub>CLK</sub>	–	–	ns	
T <sub>TENWIDEXT</sub>	Enable pulse width (external)	2 × T <sub>CLK</sub>	–	–	ns	
T <sub>TIMRESWINT</sub>	Reset pulse width (internal)	2 × T <sub>CLK</sub>	–	–	ns	
T <sub>TIMRESEXT</sub>	Reset pulse width (external)	2 × T <sub>CLK</sub>	–	–	ns	

### Counter

**Table 25. Counter DC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I <sub>CTR1</sub>	Block current consumption at 3 MHz	–	–	42	µA	16-bit counter
I <sub>CTR2</sub>	Block current consumption at 12 MHz	–	–	130	µA	16-bit counter
I <sub>CTR3</sub>	Block current consumption at 48 MHz	–	–	535	µA	16-bit counter

**Table 26. Counter AC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T <sub>CTRFREQ</sub>	Operating frequency	F <sub>CLK</sub>	–	48	MHz	–
T <sub>CTRPWINT</sub>	Capture pulse width (internal)	2 × T <sub>CLK</sub>	–	–	ns	–
T <sub>CTRPWEXT</sub>	Capture pulse width (external)	2 × T <sub>CLK</sub>	–	–	ns	–
T <sub>CTRES</sub>	Counter Resolution	T <sub>CLK</sub>	–	–	ns	–
T <sub>CENWIDINT</sub>	Enable pulse width (internal)	2 × T <sub>CLK</sub>	–	–	ns	–
T <sub>CENWIDEXT</sub>	Enable pulse width (external)	2 × T <sub>CLK</sub>	–	–	ns	–
T <sub>CTRRESWINT</sub>	Reset pulse width (internal)	2 × T <sub>CLK</sub>	–	–	ns	–
T <sub>CTRRESWEXT</sub>	Reset pulse width (external)	2 × T <sub>CLK</sub>	–	–	ns	–

Pulse Width Modulation (PWM)

**Table 27. PWM DC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I <sub>PWM1</sub>	Block current consumption at 3 MHz	–	–	42	µA	16-bit PWM
I <sub>PWM2</sub>	Block current consumption at 12 MHz	–	–	130	µA	16-bit PWM
I <sub>PWM3</sub>	Block current consumption at 48 MHz	–	–	535	µA	16-bit PWM

**Table 28. PWM AC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T <sub>PWMFREQ</sub>	Operating frequency	F <sub>CLK</sub>	–	48	MHz	–
T <sub>PWMPWINT</sub>	Pulse width (internal)	2 × T <sub>CLK</sub>	–	–	ns	–
T <sub>PWMEXT</sub>	Pulse width (external)	2 × T <sub>CLK</sub>	–	–	ns	–
T <sub>PWMKILLINT</sub>	Kill pulse width (internal)	2 × T <sub>CLK</sub>	–	–	ns	–
T <sub>PWMKILLEXT</sub>	Kill pulse width (external)	2 × T <sub>CLK</sub>	–	–	ns	–
T <sub>PWMEINT</sub>	Enable pulse width (internal)	2 × T <sub>CLK</sub>	–	–	ns	–
T <sub>PWMENEXT</sub>	Enable pulse width (external)	2 × T <sub>CLK</sub>	–	–	ns	–
T <sub>PWMRESINT</sub>	Reset pulse width (internal)	2 × T <sub>CLK</sub>	–	–	ns	–
T <sub>PWMRESEXT</sub>	Reset pulse width (external)	2 × T <sub>CLK</sub>	–	–	ns	–

LCD Direct Drive

**Table 29. LCD Direct Drive DC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I <sub>LCDLOW</sub>	Operating current in low-power mode	–	17.5	–	µA	16 × 4 small segment display at 50 Hz
C <sub>LCDCAP</sub>	LCD capacitance per segment/common driver	–	500	5000	pF	–
LCD <sub>OFFSET</sub>	Long-term segment offset	–	20	–	mV	–
I <sub>LCDOP1</sub>	LCD system operating current, V <sub>BIAS</sub> = 5 V	–	2	–	mA	32 × 4 segments. 50 Hz at 25 °C
I <sub>LCDOP2</sub>	LCD system operating current, V <sub>BIAS</sub> = 3.3 V	–	2	–	mA	32 × 4 segments 50 Hz at 25 °C

**Table 30. LCD Direct Drive AC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
F <sub>LCD</sub>	LCD frame rate	10	50	150	Hz	–

**Serial Communication**
**Table 31. Fixed I<sup>2</sup>C DC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I <sub>I2C1</sub>	Block current consumption at 100 kHz	–	–	50	µA	–
I <sub>I2C2</sub>	Block current consumption at 400 kHz	–	–	155	µA	–
I <sub>I2C3</sub>	Block current consumption at 1 Mbps	–	–	390	µA	–
I <sub>I2C4</sub>	I <sup>2</sup> C enabled in Deep-Sleep mode	–	–	1.4	µA	–

**Table 32. Fixed I<sup>2</sup>C AC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
F <sub>I2C1</sub>	Bit rate	–	–	400	kHz	–

**Table 33. Fixed UART DC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I <sub>UART1</sub>	Block current consumption at 100 kbps	–	–	55	µA	–
I <sub>UART2</sub>	Block current consumption at 1000 kbps	–	–	312	µA	–

**Table 34. Fixed UART AC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
F <sub>UART</sub>	Bit rate	–	–	1	Mbps	–

**Table 35. Fixed SPI DC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I <sub>SPI1</sub>	Block current consumption at 1 Mbps	–	–	360	µA	–
I <sub>SPI2</sub>	Block current consumption at 4 Mbps	–	–	560	µA	–
I <sub>SPI3</sub>	Block current consumption at 8 Mbps	–	–	600	µA	–

**Table 36. Fixed SPI AC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
F <sub>SPI</sub>	SPI operating frequency (master; 6x over sampling)	–	–	8	MHz	–

**Table 37. Fixed SPI Master Mode AC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T <sub>DMO</sub>	MOSI valid after SCLK driving edge	–	–	18	ns	–
T <sub>DSI</sub>	MISO valid before SCLK capturing edge Full clock, late MISO sampling used	20	–	–	ns	Full clock, late MISO sampling
T <sub>HMO</sub>	Previous MOSI data hold time	0	–	–	ns	Referred to Slave capturing edge

**Table 38. Fixed SPI Slave Mode AC Specifications**

Parameter	Description	Min	Typ	Max	Units
T <sub>DMI</sub>	MOSI valid before SCLK capturing edge	40	–	–	ns
T <sub>DSO</sub>	MISO valid after SCLK driving edge	–	–	42 + 3 × T <sub>CPU</sub>	ns
T <sub>DSO_ext</sub>	MISO Valid after SCLK driving edge in external clock mode. V <sub>DD</sub> < 3.0 V	–	–	50	ns
T <sub>HSO</sub>	Previous MISO data hold time	0	–	–	ns
T <sub>SSEL_SCK</sub>	SSEL valid to first SCK valid edge	100	–	–	ns

## Memory

**Table 39. Flash DC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
$V_{PE}$	Erase and program voltage	1.71	—	5.5	V	—
$T_{WS48}$	Number of Wait states at 32–48 MHz	2	—	—		CPU execution from flash
$T_{WS32}$	Number of Wait states at 16–32 MHz	1	—	—		CPU execution from flash
$T_{WS16}$	Number of Wait states for 0–16 MHz	0	—	—		CPU execution from flash

**Table 40. Flash AC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
$T_{ROWWRITE}^{[7]}$	Row (block) write time (erase and program)	—	—	20	ms	Row (block) = 256 bytes
$T_{ROWERASE}^{[7]}$	Row erase time	—	—	13	ms	—
$T_{ROWPROGRAM}^{[7]}$	Row program time after erase	—	—	7	ms	—
$T_{BULKERASE}^{[7]}$	Bulk erase time (256 KB)	—	—	35	ms	—
$T_{DEVPROG}^{[7]}$	Total device program time	—	—	25	seconds	—
$F_{END}$	Flash endurance	100 K	—	—	cycles	—
$F_{RET}$	Flash retention. $T_A \leq 55^\circ\text{C}$ , 100 K P/E cycles	20	—	—	years	—
$F_{RET2}$	Flash retention. $T_A \leq 85^\circ\text{C}$ , 10 K P/E cycles	10	—	—	years	—

## System Resources

*Power-on-Reset (POR)*

**Table 41. POR DC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
$V_{RISEIPOR}$	Rising trip voltage	0.80	—	1.45	V	—
$V_{FALLIPOR}$	Falling trip voltage	0.75	—	1.40	V	—
$V_{IPORHYST}$	Hysteresis	15	—	200	mV	—

**Table 42. POR AC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
$T_{PPOR\_TR}$	Precision power-on reset (PPOR) response time in Active and Sleep modes	—	—	1	μs	—

**Table 43. Brown-Out Detect**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
$V_{FALLPPOR}$	BOD trip voltage in Active and Sleep modes	1.64	—	—	V	—
$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep	1.4	—	—	V	—

**Table 44. Hibernate Reset**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
$V_{HBRTRIP}$	BOD trip voltage in Hibernate	1.1	—	—	V	—

### Note

- It can take as much as 20 ms to write to flash. During this time, the device should not be reset, or flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.

*Voltage Monitors (LVD)*
**Table 45. Voltage Monitor DC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V <sub>LVI1</sub>	LVI_A/D_SEL[3:0] = 0000b	1.71	1.75	1.79	V	–
V <sub>LVI2</sub>	LVI_A/D_SEL[3:0] = 0001b	1.76	1.80	1.85	V	–
V <sub>LVI3</sub>	LVI_A/D_SEL[3:0] = 0010b	1.85	1.90	1.95	V	–
V <sub>LVI4</sub>	LVI_A/D_SEL[3:0] = 0011b	1.95	2.00	2.05	V	–
V <sub>LVI5</sub>	LVI_A/D_SEL[3:0] = 0100b	2.05	2.10	2.15	V	–
V <sub>LVI6</sub>	LVI_A/D_SEL[3:0] = 0101b	2.15	2.20	2.26	V	–
V <sub>LVI7</sub>	LVI_A/D_SEL[3:0] = 0110b	2.24	2.30	2.36	V	–
V <sub>LVI8</sub>	LVI_A/D_SEL[3:0] = 0111b	2.34	2.40	2.46	V	–
V <sub>LVI9</sub>	LVI_A/D_SEL[3:0] = 1000b	2.44	2.50	2.56	V	–
V <sub>LVI10</sub>	LVI_A/D_SEL[3:0] = 1001b	2.54	2.60	2.67	V	–
V <sub>LVI11</sub>	LVI_A/D_SEL[3:0] = 1010b	2.63	2.70	2.77	V	–
V <sub>LVI12</sub>	LVI_A/D_SEL[3:0] = 1011b	2.73	2.80	2.87	V	–
V <sub>LVI13</sub>	LVI_A/D_SEL[3:0] = 1100b	2.83	2.90	2.97	V	–
V <sub>LVI14</sub>	LVI_A/D_SEL[3:0] = 1101b	2.93	3.00	3.08	V	–
V <sub>LVI15</sub>	LVI_A/D_SEL[3:0] = 1110b	3.12	3.20	3.28	V	–
V <sub>LVI16</sub>	LVI_A/D_SEL[3:0] = 1111b	4.39	4.50	4.61	V	–
LVI_IDD	Block current	–	–	100	µA	–

**Table 46. Voltage Monitor AC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T <sub>MONTRIP</sub>	Voltage monitor trip time	–	–	1	µs	–

*SWD Interface*
**Table 47. SWD Interface Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
F <sub>SWDCLK1</sub>	3.3 V ≤ V <sub>DD</sub> ≤ 5.5 V	–	–	14	MHz	SWDCLK ≤ 1/3 CPU clock frequency
F <sub>SWDCLK2</sub>	1.71 V ≤ V <sub>DD</sub> ≤ 3.3 V	–	–	7	MHz	SWDCLK ≤ 1/3 CPU clock frequency
T <sub>SWDI_SETUP</sub>	T = 1/f SWDCLK	0.25 × T	–	–	ns	–
T <sub>SWDI_HOLD</sub>	T = 1/f SWDCLK	0.25 × T	–	–	ns	–
T <sub>SWDO_VALID</sub>	T = 1/f SWDCLK	–	–	0.5 × T	ns	–
T <sub>SWDO_HOLD</sub>	T = 1/f SWDCLK	1	–	–	ns	–

*Internal Main Oscillator*
**Table 48. IMO DC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I <sub>IMO1</sub>	IMO operating current at 48 MHz	—	—	1000	µA	—
I <sub>IMO2</sub>	IMO operating current at 24 MHz	—	—	325	µA	—
I <sub>IMO3</sub>	IMO operating current at 12 MHz	—	—	225	µA	—
I <sub>IMO4</sub>	IMO operating current at 6 MHz	—	—	180	µA	—
I <sub>IMO5</sub>	IMO operating current at 3 MHz	—	—	150	µA	—

**Table 49. IMO AC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
F <sub>IMOTOL3</sub>	Frequency variation from 3 to 48 MHz	—	—	±2	%	With API-called calibration
F <sub>IMOTOL3</sub>	IMO startup time	—	12	—	µs	—

*Internal Low-Speed Oscillator*
**Table 50. ILO DC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
I <sub>ILO2</sub>	ILO operating current at 32 kHz	—	0.3	1.05	µA	—

**Table 51. ILO AC Specifications**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
T <sub>STARTILO1</sub>	ILO startup time	—	—	2	ms	—
F <sub>ILOTRIM1</sub>	32-kHz trimmed frequency	15	32	50	kHz	—

**Table 52. ECO Trim Value Specification**

Parameter	Description	Value	Details/Conditions
ECO <sub>TRIM</sub>	24-MHz trim value (firmware configuration)	0x00007FDC	Optimum trim value that needs to be loaded to register CY_SYS_XTAL_BLERD_BB_XO_CAPTRIM_REG

*BLE Subsystem*
**Table 53. BLE Subsystem**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
<b>RF Receiver Specification</b>						
RXS, IDLE	RX sensitivity with idle transmitter	—	—89	—	dBm	—
	RX sensitivity with idle transmitter excluding Balun loss	—	—91	—	dBm	Guaranteed by design simulation
RXS, DIRTY	RX sensitivity with dirty transmitter	—	—87	—70	dBm	RF-PHY Specification (RCV-LE/CA/01/C)
RXS, HIGHGAIN	RX sensitivity in high-gain mode with idle transmitter	—	—91	—	dBm	—
PRXMAX	Maximum input power	—10	—1	—	dBm	RF-PHY Specification (RCV-LE/CA/06/C)
CI1	Cochannel interference, Wanted signal at —67 dBm and Interferer at FRX	—	9	21	dB	RF-PHY Specification (RCV-LE/CA/03/C)

**Table 53. BLE Subsystem (continued)**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
CI2	Adjacent channel interference Wanted signal at -67 dBm and Interferer at FRX $\pm 1$ MHz	-	3	15	dB	RF-PHY Specification (RCV-LE/CA/03/C)
CI3	Adjacent channel interference Wanted signal at -67 dBm and Interferer at FRX $\pm 2$ MHz	-	-29	-	dB	RF-PHY Specification (RCV-LE/CA/03/C)
CI4	Adjacent channel interference Wanted signal at -67 dBm and Interferer at $\geq$ FRX $\pm 3$ MHz	-	-39	-	dB	RF-PHY Specification (RCV-LE/CA/03/C)
CI5	Adjacent channel interference Wanted Signal at -67 dBm and Interferer at Image frequency ( $F_{IMAGE}$ )	-	-20	-	dB	RF-PHY Specification (RCV-LE/CA/03/C)
CI3	Adjacent channel interference Wanted signal at -67 dBm and Interferer at Image frequency ( $F_{IMAGE} \pm 1$ MHz)	-	-30	-	dB	RF-PHY Specification (RCV-LE/CA/03/C)
OBB1	Out-of-band blocking, Wanted signal at -67 dBm and Interferer at F = 30–2000 MHz	-30	-27	-	dBm	RF-PHY Specification (RCV-LE/CA/04/C)
OBB2	Out-of-band blocking, Wanted signal at -67 dBm and Interferer at F = 2003–2399 MHz	-35	-27	-	dBm	RF-PHY Specification (RCV-LE/CA/04/C)
OBB3	Out-of-band blocking, Wanted signal at -67 dBm and Interferer at F = 2484–2997 MHz	-35	-27	-	dBm	RF-PHY Specification (RCV-LE/CA/04/C)
OBB4	Out-of-band blocking, Wanted signal a -67 dBm and Interferer at F = 3000–12750 MHz	-30	-27	-	dBm	RF-PHY Specification (RCV-LE/CA/04/C)
IMD	Inter modulation performance Wanted signal at -64 dBm and 1-Mbps BLE, third, fourth, and fifth offset channel	-50	-	-	dBm	RF-PHY Specification (RCV-LE/CA/05/C)
RXSE1	Receiver spurious emission 30 MHz to 1.0 GHz	-	-	-57	dBm	100-kHz measurement bandwidth ETSI EN300 328 V1.8.1
RXSE2	Receiver spurious emission 1.0 GHz to 12.75 GHz	-	-	-47	dBm	1-MHz measurement bandwidth ETSI EN300 328 V1.8.1
<b>RF Transmitter Specifications</b>						
TXP, ACC	RF power accuracy	-	$\pm 1$	-	dB	-
TXP, RANGE	RF power control range	-	20	-	dB	-
TXP, 0dBm	Output power, 0-dB Gain setting (PA7)	-	0	-	dBm	-
TXP, MAX	Output power, maximum power setting (PA10)	-	3	-	dBm	-
TXP, MIN	Output power, minimum power setting (PA1)	-	-18	-	dBm	-
F2AVG	Average frequency deviation for 10101010 pattern	185	-	-	kHz	RF-PHY Specification (TRM-LE/CA/05/C)
F1AVG	Average frequency deviation for 11110000 pattern	225	250	275	kHz	RF-PHY Specification (TRM-LE/CA/05/C)

**Table 53. BLE Subsystem (continued)**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
EO	Eye opening = $\Delta F2AVG / \Delta F1AVG$	0.8	—	—		RF-PHY Specification (TRM-LE/CA/05/C)
FTX, ACC	Frequency accuracy	-150	—	150	kHz	RF-PHY Specification (TRM-LE/CA/06/C)
FTX, MAXDR	Maximum frequency drift	-50	—	50	kHz	RF-PHY Specification (TRM-LE/CA/06/C)
FTX, INITDR	Initial frequency drift	-20	—	20	kHz	RF-PHY Specification (TRM-LE/CA/06/C)
FTX, DR	Maximum drift rate	-20	—	20	kHz/ 50 $\mu$ s	RF-PHY Specification (TRM-LE/CA/06/C)
IBSE1	In-band spurious emission at 2-MHz offset	—	—	-20	dBm	RF-PHY Specification (TRM-LE/CA/03/C)
IBSE2	In-band spurious emission at $\geq$ 3-MHz offset	—	—	-30	dBm	RF-PHY Specification (TRM-LE/CA/03/C)
TXSE1	Transmitter spurious emissions (average), <1.0 GHz	—	—	-55.5	dBm	FCC-15.247
TXSE2	Transmitter spurious emissions (average), >1.0 GHz	—	—	-41.5	dBm	FCC-15.247
<b>RF Current Specifications</b>						
IRX	Receive current in normal mode	—	18.7	—	mA	—
IRX_RF	Radio receive current in normal mode	—	16.4	—	mA	Measured at $V_{DDR}$
IRX, HIGHGAIN	Receive current in high-gain mode	—	21.5	—	mA	—
ITX, 3dBm	TX current at 3-dBm setting (PA10)	—	20	—	mA	—
ITX, 0dBm	TX current at 0-dBm setting (PA7)	—	16.5	—	mA	—
ITX_RF, 0dBm	Radio TX current at 0 dBm setting (PA7)	—	15.6	—	mA	Measured at $V_{DDR}$
ITX_RF, 0dBm	Radio TX current at 0 dBm excluding Balun loss	—	14.2	—	mA	Guaranteed by design simulation
ITX,-3dBm	TX current at -3-dBm setting (PA4)	—	15.5	—	mA	—
ITX,-6dBm	TX current at -6-dBm setting (PA3)	—	14.5	—	mA	—
ITX,-12dBm	TX current at -12-dBm setting (PA2)	—	13.2	—	mA	—
ITX,-18dBm	TX current at -18-dBm setting (PA1)	—	12.5	—	mA	—
lavg_1sec, 0dBm	Average current at 1-second BLE connection interval	—	17.1	—	$\mu$ A	TXP: 0 dBm; $\pm$ 20-ppm master and slave clock accuracy. For empty PDU exchange
lavg_4sec, 0dBm	Average current at 4-second BLE connection interval	—	6.1	—	$\mu$ A	TXP: 0 dBm; $\pm$ 20-ppm master and slave clock accuracy. For empty PDU exchange
<b>General RF Specifications</b>						
FREQ	RF operating frequency	2400	—	2482	MHz	—
CHBW	Channel spacing	—	2	—	MHz	—
DR	On-air data rate	—	1000	—	kbps	—

**Table 53. BLE Subsystem (continued)**

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
IDLE2TX	BLE.IDLE to BLE. TX transition time	–	120	140	µs	–
IDLE2RX	BLE.IDLE to BLE. RX transition time	–	75	120	µs	–
<b>RSSI Specifications</b>						
RSSI, ACC	RSSI accuracy	–	±5	–	dB	–
RSSI, RES	RSSI resolution	–	1	–	dB	–
RSSI, PER	RSSI sample period	–	6	–	µs	–

## Environmental Specifications

### Environmental Compliance

This Cypress BLE module is built in compliance with the Restriction of Hazardous Substances (RoHS) and Halogen Free (HF) directives. The Cypress module and components used to produce this module are RoHS and HF compliant.

### RF Certification

The CYBLE-212006-01 and CYBLE-202007-01 modules will be certified under the following RF certification standards at production release.

- FCC: WAP2006
- CE
- IC: 7922A-2006
- MIC: TBD
- KC: TBD

### Safety Certification

The CYBLE-212006-01 and CYBLE-202007-01 modules comply with the following regulations:

- Underwriters Laboratories, Inc. (UL) - Filing E331901
- CSA
- TUV

### Environmental Conditions

[Table 54](#) describes the operating and storage conditions for the Cypress BLE module.

**Table 54. Environmental Conditions for CYBLE-2X20XX-X1**

Description	Minimum Specification	Maximum Specification
Operating temperature	-40 °C	85 °C
Operating humidity (relative, non-condensation)	5%	85%
Thermal ramp rate	–	3 °C/minute
Storage temperature	-40 °C	85 °C
Storage temperature and humidity	–	85 °C at 85%
ESD: Module integrated into system Components <sup>[8]</sup>	–	15 kV Air 2.2 kV Contact

### ESD and EMI Protection

Exposed components require special attention to ESD and electromagnetic interference (EMI).

A grounded conductive layer inside the device enclosure is suggested for EMI and ESD performance. Any openings in the enclosure near the module should be surrounded by a grounded conductive layer to provide ESD protection and a low-impedance path to ground.

**Device Handling:** Proper ESD protocol must be followed in manufacturing to ensure component reliability.

**Note**

8. This does not apply to the RF pins (ANT, XTAL1, and XTAL0). RF pins (ANT, XTAL1, and XTAL0) are tested for 500-V HBM.



## PRELIMINARY

CYBLE-212006-01  
CYBLE-202007-01  
CYBLE-202013-11

## Regulatory Information

### FCC

#### FCC NOTICE:

The devices CYBLE-212006-01 and CYBLE-202007-01 comply with Part 15 of the FCC Rules. The device meet the requirements for modular transmitter approval as detailed in FCC public Notice DA00-1407. Transmitter Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) This device must accept any interference received, including interference that may cause undesired operation.

#### CAUTION:

The FCC requires the user to be notified that any changes or modifications made to this device that are not expressly approved by Cypress Semiconductor may void the user's authority to operate the equipment.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help

#### LABELING REQUIREMENTS:

The Original Equipment Manufacturer (OEM) must ensure that FCC labelling requirements are met. This includes a clearly visible label on the outside of the OEM enclosure specifying the appropriate Cypress Semiconductor FCC identifier for this product as well as the FCC Notice above. The FCC identifier is FCC ID: WAP2006.

In any case the end product must be labeled exterior with "Contains FCC ID: WAP2006".

#### ANTENNA WARNING:

This device is tested with a standard SMA connector and with antennas meeting the characteristics shown in [Table 7 on page 13](#). When integrated in the OEMs product, these fixed antennas require installation preventing end-users from replacing them with non-approved antennas. Any antenna not in the following table must be tested to comply with FCC Section 15.203 for unique antenna connectors and Section 15.247 for emissions.

#### RF EXPOSURE:

RF Exposure distance of the device is 15mm.

To comply with FCC RF Exposure requirements, the Original Equipment Manufacturer (OEM) must ensure to install the approved antenna in the previous.

The preceding statement must be included as a CAUTION statement in manuals, for products operating with the approved antennas in [Table 6](#) and [Table 7 on page 13](#), to alert users on FCC RF Exposure compliance. Any notification to the end user of installation or removal instructions about the integrated radio module is not allowed.

The radiated output power of CYBLE-212006-01 with the trace antenna is far below the FCC radio frequency exposure limits. Nevertheless, use CYBLE-212006-01 in such a manner that minimizes the potential for human contact during normal operation.

End users may not be provided with the module installation instructions. OEM integrators and end users must be provided with transmitter operating conditions for satisfying RF exposure compliance.

### Industry Canada (IC) Certification

CYBLE-212006-01 and CYBLE-202007-01 are licensed to meet the regulatory requirements of Industry Canada (IC),

License: IC: 7922A-2006

Manufacturers of mobile, fixed or portable devices incorporating this module are advised to clarify any regulatory questions and ensure compliance for SAR and/or RF exposure limits. Users can obtain Canadian information on RF exposure and compliance from [www.ic.gc.ca](http://www.ic.gc.ca).

This device has been designed to operate with the antennas listed in [Table 6](#) and [Table 7 on page 13](#), having a maximum gain of 2.2 dBi. Antennas not included in this list or having a gain greater than 2.2 dBi are strictly prohibited for use with this device. The required antenna impedance is 50 ohms. The antenna used for this transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

#### IC NOTICE:

The device CYBLE-212006-01 including the built-in trace antenna complies with Canada RSS-GEN Rules. The device meets the requirements for modular transmitter approval as detailed in RSS-GEN. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) This device must accept any interference received, including interference that may cause undesired operation.

#### IC RADIATION EXPOSURE STATEMENT FOR CANADA

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

RF Exposure distance of the device is 15mm.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

la distance d'exposition RF de l'appareil est de 15mm.

#### LABELING REQUIREMENTS:

The Original Equipment Manufacturer (OEM) must ensure that IC labelling requirements are met. This includes a clearly visible label on the outside of the OEM enclosure specifying the appropriate Cypress Semiconductor IC identifier for this product as well as the IC Notice above. The IC identifier is 7922A-2006. In any case, the end product must be labeled in its exterior with "Contains IC: 7922A-2006"

### European R&TTE Declaration of Conformity

Hereby, Cypress Semiconductor declares that the Bluetooth module CYBLE-212006-01 and CYBLE-202007-01 comply with the essential requirements and other relevant provisions of Directive 1999/5/EC. As a result of the conformity assessment procedure described in Annex III of the Directive 1999/5/EC, the end-customer equipment should be labeled as follows:



All versions of the CYBLE-212006-01 and CYBLE-202007-01 in the specified reference design can be used in the following countries: Austria, Belgium, Cyprus, Czech Republic, Denmark, Estonia, Finland, France, Germany, Greece, Hungary, Ireland, Italy, Latvia, Lithuania, Luxembourg, Malta, Poland, Portugal, Slovakia, Slovenia, Spain, Sweden, The Netherlands, the United Kingdom, Switzerland, and Norway.

**MIC Japan**

CYBLE-212006-01 and CYBLE-202007-01 are certified as a module with type certification number TBD. End products that integrate CYBLE-212006-01 and CYBLE-202007-01 do not need additional MIC Japan certification for the end product.

End product can display the certification label of the embedded module.

**KC Korea**

CYBLE-212006-01 and CYBLE-202007-01 are certified for use in Korea with certificate number TBD.

## Packaging

**Table 55. Solder Reflow Peak Temperature**

Module Part Number	Package	Maximum Peak Temperature	Maximum Time at Peak Temperature	No. of Cycles
CYBLE-2X20XX-X1	30-pad SMT	260 °C	30 seconds	2

**Table 56. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2**

Module Part Number	Package	MSL
CYBLE-2X20XX-X1	30-pad SMT	MSL 3

The CYBLE-2X20XX-X1 is offered in tape and reel packaging. [Figure 10](#) details the tape dimensions used for the CYBLE-2X20XX-X1.

**Figure 10. CYBLE-2X20XX-X1 Tape Dimensions**

Item	W	A <sub>0</sub>	B <sub>0</sub>	K <sub>0</sub>	K <sub>1</sub>	P <sub>1</sub>	F	E	D <sub>0</sub>	D <sub>1</sub>	P <sub>0</sub>	P <sub>2</sub>	T
Measurement	24.0 <sup>+0.30</sup> <sub>-0.30</sub>	19.5 <sup>+0.10</sup> <sub>-0.10</sub>	14.8 <sup>+0.10</sup> <sub>-0.10</sub>	2.5 <sup>+0.10</sup> <sub>-0.10</sub>	/	24.0 <sup>+0.10</sup> <sub>-0.10</sub>	11.5 <sup>+0.10</sup> <sub>-0.10</sub>	1.75 <sup>+0.10</sup> <sub>-0.10</sub>	1.50 <sup>+0.10</sup> <sub>-0.00</sub>	1.50 <sup>+0.10</sup> <sub>-0.10</sub>	4.00 <sup>+0.10</sup> <sub>-0.10</sub>	2.00 <sup>+0.10</sup> <sub>-0.10</sub>	0.30 <sup>+0.05</sup> <sub>-0.05</sub>

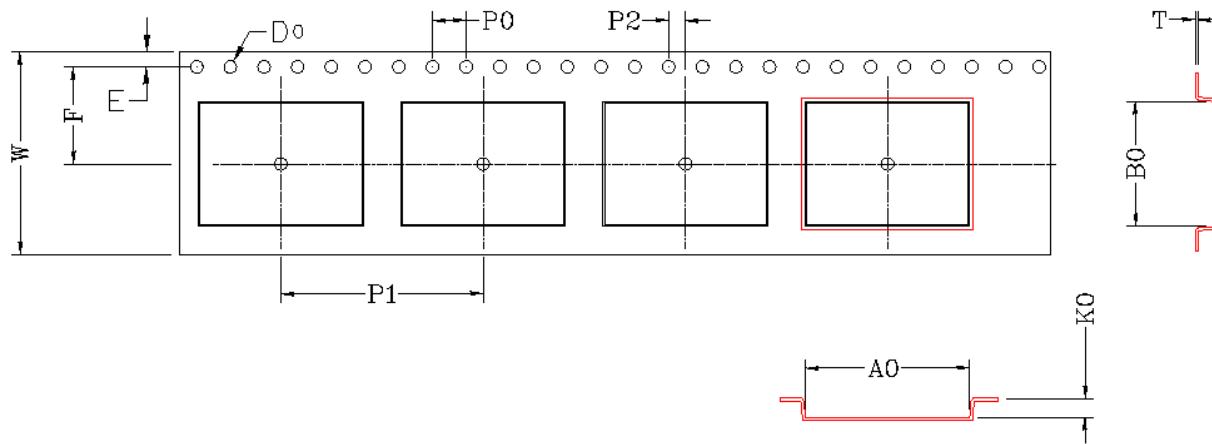
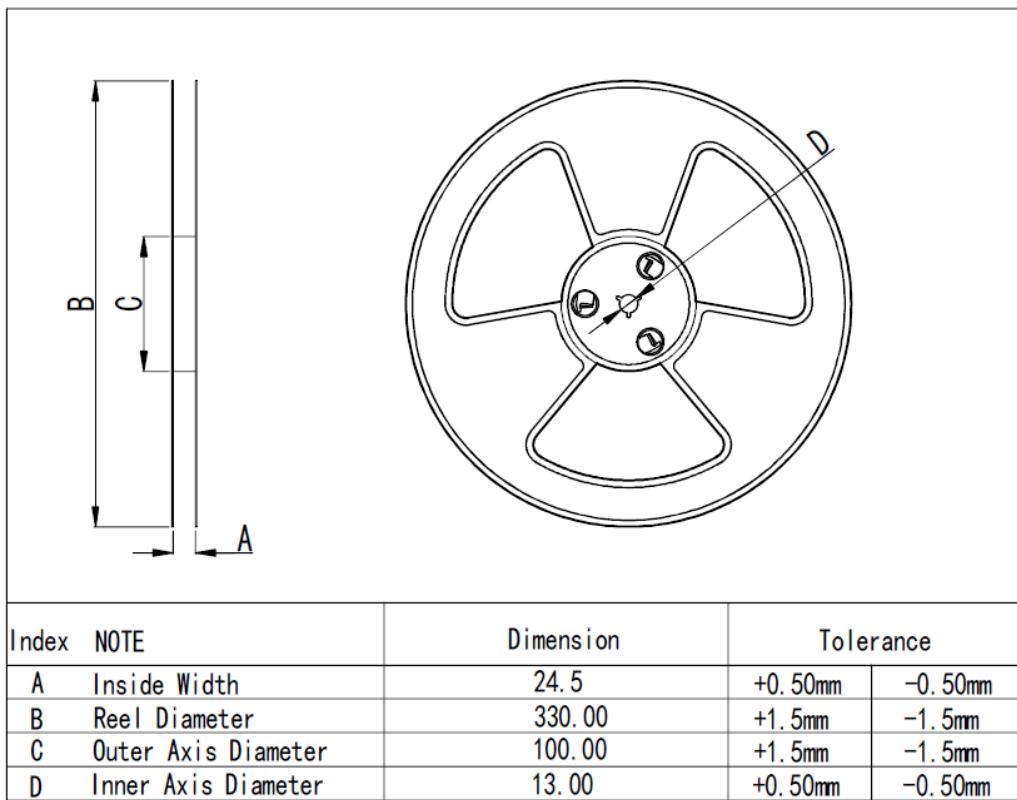


Figure 11 details the orientation of the CYBLE-2X20XX-X1 in the tape as well as the direction for unreeling.

**Figure 11. Component Orientation in Tape and Unreeling Direction (Illustration Only) - TBD**

Figure 12 details reel dimensions used for the CYBLE-2X20XX-X1.

**Figure 12. Reel Dimensions**



The CYBLE-2X20XX-X1 is designed to be used with pick-and-place equipment in an SMT manufacturing environment. The center-of-mass for the CYBLE-2X20XX-X1 is detailed in [Figure 13](#).

**Figure 13. CYBLE-2X20XX-X1 Center of Mass (Seen from Top) - TBD**

## Ordering Information

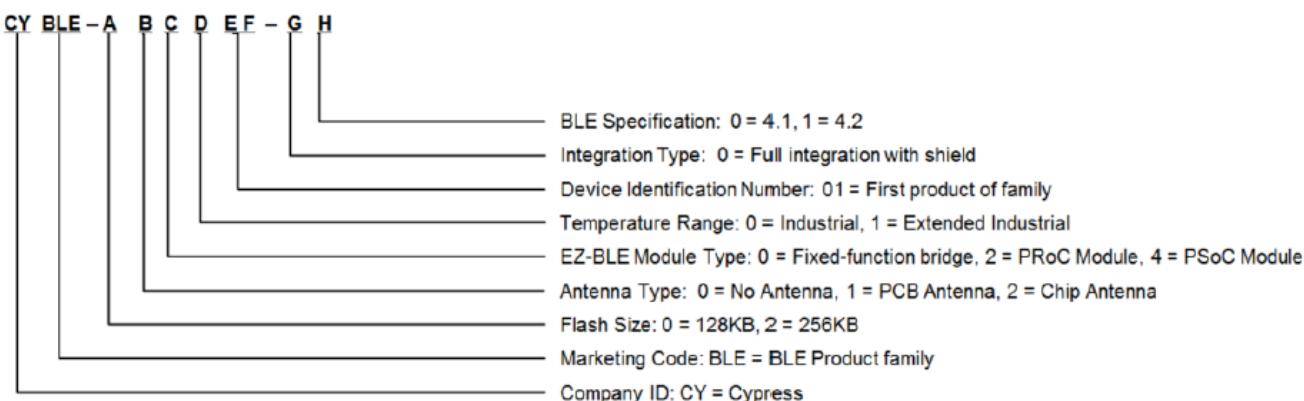
Table 57 lists the CYBLE-2X20XX-X1 part numbers and features.

**Table 57. Ordering Information**

Part Number	CPU Speed (MHz)	Flash Size (KB)	CapSense	SCB	TCPWM	12-Bit SAR ADC	I <sup>2</sup> S	LCD	Package	Packing	Certified
CYBLE-212006-01	48	256	Yes	2	4	1 Msps	Yes	Yes	30-SMT	Tape and Reel	Yes
CYBLE-202007-01	48	256	Yes	2	4	1 Msps	Yes	Yes	30-SMT	Tape and Reel	Yes
CYBLE-202013-11	48	256	Yes	2	4	1 Msps	Yes	Yes	30-SMT	Tape and Reel	No

### Part Numbering Convention

The part numbers are of the form CYBLE-ABCDEF-GH where the fields are defined as follows.



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## Acronyms

**Table 58. Acronyms Used in this Document**

Acronym	Description
BLE	Bluetooth Low Energy
Bluetooth SIG	Bluetooth Special Interest Group
CE	European Conformity
CSA	Canadian Standards Association
EMI	electromagnetic interference
ESD	electrostatic discharge
FCC	Federal Communications Commission
GPIO	general-purpose input/output
IC	Industry Canada
IDE	integrated design environment
KC	Korea Certification
MIC	Ministry of Internal Affairs and Communications (Japan)
PCB	printed circuit board
RX	receive
QDID	qualification design ID
SMT	surface-mount technology; a method for producing electronic circuitry in which the components are placed directly onto the surface of PCBs
TCPWM	timer, counter, pulse width modulator (PWM)
TUV	Germany: Technischer Überwachungs-Verein (Technical Inspection Association)
TX	transmit

## Document Conventions

### Units of Measure

**Table 59. Units of Measure**

Symbol	Unit of Measure
°C	degree Celsius
kV	kilovolt
mA	milliamperes
mm	millimeters
mV	millivolt
µA	microamperes
µm	micrometers
MHz	megahertz
GHz	gigahertz
V	volt

## Document History Page

**Document Title:** CYBLE-212006-01, CYBLE-202007-01, CYBLE-202013-11 EZ-BLE™ PRoC™ 4.2 XR Module  
**Document Number:** 002-09764

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	PRELIM-INARY	MINS	PRELIM-INARY	Preliminary datasheet for CYBLE-212006-01, CYBLE-202007-01 and CYBLE-202013-11 module.

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