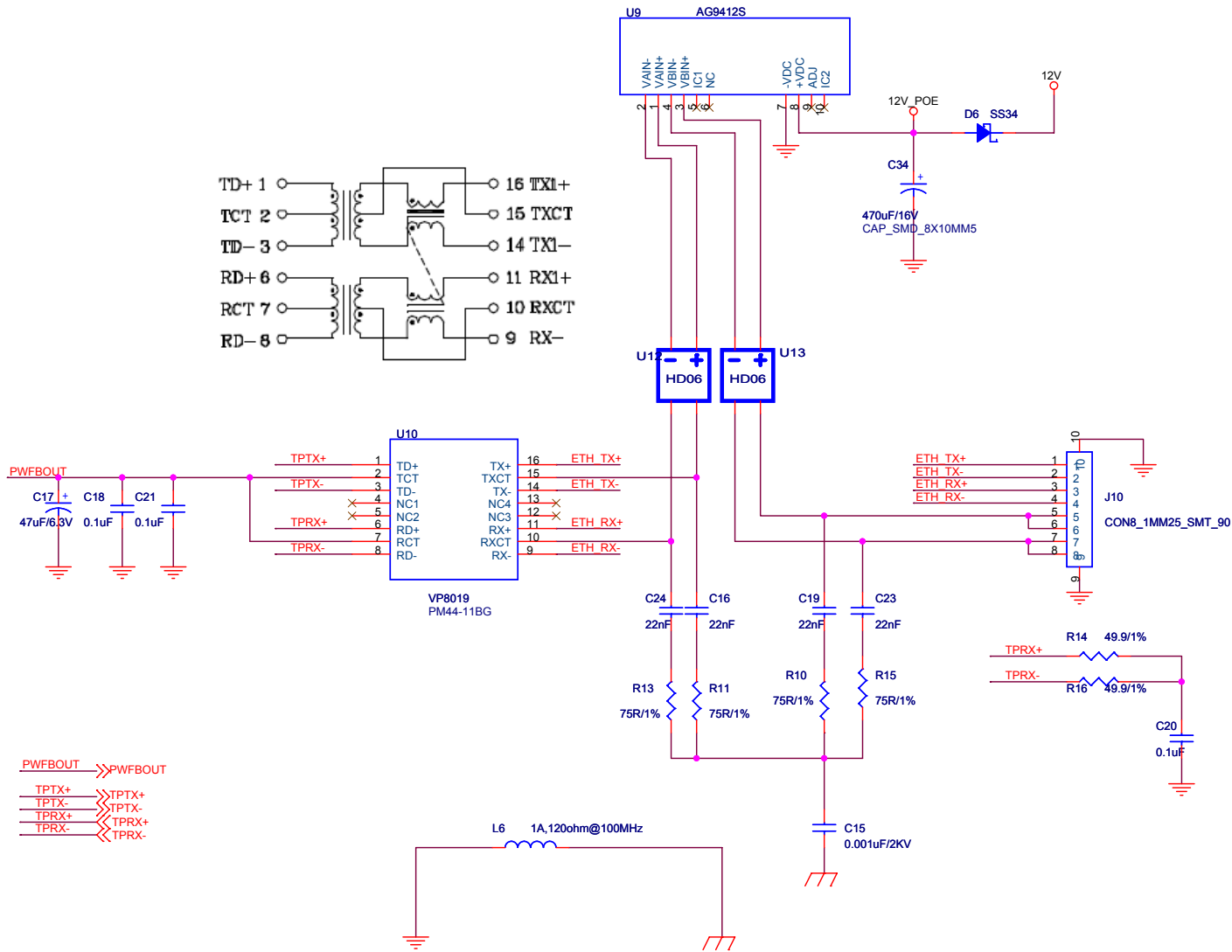


Data code/ Version	Modification
1.0	-First release

Change log:

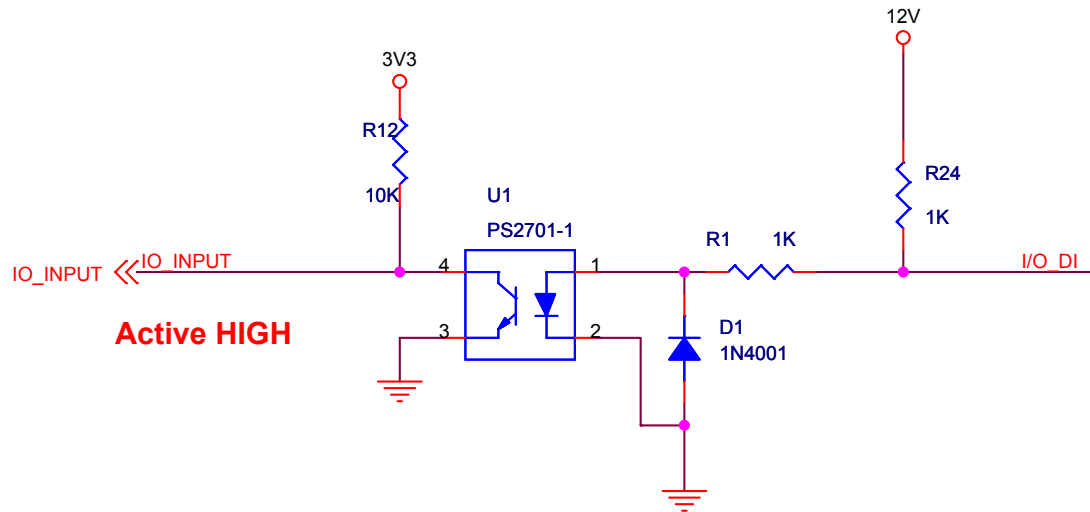
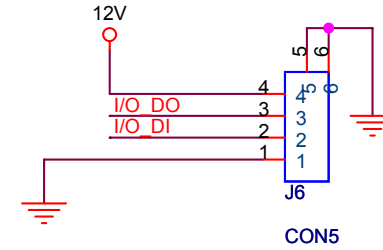
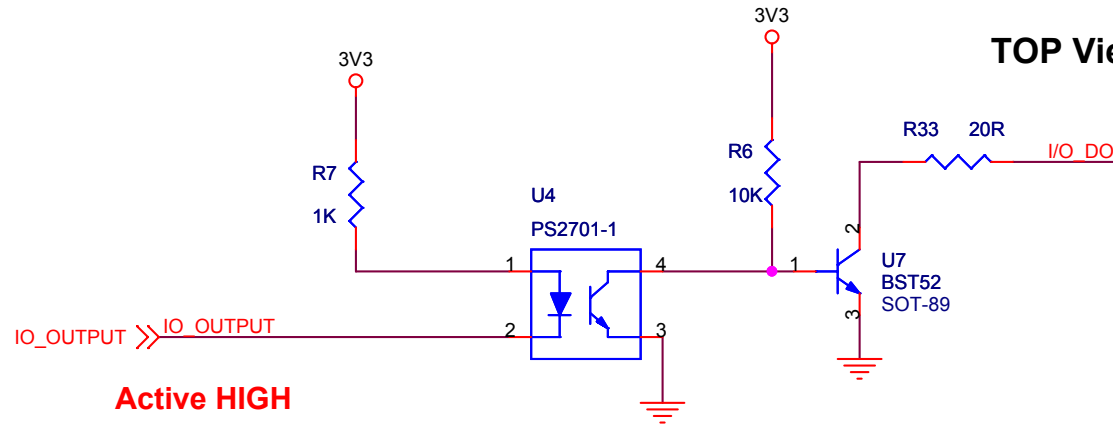
ORANTEK Co.,Ltd		
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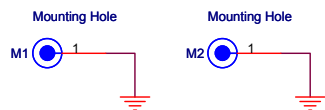
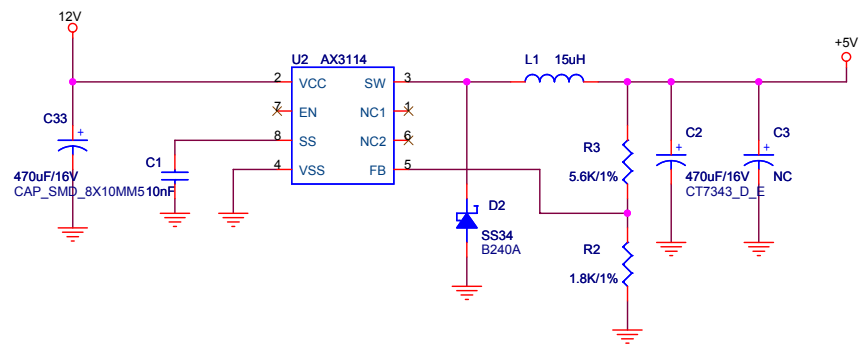
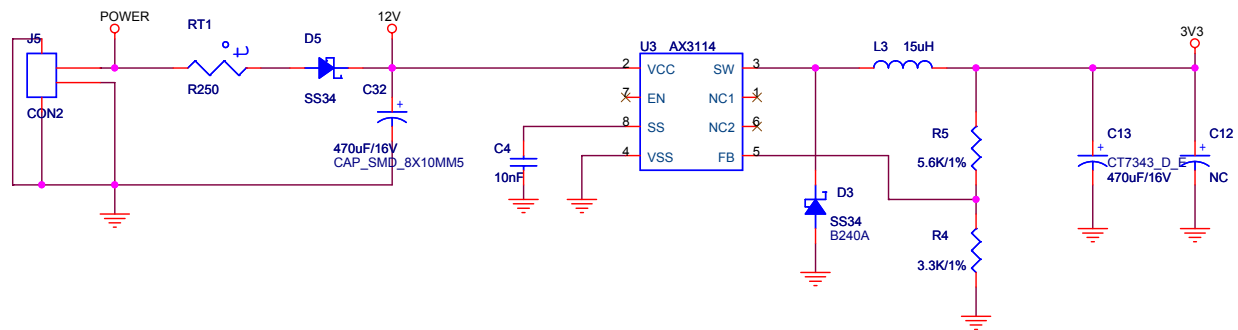
ORANTEK Co.,Ltd

Title		
Network,POE		
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TOP View

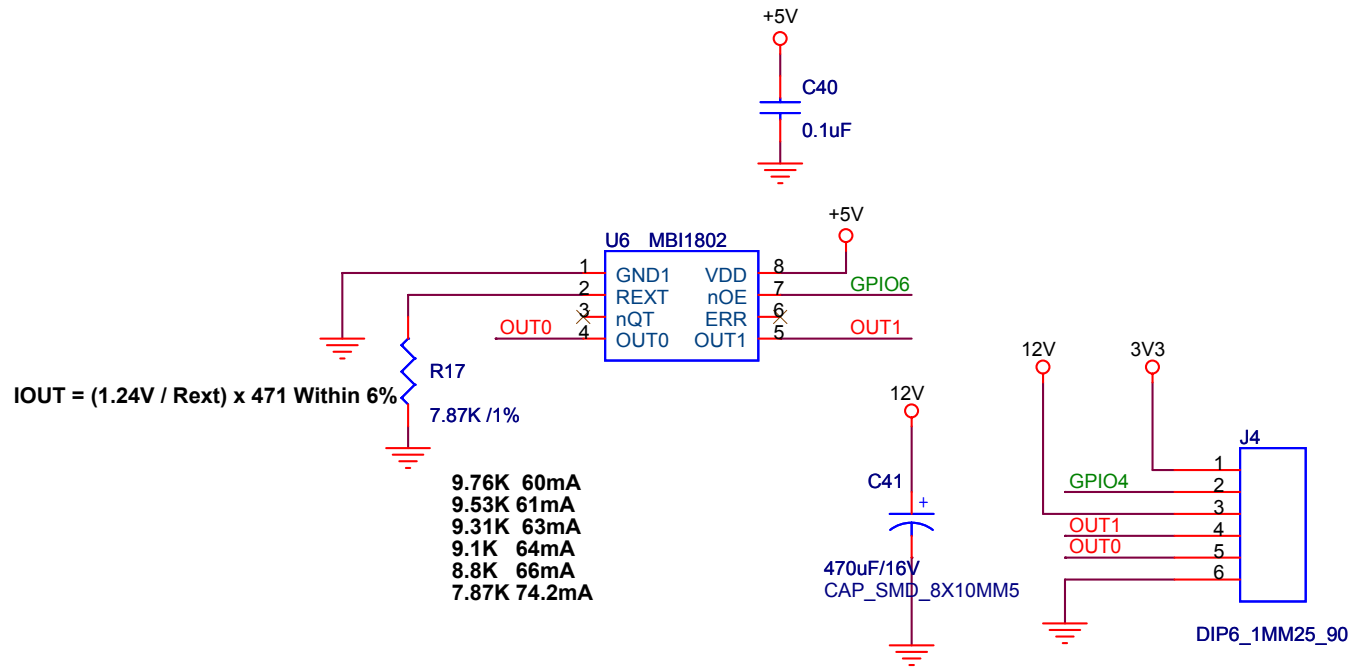


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GPIO4
GPIO6



ORANTEK Co.,Ltd

Title

IRLED

Size

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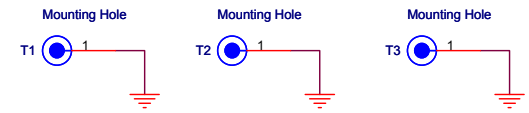
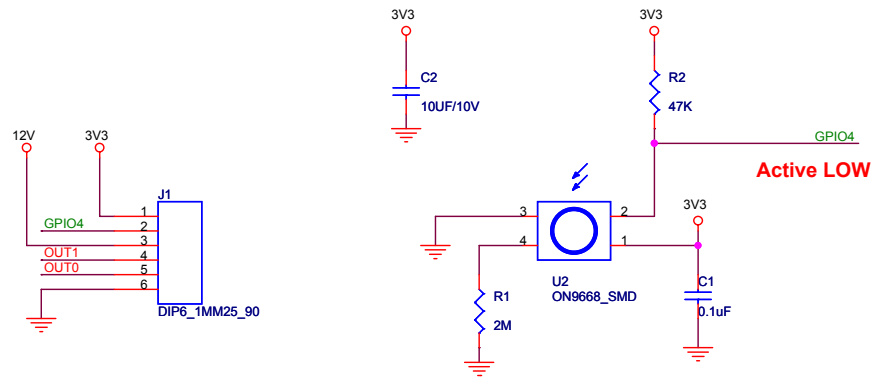
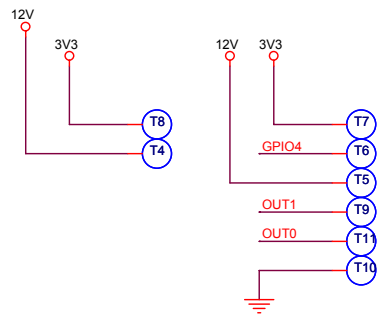
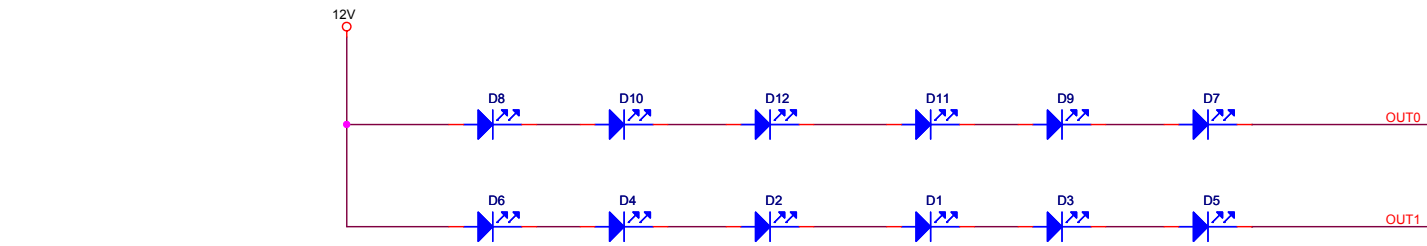
of

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Data code/ Version	Modification

Change log:

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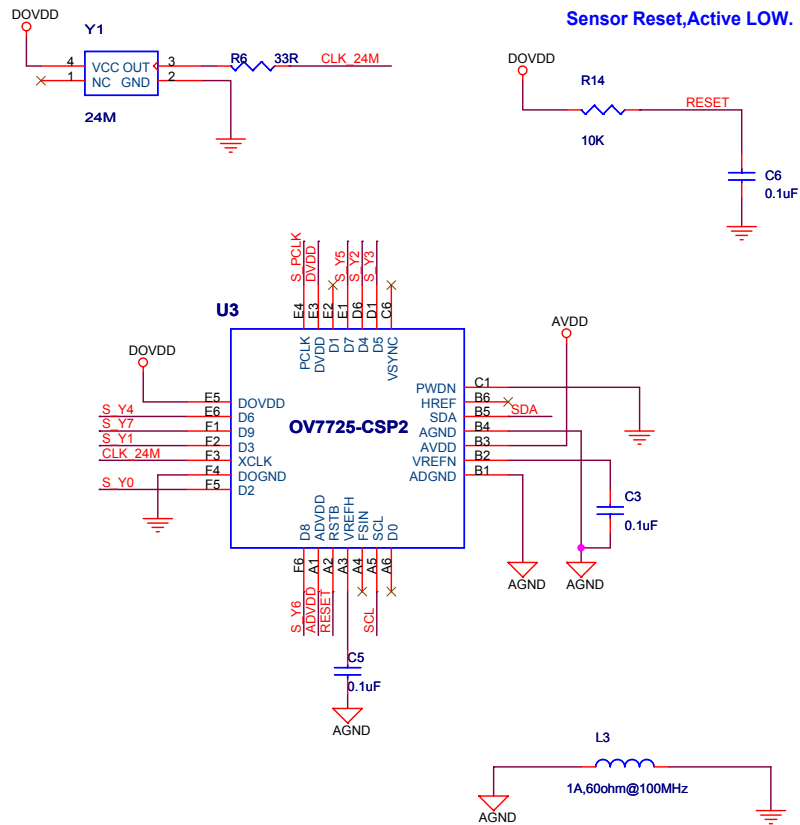


ORANTEK Co.,Ltd			
Title			
IRLED			
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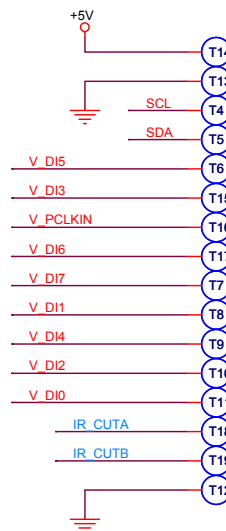
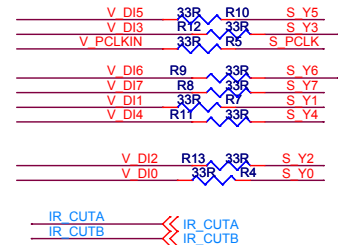
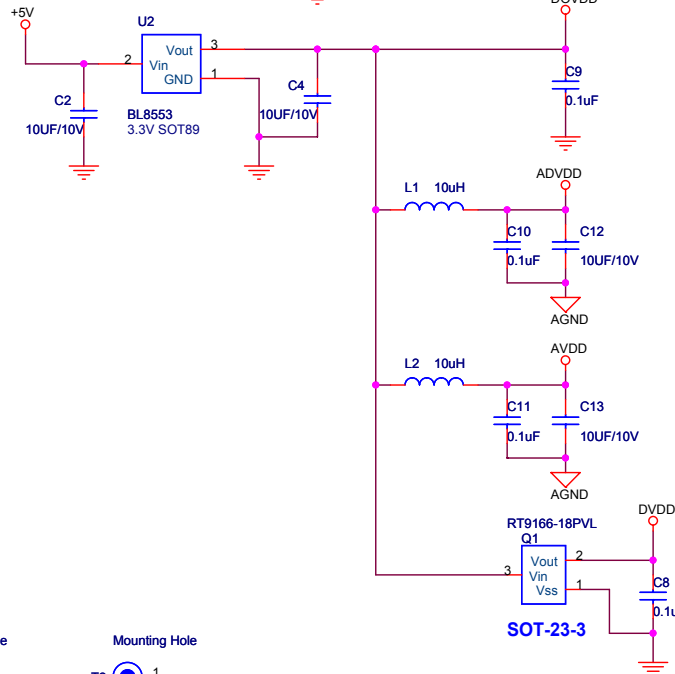
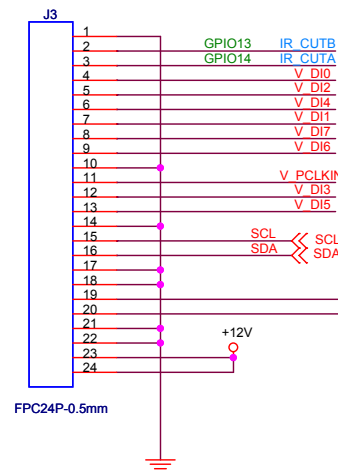
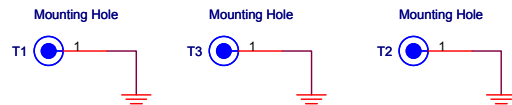
Data code/ Version	Modification
1.0	-First release

Change log:

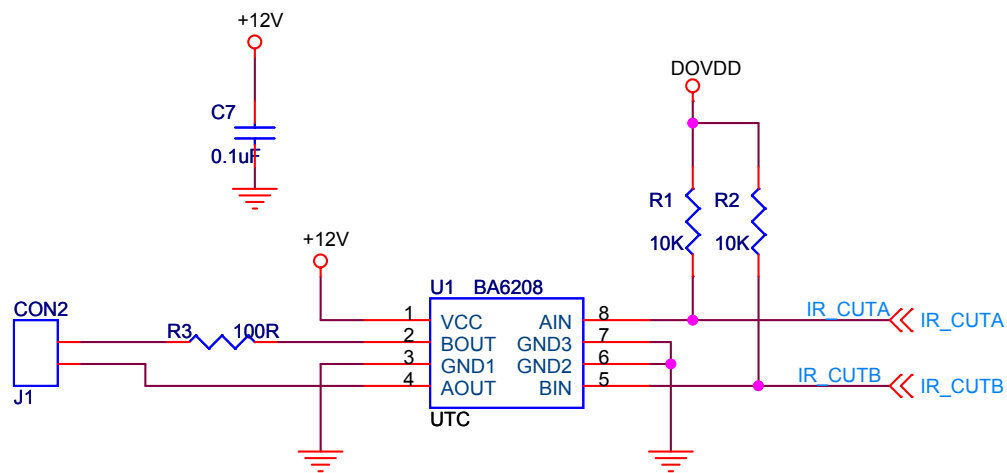
ORANTEK Co.,Ltd		
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Note		
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As most optical assemblies invert and mirror the image, the chip is typically mounted with pins A1 to A6 oriented down on the PCB.



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IR CUT			
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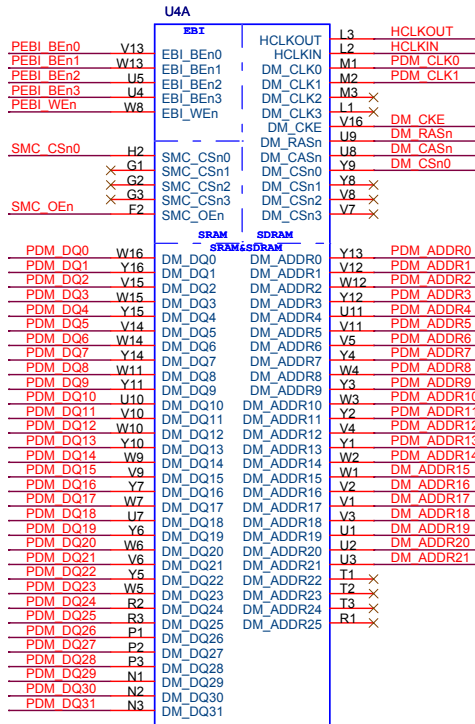
Data code/ Version	Modification
1.0	-First release

Change log:

ORANTEK Co.,Ltd		
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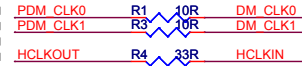
DM_DQ[0..31]  DM_DQ[0..31]

DM_CLK[0..1]  DM_CLK[0..1]
EBI_BEn[0..3]  EBI_BEn[0..3]
EBI_WEn  EBI_WEn
DM_ADDR[0..21]  DM_ADDR[0..21]
DM_CS[0]  DM_CS[0]
DM_RASn  DM_RASn
DM_CASn  DM_CASn
DM_CKE  DM_CKE
SMC_CS[0]  SMC_CS[0]
SMC_OEn  SMC_OEn



FIC8120_TFBGA256

Place near FIC8120



Remove the Series Resistor

PDM_ADDR0	DM_ADDR0	PDM_DQ0	DM_DQ0	PDM_DQ16	DM_DQ16
PDM_ADDR1	DM_ADDR1	PDM_DQ1	DM_DQ1	PDM_DQ17	DM_DQ17
PDM_ADDR2	DM_ADDR2	PDM_DQ2	DM_DQ2	PDM_DQ18	DM_DQ18
PDM_ADDR3	DM_ADDR3	PDM_DQ3	DM_DQ3	PDM_DQ19	DM_DQ19
PDM_ADDR4	DM_ADDR4	PDM_DQ4	DM_DQ4	PDM_DQ20	DM_DQ20
PDM_ADDR5	DM_ADDR5	PDM_DQ5	DM_DQ5	PDM_DQ21	DM_DQ21
PDM_ADDR6	DM_ADDR6	PDM_DQ6	DM_DQ6	PDM_DQ22	DM_DQ22
		PDM_DQ7	DM_DQ7	PDM_DQ23	DM_DQ23

PDM_ADDR7	DM_ADDR7	PDM_DQ8	DM_DQ8	PDM_DQ24	DM_DQ24
PDM_ADDR8	DM_ADDR8	PDM_DQ9	DM_DQ9	PDM_DQ25	DM_DQ25
PDM_ADDR9	DM_ADDR9	PDM_DQ10	DM_DQ10	PDM_DQ26	DM_DQ26
PDM_ADDR10	DM_ADDR10	PDM_DQ11	DM_DQ11	PDM_DQ27	DM_DQ27
PDM_ADDR11	DM_ADDR11	PDM_DQ12	DM_DQ12	PDM_DQ28	DM_DQ28
PDM_ADDR12	DM_ADDR12	PDM_DQ13	DM_DQ13	PDM_DQ29	DM_DQ29
PDM_ADDR13	DM_ADDR13	PDM_DQ14	DM_DQ14	PDM_DQ30	DM_DQ30
PDM_ADDR14	DM_ADDR14	PDM_DQ15	DM_DQ15	PDM_DQ31	DM_DQ31

PSMC_OEn	SMC_OEn
PDM_RASn	DM_RASn
PDM_CASn	DM_CASn
PEBI_WEn	EBI_WEn
PDM_CKE	DM_CKE

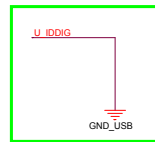
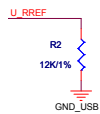
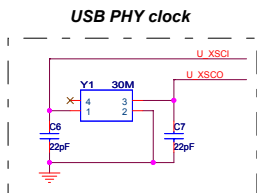
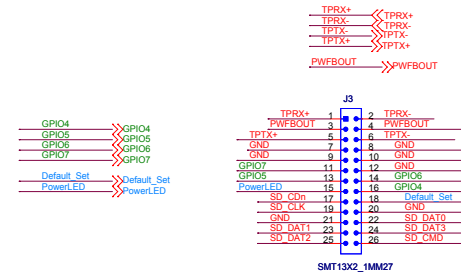
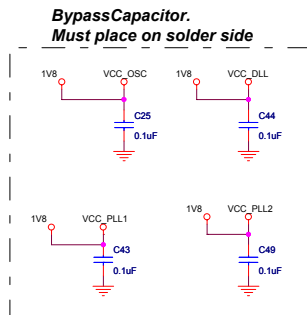
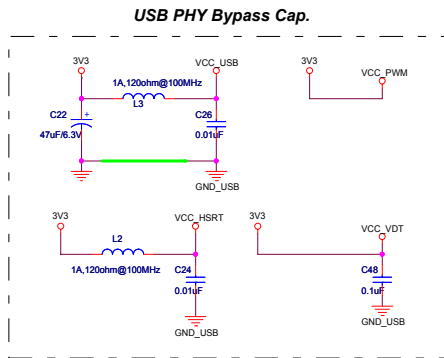
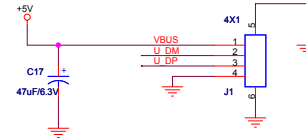
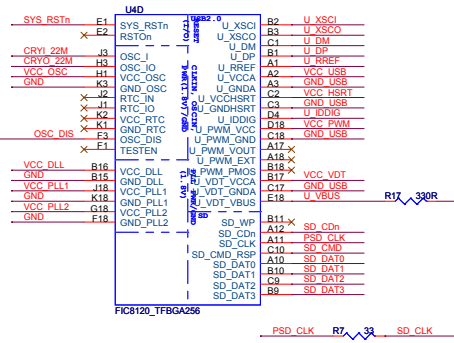
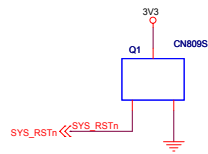
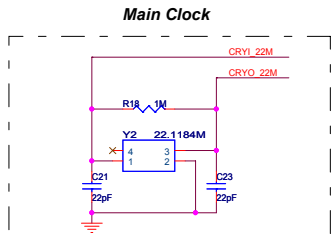
PDM_CS[0]	DM_CS[0]
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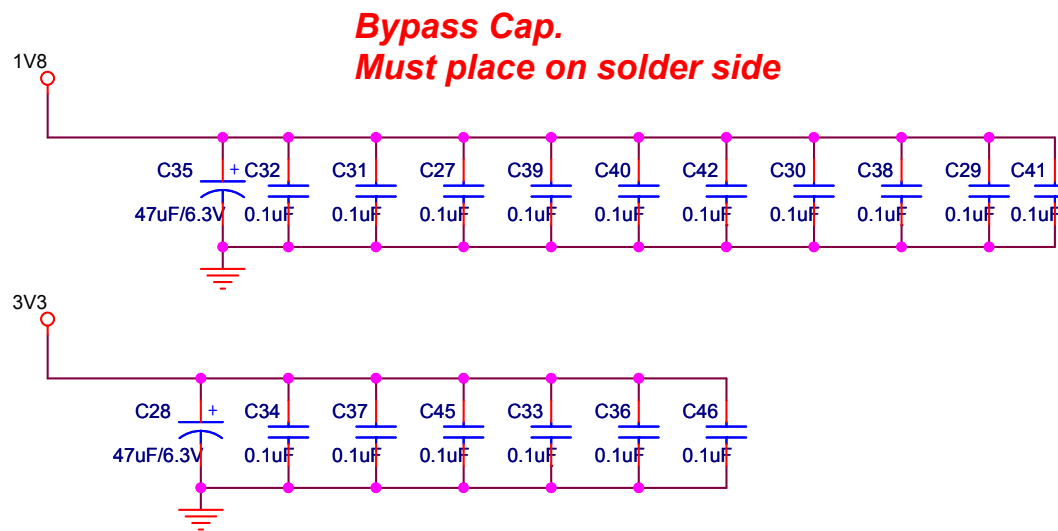
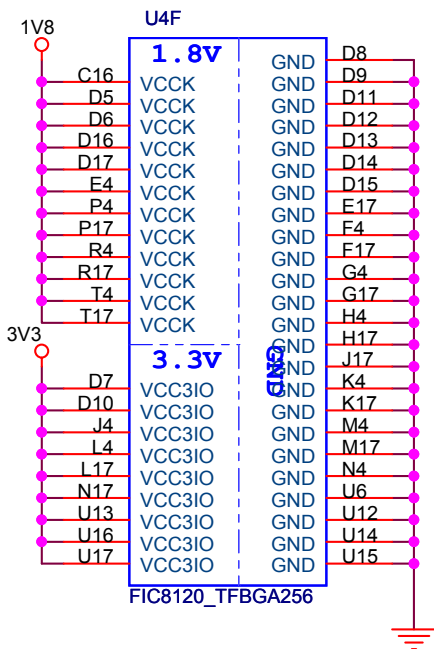
PSMC_CS[0]	SMC_CS[0]
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PEBI_BEn0	EBI_BEn0
PEBI_BEn1	EBI_BEn1
PEBI_BEn2	EBI_BEn2
PEBI_BEn3	EBI_BEn3

ORANTEK Co.,Ltd

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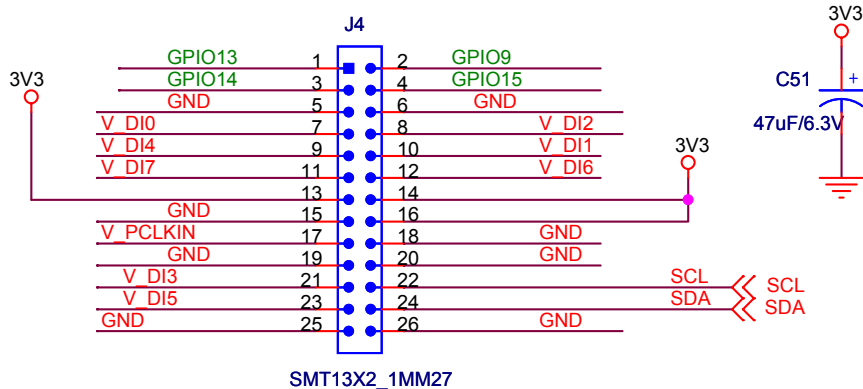
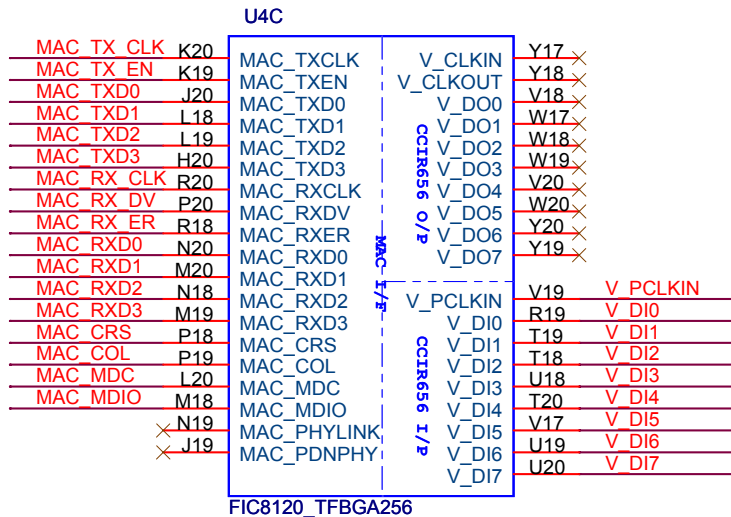




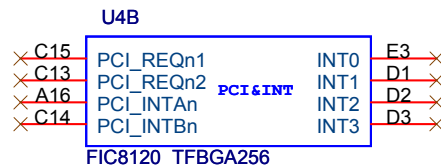
ORANTEK Co.,Ltd		
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MAC_TX_CLK >> MAC TX CLK
 MAC_TX_EN >> MAC TX EN
 MAC_TXD[0..3] >> MAC_TXD[0..3]

MAC_RX_CLK >> MAC RX CLK
 MAC_RX_DV >> MAC RX DV
 MAC_RX_ER >> MAC RX ER
 MAC_RXD[0..3] >> MAC_RXD[0..3]
 MAC_CRD >> MAC CRS
 MAC_COL >> MAC COL
 MAC_MDC >> MAC MDC
 MAC_MDIO >> MAC MDIO



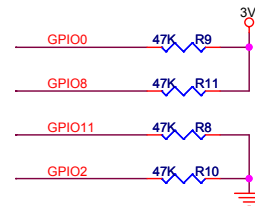
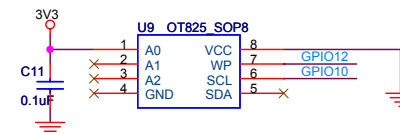
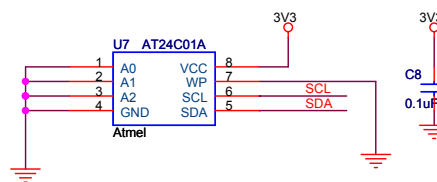
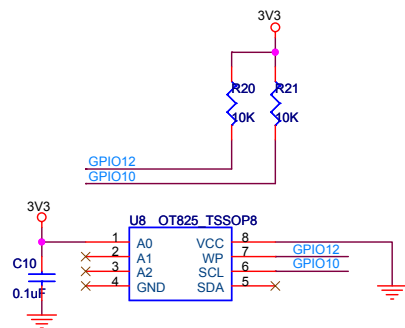
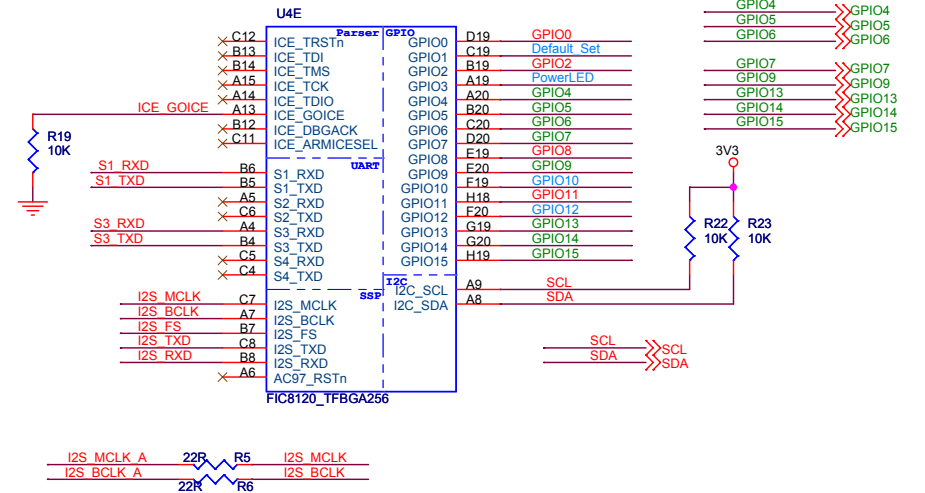
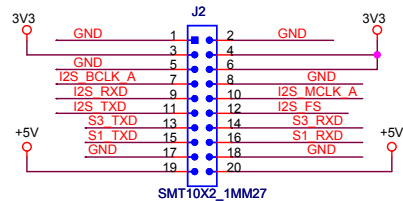
External devices interrupt input. Active high.
 (internal pull-down)



GPIO9 >> GPIO9
 GPIO13 >> GPIO13
 GPIO14 >> GPIO14
 GPIO15 >> GPIO15

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Title		
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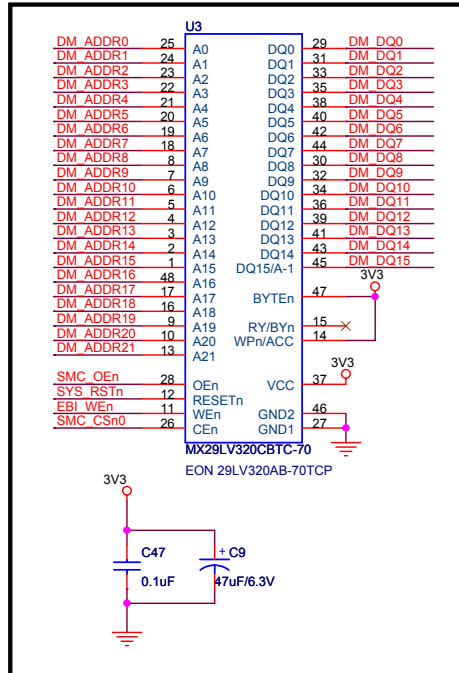


GPIO[11] Timer test. Should be pull-low in normal use.
 GPIO[8] CPU operating mode. 0=sync mode, 1=asyn mode
 At-speed testing use sync mode, but normal operation use asyn mode.
 Should be pull-high in normal use.
 GPIO[2] Bypass PLL or not. IC Tester use this jumper setting.
 Should be pull-low in normal use.
 GPIO[0] Define 8-bit or 16-bit booting.
 pull-low: 8-bit booting pull-high: 16-bit booting

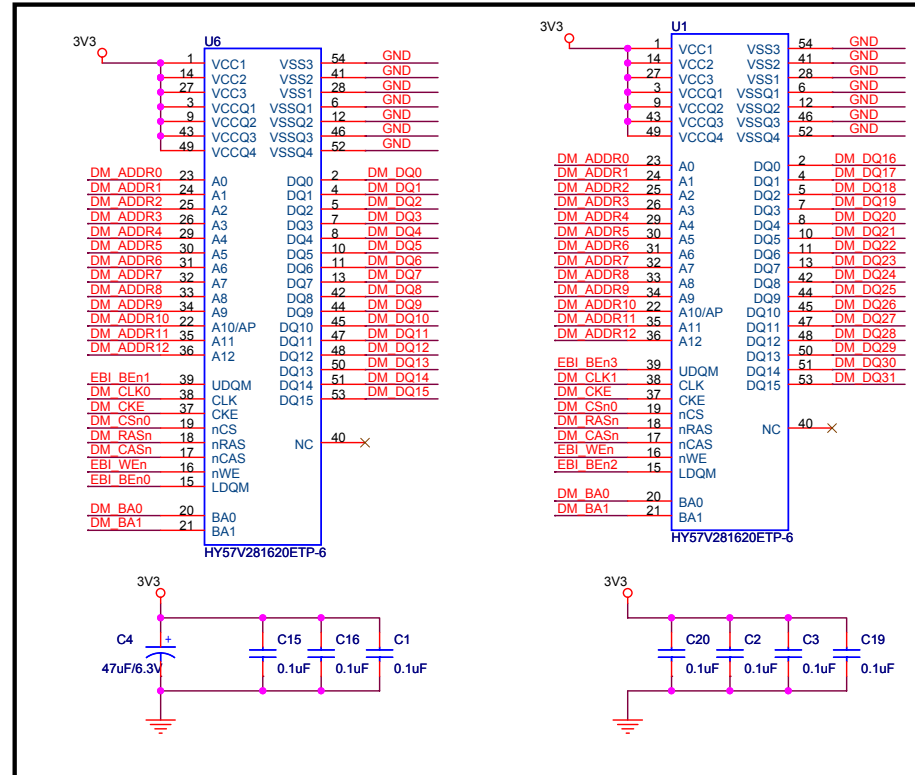
DM_ADDR[0..21] >> DM_ADDR[0..21]
 DM_DQ[0..31] << DM_DQ[0..31]
 EBI_BEn[0..3] >> EBI_BEn[0..3]
 EBI_WEn >> EBI_WEn
 DM_CSn0 >> DM_CSn0
 DM_RASn >> DM_RASn
 DM_CASn >> DM_CASn
 DM_CLK[0..1] >> DM_CLK[0..1]
 DM_CKE >> DM_CKE
 SMC_CSn0 >> SMC_CSn0
 SMC_OEn >> SMC_OEn
 SYS_RSTn >> SYS_RSTn

DM_ADDR13 DM_BA0
 DM_ADDR14 DM_BA1

On Board Flash (2Mx16)



On Board SDRAM(8Mx16)x2



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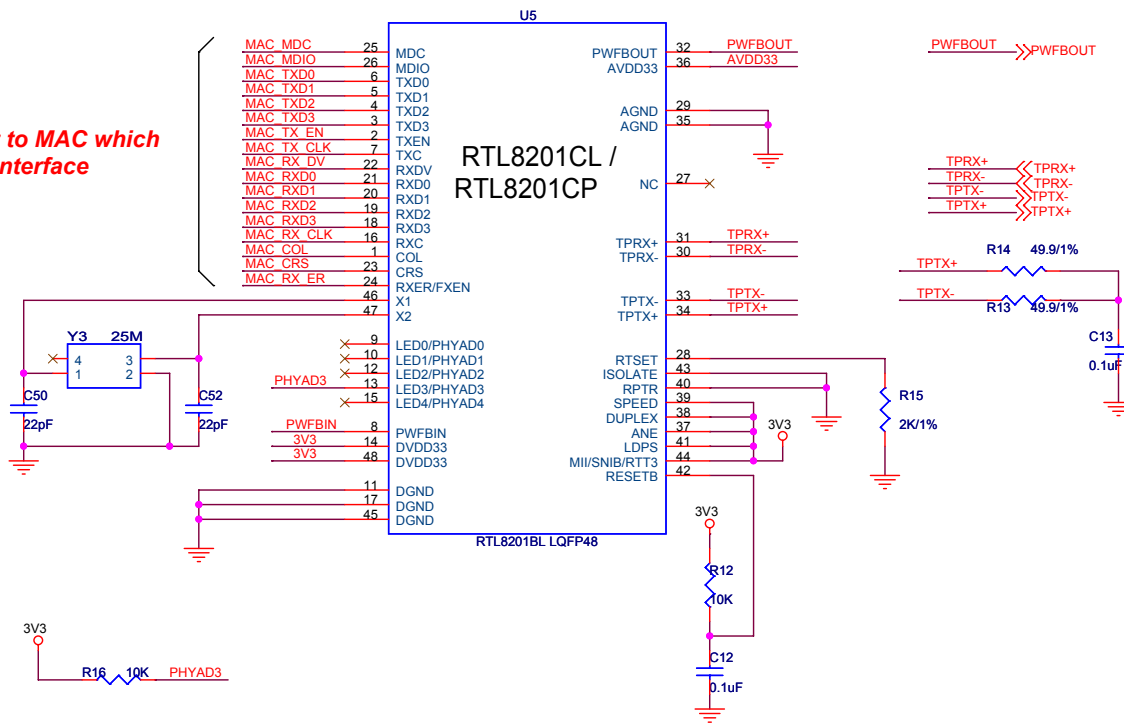
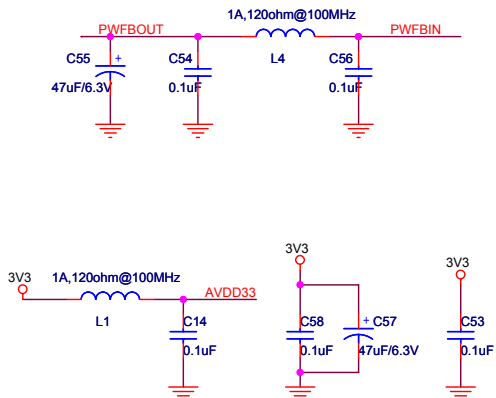
Title		
Memory		
Size	Document Number	Rev
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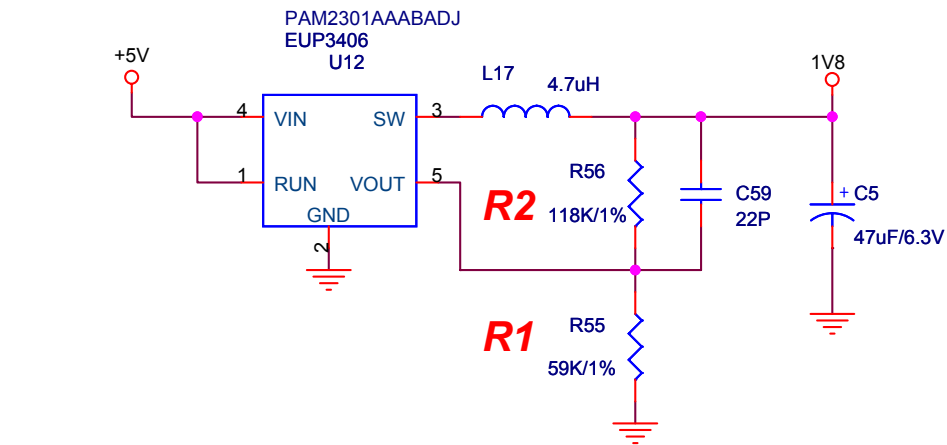
MAC_RXD[0..3] << MAC_RXD[0..3]
 MAC_RX_CLK << MAC_RX_CLK
 MAC_RX_DV << MAC_RX_DV
 MAC_RX_ER << MAC_RX_ER

MAC_CRS << MAC_CRS
 MAC_COL << MAC_COL

MAC_TXD[0..3] >> MAC_TXD[0..3]
 MAC_TX_CLK << MAC_TX_CLK
 MAC_TX_EN >> MAC_TX_EN

Connect to MAC which has MII interface





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