

# CZC Digital technologies Co.,LTD

Board name: Mother Board Schematic

Project name: **T9**

Version: VerB

Start Date:May 7,2008

VerA Release Data:

1. System Block Diagram & Schematic page description;
2. Power Block Diagram & Discription;
3. Annotations & information;
4. Schematic modify Item and history;
5. Power on & off Sequence;
6. ACPI Mode Switch Timings;
7. Power On Sequence Map;
8. CLOCK Distribution;

Hardware drawing by:

\_\_\_\_\_

Hardware check by:

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EMI Check by:

\_\_\_\_\_

Power drawing by:


\_\_\_\_\_

Power check by:

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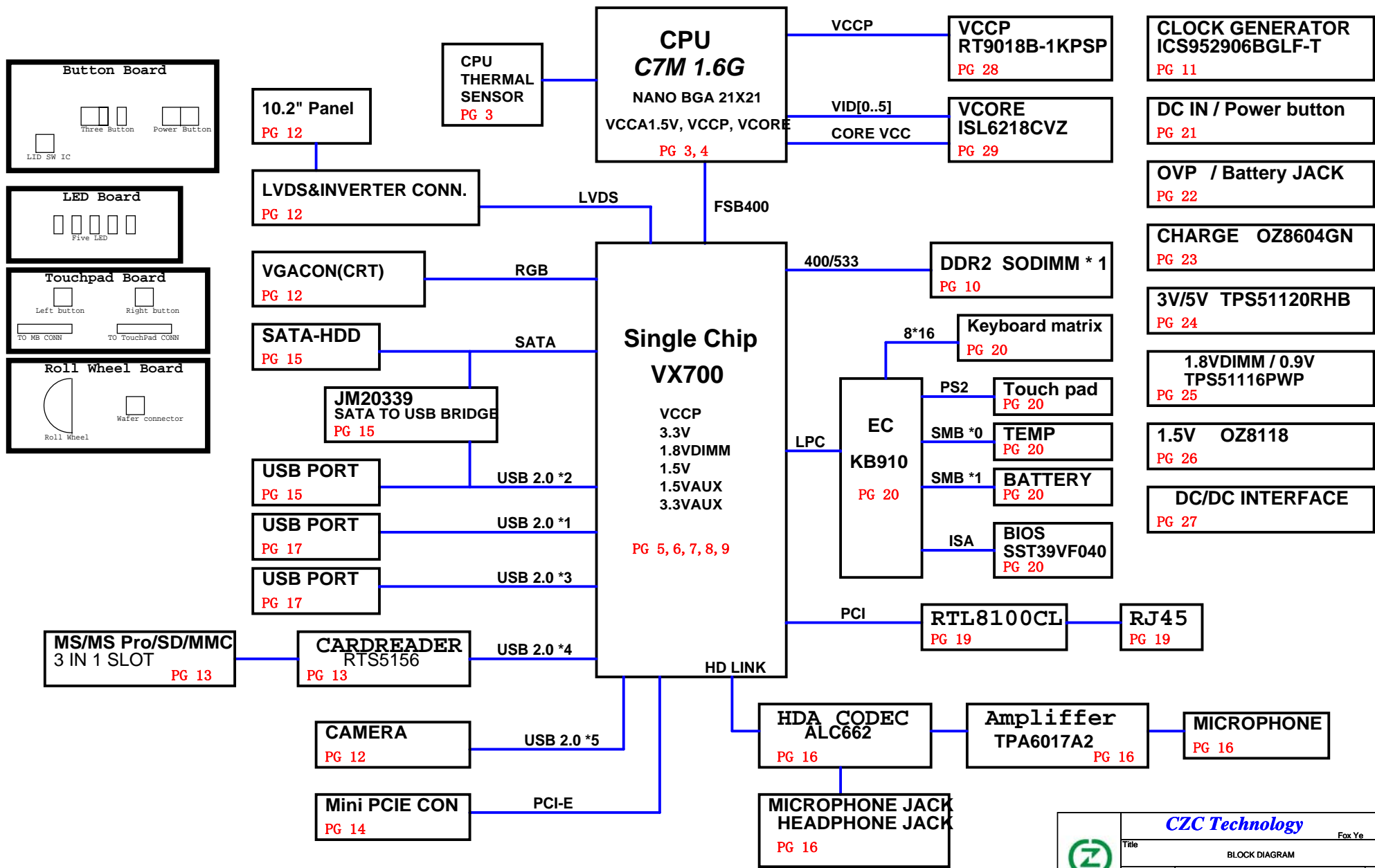
Manager Sign by:

\_\_\_\_\_

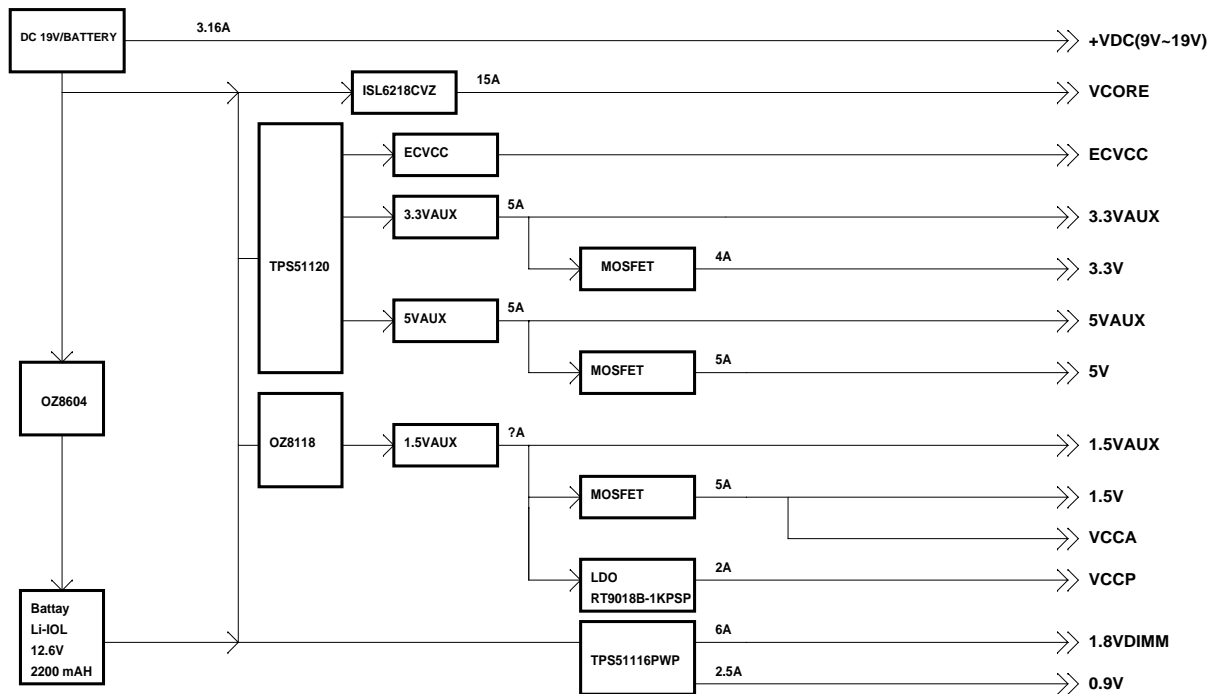
	<b>CZC Technology</b>		
	Title BLOCK DIAGRAM		
	Size A4	Project Name T9	Rev B
	Date: Wednesday, August 13, 2008		Sheet 0 of 42

# Porject Name: NVX700\_T9

## 1. System Block Diagram & Schematic page description;



## 2. Power Block Diagram & Discription:

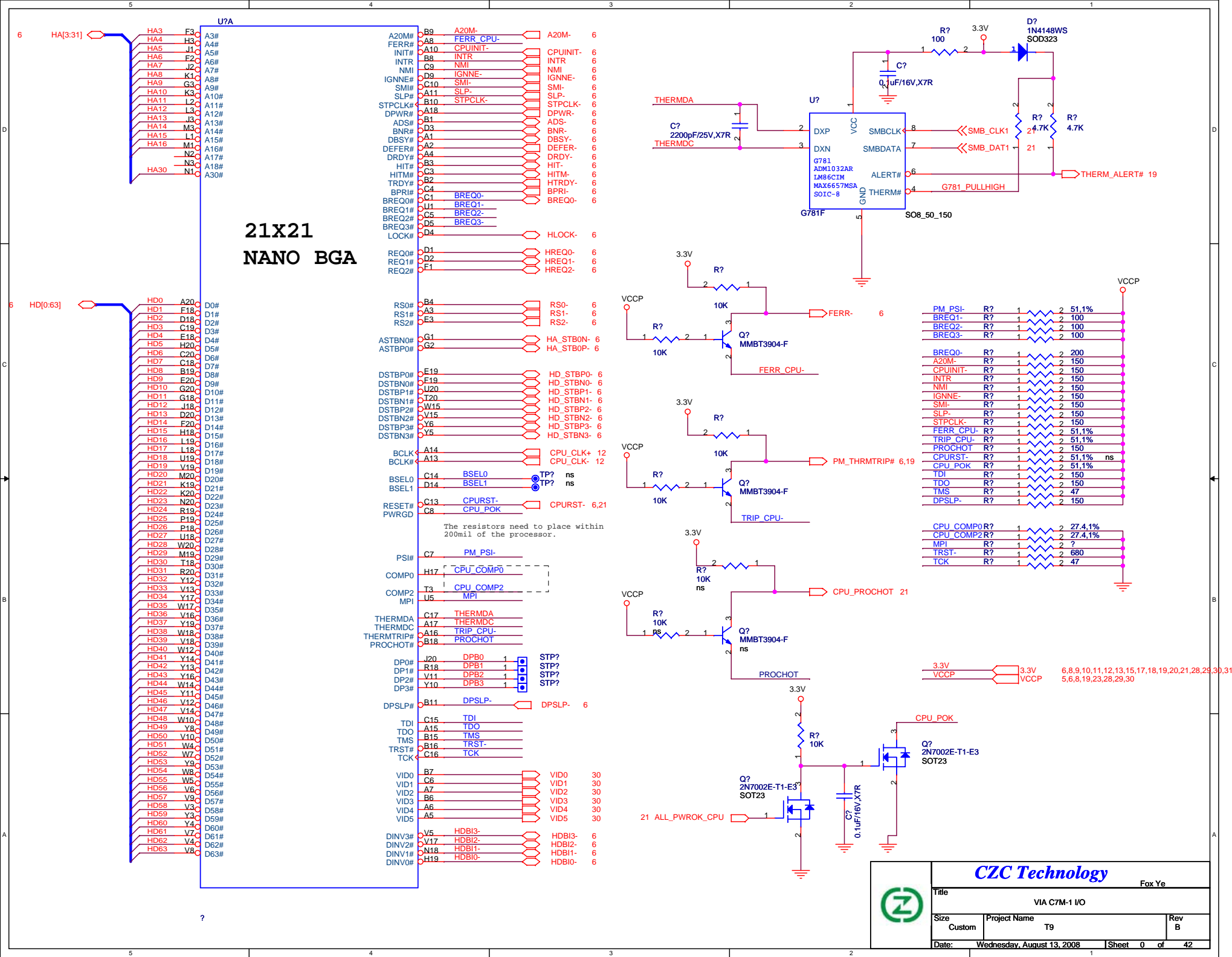


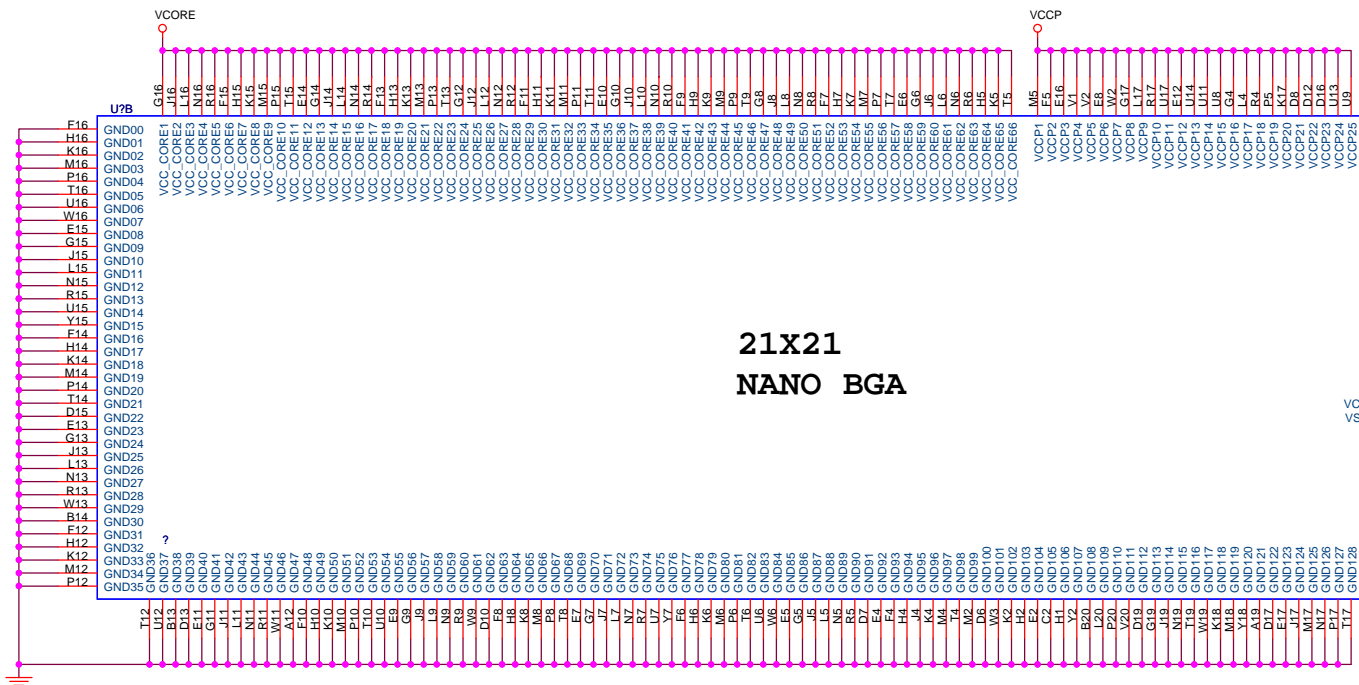
S0/S1	S3	S4	S5	DEVICE	MAX Power consumption
X	X	X	X		
X				CPU	
X	X	X	X	EC	
X	X	X	X	VX700	
X				VX700,mini PCI_E, PCI LAN ICS952906,LCD,Audio	
X	X	X	X	CAMERA,USB	
X				CARDREADER,PANEL, SATA,AUDIO,CPU FAN	
X	X	X	X	VX700	
X				VX700	
X				CPU	
X				CPU,VX700	
X	X			VX700,DDR2 SODIMM x1	
X				DDR2 SODIMM x1	

VX700

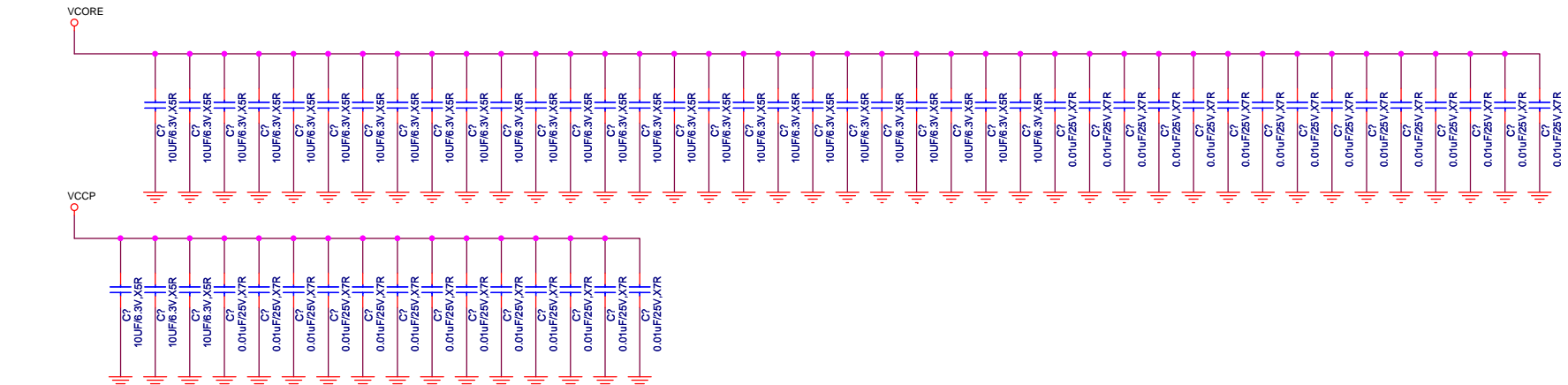
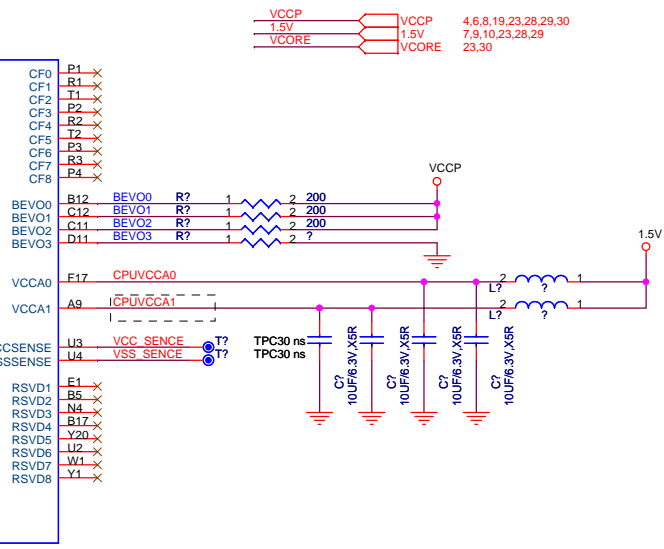
VIA C7M  
Vcore:0.724V-1.146V,15A,S0  
VCCP:1.05V, A,S0  
VCCA:1.5V,156mA,S0

VccCORE VREG	Vccp/VccGMCH VREG	DDR11 VREG	2.5 VREG	V1.5 VREG	V3.3 VREG
0.724V-1.146V,	1.05V +/-3%	1.8V/0.9V	2.5V +/-5%	1.5V +/-3%	3.3V +/-5%





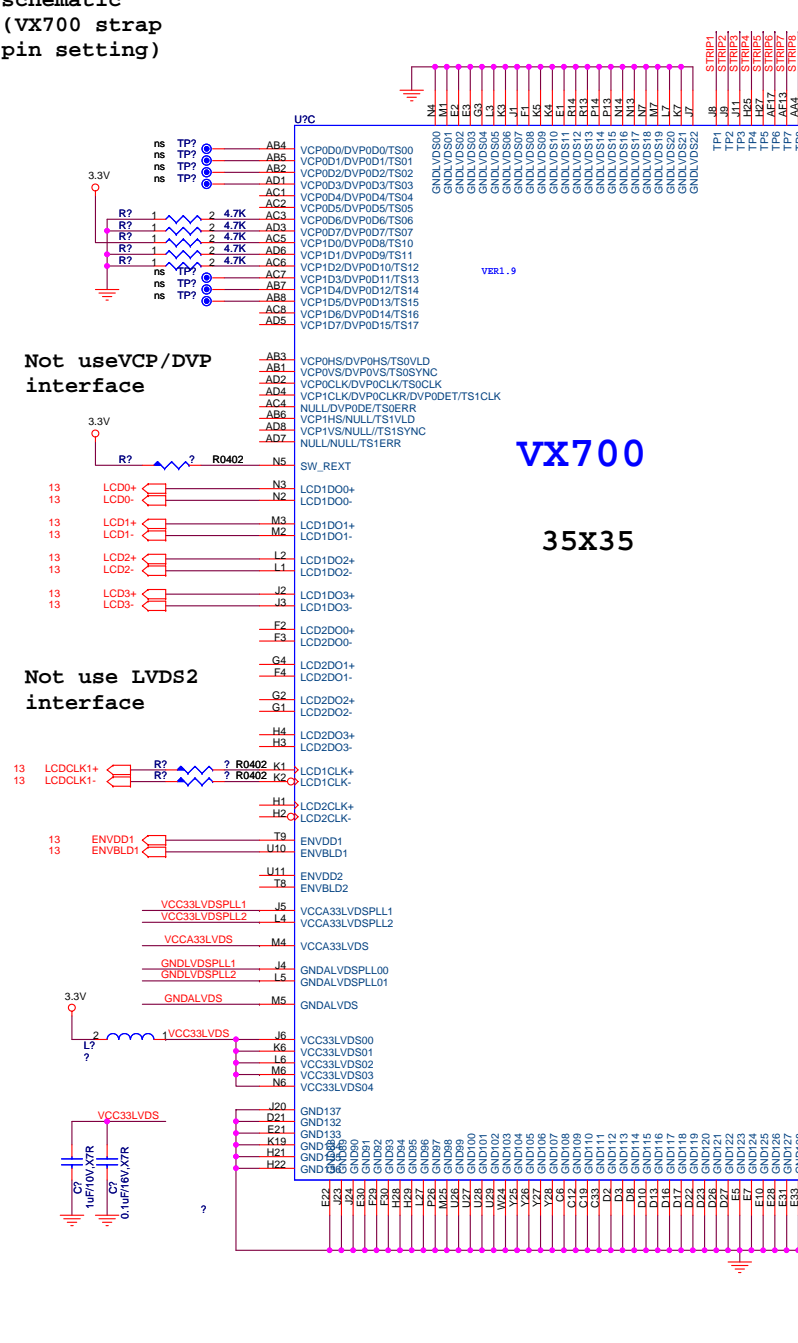
21X21  
NANO BGA







For VIA suggest  
schematic  
(VX700 strap  
pin setting)

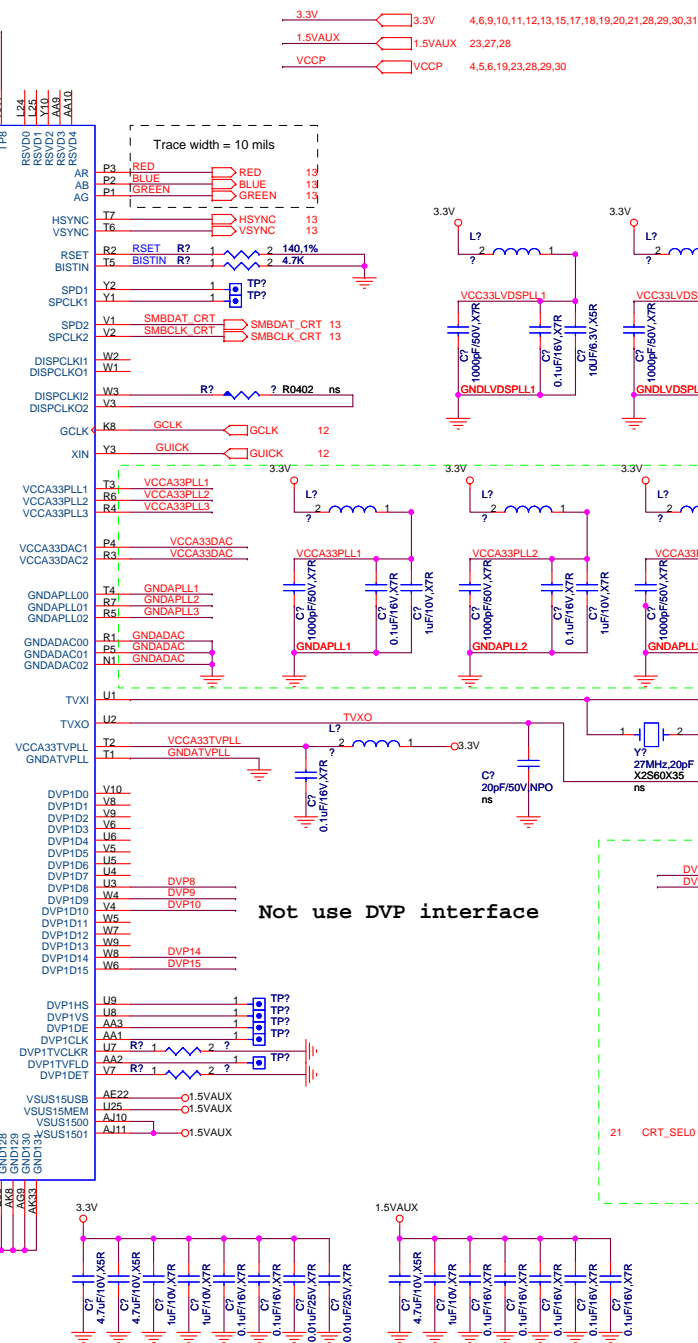


Not use VCP/DVP  
interface

Not use LVDS2  
interface

**VX700**

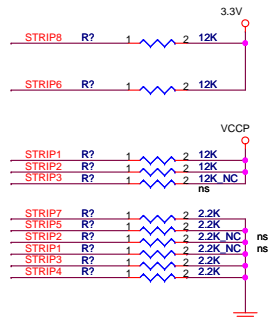
**35x35**



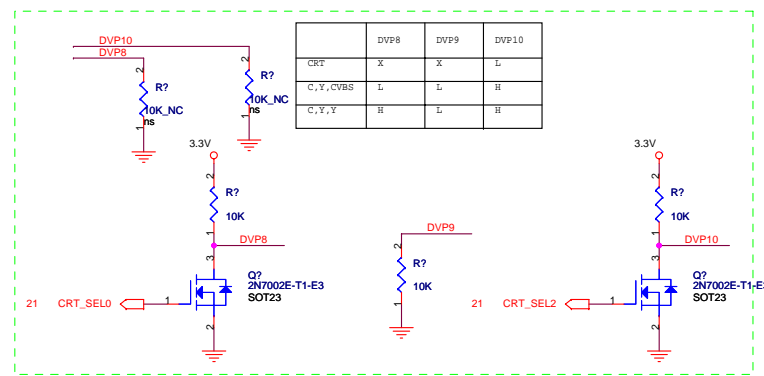
Not use DVP interface

	STRIP4	STRIP3	STRIP5	STRIP6	STRIP7	STRIP8
DESCRIPTION	GTL FULL	IO QUEUE DEPTH	RCPU BUS	P4 or V4	64/32bit Mode	MEM TYPE
LEVEL H	NO FULL	1 LEVEL	C3	V4	HD32bit	DDR2
LEVEL L	FULL	8 LEVEL	P4 or V4	P4	HD64bit	DDR1


STRIP1	STRIP2	STATE
LOW	LOW	100MHz
LOW	HIGH	Reserved
HIGH	LOW	133MHz
HIGH	HIGH	Auto Mode



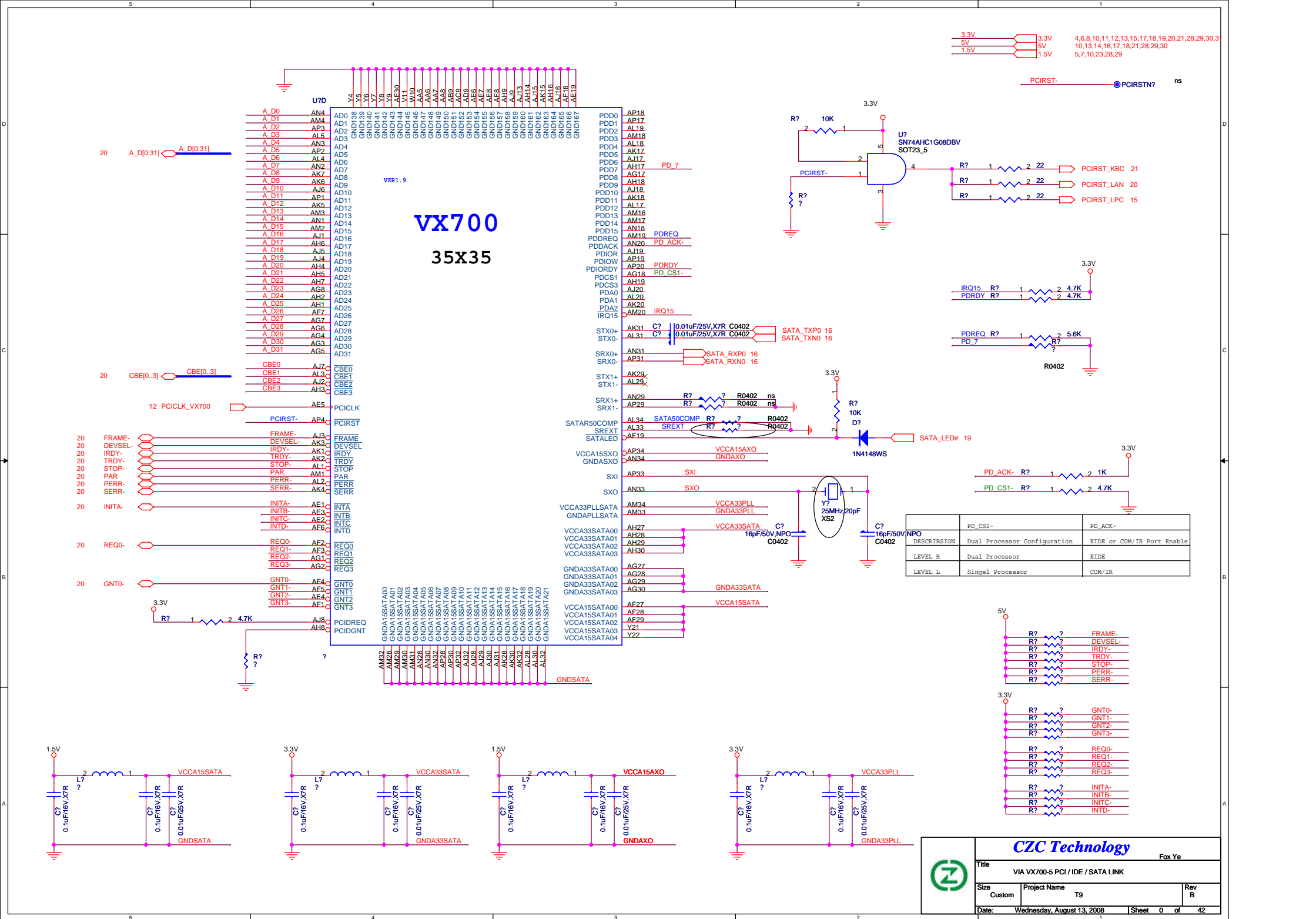
DVP14	DVP15	
LOW	LOW	Two Single LVDS Channel
HIGH	LOW	Reserved
LOW	HIGH	One Dual LVDS Channel
HIGH	HIGH	Only DWI



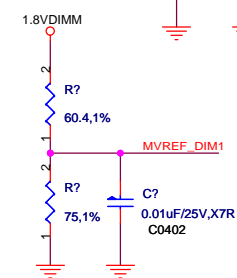
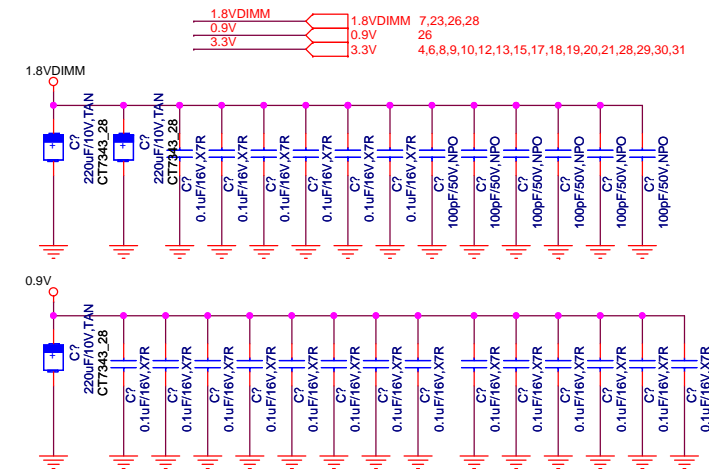
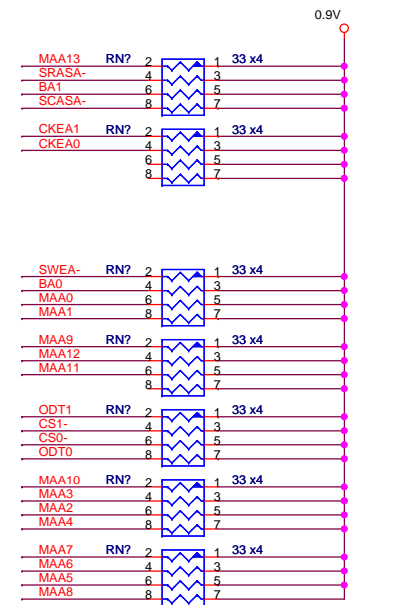
	DVP8	DVP9	DVP10
CRT	X	X	L
C,Y,CVBS	L	L	H
C,Y,Y	H	L	H

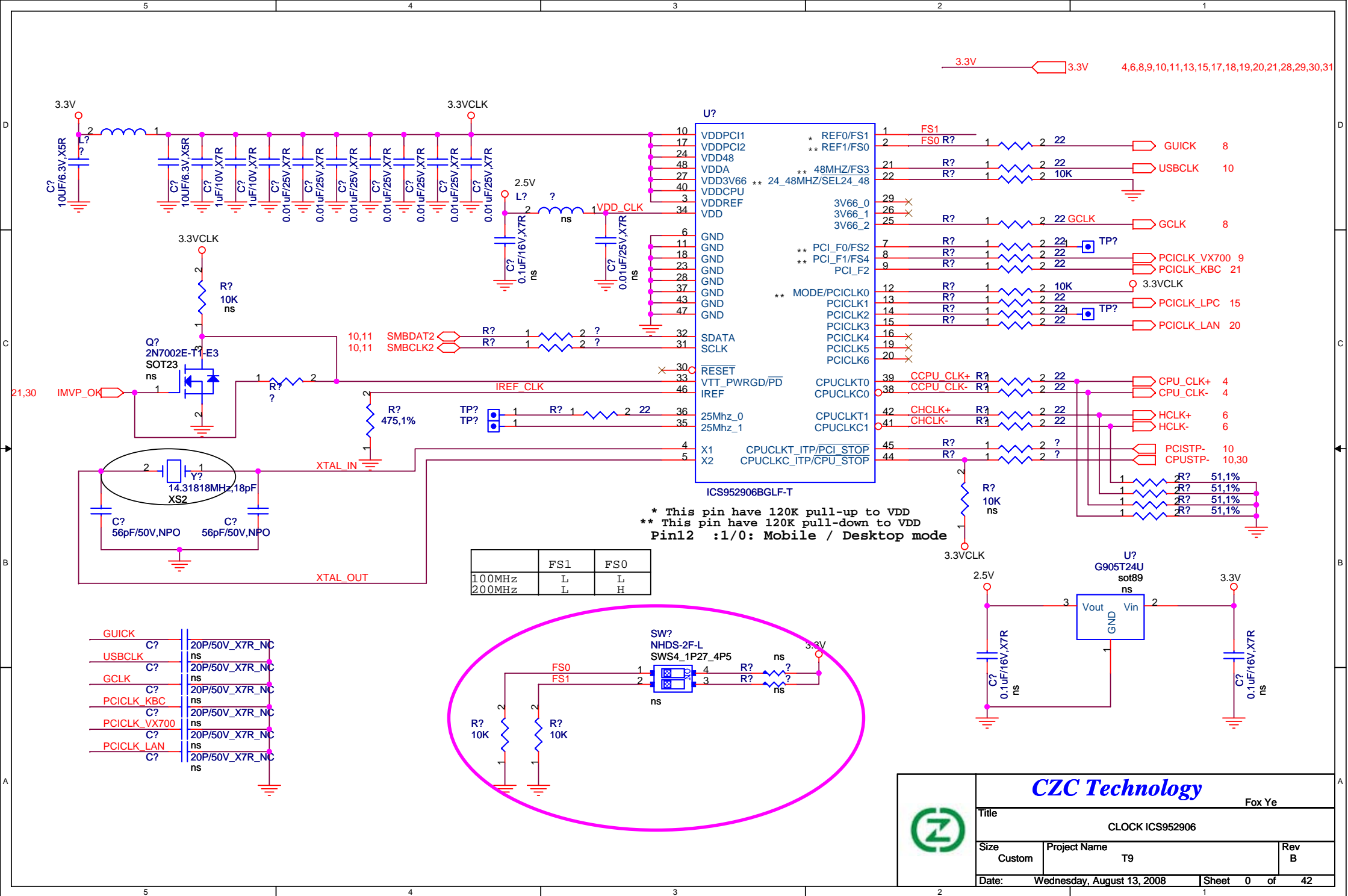
	<b><i>CZC Technology</i></b>			Fox Ye
	Title			
	VIA VX700-3 VGA LINK			
	Size	Project Name	Rev	
Custom	T9	B		
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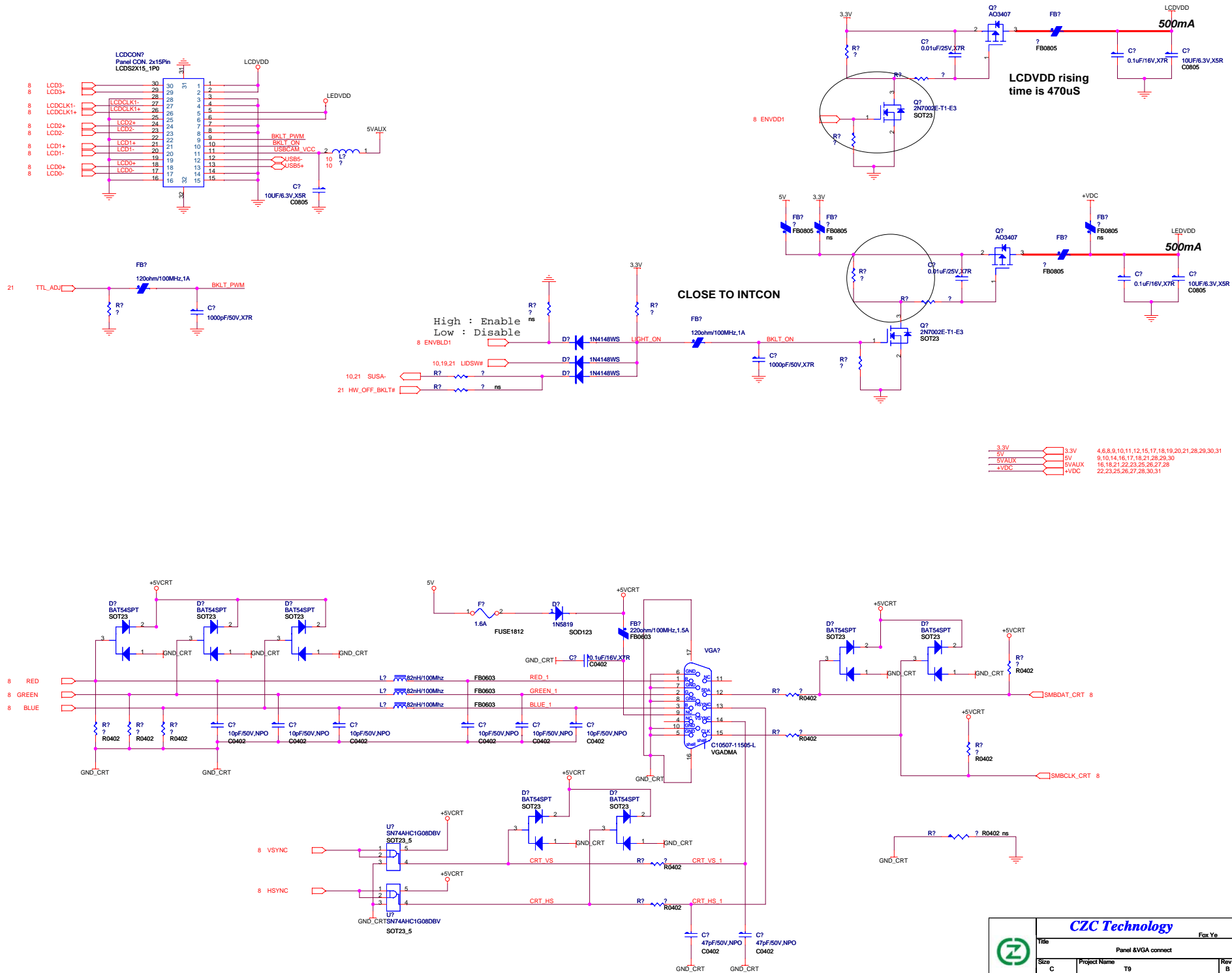




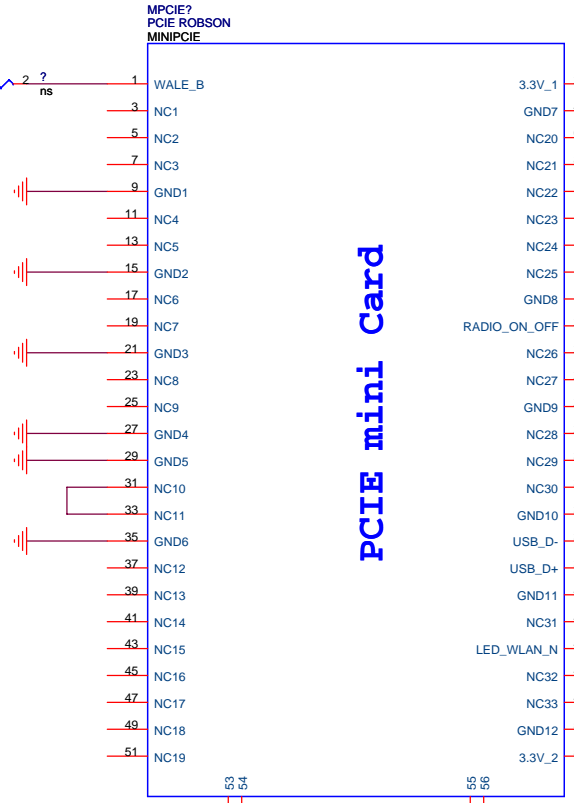
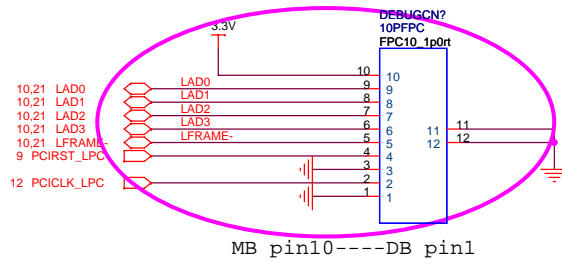
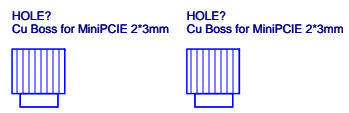




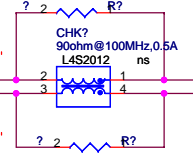
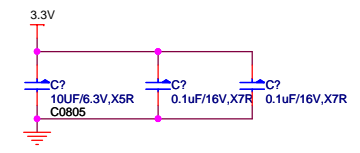
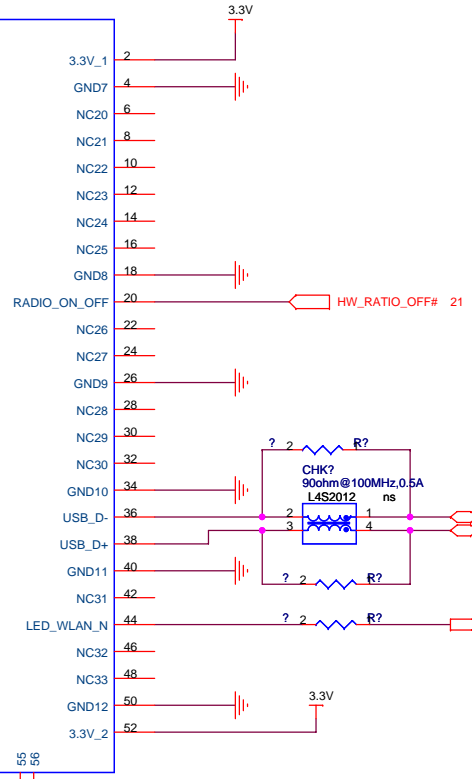









PCIE mini Card



	<b><i>CZC Technology</i></b>			
	Title			Fox Ye
	Mini PCI connect			
	Size A3	Project Name T9		Rev B
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