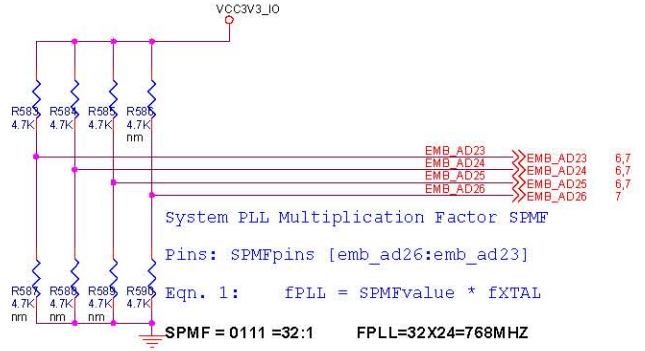

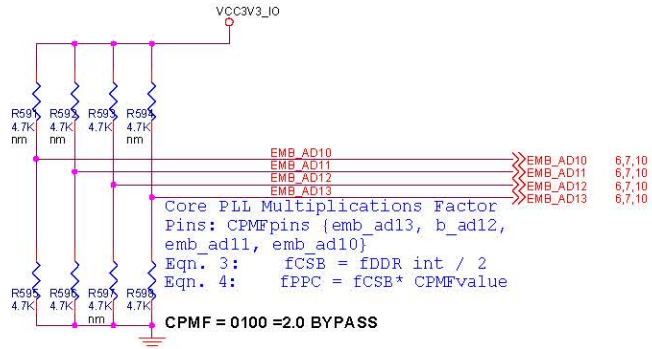

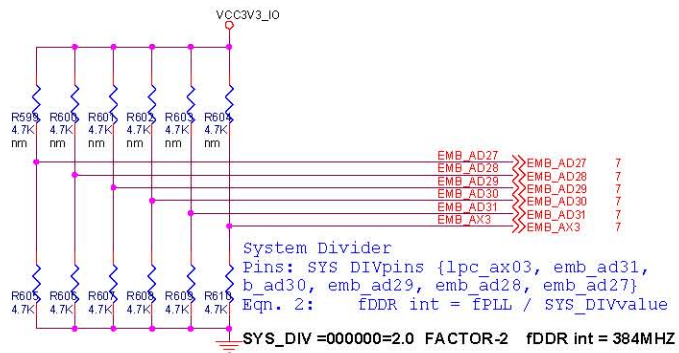

Limits	Min	Max
Xtal	11MHz	75MHz
SysPLL	350MHz	850MHz
CorePLL in	50MHz	333MHz

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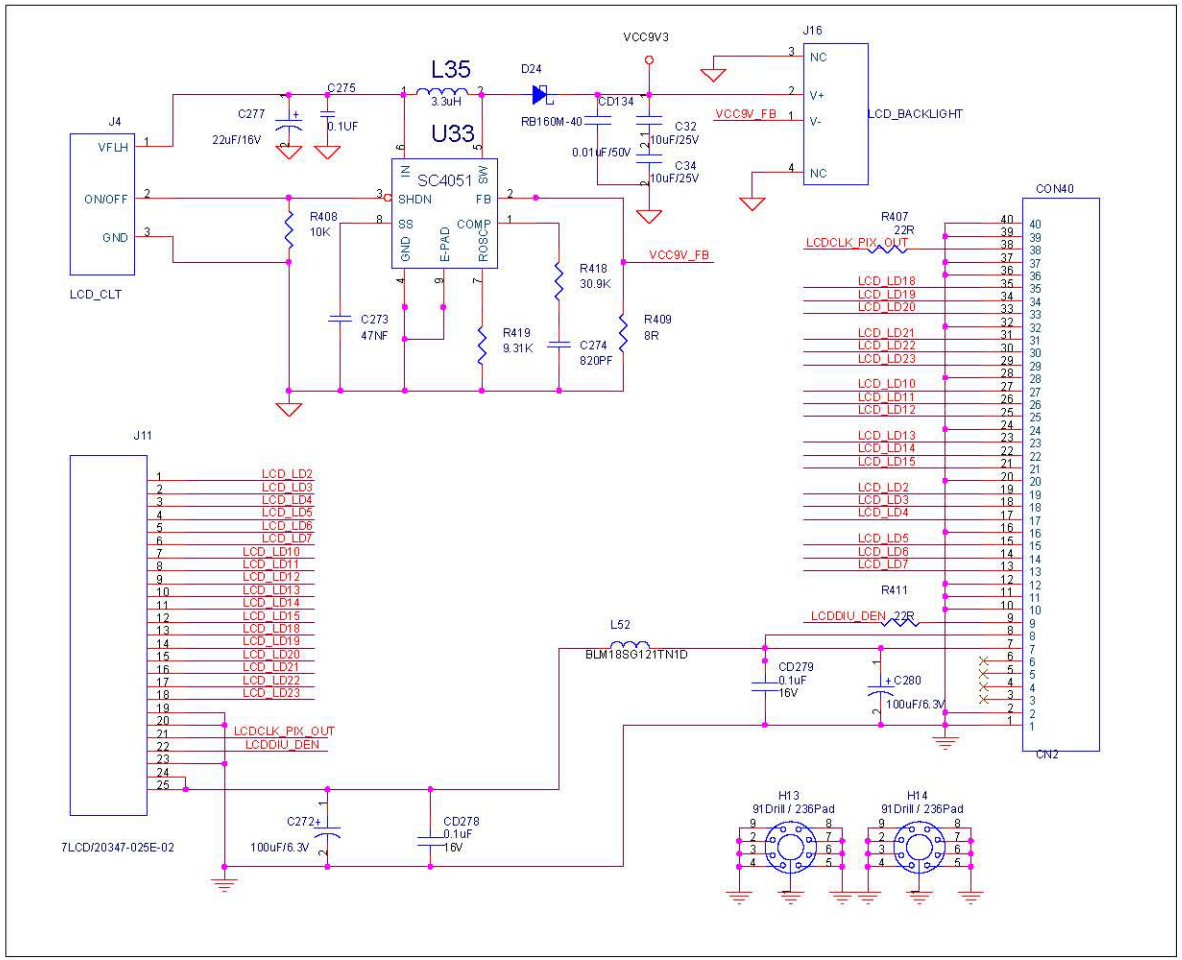
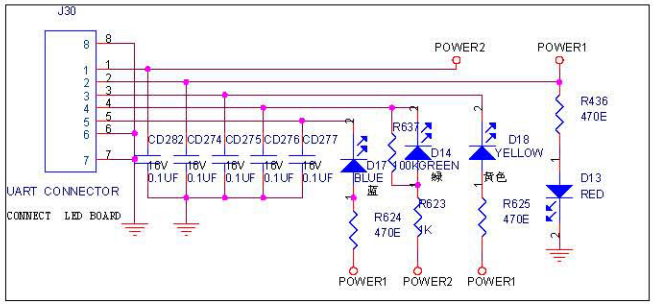
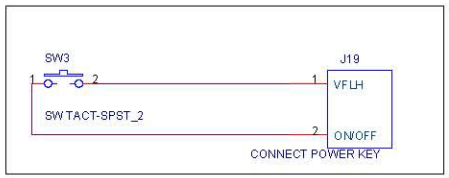
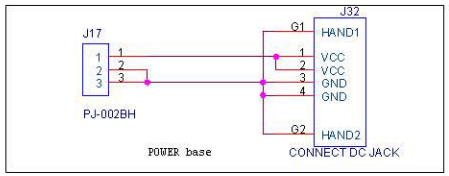
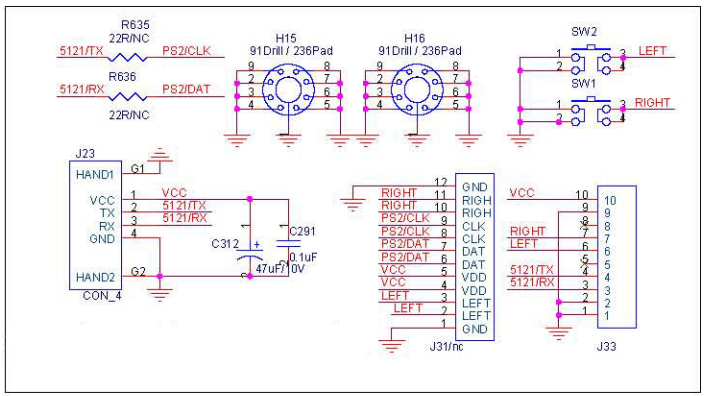

VCC9V3
L35
3.3uH
D24
RB160M-40
C275
0.1UF
C277
22uF/16V
U33
SC4051
IN
SW
SHDN
FB
SS
COMP
GND
E-PAD
ROSC
J4
VFLH
ON/OFF
GND
LCD_CLT
R408
10K
C273
47NF
R418
30.9K
R419
9.31K
C274
820PF
R409
8R
VCC9V_FB
CD134
0.01uF/50V
C32
10uF/25V
C34
10uF/25V
J16
NC
V+
V-
LCD_BACKLIGHT
CON40
R407
22R
LCDCLK_PIX_OUT
LCD_LD18
LCD_LD19
LCD_LD20
LCD_LD21
LCD_LD22
LCD_LD23
LCD_LD10
LCD_LD11
LCD_LD12
LCD_LD13
LCD_LD14
LCD_LD15
LCD_LD2
LCD_LD3
LCD_LD4
LCD_LD5
LCD_LD6
LCD_LD7
R411
LCDDIU_DEN_22R
L52
BLM18SG121TN1D
CD279
0.1uF
16V
C280
100uF/6.3V
CN2
J11
LCDCLK_PIX_OUT
LCDDIU_DEN
7LCD/20347-025E-02
C272
100uF/6.3V
CD278
0.1uF
16V
H13
91Drill / 236Pad
H14
91Drill / 236Pad


J30
POWER2
POWER1
R436
470E
CD282
CD274
CD275
CD276
CD277
16V
0.1UF
D17
BLUE
蓝
R637
100K
D14
GREEN
绿
D18
YELLOW
黄色
D13
RED
R624
470E
R623
1K
R625
470E
UART CONNECTOR
CONNECT LED BOARD


SW3
J19
VFLH
ON/OFF
SW TACT-SPST_2
CONNECT POWER KEY


J17
PJ-002BH
J32
HAND1
HAND2
VCC
GND
POWER base
CONNECT DC JACK


R635
22R/NC
R636
22R/NC
5121/TX
5121/RX
PS2/CLK
PS2/DAT
H15
91Drill / 236Pad
H16
91Drill / 236Pad
SW2
SW1
LEFT
RIGHT
J23
HAND1
HAND2
CON_4
C312
47uF/10V
C291
0.1uF
J31/nc
J33

Designed in Allegro 15.5

GDA07KB002-BALI REFERENCE DESIGN SCHEMATIC (VGA)

PAGE#	TITLE	PAGE#	TITLE	PAGE#	TITLE
01	COVER_PAGE	15	RESET_XTAL_CIRCUITS		
02	OVERALL_BLOCK_DIAG	16	POWER_SUPPLY_CHARGER		
03	FLASH_EMB_PATA_MPC5121	17	STRAPPING_OPTIONS_BOOT		
04	DDR2_MPC5121E	18	STRAPPINGS_PLL		
05	DDR2_COMPONENTS	19	MOUSE_LCD_LED		
06	FLASH_MEMORIES	20			
07	MPC5121 PSC	21			
08	USB_OTG_HUB	22			
09	ETHRENET_PHY	23			
10	PATA_HDD_1.8"_SATA				
11	AUDIO_CODEC				
12	VGA_TFT-LCD_LVDS				
13					
14	MPC5121E_POWER_PINS				

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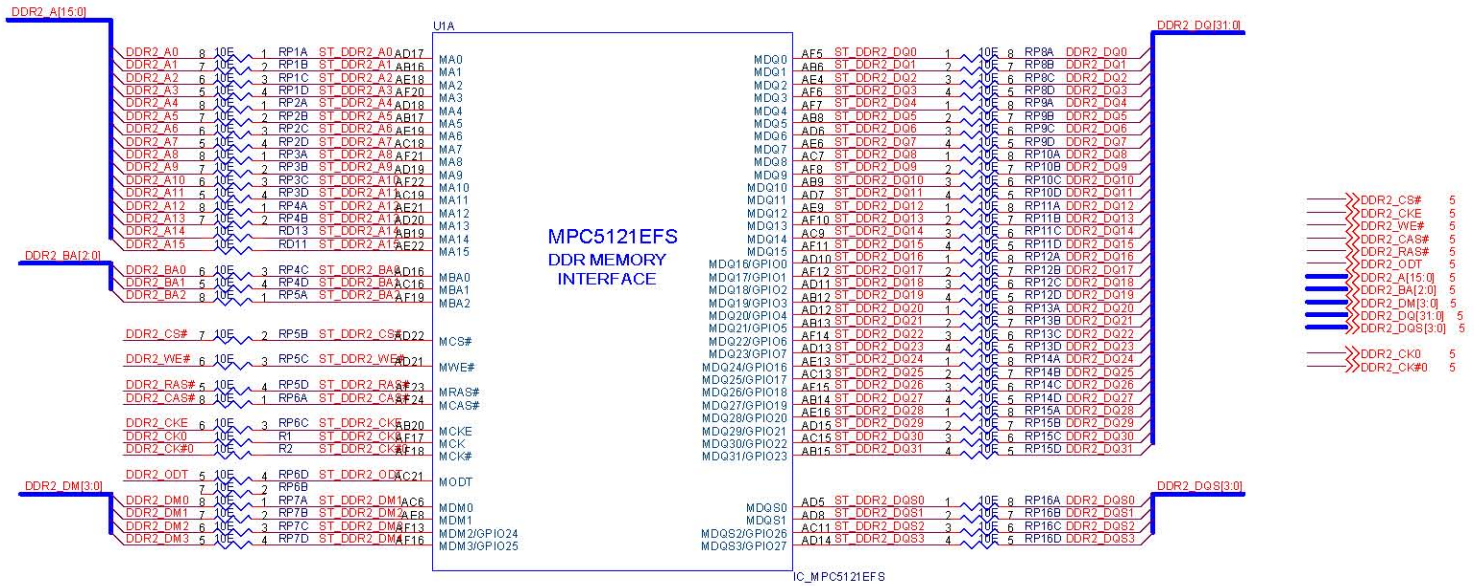

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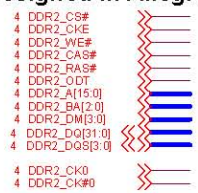
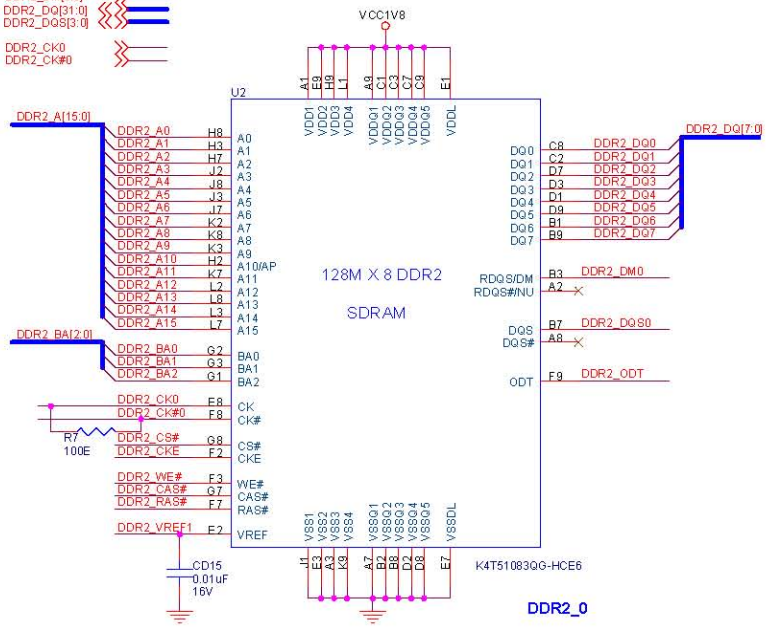
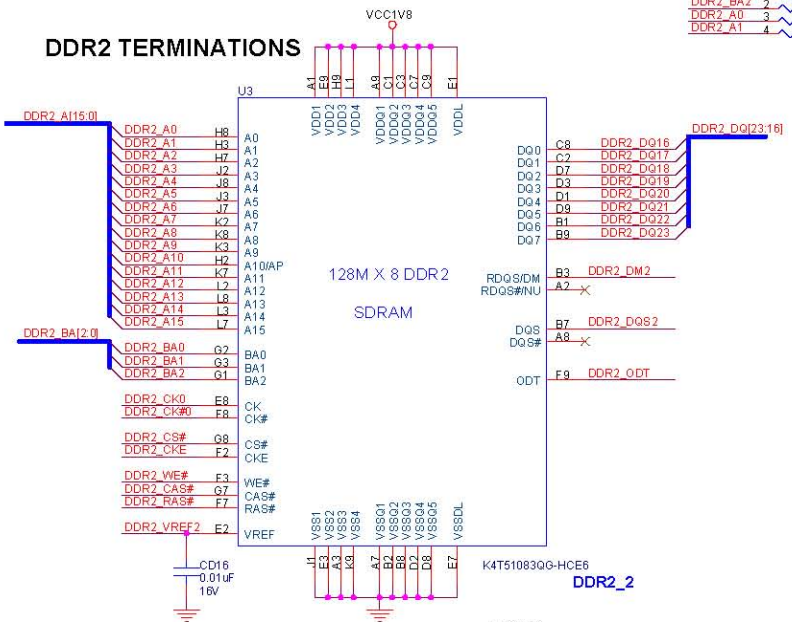
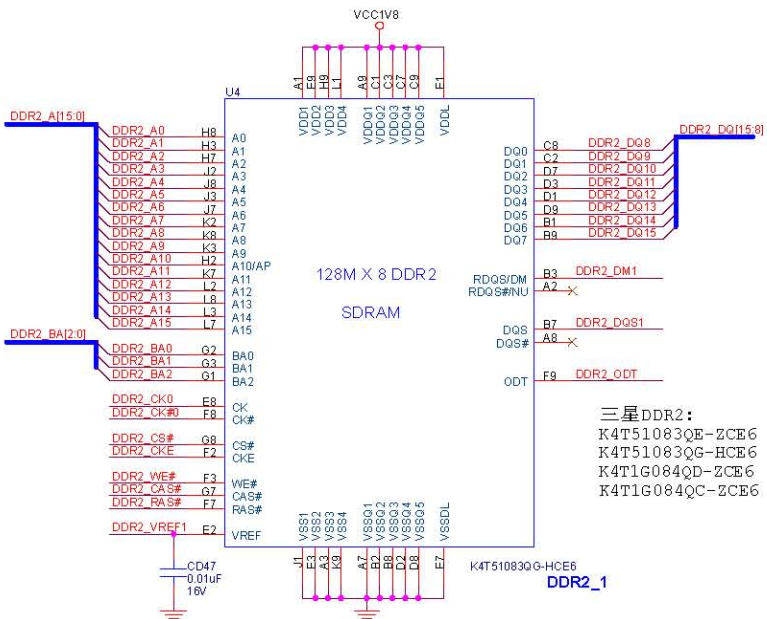
DDR2 MEMORY

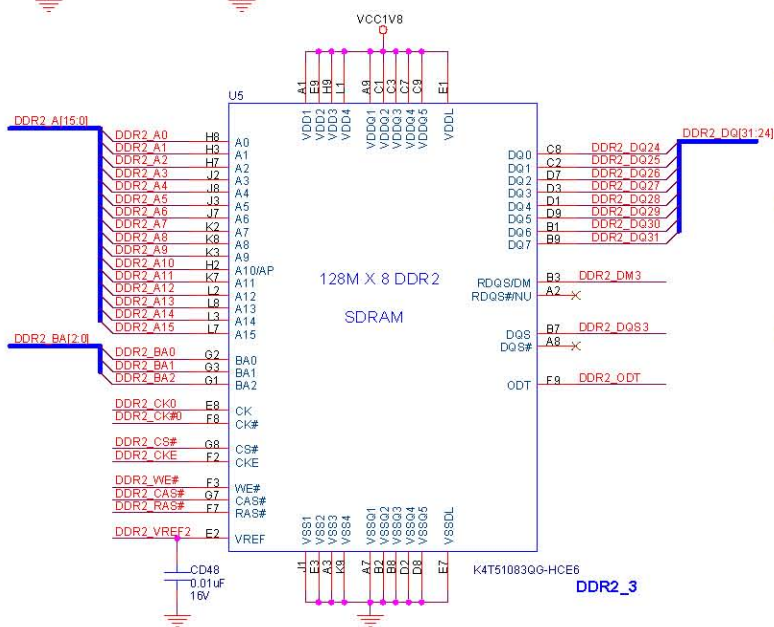




DDR2 TERMINATIONS

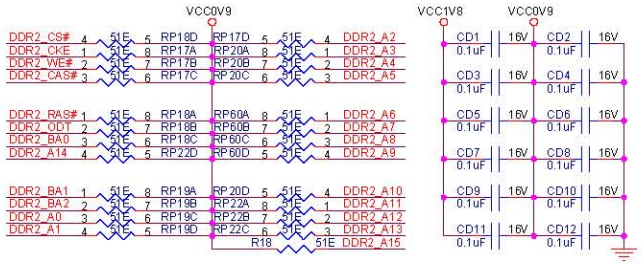




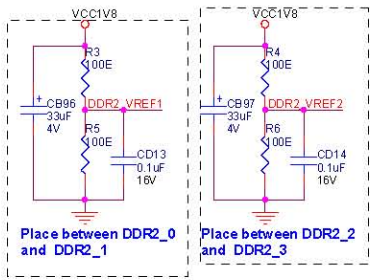


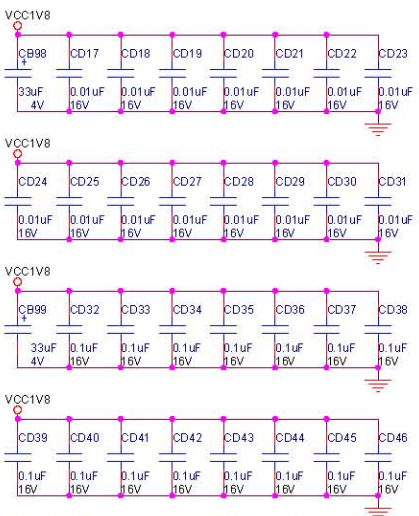
三星DDR2:

K4T51083QE-ZCE6 64X8Mb /333MHZ
K4T51083QG-HCE6 64X8Mb/333MHZ
K4T1G084QD-ZCE6 128X8Mb /333MHZ
K4T1G084QC-ZCE6 128X8Mb/333MHZ



Place decaps such that each resistor pack should have one decap to GND and one to VCC1V8





Place a 0.1uF capacitor Very close to VDDL of each DDR2 chip

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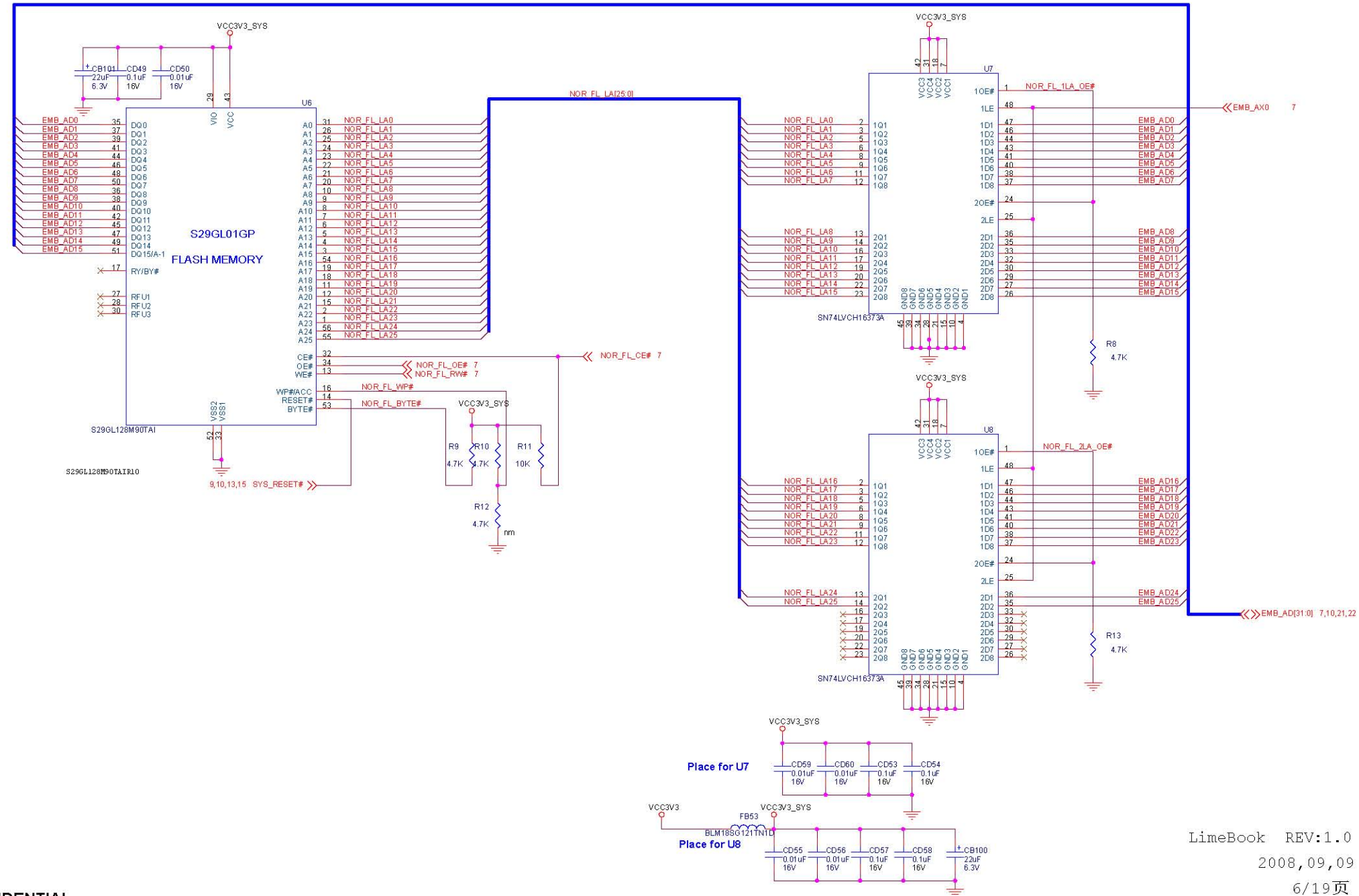

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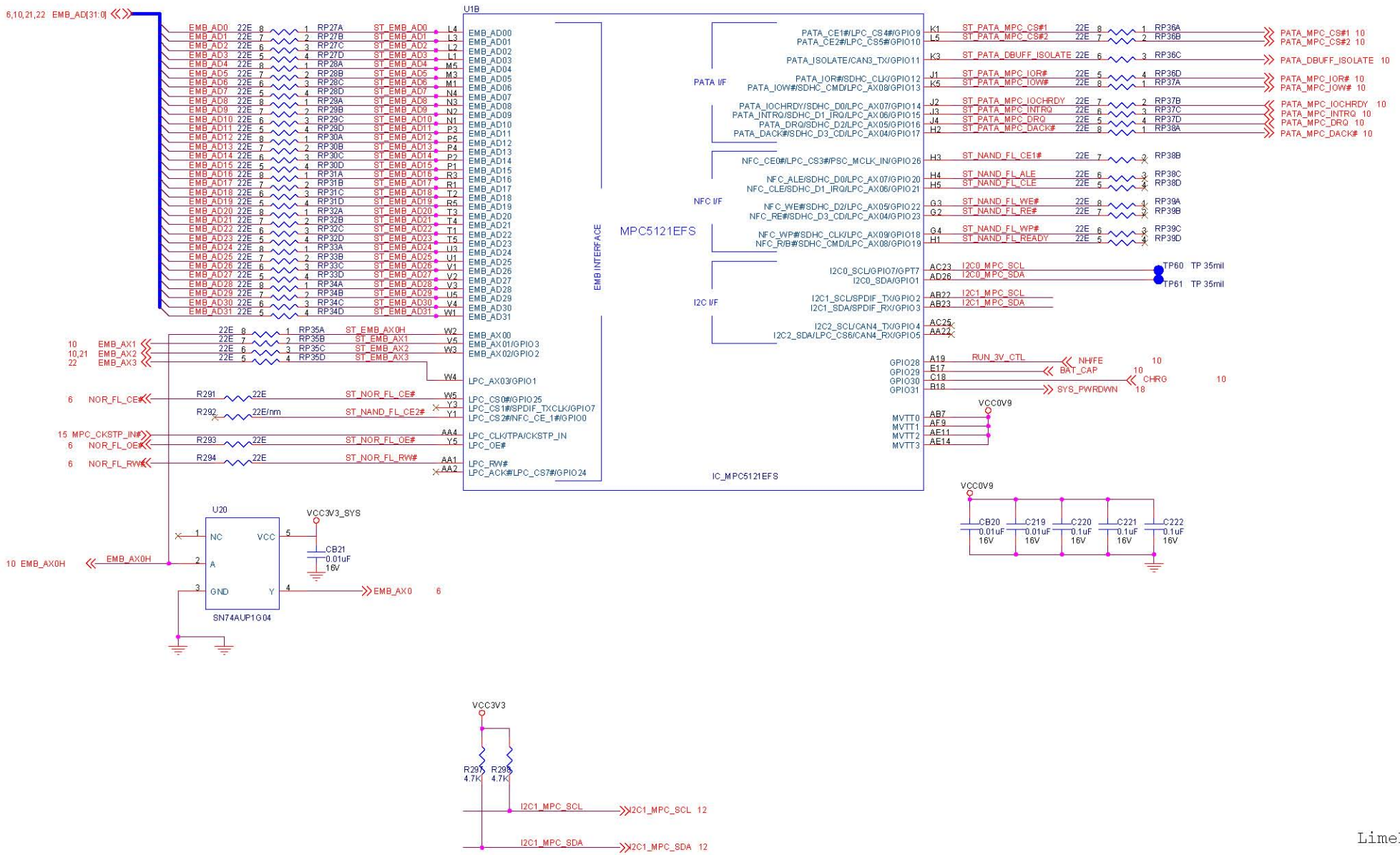

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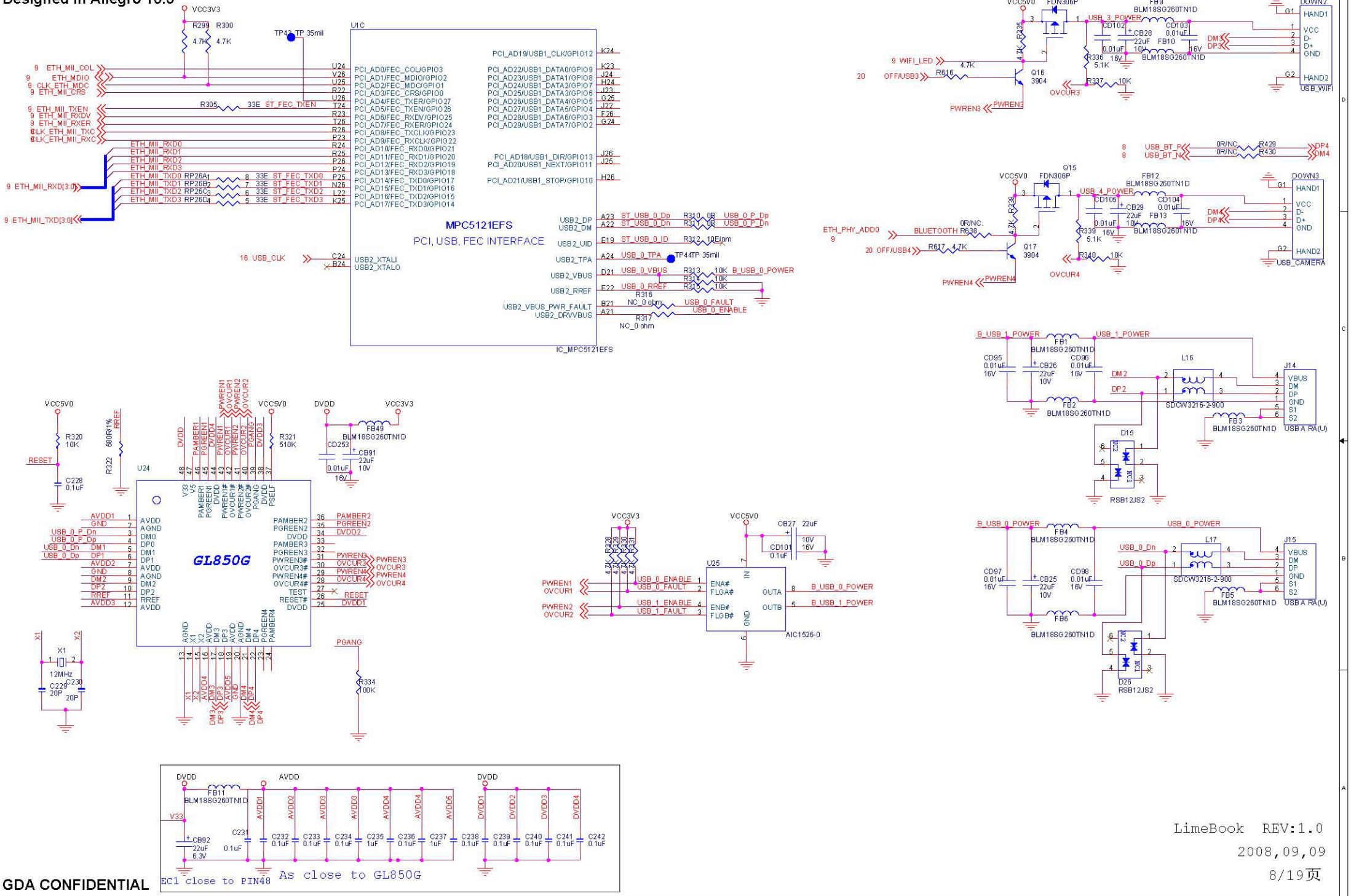

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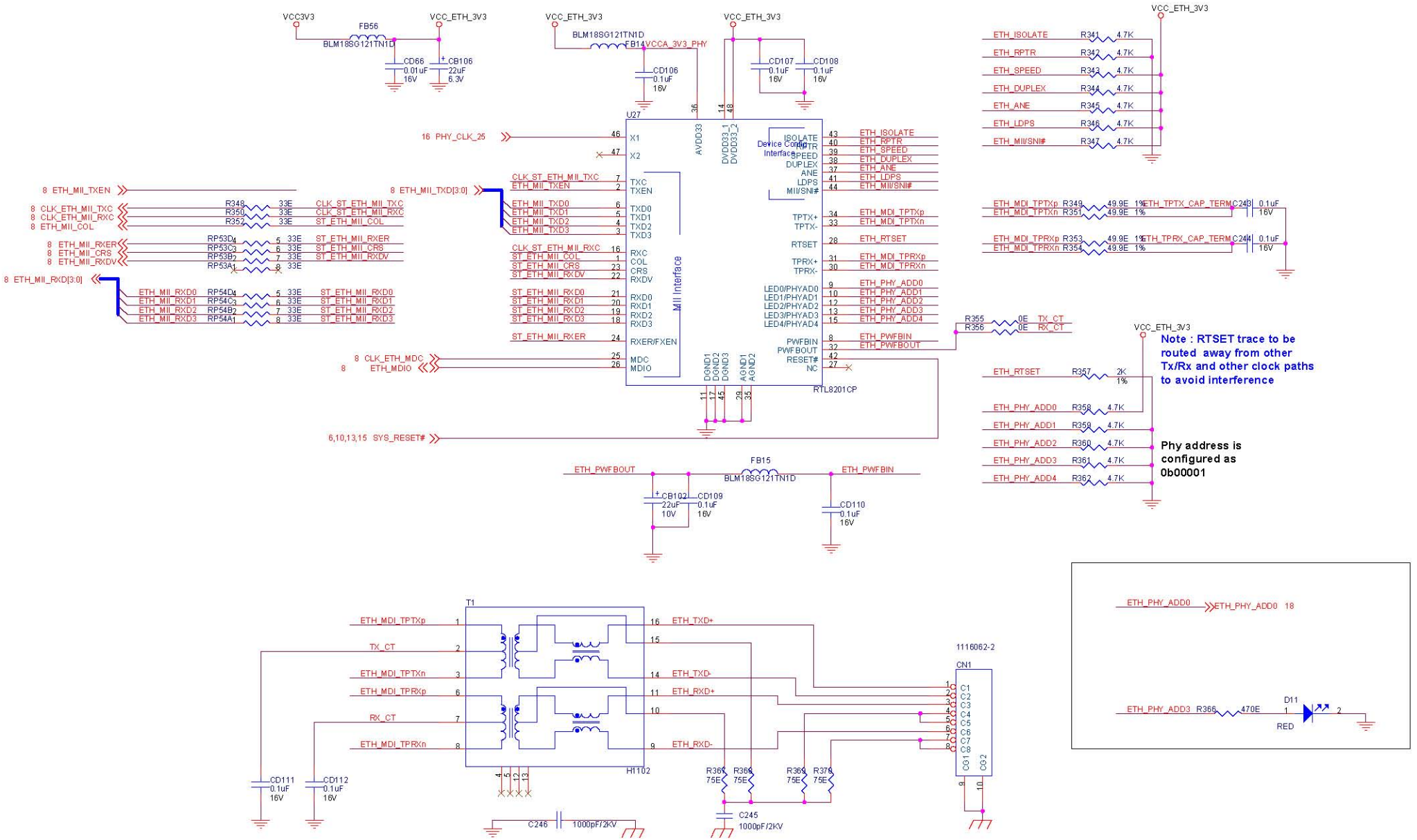

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