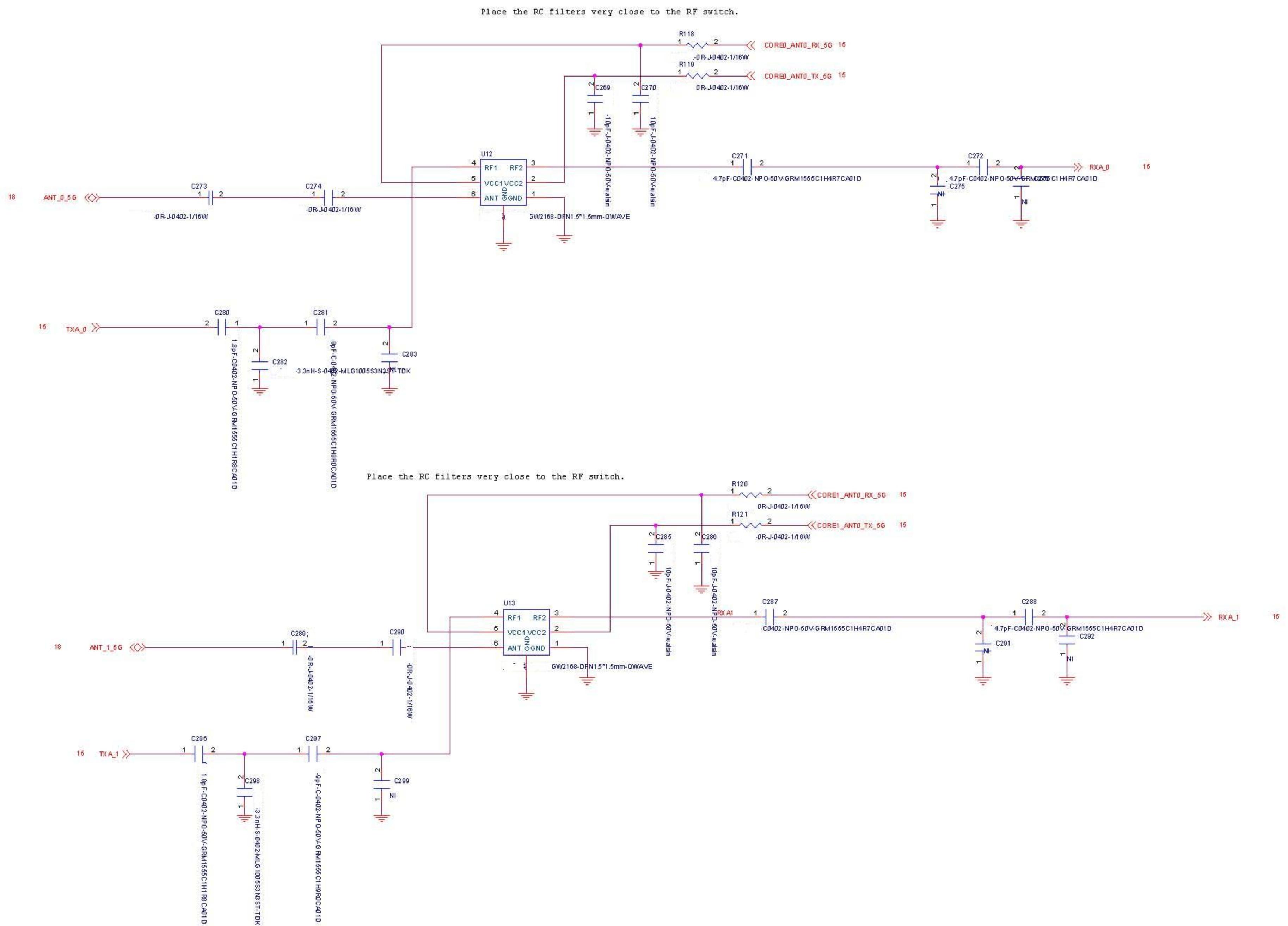
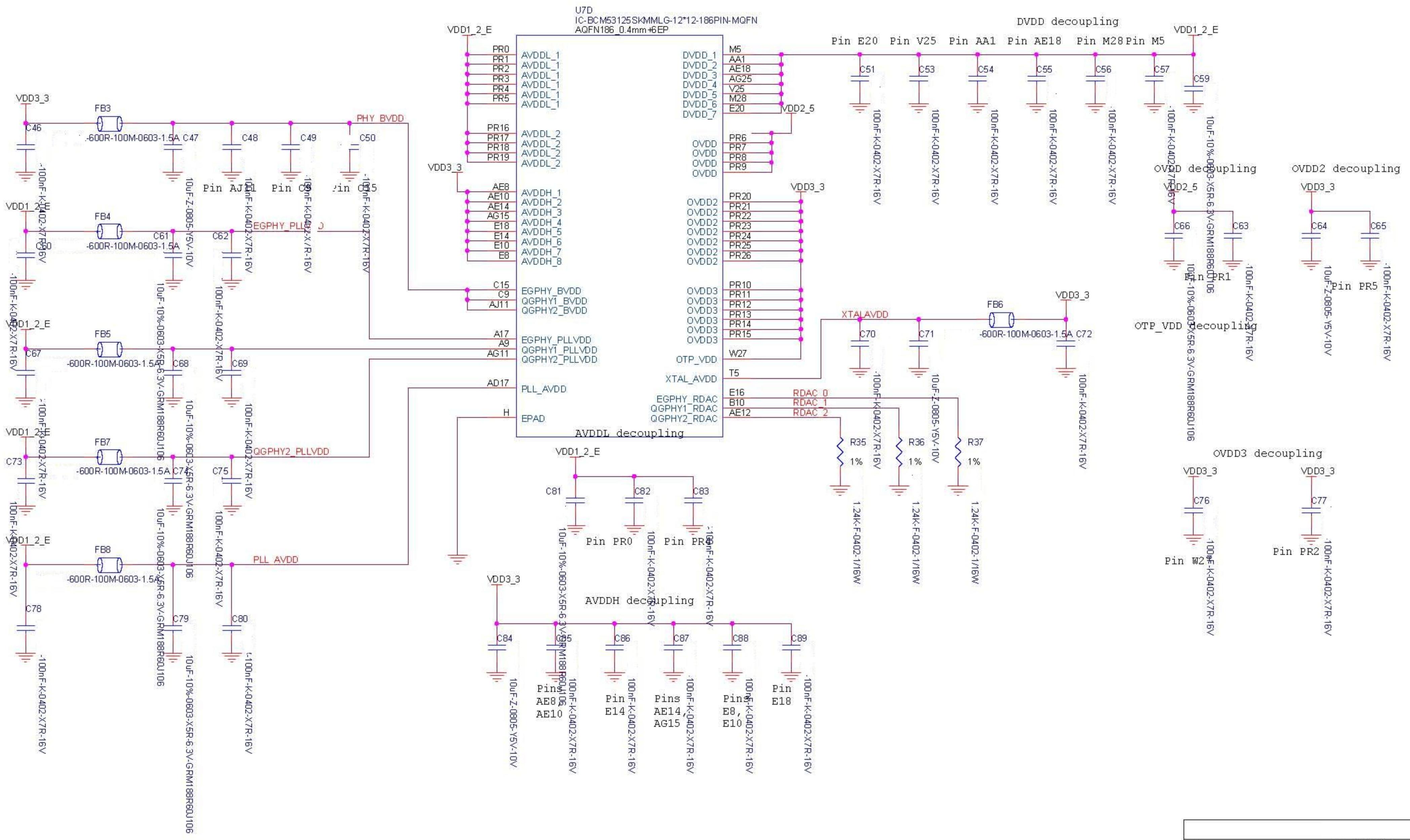
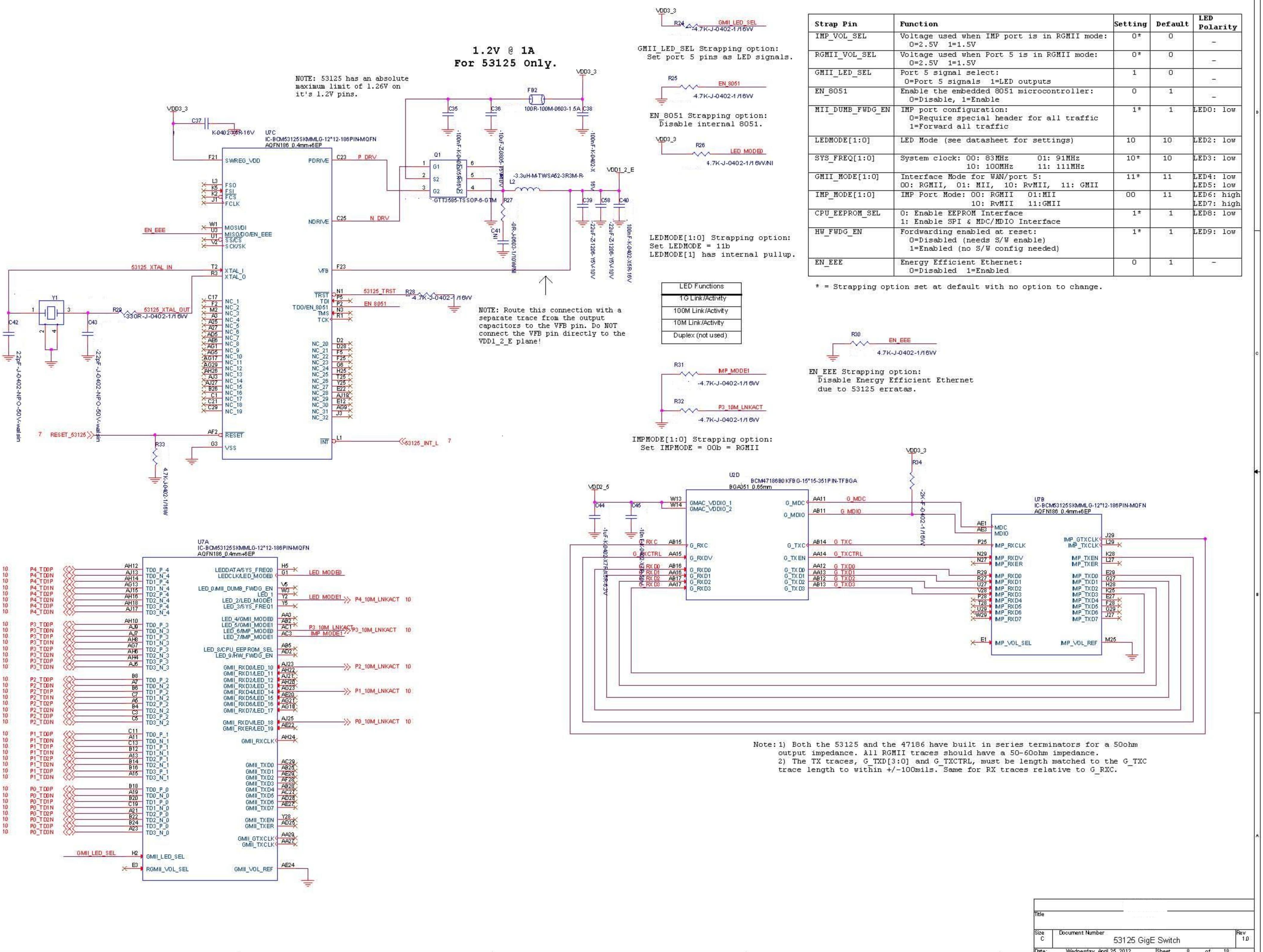


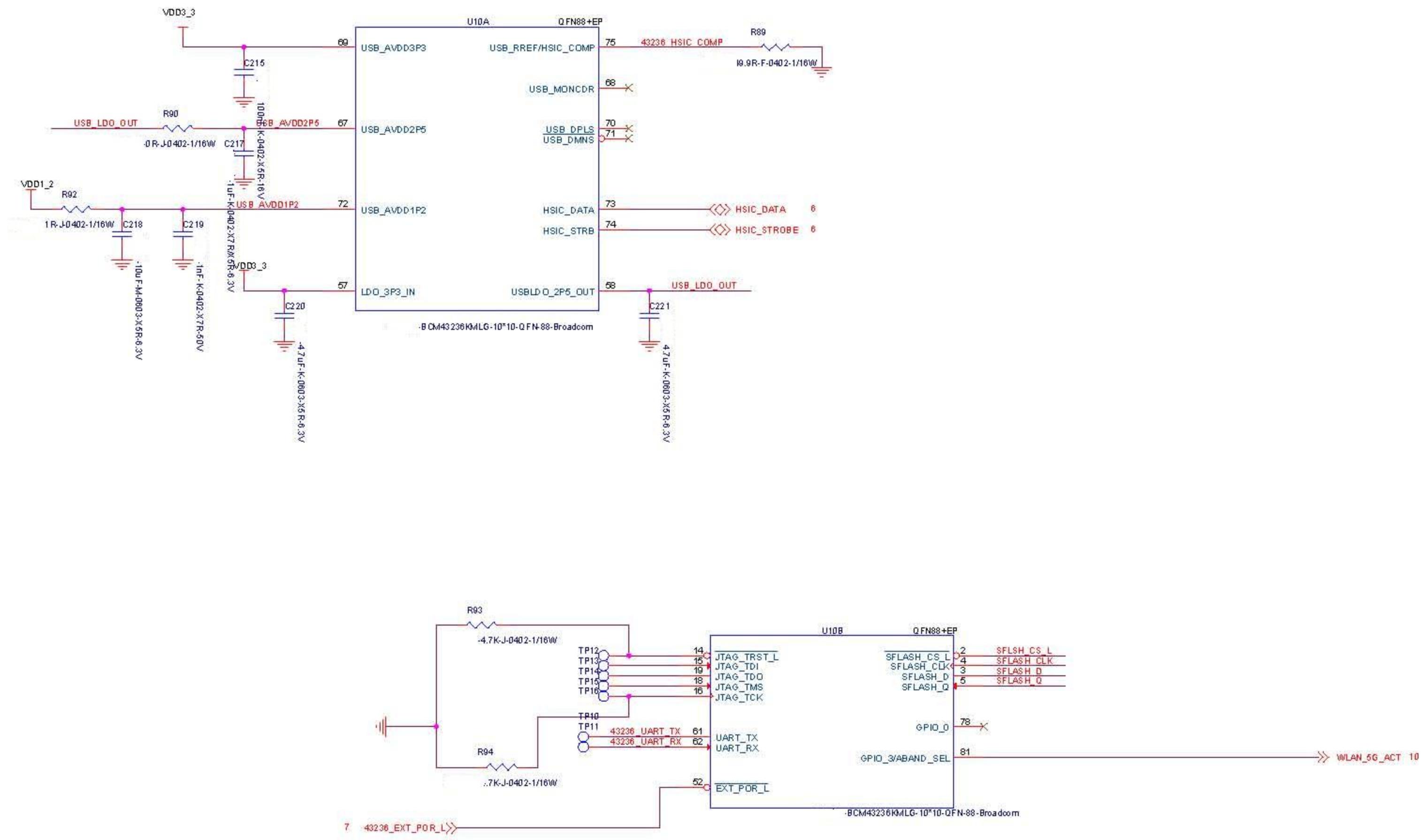
Title		
Size C	Document Number 2.4G RF	Rev 1.0
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Title				
Size B	Document Number	53125 Power		Rev 1.0
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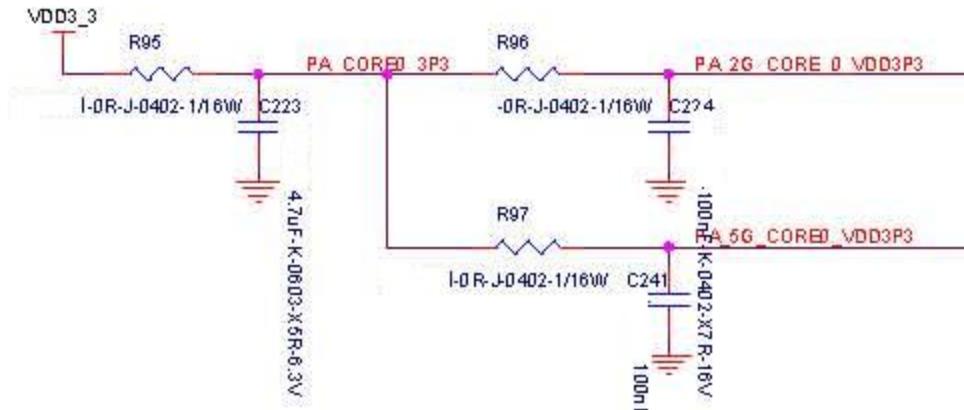




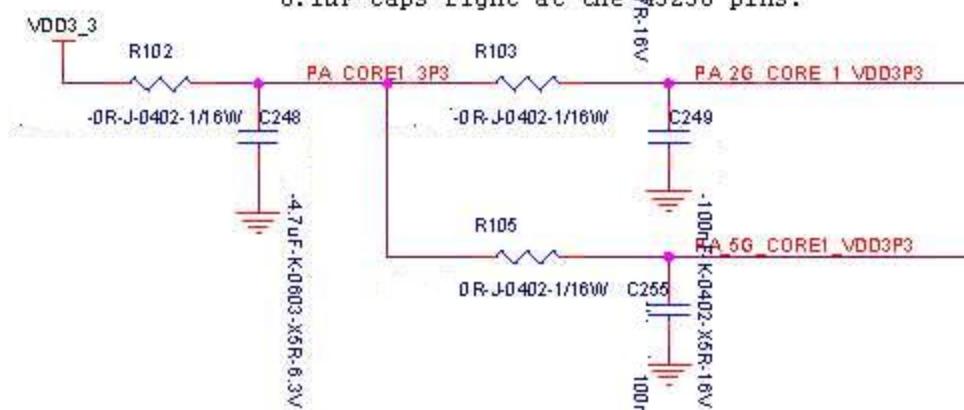
Title		
Size	Document Number	Rev
C	43236 HSIC, JTAG, etc	1.0

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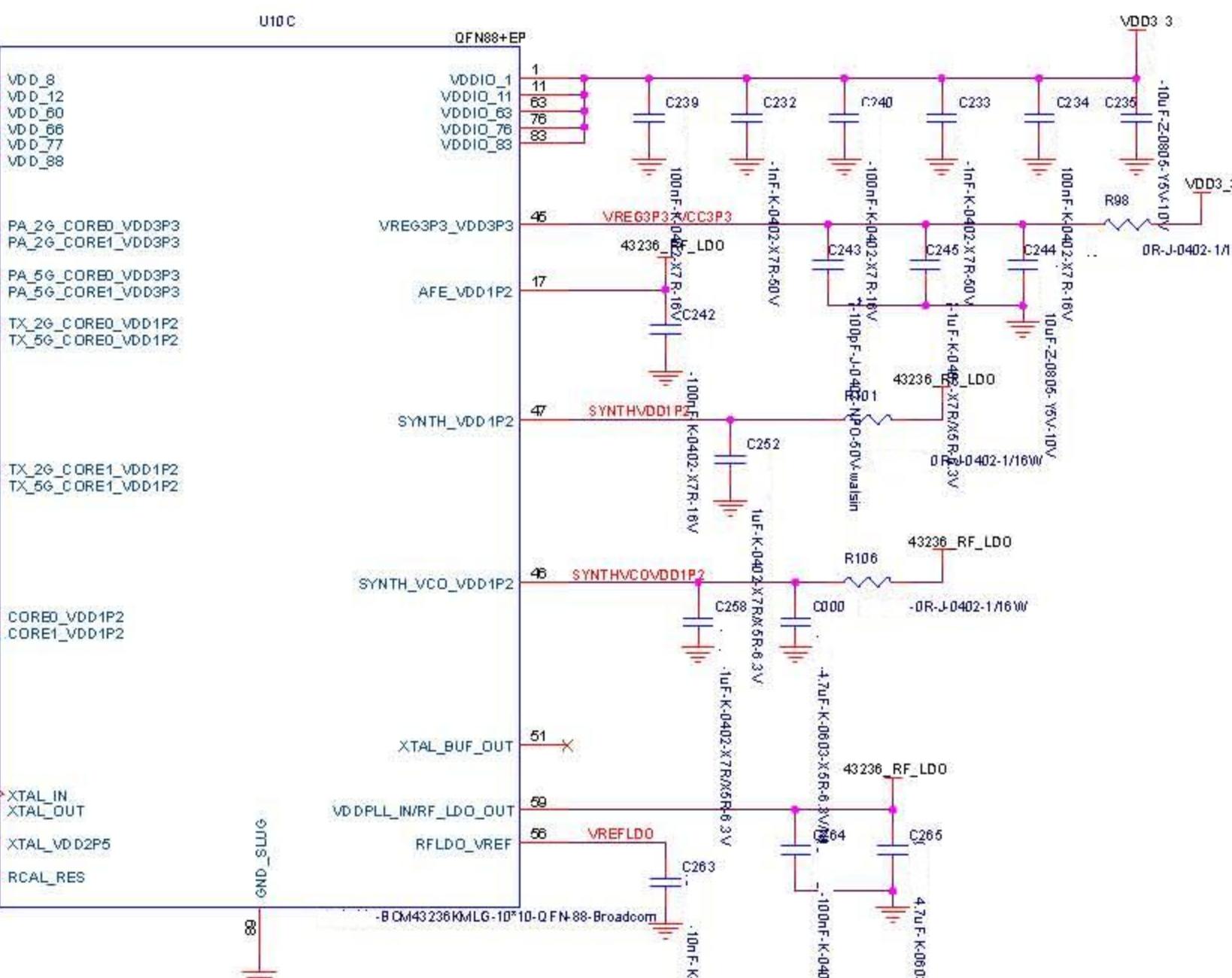
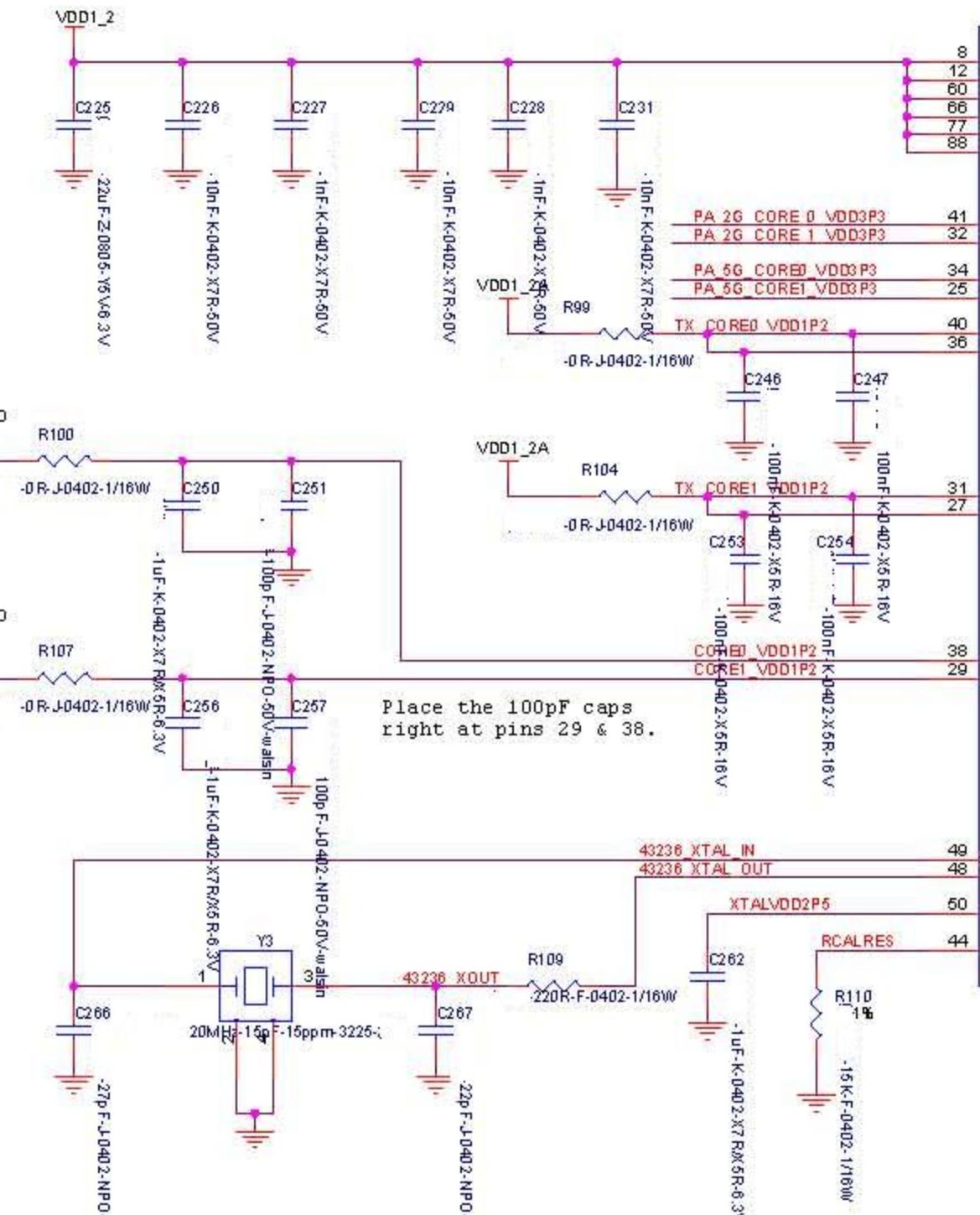
Connections from C223 to R96 & R97
needs to be a "star-point". Place the
0.1uF caps right at the 43236 pins.



Connections from C248 to R103 & R105
needs to be a "star-point". Place the
0.1uF caps right at the 143236 pins.

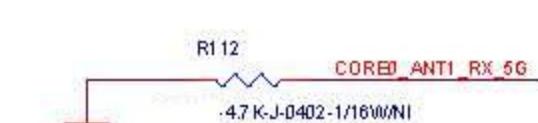
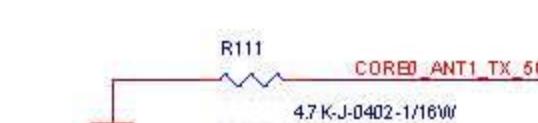


Circuit diagram showing a power supply path from **VDD1_2** through **R108** to ground, and a feedback path from ground through **C259**, **C260**, and **C261** to **VDD1_2A**. The feedback path also includes a resistor labeled **-0R-J-0402-1/16W** and a capacitor labeled **-4.7uF-K-0603-X5R-6.31**.



43236 Strapping Option Pin	Function	Setting	Default Pull
CORE1_ANTO_TX	0 = Serial Flash NOT present [default] 1 = Serial Flash present	0	PD
CORE0_ANTO_RX	0 = Serial Flash Type is ST Micro [default] 1 = Serial Flash Type is Atmel	0*	PD
CORE0_ANT1_TX	0 = HSIC mode (board setting) 1 = USB 2.0 PHY mode [default]	0	PU
CORE0_ANT1_RX	0 = backplane at 96 (98.4) MHz 1 = backplane at 120 (123) MHz [default]	1	PU
CORE0_ANTO_RX	0 = Do not use OTP for configuration (setting) 1 = Use OTP for configuration [default]	0	PU
GPIO[7:6] LNA_5G_PU_1/ LNA_5G_PU_0	00 = boot from RAM, ARM held in reset 01 = boot from ROM [default] 10 = Reserved 11 = Reserved	01	none

t = Strapping option set at the default with no option to change.

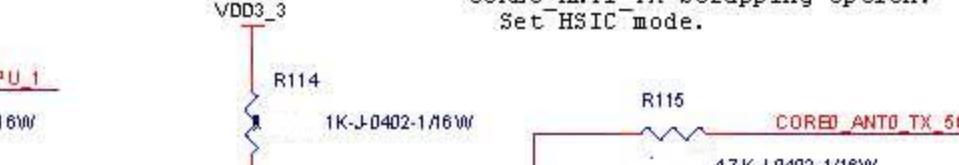
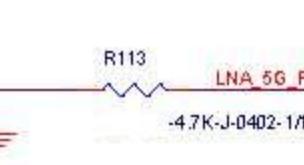


CORE0_ANTI_TX Strapping Option:
Set_HSIC_mode

COREO ANT1_RX Strapping Option:
Option to set 96(98.4) backplane clock

GPIO[7:6] Strapping Options:
Set to boot from ROM. If serial flash present and programmed, 43236 will boot from serial flash.

A standard 4.7K pullup will not be able to overpower the R174/Q6 load on page 14 so a strong external pullup is needed to assure "1" is read for the strapping option when "Read from ROM" is set.



CORE0_ANTO_TX Strapping Option:

4.7K-J-0402-1/16W/NI

4.7K-J-0402-1/16W/WI

Title		
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