
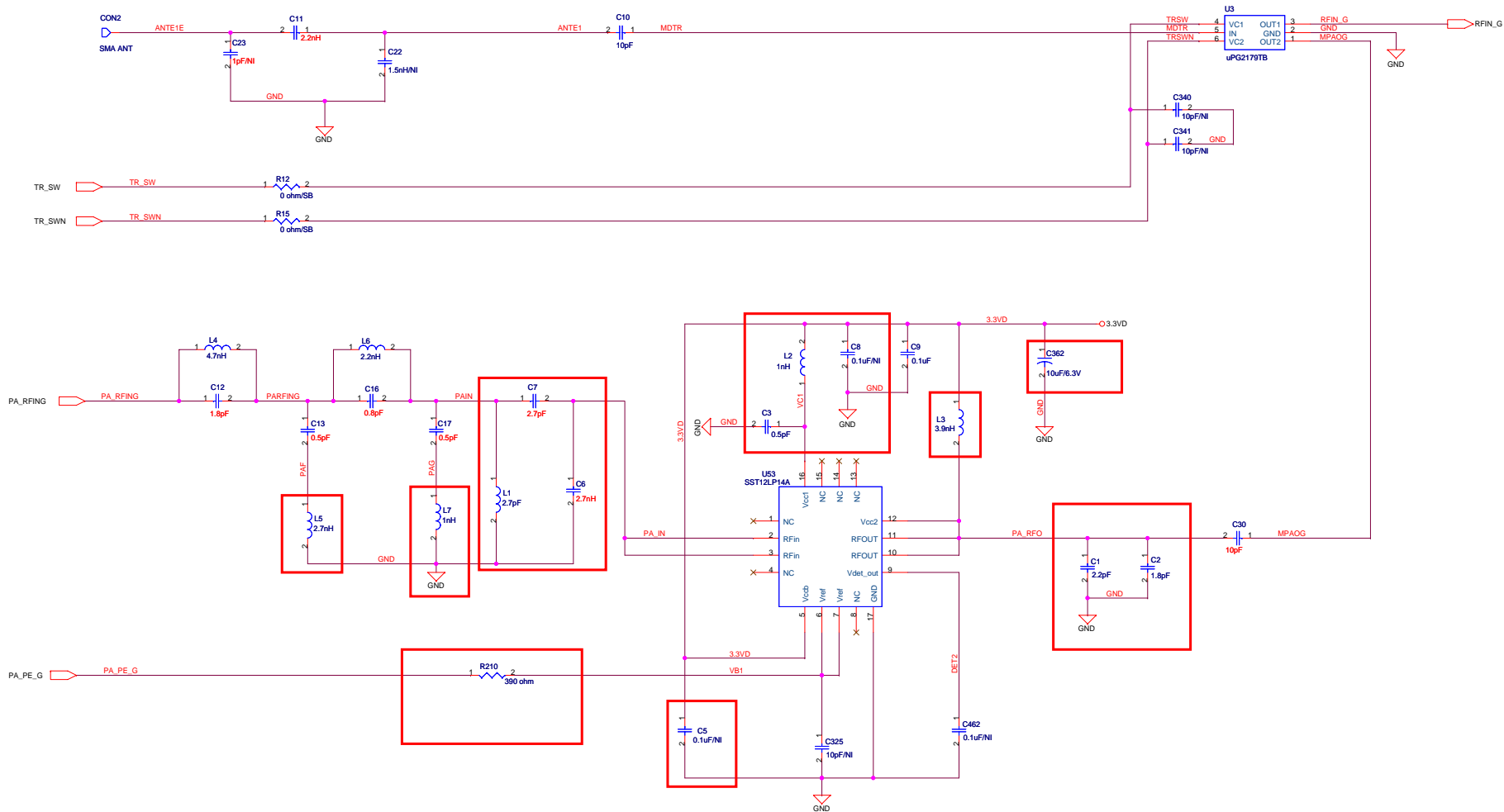


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**Filename:**  
**USB-PEN-RT2501W-V31ST-4L-NOBPF-D2359-060330.DSN**

		<b><i>RALINK TECHNOLOGY, CORP.</i></b>			
		Title USB 2.0 PEN TYPE System - RT2571W + RT2528			
Size B	Document Number USB-RT2501WUSB-V31ST-X.SCH			Rev 3.1	
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	3-PA-SST12LP14A.SCH		3.1	
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DESIGN NOTE: See LX layout guidelines for latest recommendations on memory routing.

DESIGN NOTE: Use SDCLK pairs that are most convenient for clean routing.

DESIGN NOTE: BA0,BA1 must be trace length matched to within 50 mils.

DESIGN NOTE: Do not swap series resistors on the DQS, DQM or Data lines with the Address or control lines.

DESIGN NOTE: Swap series resistors on the data lines in order to minimize the number of vias.

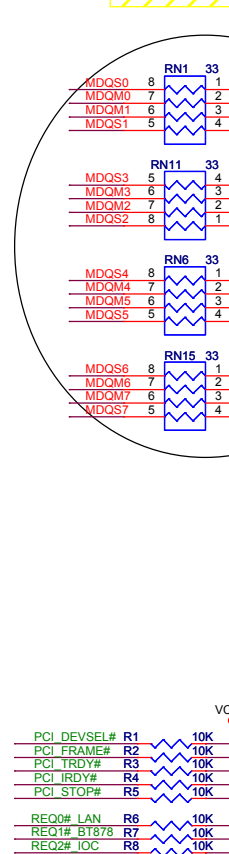
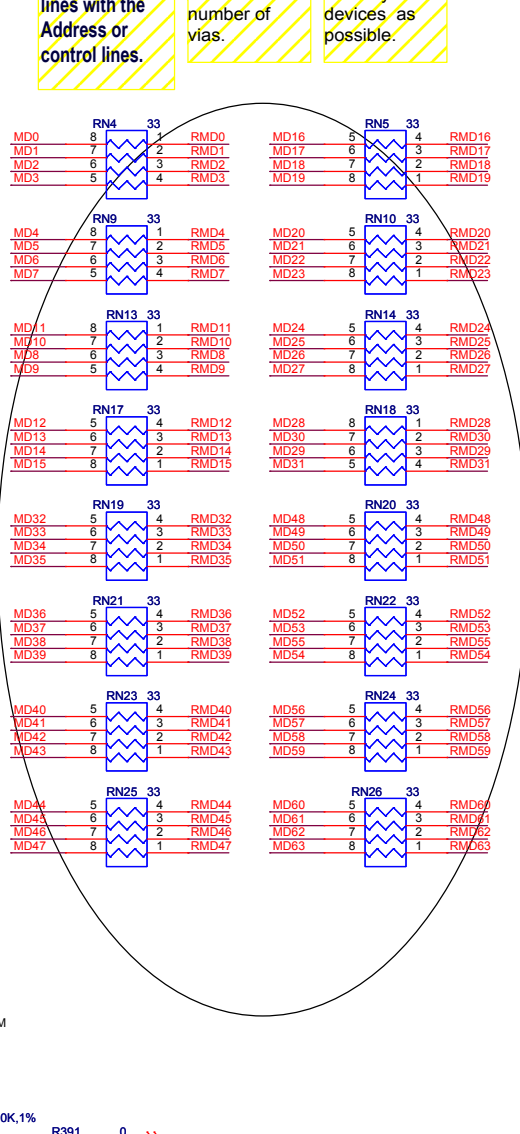
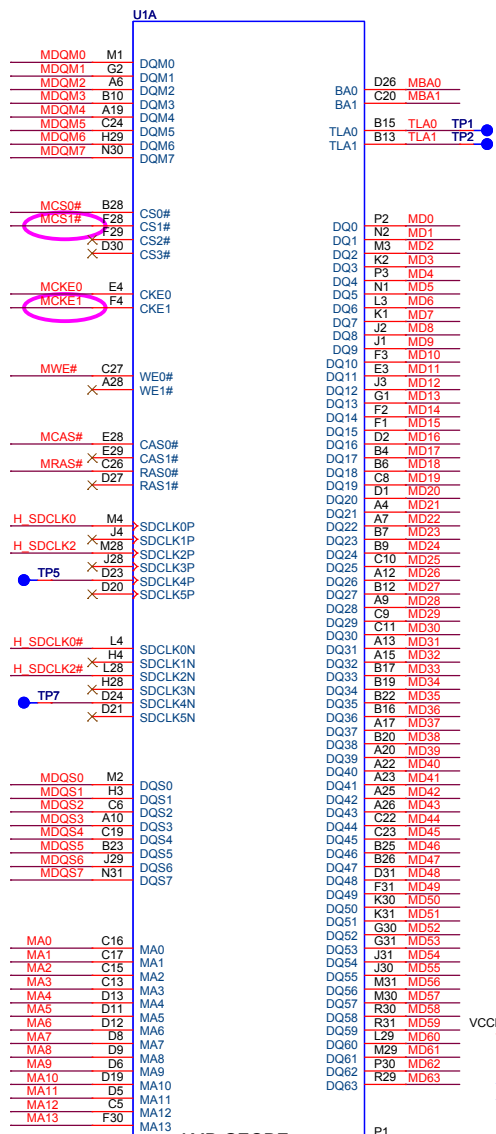
DESIGN NOTE: Place data bus series resistors as close to the memory devices as possible.

DESIGN NOTE: Swap series resistors on the DQS lines in order to minimize the number of vias.

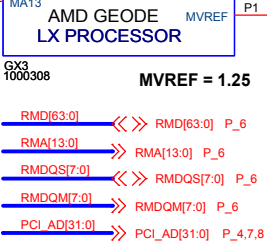
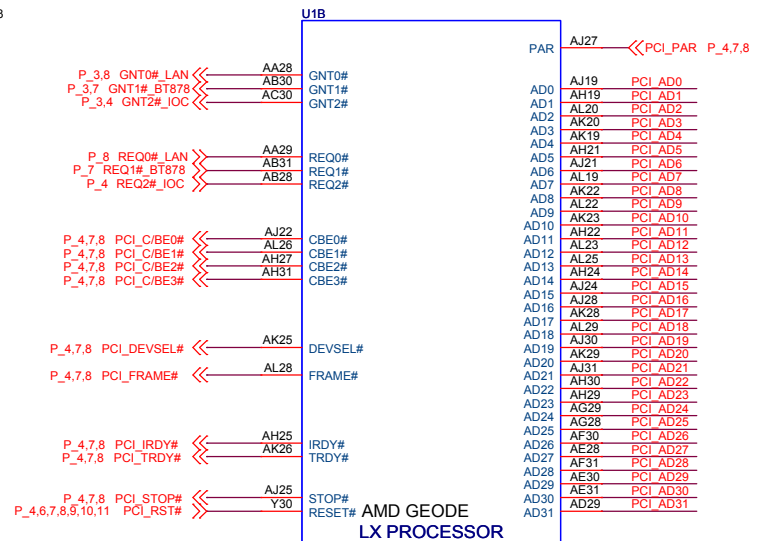
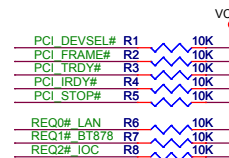
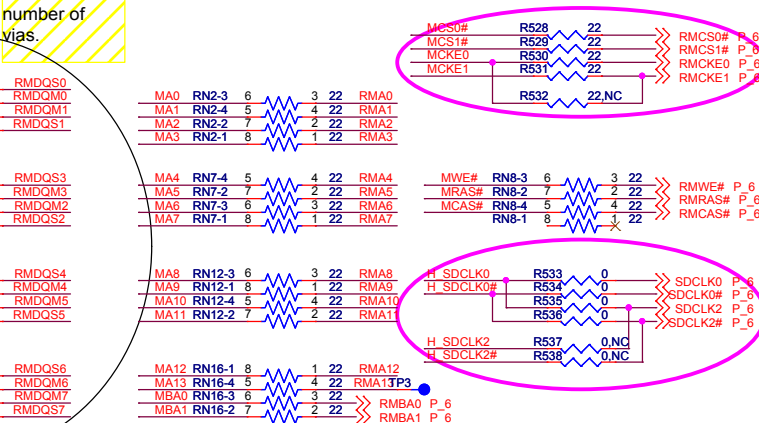
DESIGN NOTE: Swap series resistors on the address lines in order to minimize the number of vias.

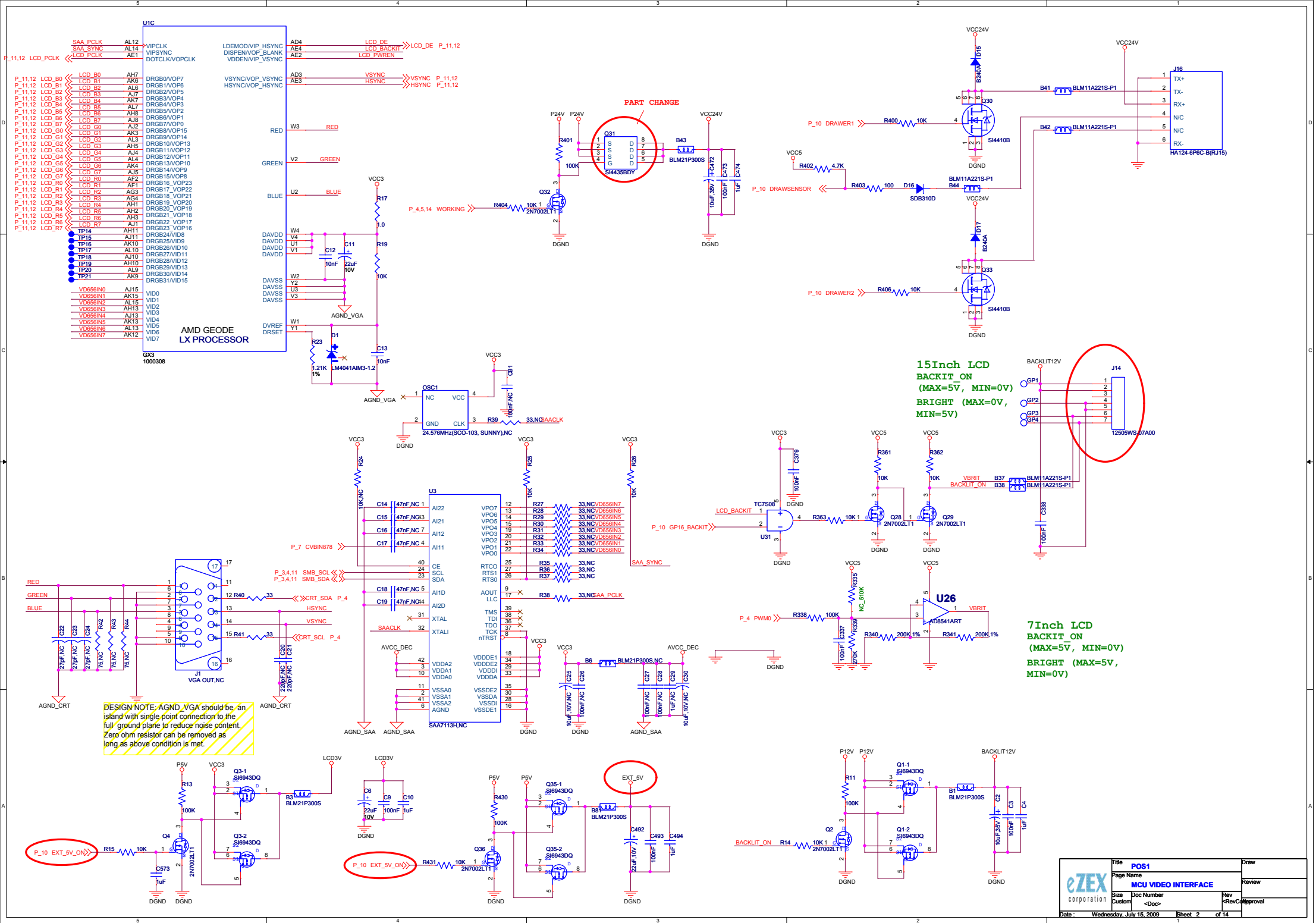
DESIGN NOTE: Place address and control series resistors as close to the processor as possible.

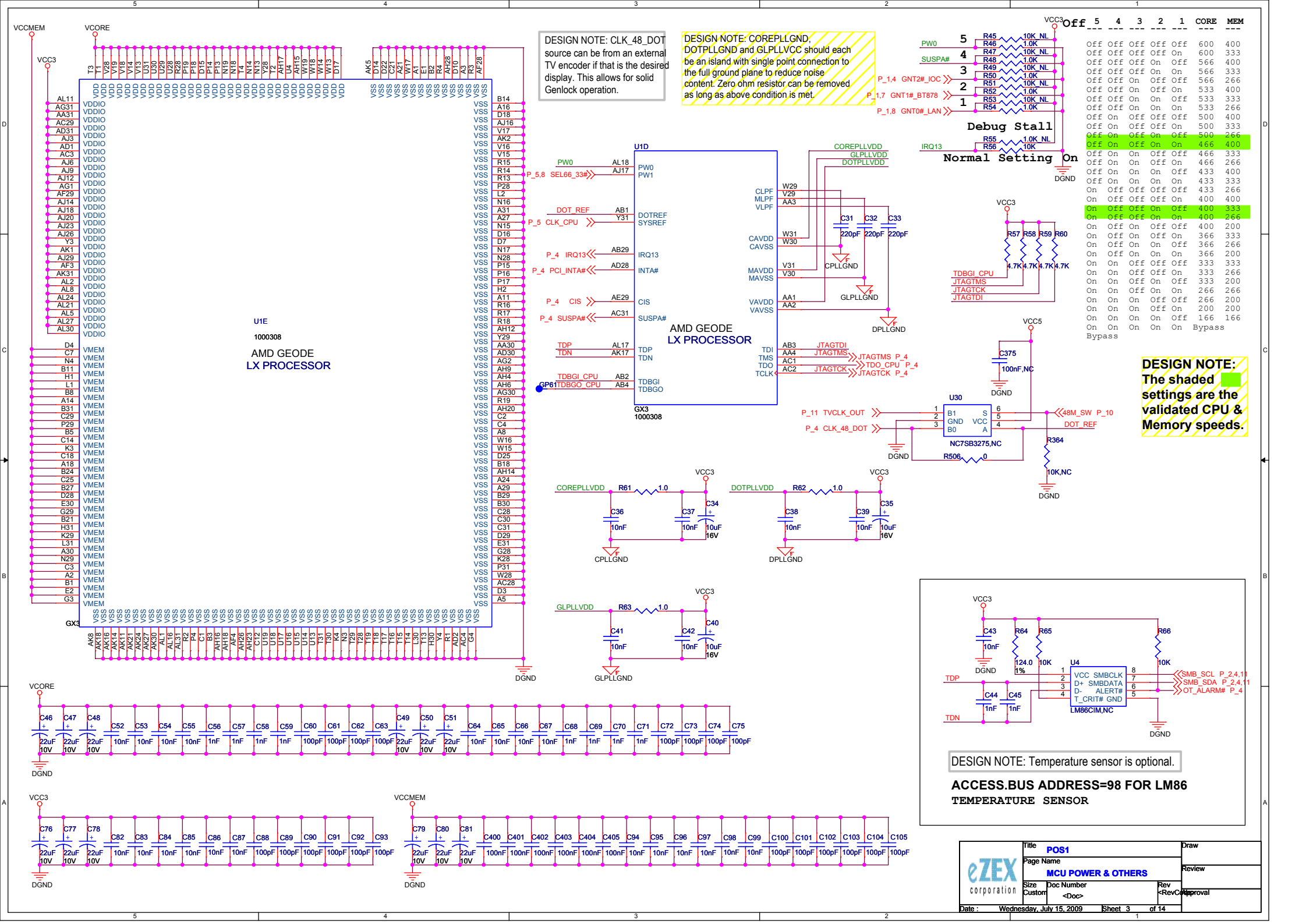
DESIGN NOTE: Place DQS and DQM series resistors as close to the SODIMM connector as possible.



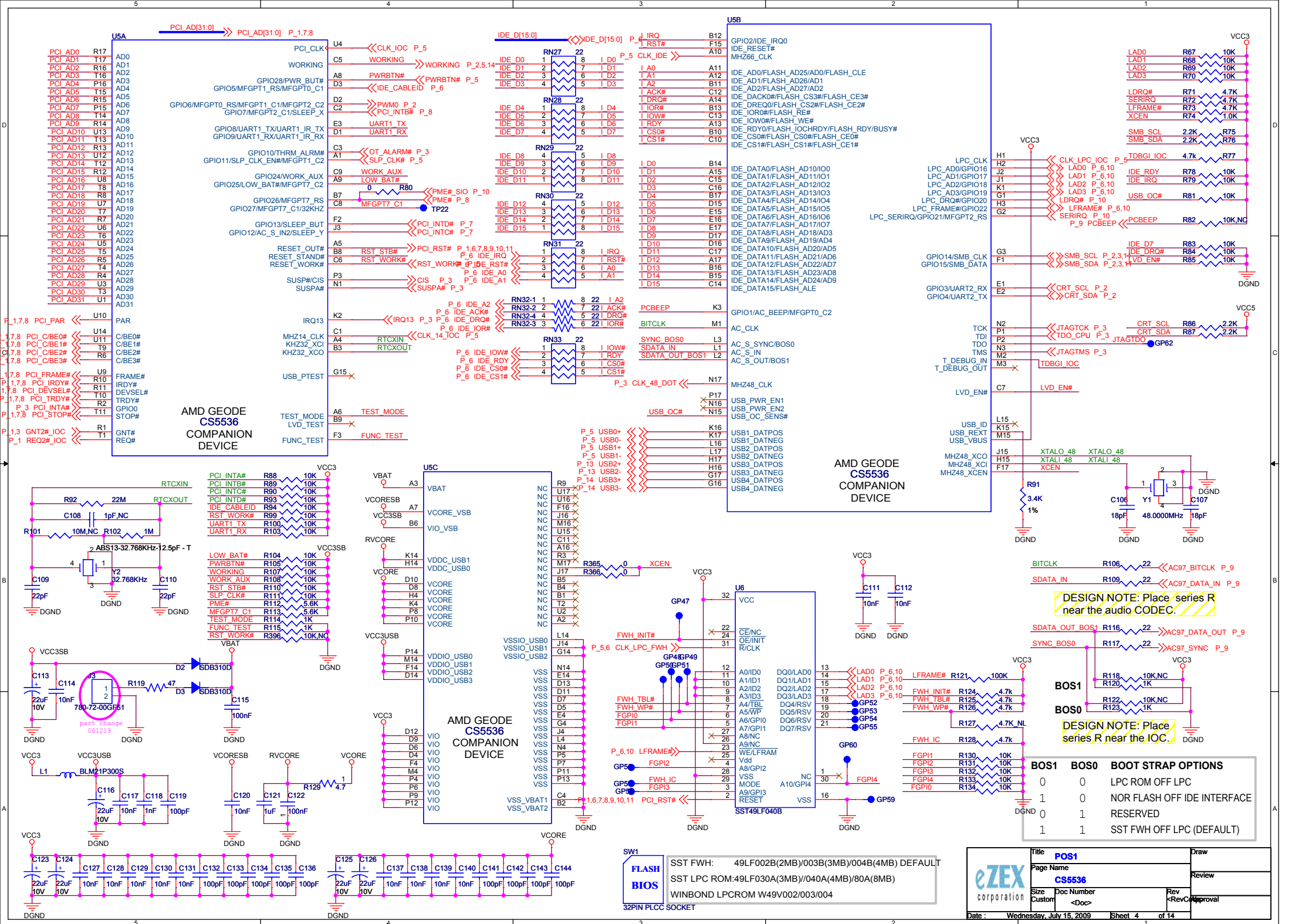
DESIGN NOTE: This schematic shows a non-parallel terminated DDR solution. There may be restrictions as to the total number of DRAMS and the number of banks supported on the SODIMM. See LX layout guidelines for current restrictions.

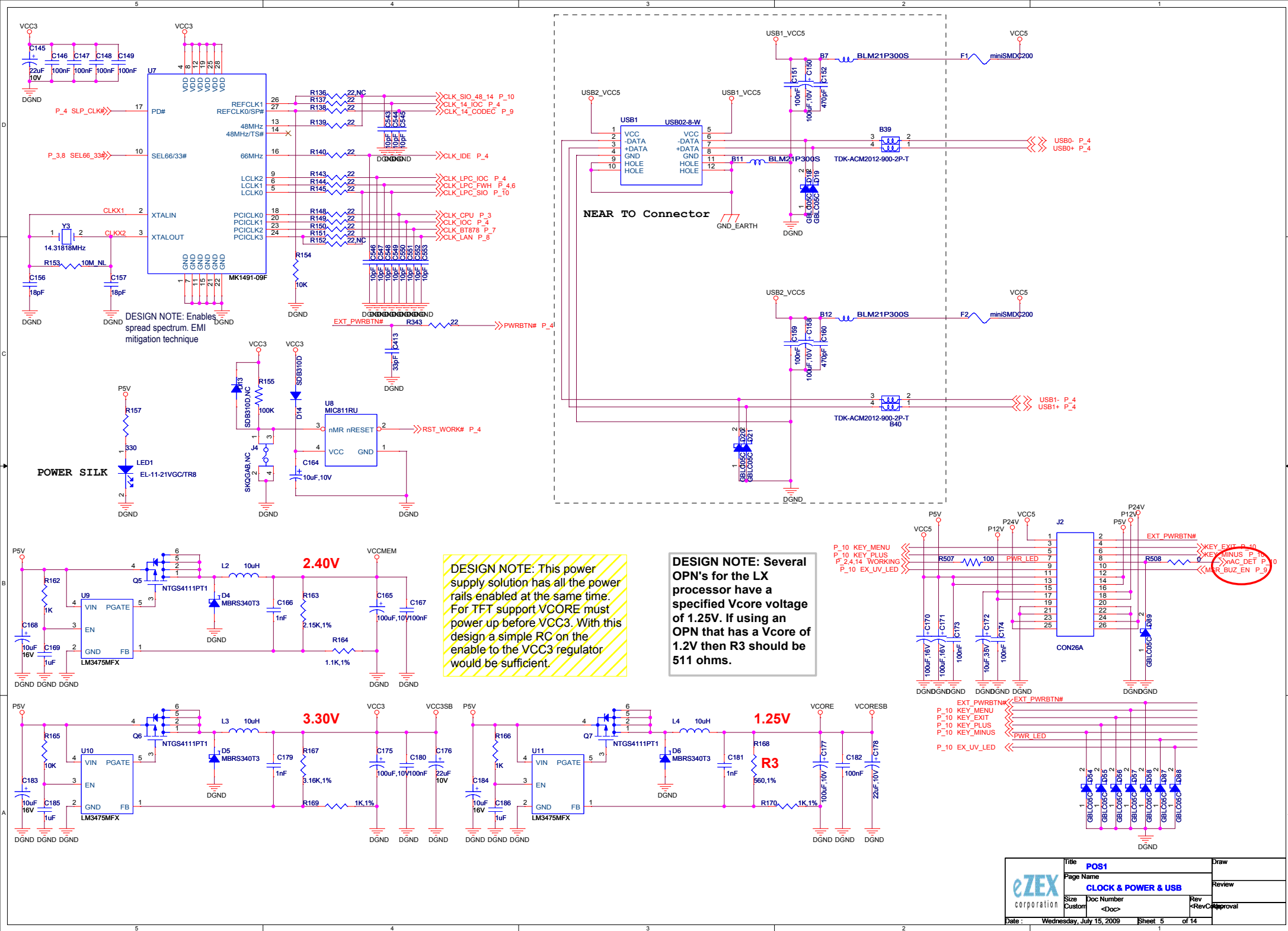


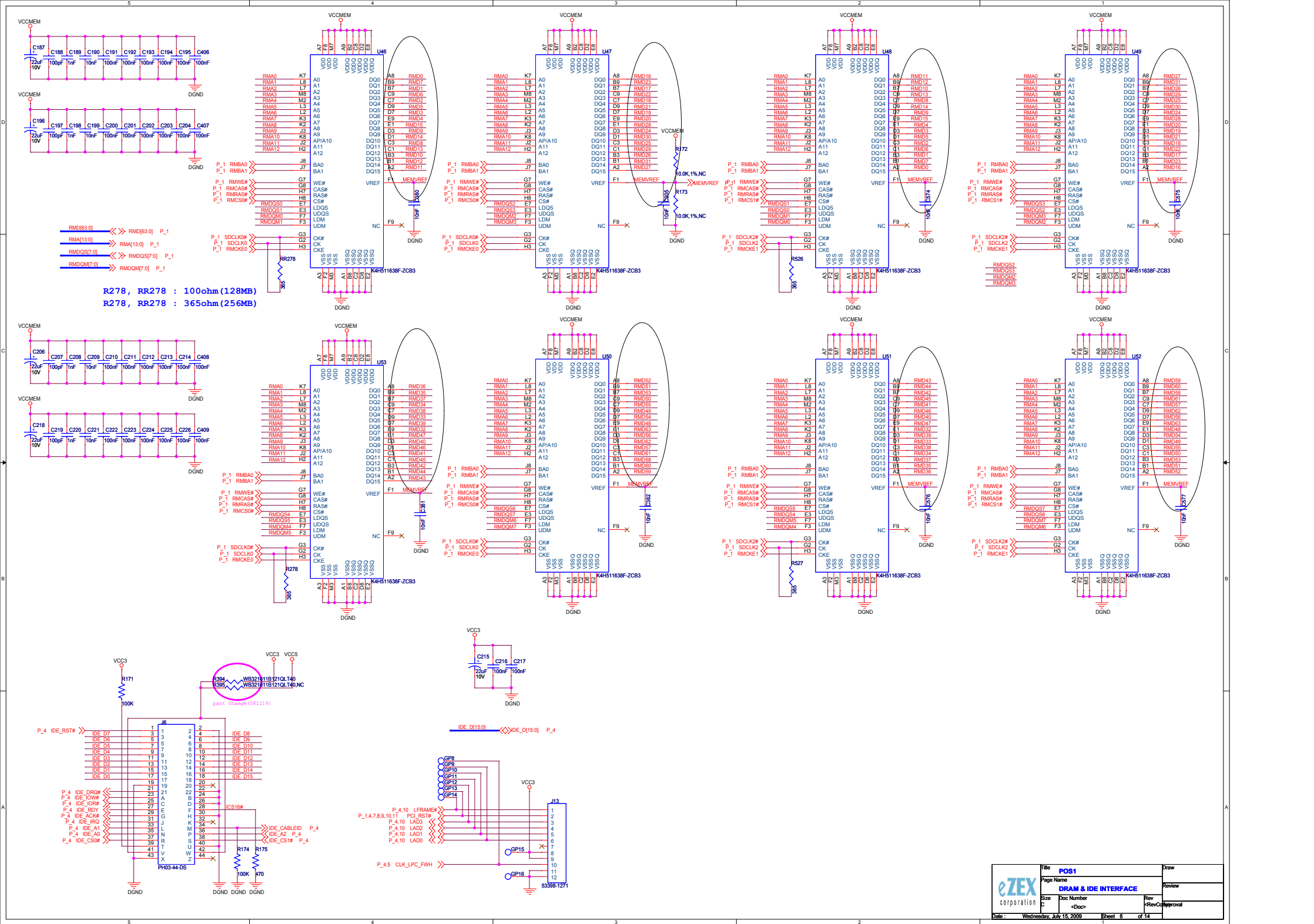


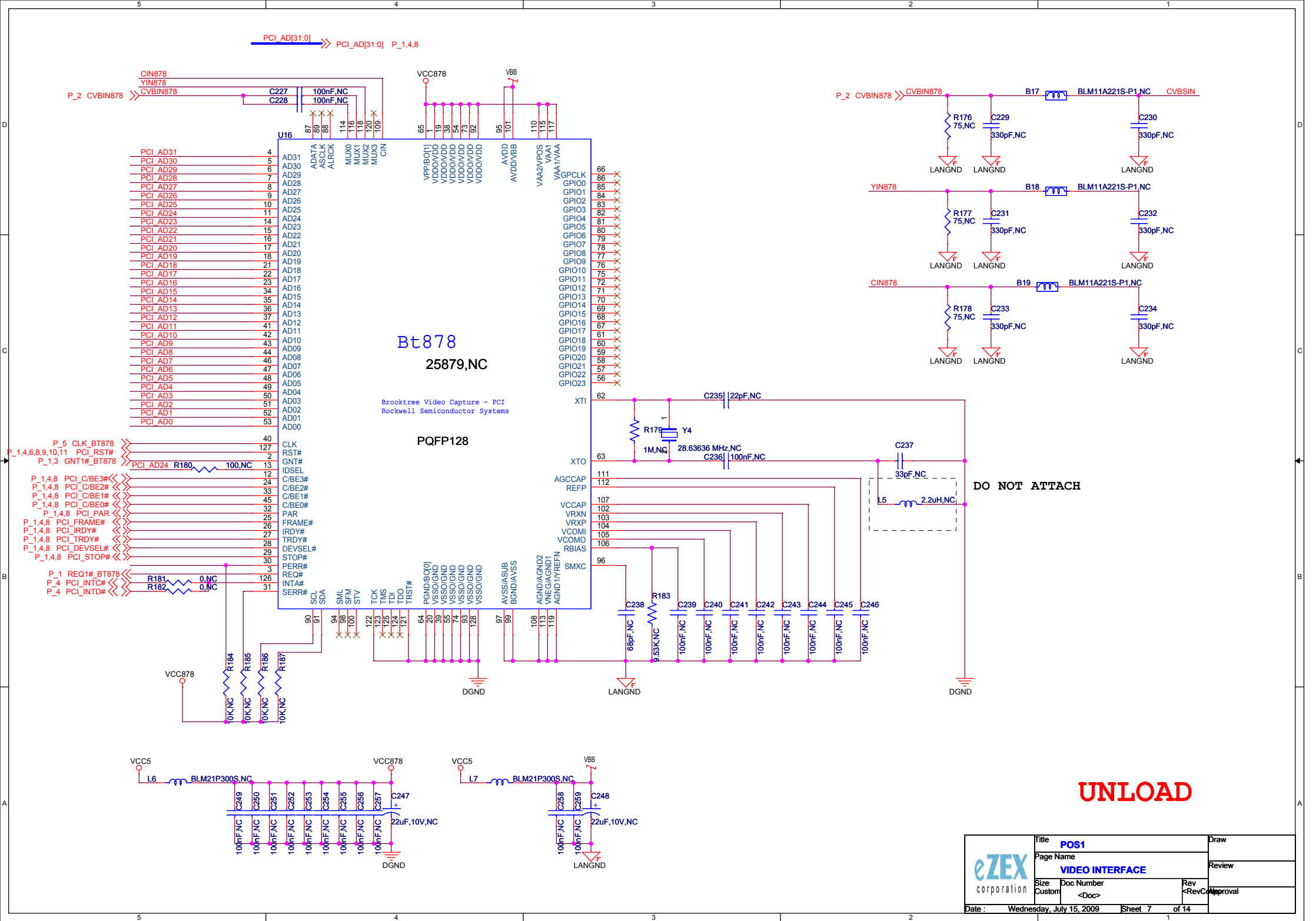








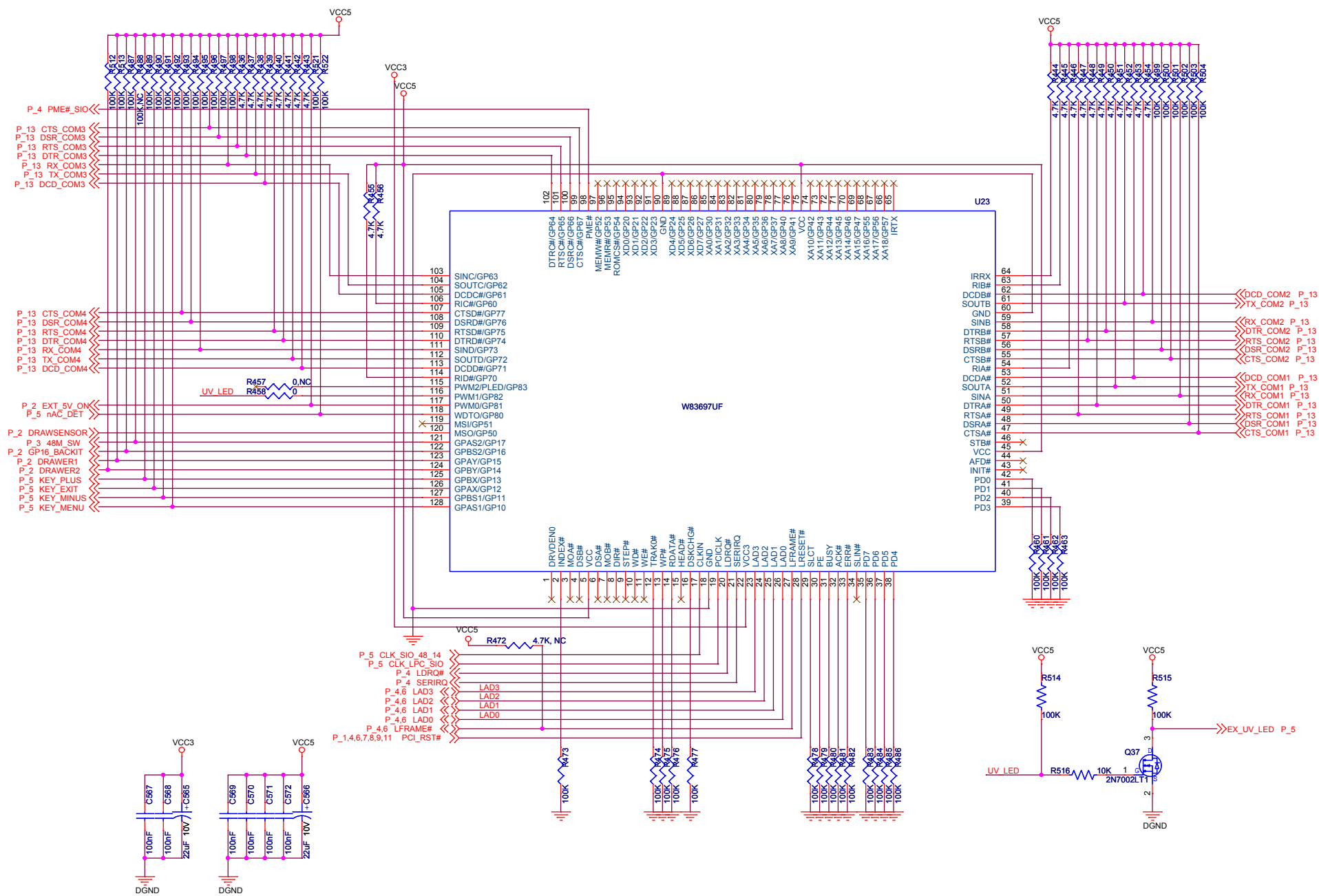








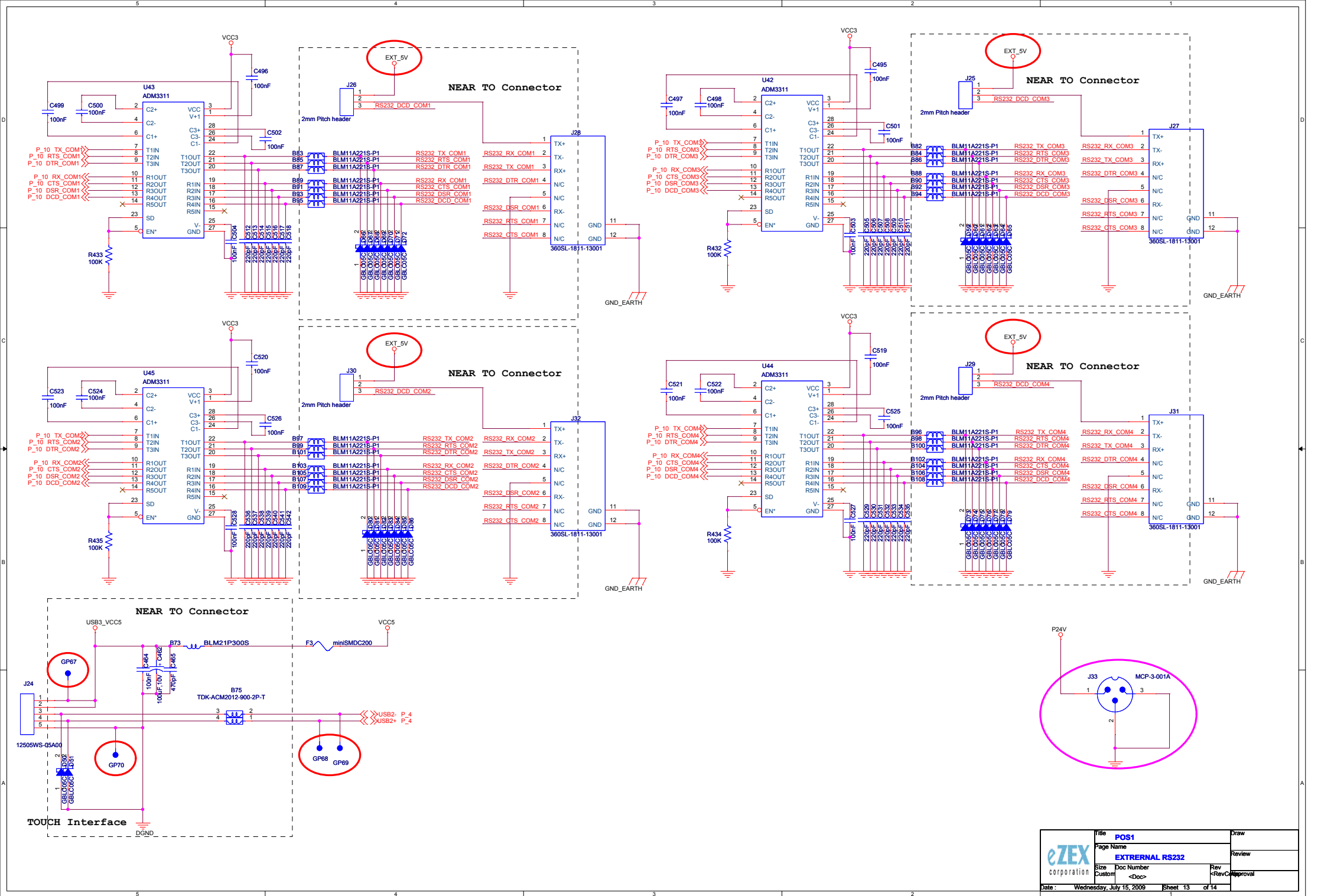


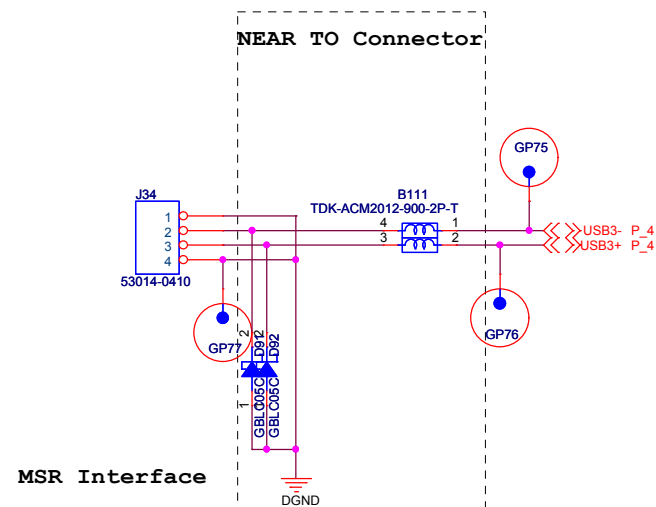
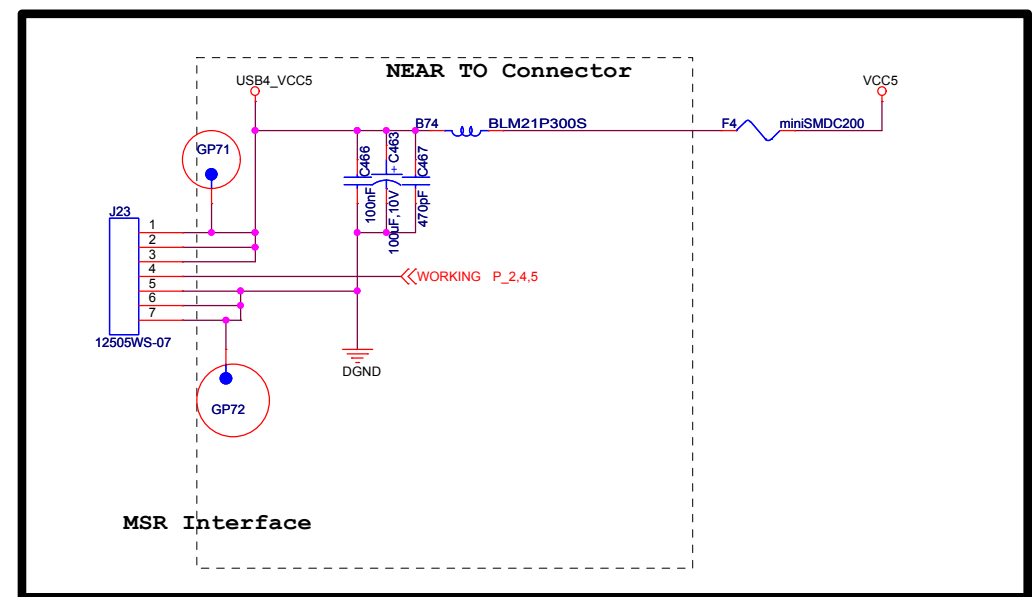













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	Page Name <b>USB_HUB</b>		Review
	Size B	Doc Number <b>&lt;Doc&gt;</b>	Rev <b>&lt;RevC&gt;</b>
			Approval
Date : Wednesday, July 15, 2009 Sheet 14 of 14			