FCC ID: X8V68038

Technical Description:

The brief circuit description is listed as follows:

- L2 acts as Loop Antenna.
- U2 (HL5233) acts as RFID Reader IC.
- X1 and associated circuit act as 13.56 MHz Oscillator.
- U1 (GPC11024) acts as MCU with Sound Synthesizer.
- PB1 act as StartKey Button.

Antenna Used:

A loop antenna has been used.



Features

- Low standby current.
- Low power consumption.
- Simple application circuit.
- Stable performance.
- The system and oscillator can be enable separately.
- 3 kinds of decoder outputs.
- Level hold mode and one-shot trigger mode.
- High active and low active output selectable.

<Patent : US6731177B2>

Applications

- Toy RFID.
- Asset control.
- Contactless entry control.
- Education.

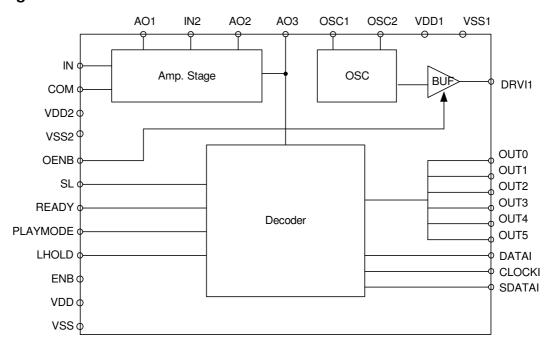
General Description

HL5233 is a CMOS IC used to perform the function of a RFID Reader. A RFID contains two parts: RFID TAG (HL5230) and RFID Reader (HL5233). HL5233 contains of a 13.56MHz crystal oscillator, a 13.56MHz output buffer, a preamplifier and data decoder. The output buffer drives an antenna which can transmits RF signal to the RFID TAG.

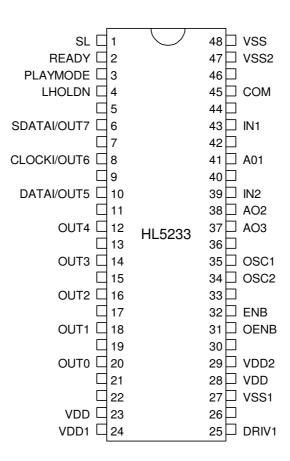
If TAG is close enough to the Reader, the encoder of TAG will send out a data train. The data train is used to modulate the RF signal in the TAG, and the amplitude of RF signal in the Reader will be modulated also. Preamplifier is used to amplify the modulating signal. The decoder is used to decoder the encoded data transmitted from TAG.

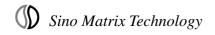
There are three kinds of output data: Synchronous, Asynchronous and Direct drive outputs. In order to interface to most of power Speech IC, the data rate of the outputs is slower than the data rate of the RFID TAG.

Block Diagram



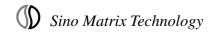
Pin Connection





Pin Description

PIN NO.	PIN NAME	DESCRIPTION				
1	SL	Data Bit Rate Select Pin. It is used to determine the bit rate received from TAG. SL = 1, Bit rate = 8KHz; SL = 0, Bit rate = 4KHz				
2	READY	Play Mode Select Pin. When PLAYMODE pin is high, this pin is used as Output Polarity Control Pin. When PLAYMODE pin is low this pin is used as Ready input pin. When READY = 0, output signal is not available.				
3	PLAYMODE	Output DATA Mode Control Pin. When PLAYMODE = 1, Out0 ~ Out4, DATAI, CLOCKI, and SDATAI is used as direct output pin. When PLAYMODE = 0, Out0 ~ Out4 is also used as direct output, but DATAI, CLOCKI and SDATAI is used as serial data output pin.				
4	LHOLDN	Level-Hold Control Pin. When LHOLDN = 0, DATA will be sent out continuously or output will active as long as TAG is closed to Reader. When LHOLDN = 1, only one set of DATA will be sent out or output will active for a short time.				
5	SDATAI	Serial Data Output. When PLAYMODE = 0, this pin is used as serial data output, i.e., DATA and CLOCK exist at same output. When PLAYMODE = 1, this pin is used as one of the direct output.				
6	CLOCKI	CLOCK Output. When PLAYMODE = 0, this pin (combined with DATAI,) is used as synchronous DATA output pin. When PLAYMODE = 1, this pin is used as one of the direct output pins.				
7	DATAI	DATA Output. (As illustrated in CLOCKI)				
8~12	Out0~Out4	Direct Output Pin.				
13	VDD	Positive Power Supply Terminal.				
14	VDD1	Positive Power Supply Terminal.				
15	DRIV1	Coil Driver Output of 13.56MHz oscillator.				
16	VSS1	Negative Power Supply Terminal.				
17	VDD	Positive Power Supply Terminal.				
18	VDD2	Positive Power Supply Terminal of Preamplifier.				
19	OENB	Coil Driver Enable Pin. When OENB = 0, coil driver will disable, others circuit still work. When OENB = 1, coil driver enable.				
20	ENB	Enable Input Pin of the whole system.				
21	OSC2	Oscillator Output Pin.				
22	OSC1	Oscillator Input Pin.				
23	AO3	Output Pin of 3 rd stage of Preamplifier.				
24	AO2	Output Pin of 2 nd stage of Preamplifier.				
25	IN2	Inverting Input Pin of 2 nd stage of Preamplifier.				
26	AO1	Output Pin of 1 st stage of Preamplifier.				
27	IN1	Inverting Input Pin of 1 st stage of Preamplifier.				
28	COM	Common Input Pin of Preamplifier.				
29	VSS2	Negative Power Supply Terminal of Preamplifier.				
30	VSS	Negative Power Supply Terminal.				



Absolute Maximum Ratings

Power Supply 5V

Input Voltage VSS-0.3V to VDD+0.3V

Electrical Characteristics

SYSTEM	DESCRIPTION	TEST CONDITION	LIMIT			UNIT
OTOTEM			MIN.	TYP.	MAX.	OIVIII
VDD	Supply Voltage		3	4.5	5	V
VIL	Input Voltage Low	VDD=4.5V			0.3*VDD	V
VIH	Input Voltage High	VDD=4.5V	0.7*VDD			V
VOSC	Oscillator Starting Voltage			2.2		V
IOP1	Operating Current 1	VDD=4.5V		19*		mA
IOP2	Operating Current 2 (Driver Off)	VDD=4.5V		0.4		mA
IST	Stand-by Current	VDD=4.5V		0.5		uA

^{*} IOP depends on external coil.

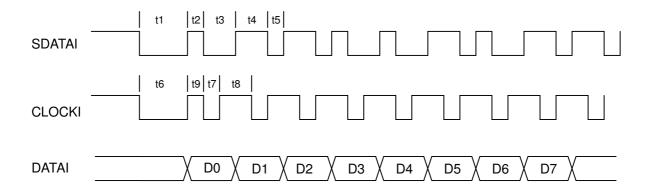
Functional Description

There are three major function provided by HL5233: support a 13.56MHz driver, to transform DATA Bit rate for easy interface with MCU or power Speech IC and to provide direct decoder output.

After received the modulating signal from the RFID TAG, the modulating signal is amplified and filtered by preamplifier. There is decoder and error detector built in the HL5233. The decoded output can be sent to output pin directly, or encoded again at a slower bit rate. When PLAYMODE = 1, there are 8 direct output provided. Besides the 3 bits which is used as decoder inputs, there is 1 bit, which is used as parity check bit. The output will be activated only when parity is correct. In HL5233 even parity is used, Bit0~Bit2 is used as decoder input and Bit7 is parity Bit.

OENB is coil driver enable pin. When OENB=0, coil driver is off, while others circuit still work.

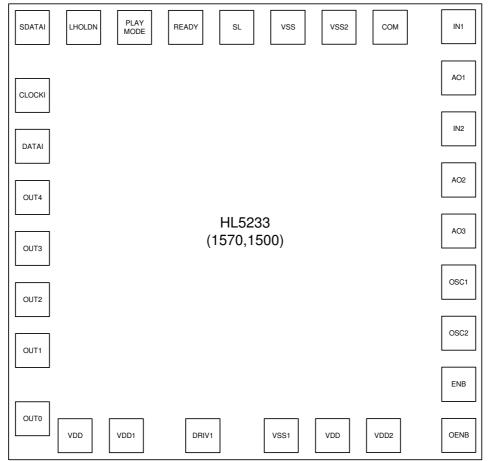
Data I/O Format in Serial Mode



SL = 0			
t1 (Start)	: 2.84 ms	t6 (Start)	: 2.84 ms
t2 (Data Low Front-end)	: 0.95 ms	t7 (Clock Low Period)	: 0.95 ms
t3 (Data Low Back-end)	: 1.89 ms	t8 (Clock High Back-end)	: 1.89 ms
t4 (Data High Front-end)	: 1.89 ms	t9 (Clock High Front-end)	: 0.95 ms
t5 (Data High Back-end)	: 0.95 ms		

SL = 1			
t1 (Start)	: 1.42 ms	t6 (Start)	: 1.42 ms
t2 (Data Low Front-end)	: 0.47 ms	t7 (Clock Low Period)	: 0.47 ms
t3 (Data Low Back-end)	: 0.95 ms	t8 (Clock High Back-end)	: 0.95 ms
t4 (Data High Front-end)	: 0.95 ms	t9 (Clock High Front-end)	: 0.47 ms
t5 (Data High Back-end)	: 0.47 ms		

Bonding Pad Diagram

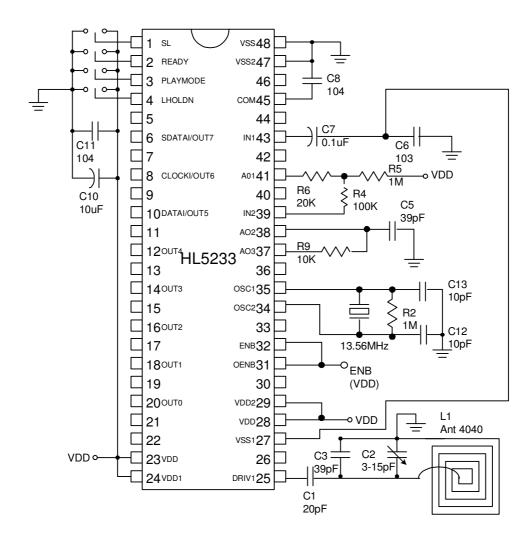


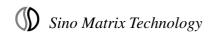
Note: Substrate is connected to VSS.

PAD	X, Y Unit: μm	PAD	X, Y Unit: μm	PAD	X, Y Unit: μm
VDD	278, 98	A03	1373, 703	PLAYMODE	428, 1303
VDD1	428, 98	AO2	1373, 853	LHOLDN	278, 1303
DRIV1	662, 98	IN2	1373, 1003	SDATAI	128, 1303
VSS1	872, 98	AO1	1373,1153	SLOCKI	128, 1099
VDD	1026, 98	IN1	1373, 1303	DATAI	128, 946
VDD2	1176, 98	COM	1178, 1303	OUT4	128, 796
OENB	1373, 98	VSS2	1028, 1303	OUT3	128, 643
ENB	1373, 248	VSS	878, 1303	OUT2	128, 493
OSC2	1373, 403	SL	728, 1303	OUT1	128, 304
OSC1	1373, 553	READY	578, 1303	OUT0	128, 138

Application Circuit 1

(Envelope Detector with Diode)





Document History

Change History					
Rev A	7/16/2007	Final Document			

Sino Matrix Technology does not assume any responsibility for use of any circuitry described and Sino Matrix Technology reserves the right to change the circuitry and specifications without notice at any time.

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