DISCRETE SEMICONDUCTORS

DATA SHEET

BF1201; BF1201R; BF1201WR N-channel dual-gate PoLo MOS-FETs

Product specification Supersedes data of 1999 Dec 01 2000 Mar 29





N-channel dual-gate PoLo MOS-FETs

BF1201; BF1201R; BF1201WR

FEATURES

- Short channel transistor with high forward transfer admittance to input capacitance ratio
- Low noise gain controlled amplifier
- Partly internal self-biasing circuit to ensure good cross-modulation performance during AGC and good DC stabilization.

APPLICATIONS

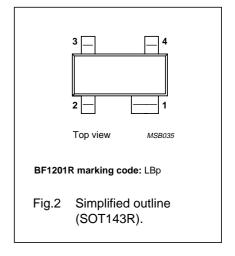
 VHF and UHF applications with 3 to 9 V supply voltage, such as digital and analogue television tuners and professional communications equipment.

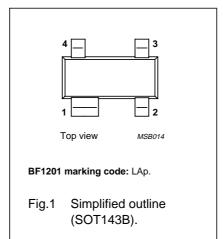
DESCRIPTION

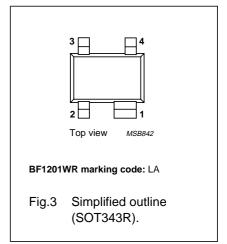
Enhancement type N-channel field-effect transistor with source and substrate interconnected. Integrated diodes between gates and source protect against excessive input voltage surges. The BF1201, BF1201R and BF1201WR are encapsulated in the SOT143B, SOT143R and SOT343R plastic packages respectively.

PINNING

PIN	DESCRIPTION
1	source
2	drain
3	gate 2
4	gate 1







QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{DS}	drain-source voltage		-	-	10	V
I _D	drain current		_	1-	30	mA
P _{tot}	total power dissipation		_	_	200	mW
y _{fs}	forward transfer admittance		23	28	35	mS
C _{ig1-ss}	input capacitance at gate 1		_	2.6	3.1	pF
C _{rss}	reverse transfer capacitance	f = 1 MHz	_	15	30	fF
F	noise figure	f = 400 MHz	_	1	1.8	dB
X _{mod}	cross-modulation	input level for k = 1% at 40 dB AGC	105	_	_	dBμV
Ti	operating junction temperature		_	_	150	°C

CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

N-channel dual-gate PoLo MOS-FETs

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

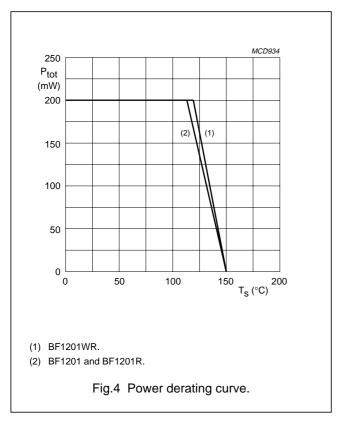
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		_	10	V
I _D	drain current (DC)		_	30	mA
I _{G1}	gate 1 current		_	±10	mA
I _{G2}	gate 2 current		_	±10	mA
P _{tot}	total power dissipation				
	BF1201; BF1201R	T _s ≤ 113 °C; note 1	_	200	mW
	BF1201WR	T _s ≤ 109 °C; note 1	_	200	mW
T _{stg}	storage temperature		-65	+150	°C
T _i	operating junction temperature		_	150	°C

Note

1. T_s is the temperature of the soldering point of the source lead.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
R _{th j-s}	thermal resistance from junction to soldering point		
	BF1201; BF1201R	185	K/W
	BF1201WR	155	K/W



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BF1201; BF1201R; BF1201WR

STATIC CHARACTERISTICS

 $T_i = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{(BR)DSS}	drain-source breakdown voltage	$V_{G1-S} = V_{G2-S} = 0$; $I_D = 10 \mu A$	10	_	V
V _{(BR)G1-SS}	gate 1-source breakdown voltage	$V_{G2-S} = V_{DS} = 0$; $I_{G1-S} = 10 \text{ mA}$	6	_	V
V _{(BR)G2-SS}	gate 2-source breakdown voltage	$V_{G1-S} = V_{DS} = 0$; $I_{G2-S} = 10 \text{ mA}$	6	_	V
V _{(F)S-G1}	forward source-gate 1 voltage	$V_{G2-S} = V_{DS} = 0$; $I_{S-G1} = 10 \text{ mA}$	0.5	1.5	V
V _{(F)S-G2}	forward source-gate 2 voltage	$V_{G1-S} = V_{DS} = 0$; $I_{S-G2} = 10 \text{ mA}$	0.5	1.5	V
V _{G1-S(th)}	gate 1-source threshold voltage	$V_{G2-S} = 4 \text{ V}; V_{DS} = 5 \text{ V}; I_D = 100 \mu\text{A}$	0.3	1.0	V
V _{G2-S(th)}	gate 2-source threshold voltage	$V_{G1-S} = V_{DS} = 5 \text{ V}; I_D = 100 \mu\text{A}$	0.3	1.2	V
I _{DSX}	drain-source current	$V_{G2-S} = 4 \text{ V}; V_{DS} = 5 \text{ V}; R_{G1} = 62 \text{ k}\Omega;$ note 1	11	19	mA
I _{G1-SS}	gate 1 cut-off current	$V_{G2-S} = V_{DS} = 0; V_{G1-S} = 5 \text{ V}$	_	50	nA
I _{G2-SS}	gate 2 cut-off current	$V_{G1-S} = V_{DS} = 0; V_{G2-S} = 4 \text{ V}$	_	20	nA

Note

1. R_{G1} connects G_1 to $V_{GG} = 5$ V.

DYNAMIC CHARACTERISTICS

Common source; $T_{amb} = 25$ °C; $V_{G2-S} = 4$ V; $V_{DS} = 5$ V; $I_D = 15$ mA; unless otherwise specified.

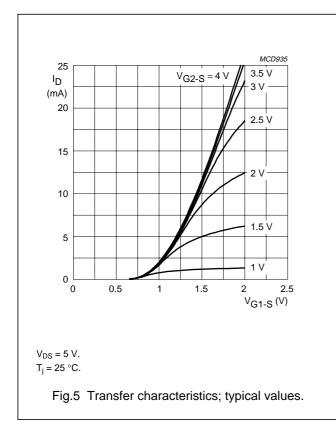
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
y _{fs}	forward transfer admittance	pulsed; T _j = 25 °C	23	28	35	mS
C _{ig1-ss}	input capacitance at gate 1	f = 1 MHz	_	2.6	3.1	pF
C _{ig2-ss}	input capacitance at gate 2	f = 1 MHz	_	1.1	_	pF
C _{oss}	output capacitance	f = 1 MHz	_	0.9	_	pF
C _{rss}	reverse transfer capacitance	f = 1 MHz	_	15	30	fF
F	noise figure	$f = 10.7 \text{ MHz}; G_S = 20 \text{ mS}; B_S = 0$	_	5	7	dB
		$f = 400 \text{ MHz}; Y_S = Y_{S \text{ opt}}$	_	1	1.8	dB
		f = 800 MHz; Y _S = Y _{S opt}	_	1.9	2.5	dB
G _{tr}	power gain	$f = 200 \text{ MHz}; G_S = 2 \text{ mS}; B_S = B_{S \text{ opt}};$	_	33.5	_	dB
		$G_L = 0.5 \text{ mS}; B_L = B_{L \text{ opt}};$				
		$f = 400 \text{ MHz}; G_S = 2 \text{ mS}; B_S = B_{S \text{ opt}};$ $G_L = 1 \text{ mS}; B_L = B_{L \text{ opt}};$	_	29	_	dB
		$f = 800 \text{ MHz}; G_S = 3.3 \text{ mS}; B_S = B_{S \text{ opt}};$ $G_L = 1 \text{ mS}; B_L = B_{L \text{ opt}};$	_	24	_	dB
X _{mod}	cross-modulation	input level for k = 1%; f _w = 50 MHz; f _{unw} = 60 MHz; note 1				
		at 0 dB AGC	90	_	_	dΒμV
		at 10 dB AGC	_	95	_	dBμV
		at 40 dB AGC	105	_	_	dΒμV

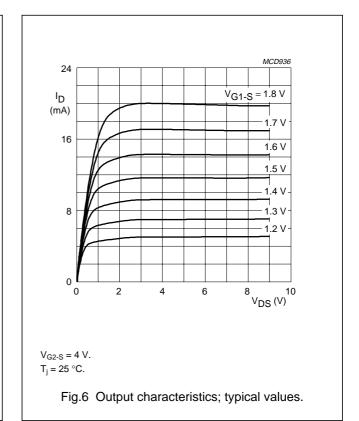
Note

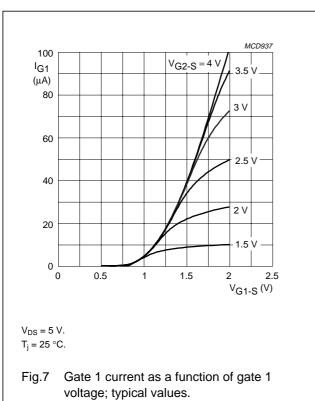
1. Measured in Fig.21 test circuit.

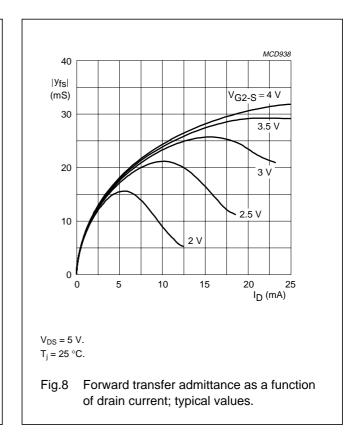
N-channel dual-gate PoLo MOS-FETs

BF1201; BF1201R; BF1201WR



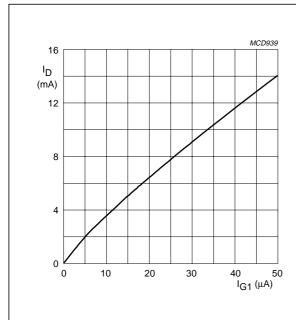






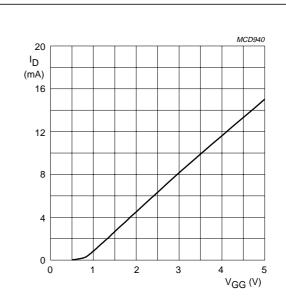
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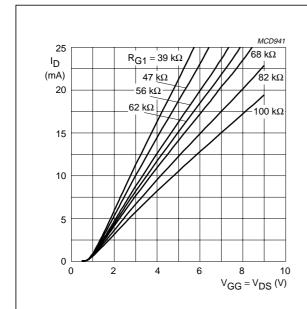
 V_{DS} = 5 V; V_{G2-S} = 4 V. T_j = 25 °C.

Fig.9 Drain current as a function of gate 1 current; typical values.



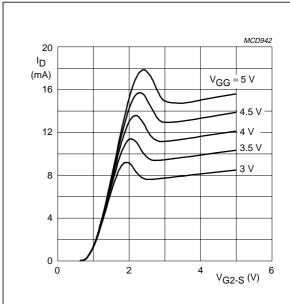
 V_{DS} = 5 V; $V_{G2\text{-}S}$ = 4 V; T_j = 25 °C. R_{G1} = 62 k Ω (connected to V_{GG}); see Fig.21.

Fig.10 Drain current as a function of gate 1 supply voltage (= V_{GG}); typical values.



 V_{G2-S} = 4 V; T_j = 25 °C. R_{G1} connected to V_{GG} ; see Fig.21.

Fig.11 Drain current as a function of gate 1 (= V_{GG}) and drain supply voltage; typical values.



 $V_{DS} = 5 \text{ V}; T_j = 25 \,^{\circ}\text{C}.$

 R_{G1} = 62 k Ω (connected to V_{GG}); see Fig.21.

Fig.12 Drain current as a function of gate 2 voltage; typical values.

N-channel dual-gate PoLo MOS-FETs

BF1201; BF1201R; BF1201WR

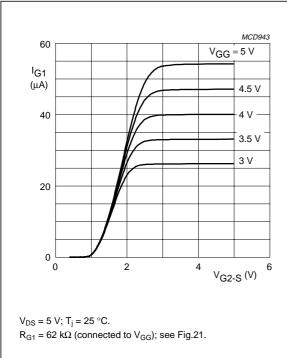


Fig.13 Gate 1 current as a function of gate 2 voltage; typical values.

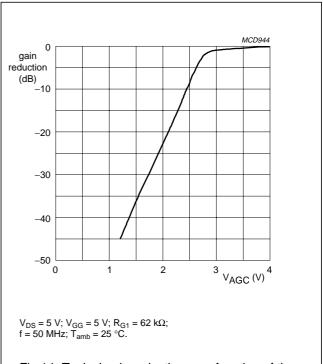


Fig.14 Typical gain reduction as a function of the AGC voltage; see Fig.21.

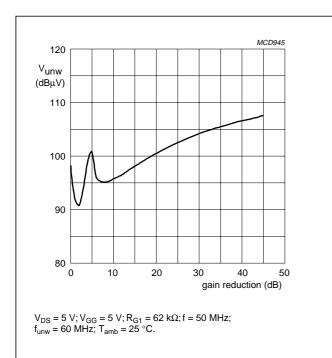
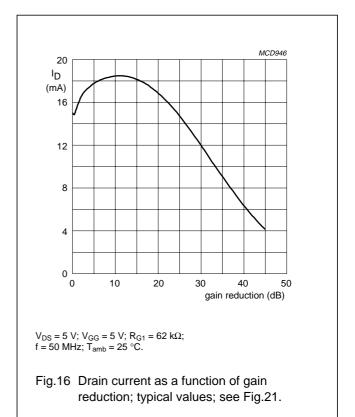
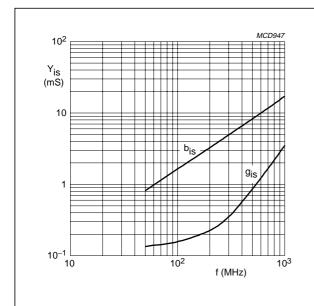


Fig.15 Unwanted voltage for 1% cross-modulation as a function of gain reduction; typical values; see Fig.21.



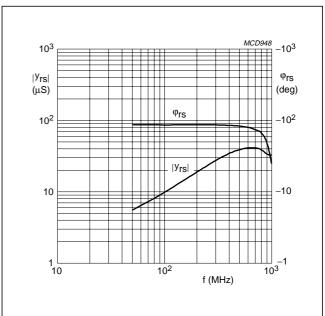
N-channel dual-gate PoLo MOS-FETs

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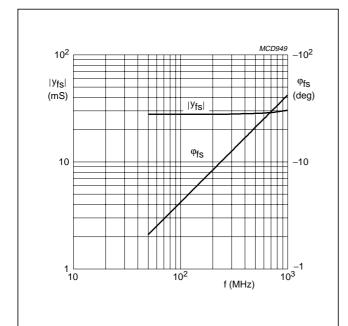
 V_{DS} = 5 V; V_{G2} = 4 V. I_{D} = 15 mA; T_{amb} = 25 °C.

Fig.17 Input admittance as a function of frequency; typical values.



 $V_{DS} = 5 \text{ V}; V_{G2} = 4 \text{ V}.$ $I_{D} = 15 \text{ mA}; T_{amb} = 25 ^{\circ}\text{C}.$

Fig.18 Reverse transfer admittance and phase as a function of frequency; typical values.



 V_{DS} = 5 V; V_{G2} = 4 V. I_{D} = 15 mA; T_{amb} = 25 °C.

Fig.19 Forward transfer admittance and phase as a function of frequency; typical values.

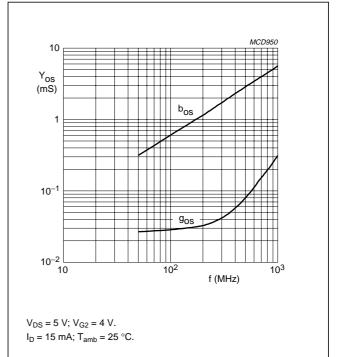


Fig.20 Output admittance as a function of frequency; typical values.

N-channel dual-gate PoLo MOS-FETs

BF1201; BF1201R; BF1201WR

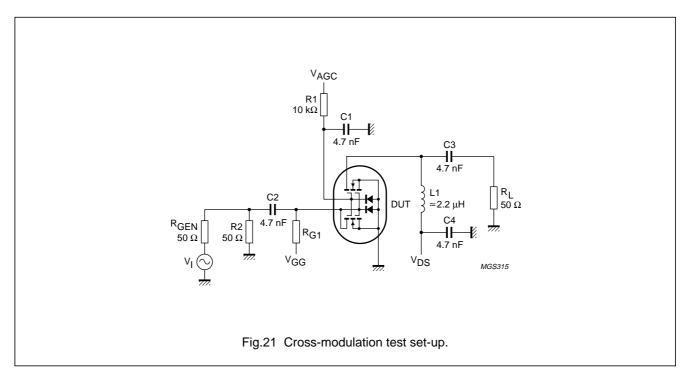


Table 1 Scattering parameters: $V_{DS} = 5 \text{ V}$; $V_{G2-S} = 4 \text{ V}$; $I_D = 15 \text{ mA}$; $T_{amb} = 25 ^{\circ}\text{C}$

f	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
(MHz)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
50	0.987	-4.72	2.775	174.6	0.0006	88.8	0.997	-1.84
100	0.985	-9.39	2.774	169.5	0.0010	86.7	0.997	-3.37
200	0.978	-18.59	2.731	159.1	0.0019	79.7	0.996	-6.72
300	0.976	-27.74	2.671	148.8	0.0026	74.2	0.994	-10.02
400	0.949	-36.59	2.599	138.8	0.0032	69.9	0.992	-13.33
500	0.928	-45.08	2.501	129.1	0.0035	65.9	0.989	-16.55
600	0.905	-53.26	2.400	119.8	0.0035	64.6	0.986	-19.64
700	0.882	-61.07	2.297	110.9	0.0033	65.7	0.982	-22.63
800	0.860	-68.48	2.199	102.4	0.0029	69.1	0.979	-25.54
900	0.838	-75.55	2.096	94.2	0.0024	83.3	0.975	-28.44
1000	0.818	-82.23	1.997	86.3	0.0021	103.8	0.971	-31.42

Table 2 Noise data: $V_{DS} = 5 \text{ V}$; $V_{G2-S} = 4 \text{ V}$; $I_D = 15 \text{ mA}$; $T_{amb} = 25 ^{\circ}\text{C}$

f	F _{min}	Γ	opt	R _n
(MHz)	(dB)	(ratio)	(deg)	(Ω)
400	1	0.825	38.93	50
800	1.9	0.753	70.65	38.75

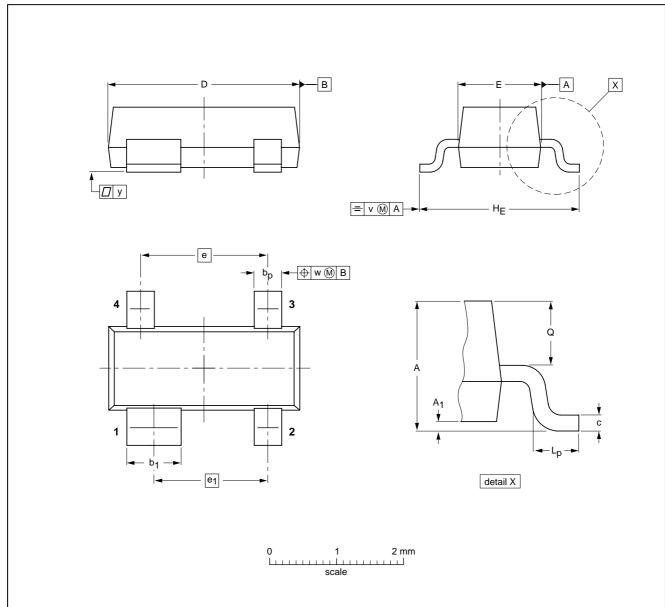
N-channel dual-gate PoLo MOS-FETs

BF1201; BF1201R; BF1201WR

PACKAGE OUTLINES

Plastic surface mounted package; 4 leads

SOT143B



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max	bp	b ₁	C	D	E	е	e ₁	HE	Lp	Q	v	w	у
mm	1.1 0.9	0.1	0.48 0.38	0.88 0.78	0.15 0.09	3.0 2.8	1.4 1.2	1.9	1.7	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1	0.1

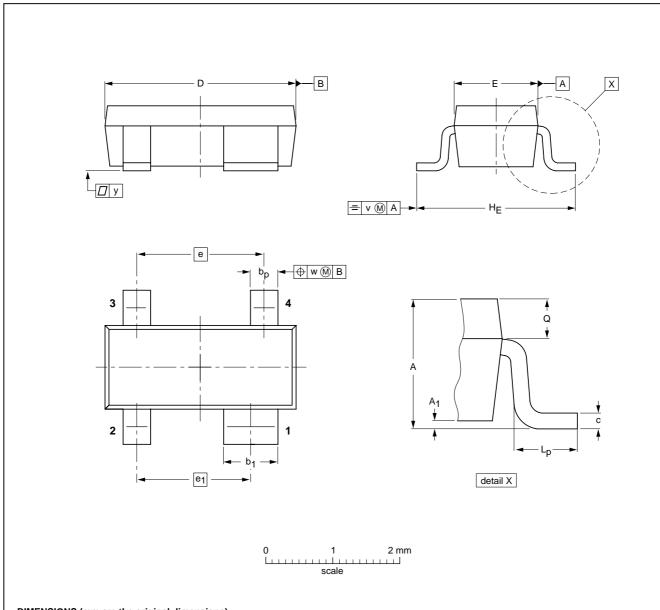
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VERSION	IEC JEDEC EIAJ			PROJECTION	ISSUE DATE	
SOT143B						97-02-28

N-channel dual-gate PoLo MOS-FETs

BF1201; BF1201R; BF1201WR

Plastic surface mounted package; reverse pinning; 4 leads

SOT143R



DIMENSIONS (mm are the original dimensions)

UNIT	Α	A ₁ max	bp	b ₁	С	D	E	е	e ₁	HE	Lp	Q	v	w	у
mm	1.1 0.9	0.1	0.48 0.38	0.88 0.78	0.15 0.09	3.0 2.8	1.4 1.2	1.9	1.7	2.5 2.1	0.55 0.25	0.45 0.25	0.2	0.1	0.1

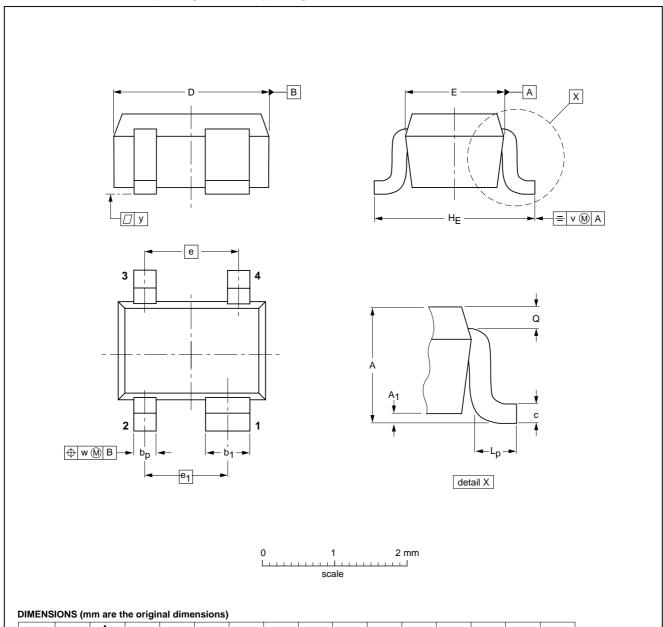
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VERSION	IEC	JEDEC	EIAJ	PROJECTION	ISSUE DATE	
SOT143R			SC-61B		97-03-10 99-09-13	

N-channel dual-gate PoLo MOS-FETs

BF1201; BF1201R; BF1201WR

Plastic surface mounted package; reverse pinning; 4 leads

SOT343R



UNIT	А	A ₁ max	bp	b ₁	С	D	E	е	e ₁	HE	Lp	Q	v	w	у
mm	1.1 0.8	0.1	0.4 0.3	0.7 0.5	0.25 0.10	2.2 1.8	1.35 1.15	1.3	1.15	2.2 2.0	0.45 0.15	0.23 0.13	0.2	0.2	0.1

OUTLINE		REFER	EUROPEAN	ICCUIE DATE			
VERSION	IEC	JEDEC	EIAJ		PROJECTION	ISSUE DATE	
SOT343R						97-05-21	

N-channel dual-gate PoLo MOS-FETs

BF1201; BF1201R; BF1201WR

DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS (1)
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Note

Please consult the most recently issued data sheet before initiating or completing a design.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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2000 Mar 29

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NOTES

N-channel dual-gate PoLo MOS-FETs

BF1201; BF1201R; BF1201WR

NOTES

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