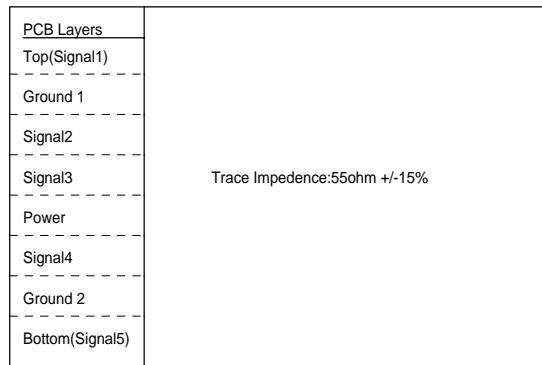


Voltage Rails

+VDC	Primary DC system power supply (6V-9.5V)
+VBATTERY	Battery Power supply (6-8.4V)
+VCC_CORE	Core Voltage for CPU
+V1.05S	1.05V for Calistoga & ICH7M core / FSB VTT
+V1.8	1.8V power rail for DDR2
+V0.9S	0.9V DDR2 Termination voltage
+V3.3AL	3.3V always on power rail
+V5AL	5V for ICH7-M's VCC5 Refsus
+V3.3S	3.3V main power rail
+V5S	5V main power rail
+V2.5S	2.5V power rail for 945GMS

Board stack up description



USB Table

USB Port#	Function Description
0	
1	
2	
3	
4	
5	
6	
7	

I2C SMB Address

Device	Address	Hex	Master
Clock Generator	1101 001x	D2	ICH7-M
SO-DIMMO	1010 000x	A0	ICH7-M
CPU Thermal Sensor	1001 100x	98	KBC
Smart Battery	0001 011x	16	KBC
PCIE Slot	TBD	TBD	ICH7-M

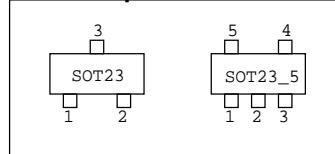
Power States

Signal	SLP_S3#	SLP_S4#	SLP_S5#	+V*ALW	+V*	+V*S	Clock
S0 (Full On)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (STM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (STD)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (SoftOff)	LOW	LOW	LOW	ON	OFF	OFF	OFF

Wake up Events

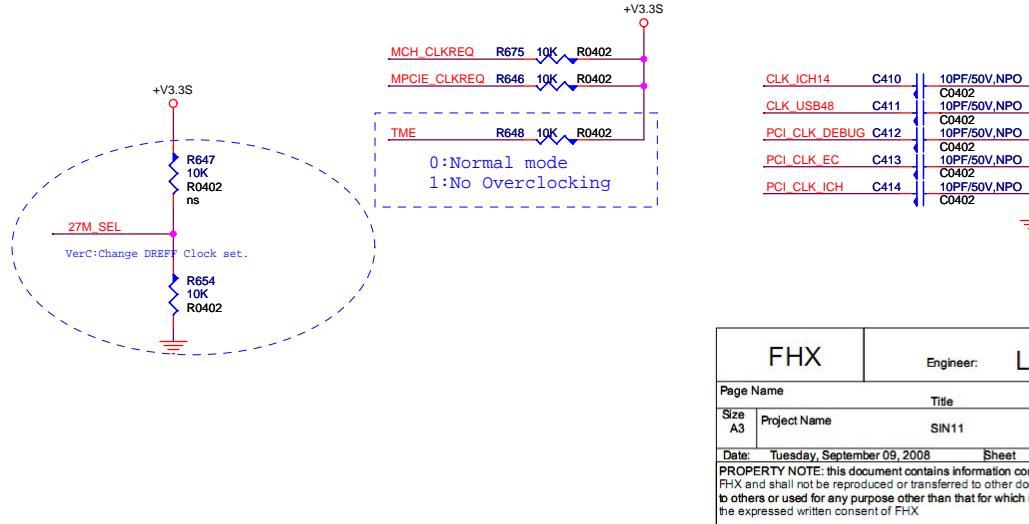
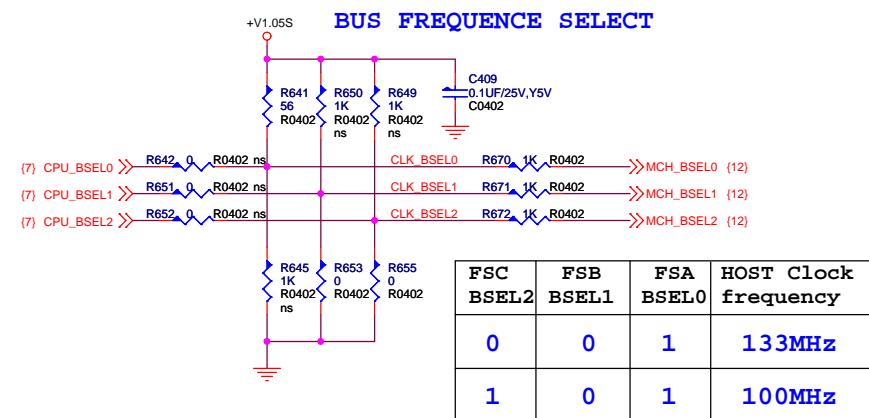
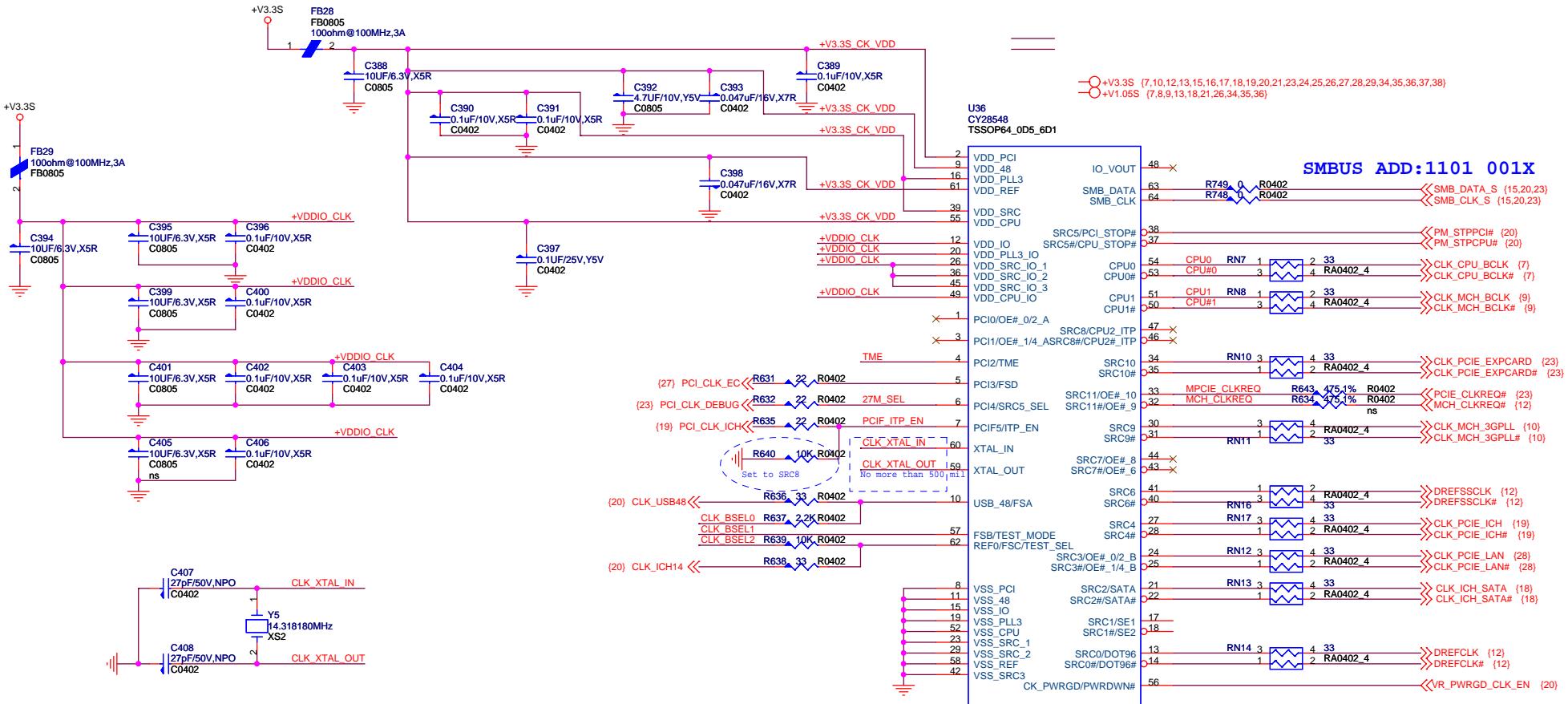
LID switch from EC
Power switch from EC

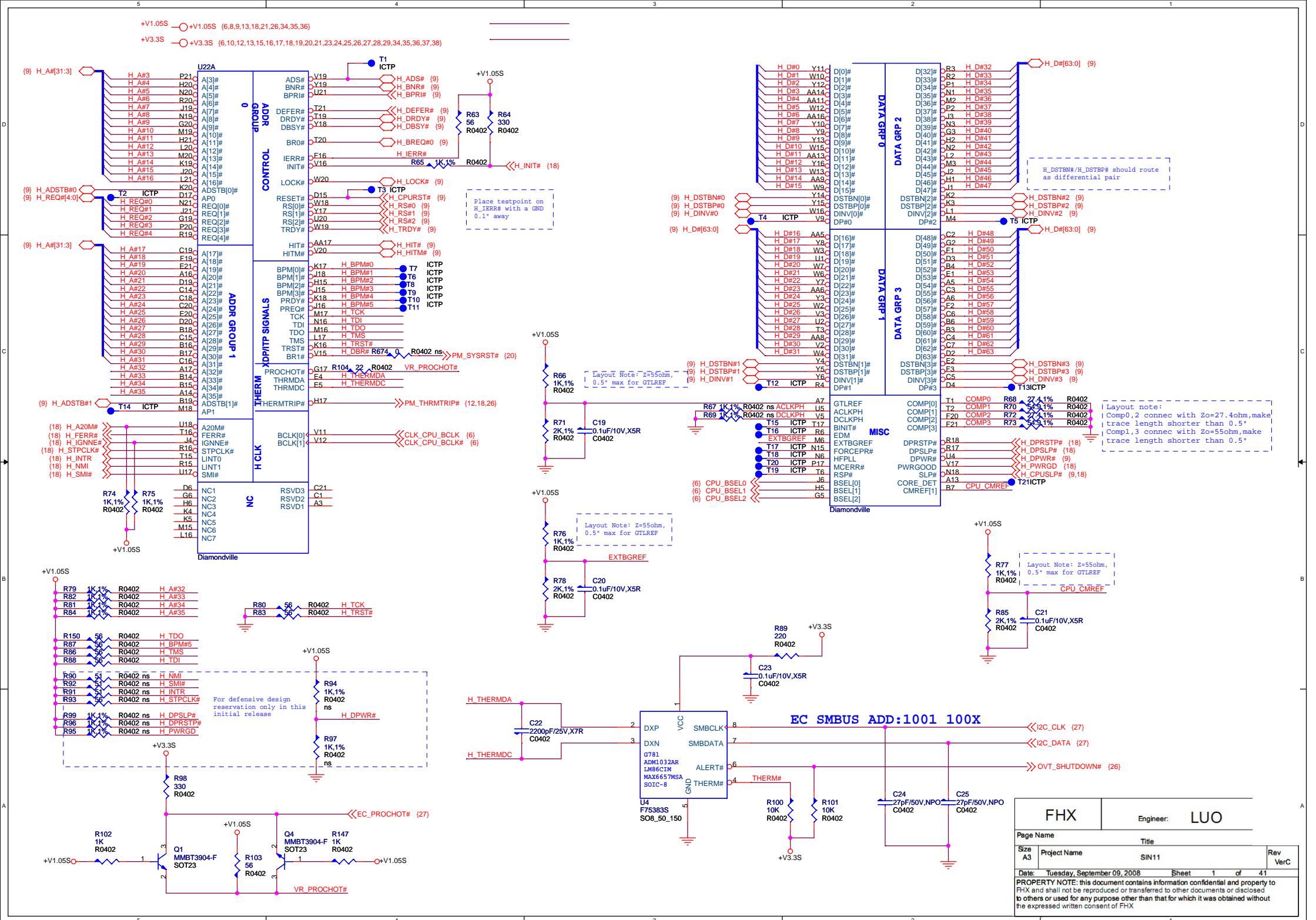
PCB Footprints

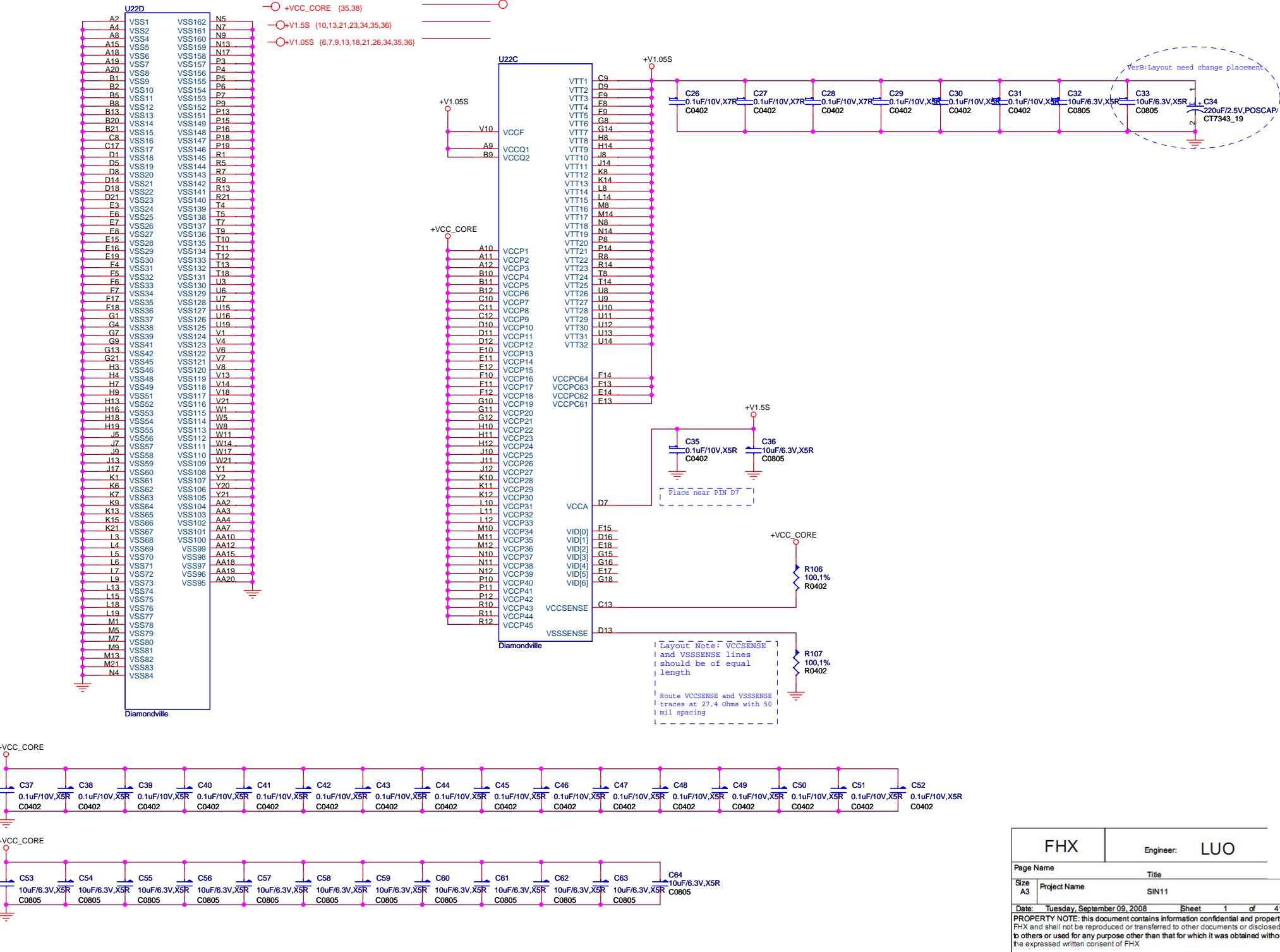


ns: Component marked "ns" is not stuff

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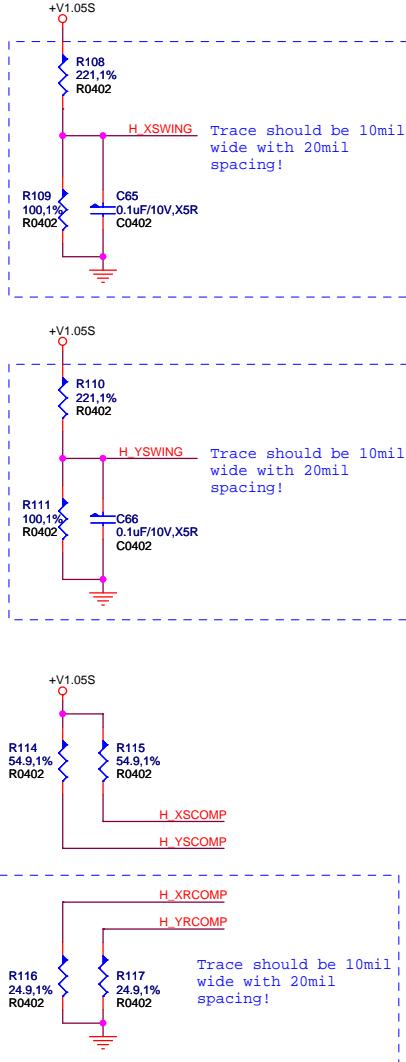






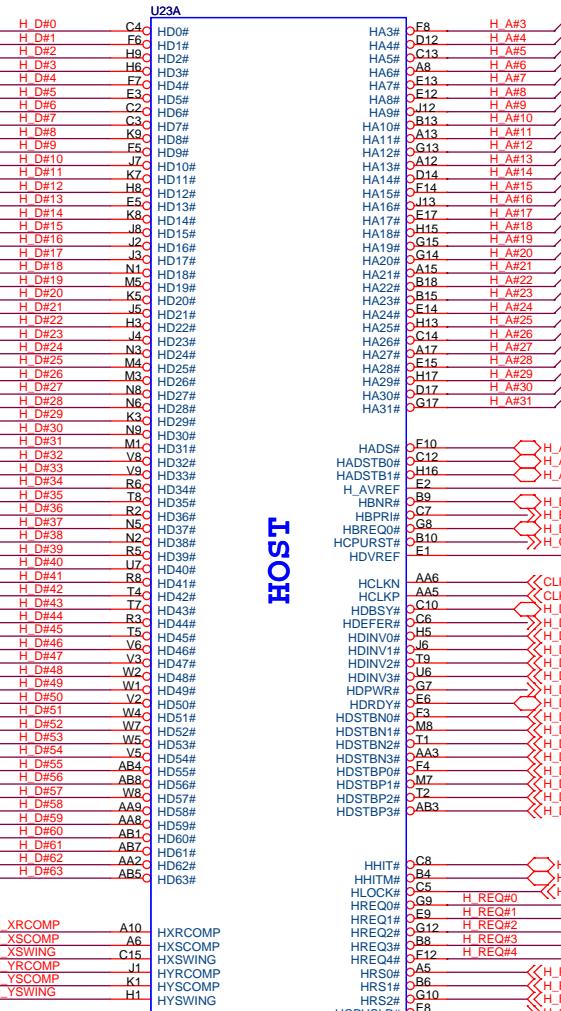
FHX		Engineer: LUO
Page Name	Title	
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+V1.05S —○+V1.05S {6,7,8,13,18,21,26,34,35,36}



(7) H_D#[63:0]

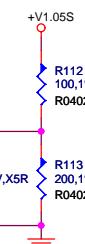
U23A



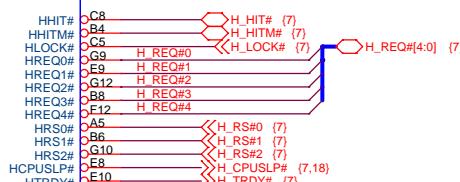
HOST

945GMS

H_A#[31:3] (7)

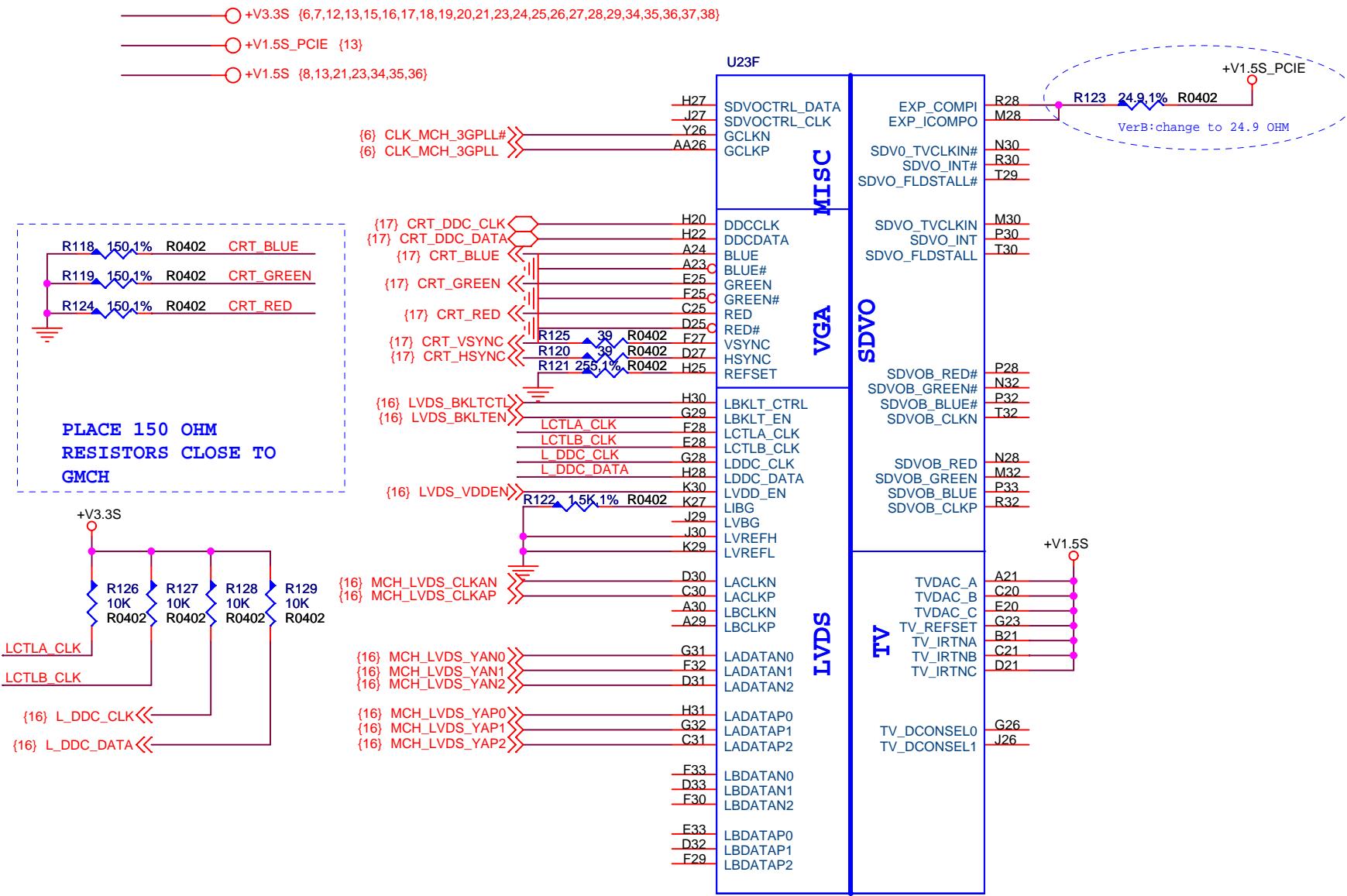


Place close to PIN-E1/E2



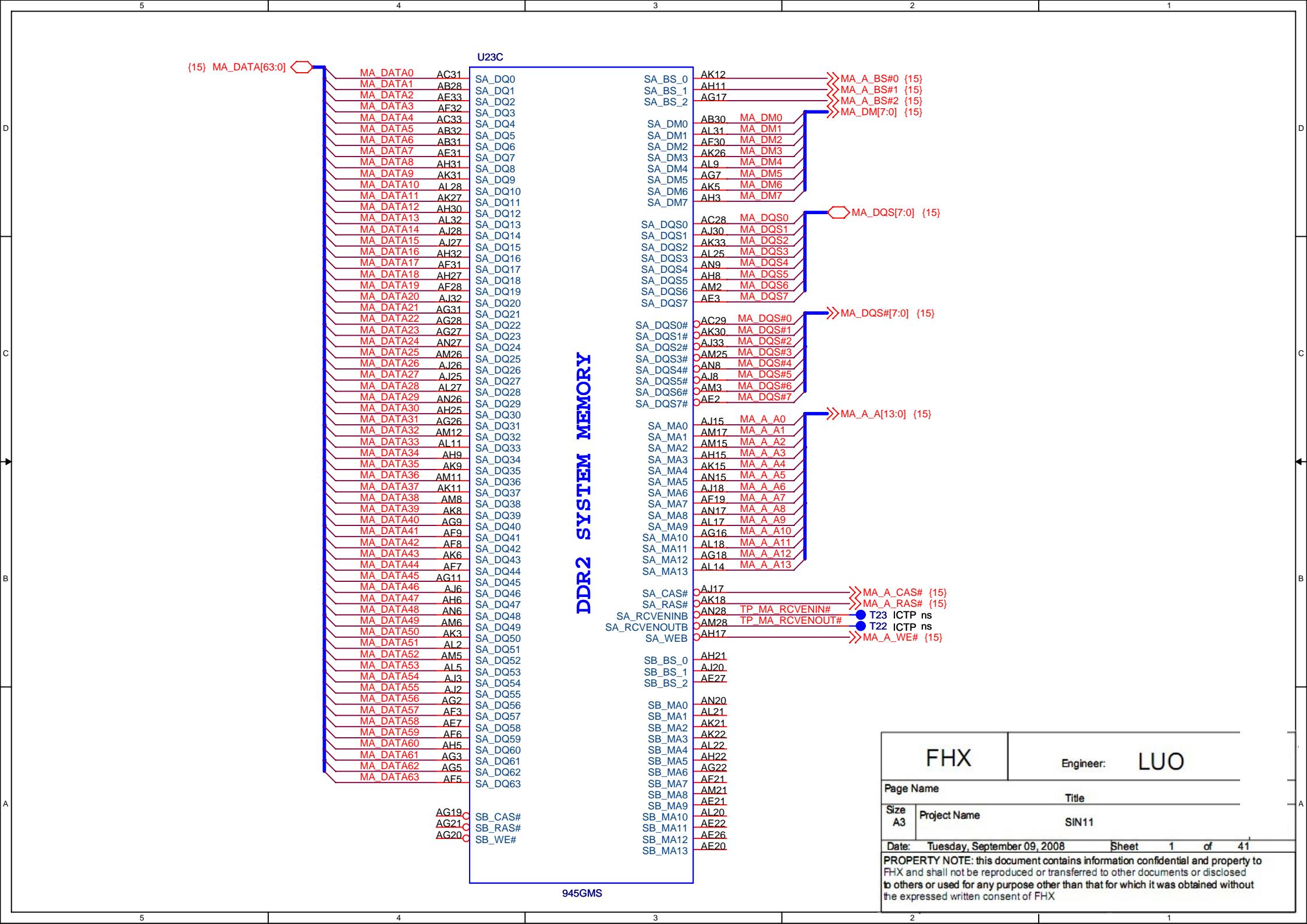
HHIT# H HIT# (7)
HHITM# H HITM# (7)
HLOCK# H LOCK# (7)
HREQ# H REQ# (7)
HREQ1# H REQ#1
HREQ2# H REQ#2
HREQ3# H REQ#3
HREQ4# H REQ#4
HRS0# H RS#0 (7)
HRS1# H RS#1 (7)
HRS2# H RS#2 (7)
HCPUSLP# H CPUSLP# (7,18)
HTRDY# H TRDY# (7)

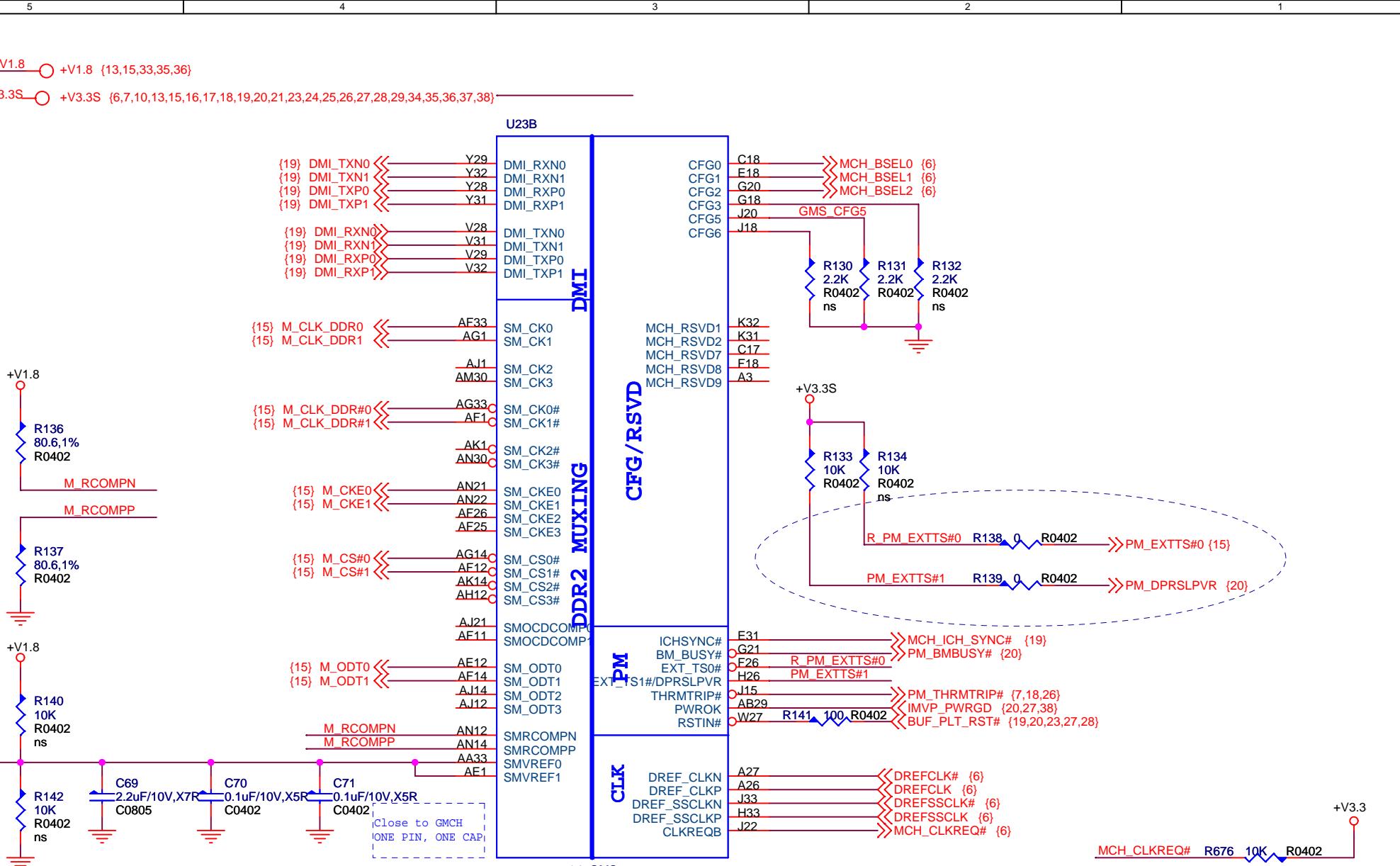
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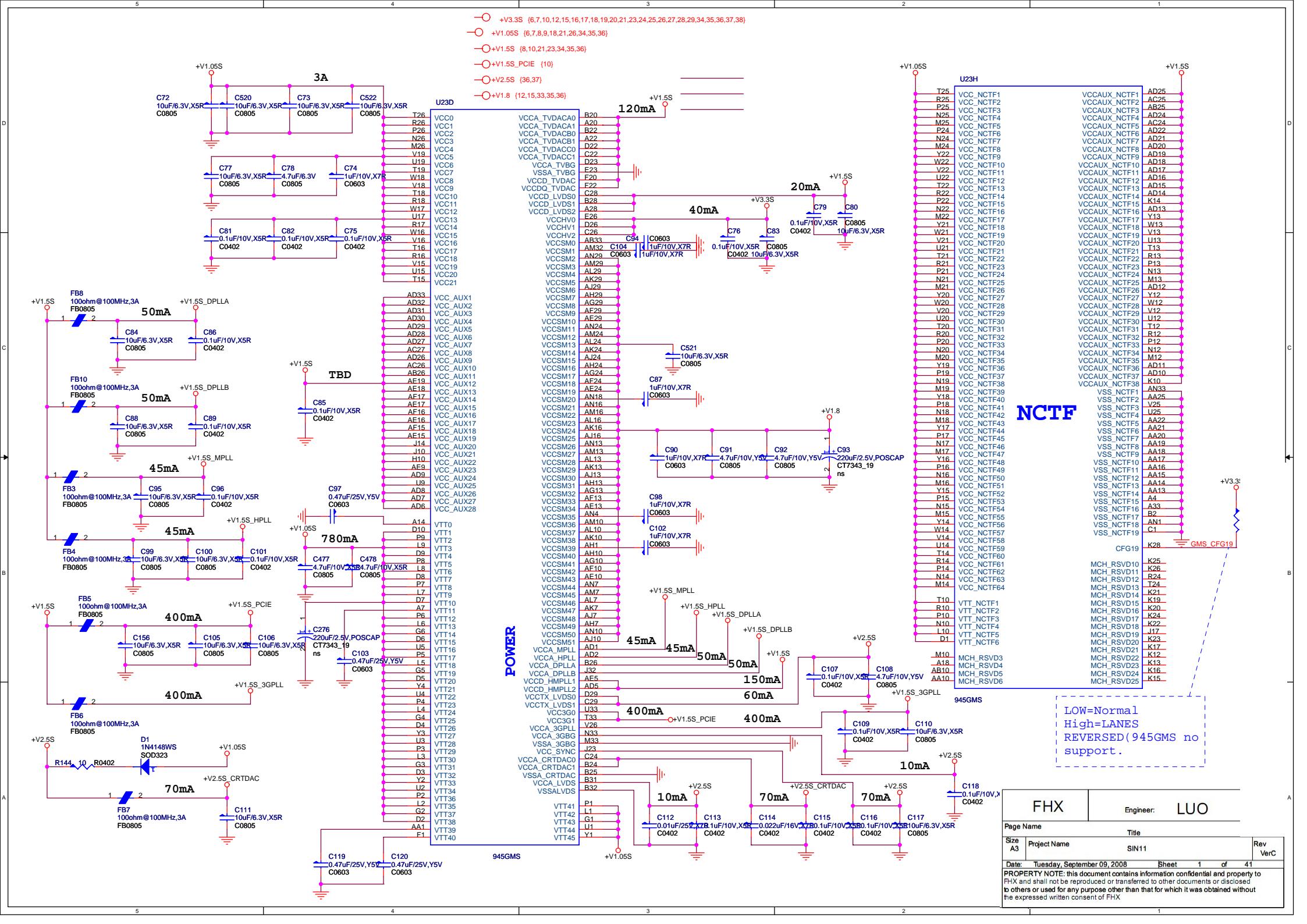
945GMS

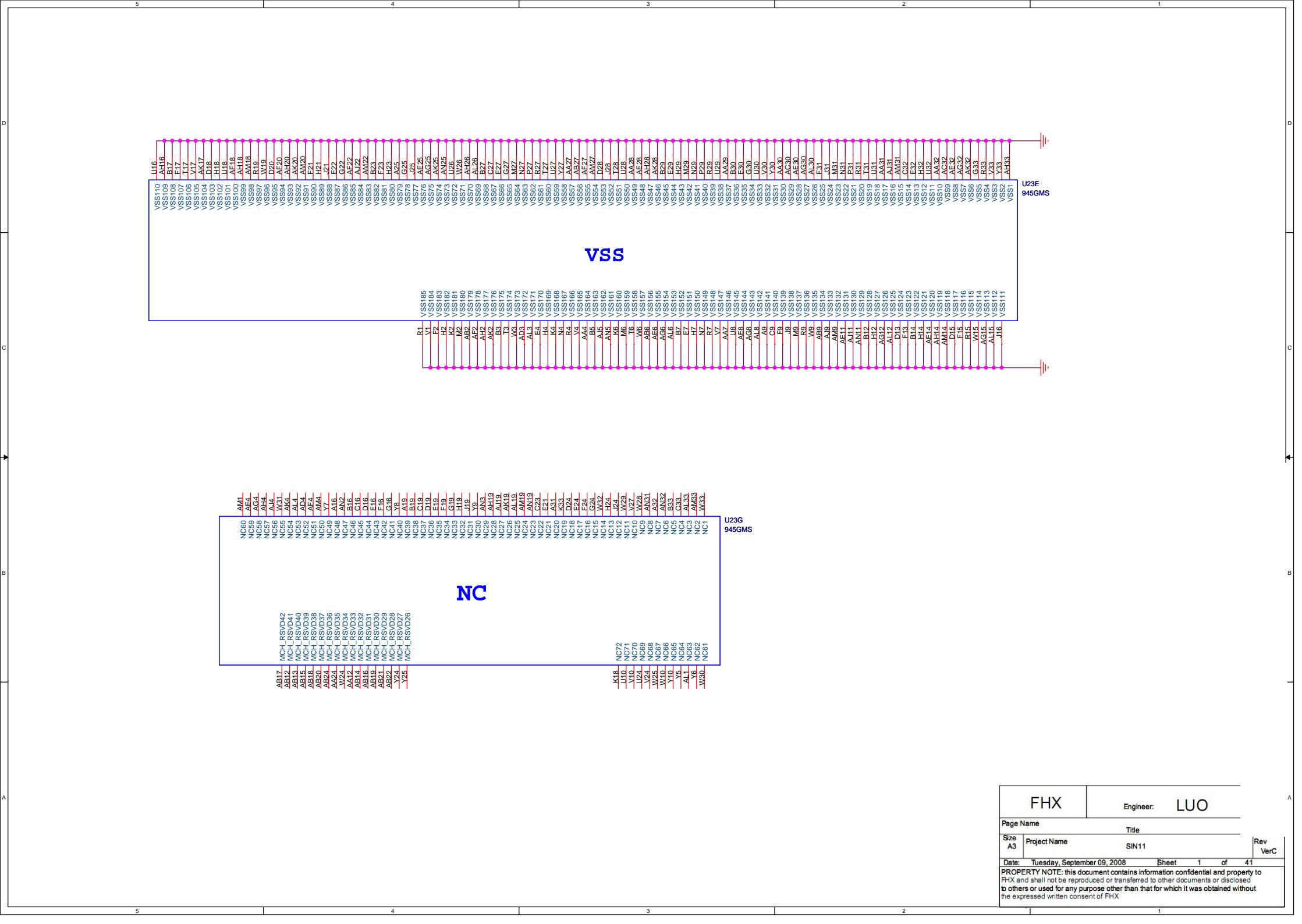
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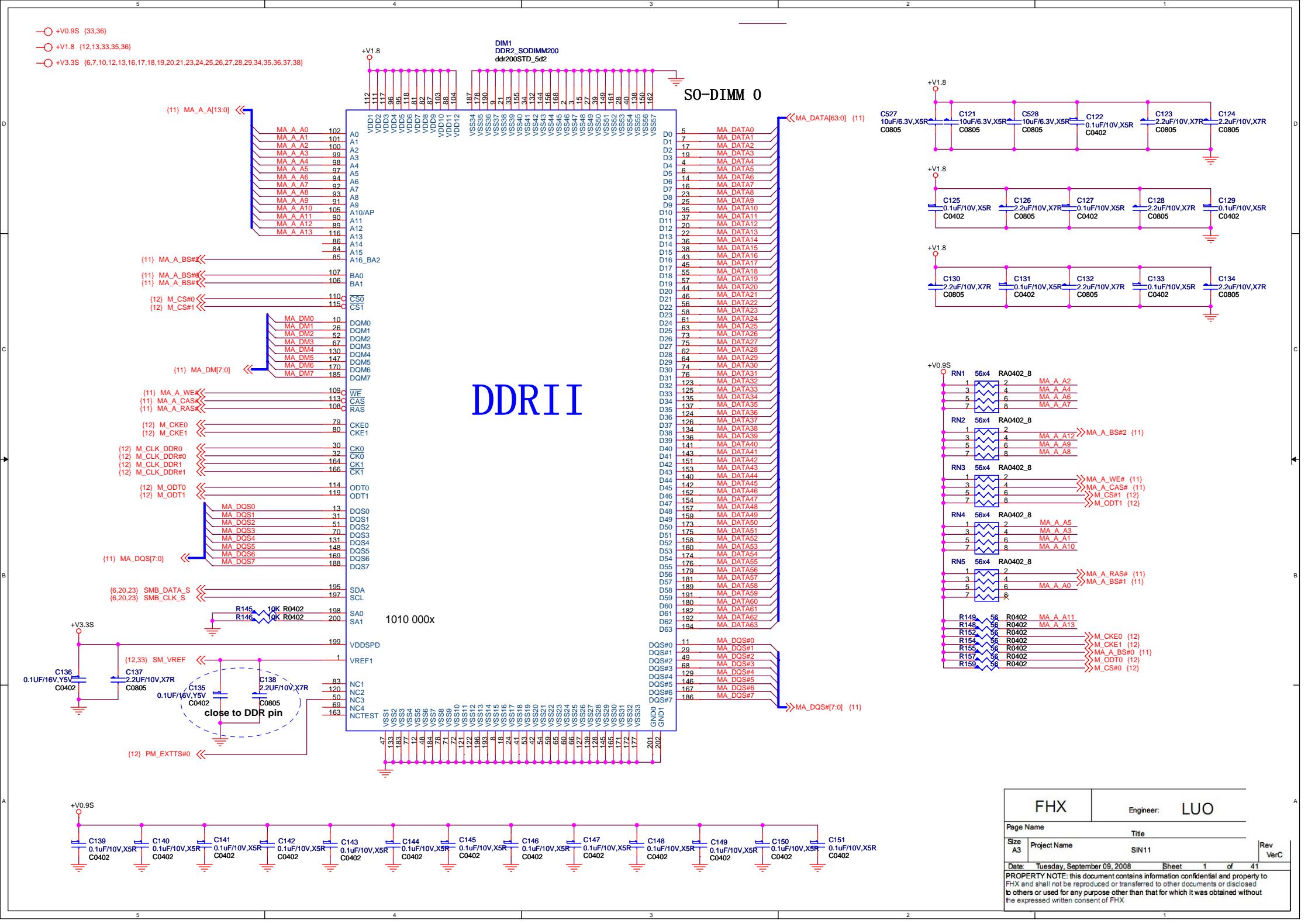


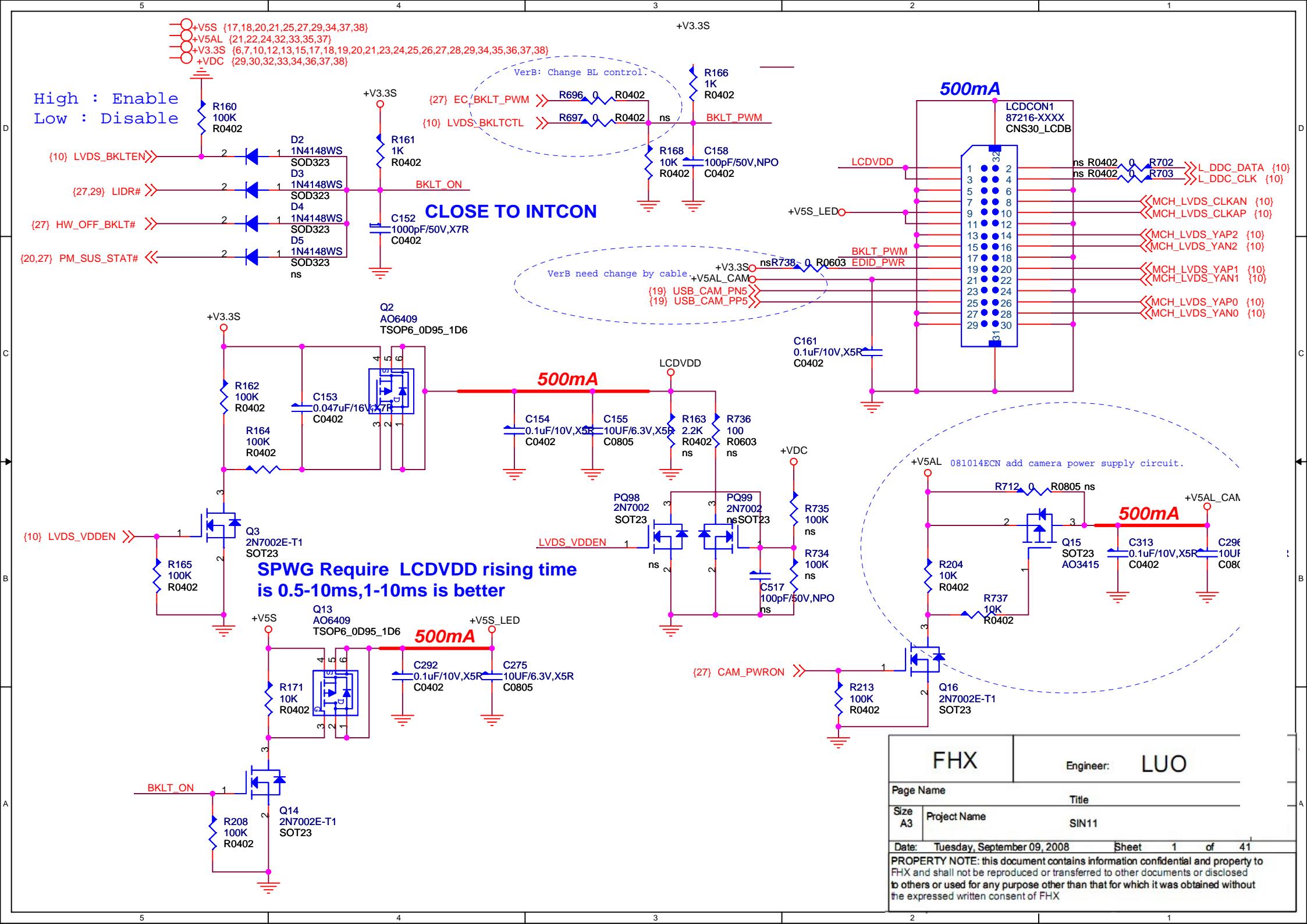


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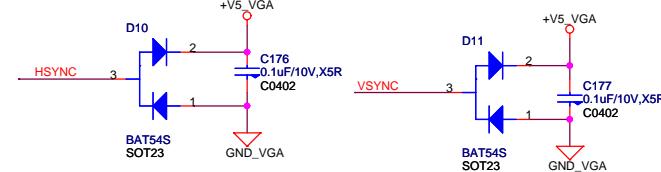
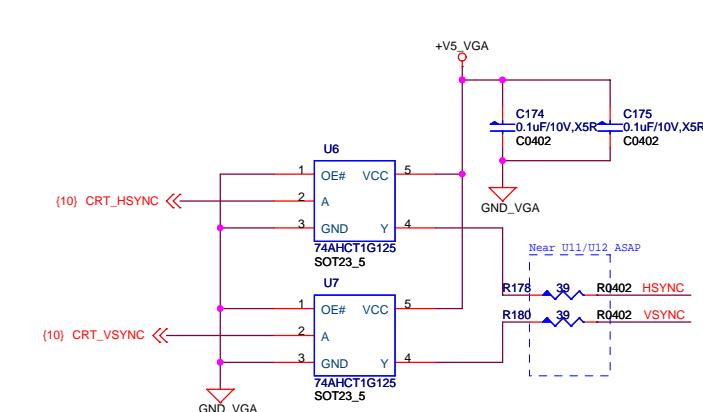
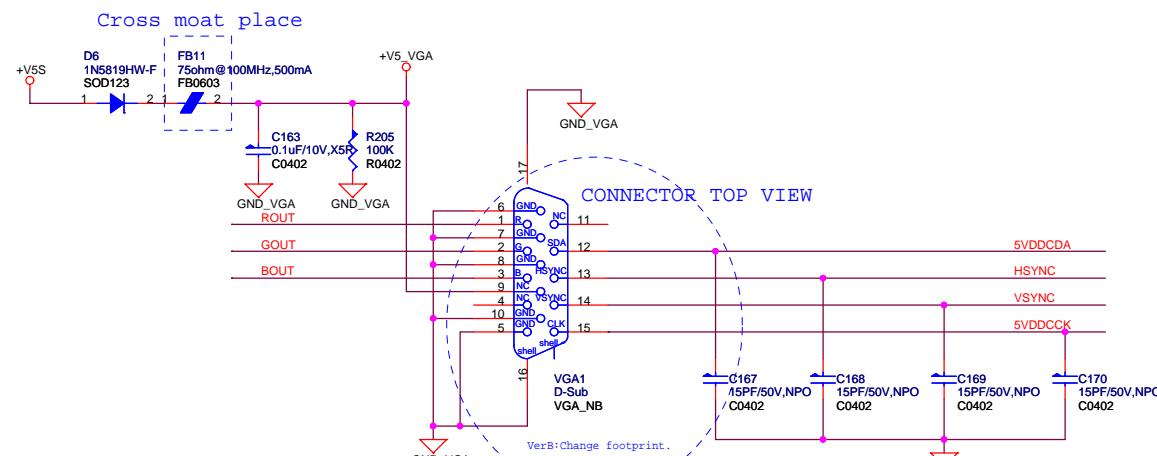
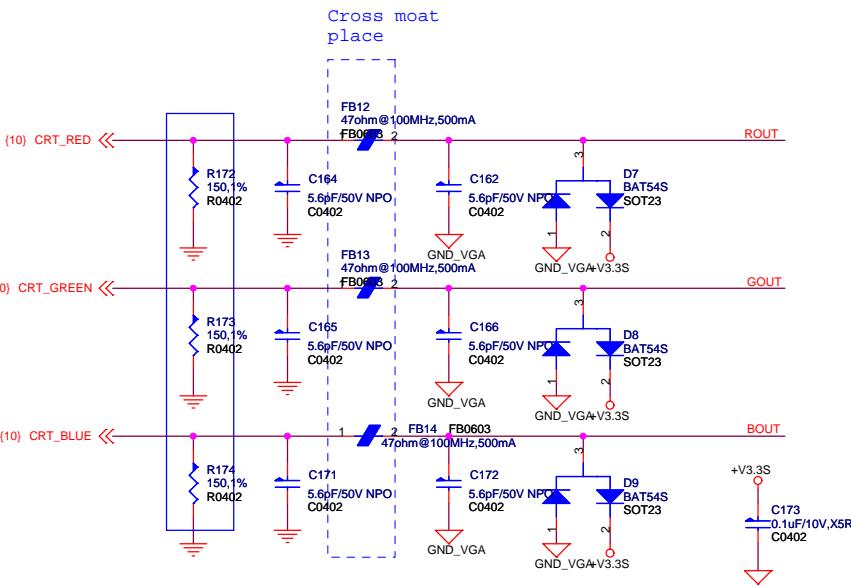




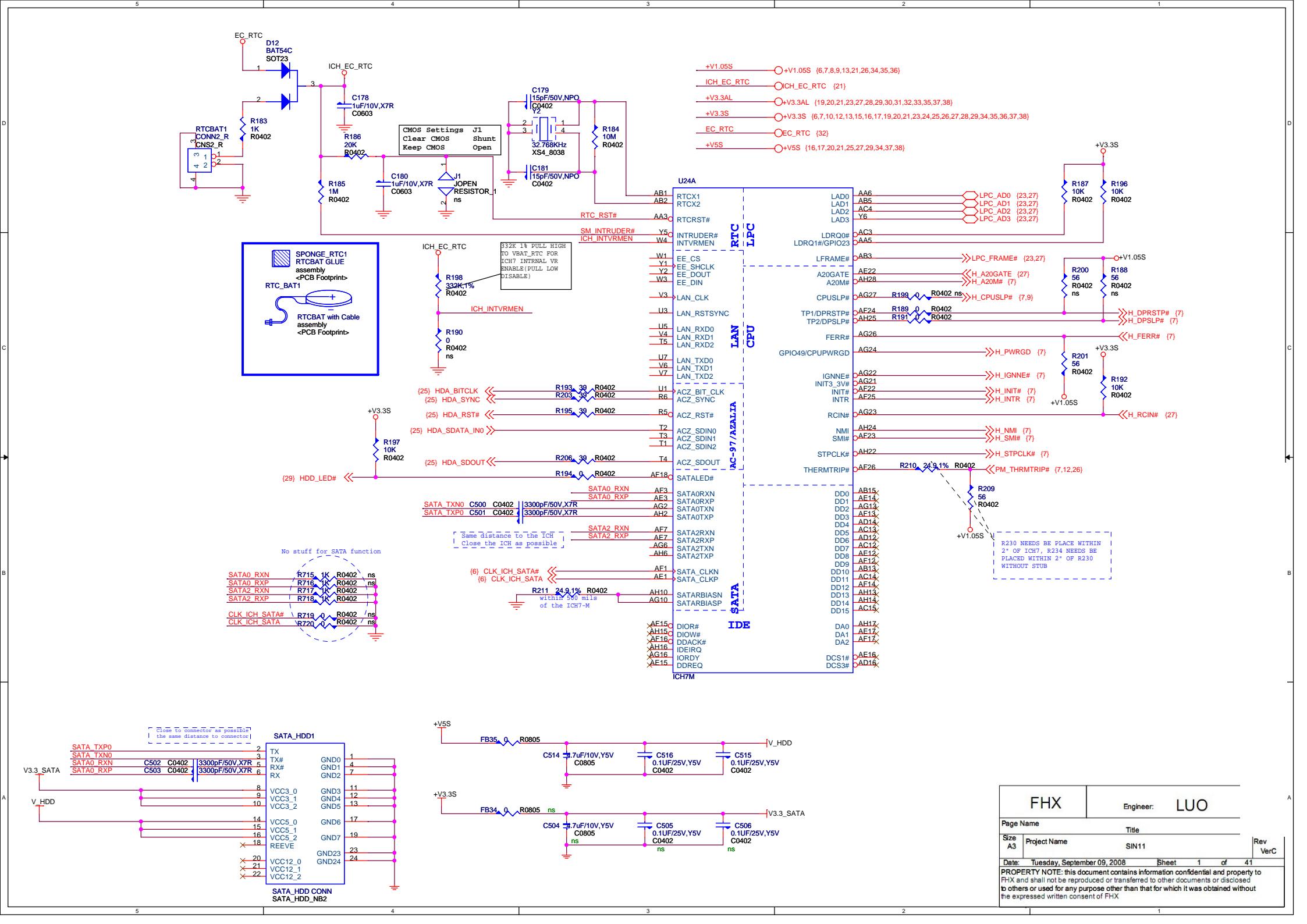


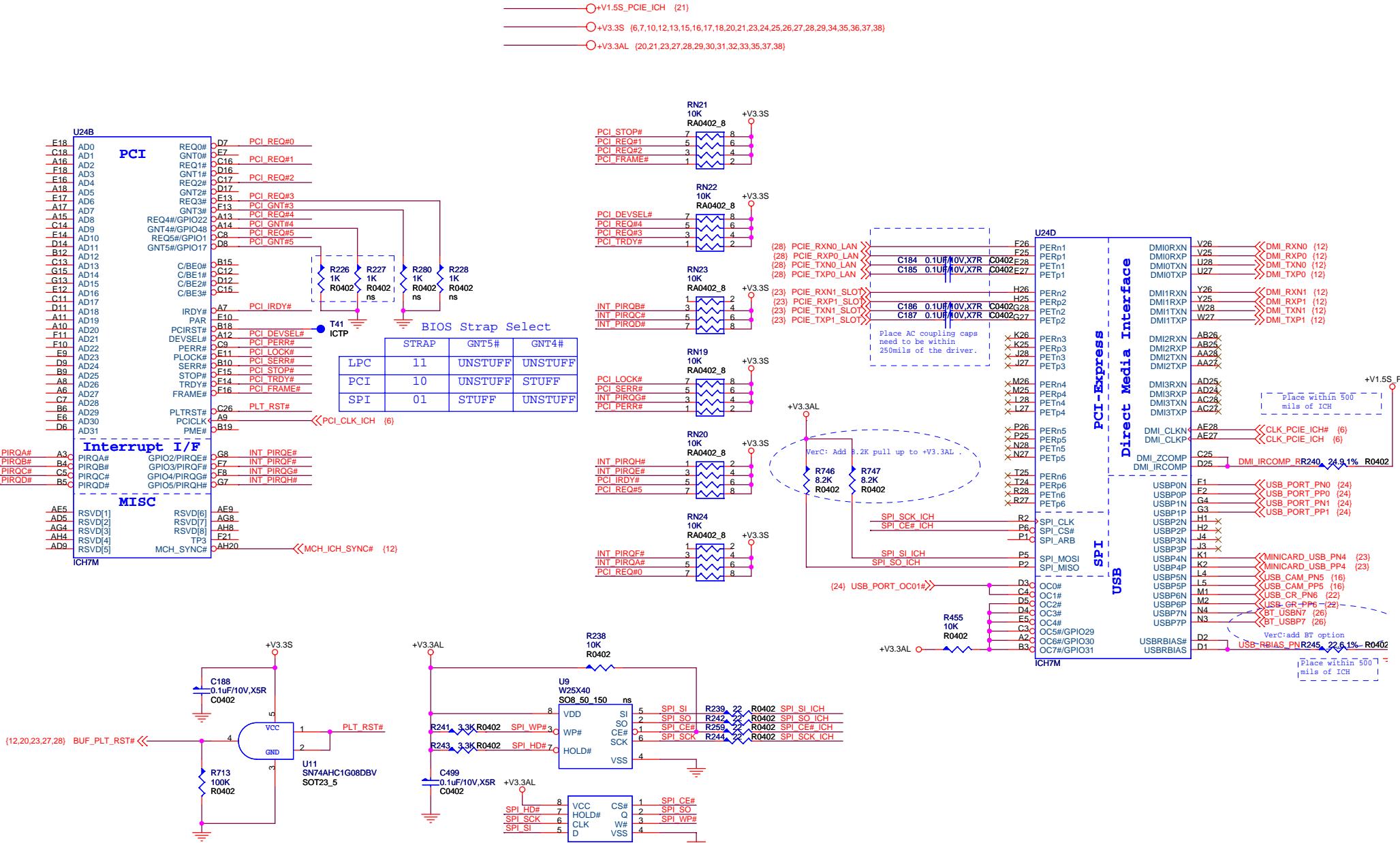


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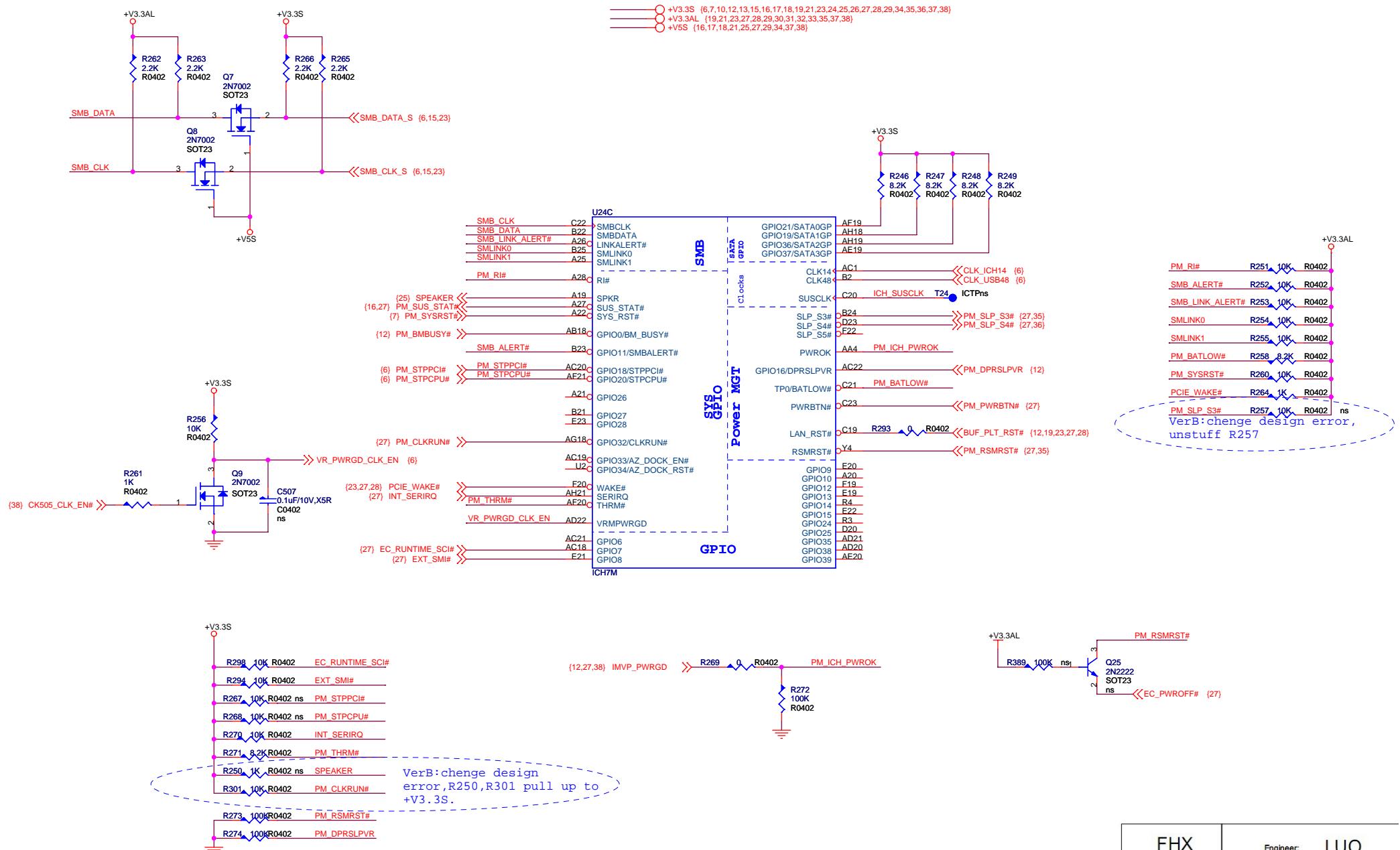


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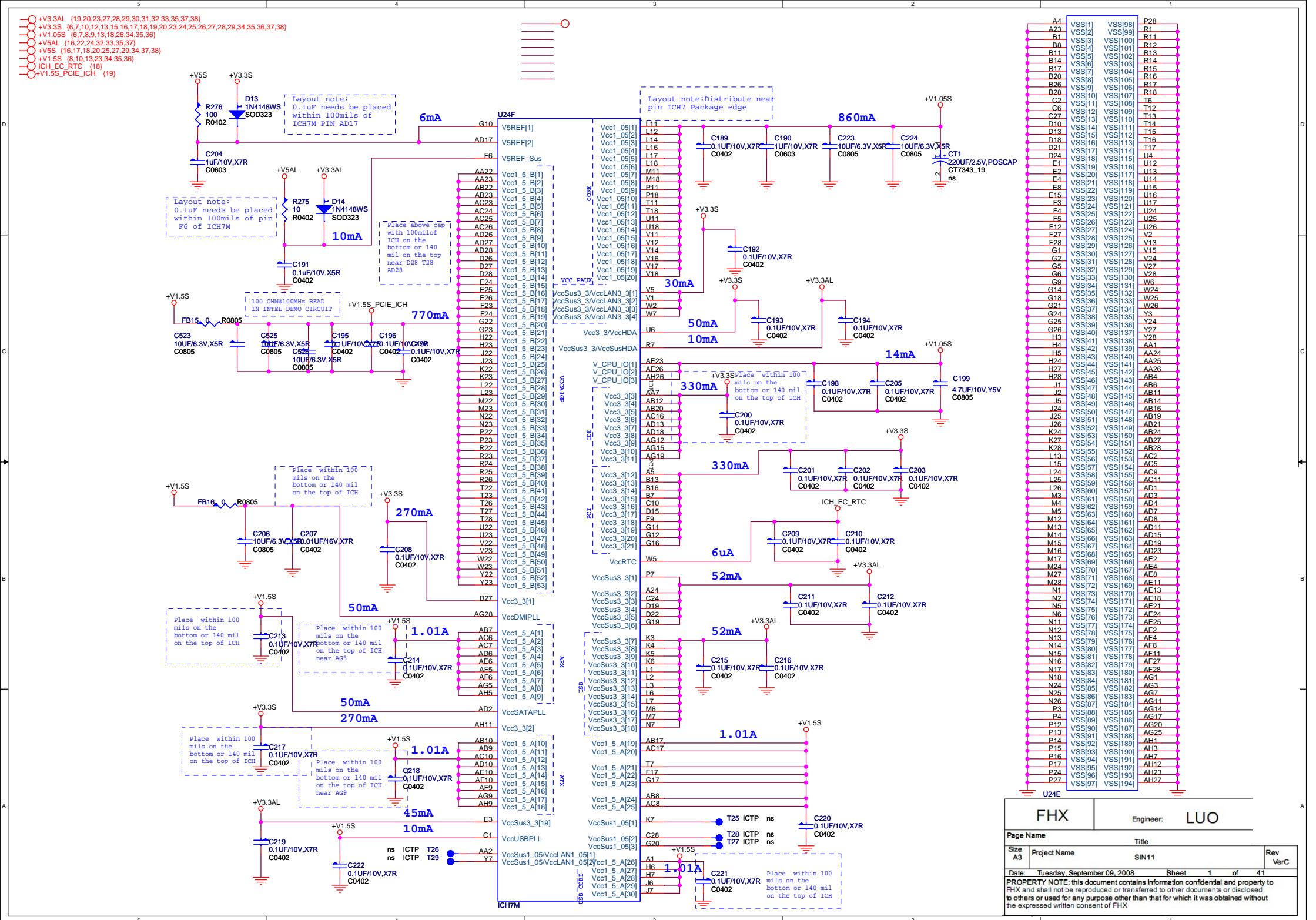


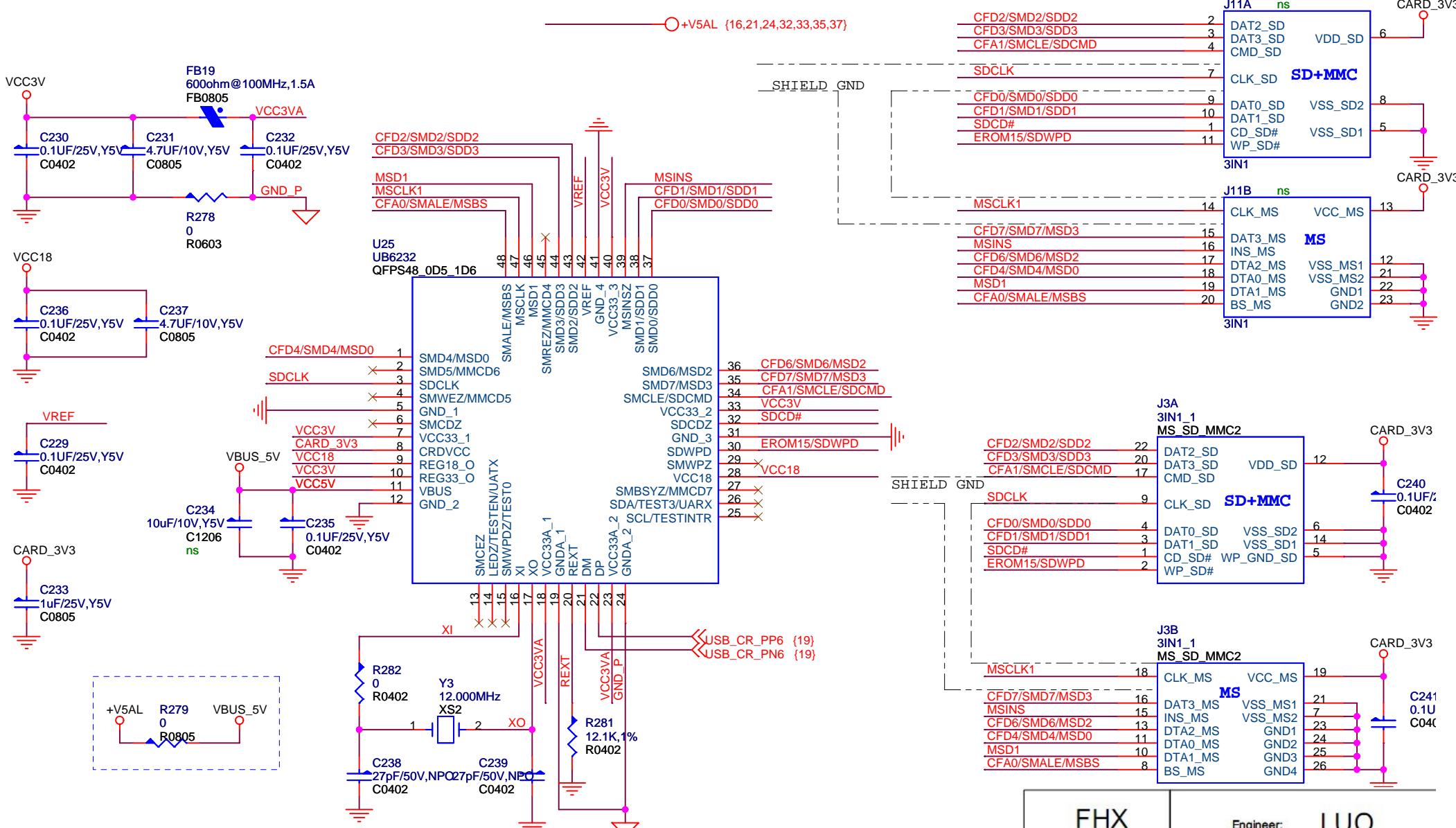


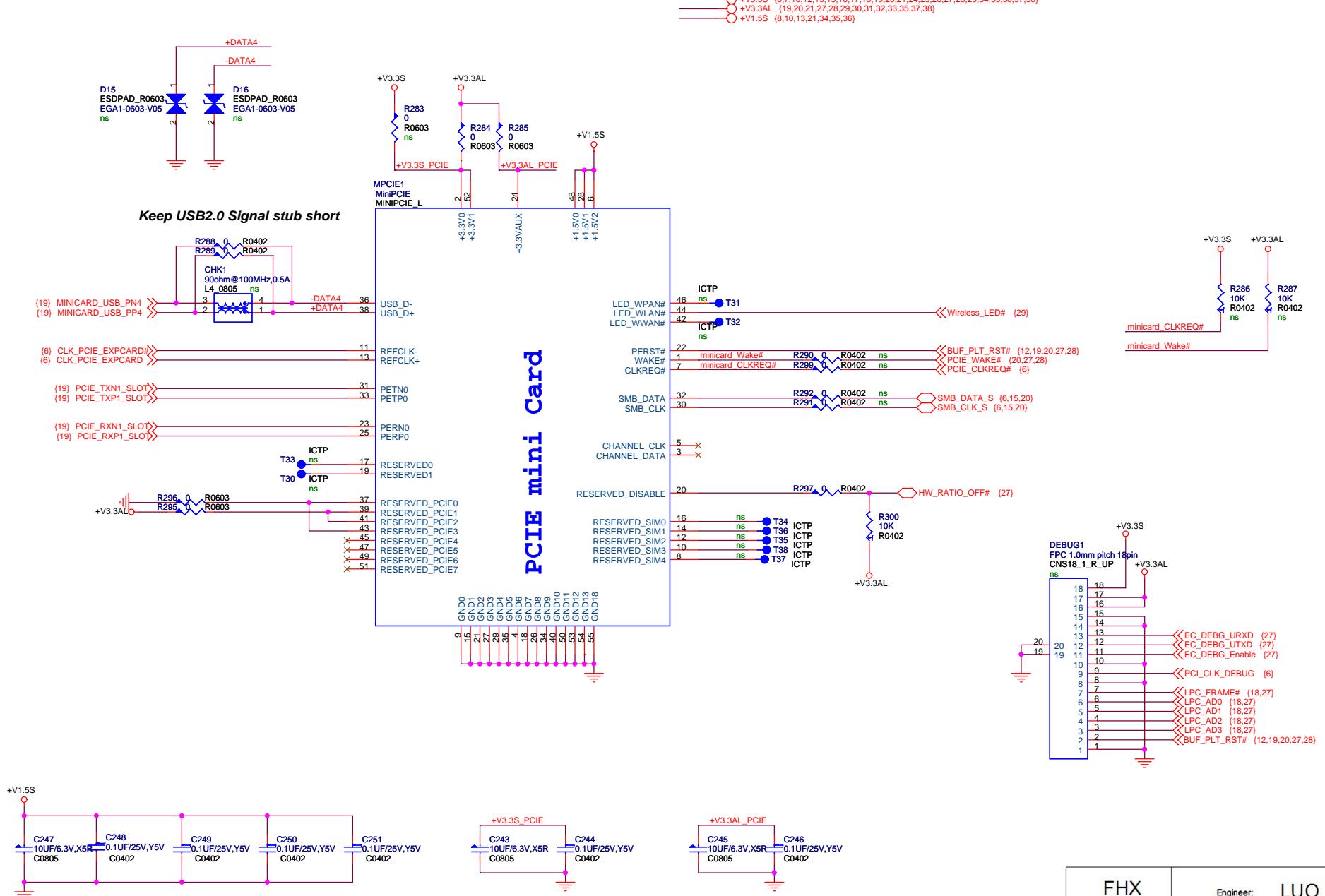
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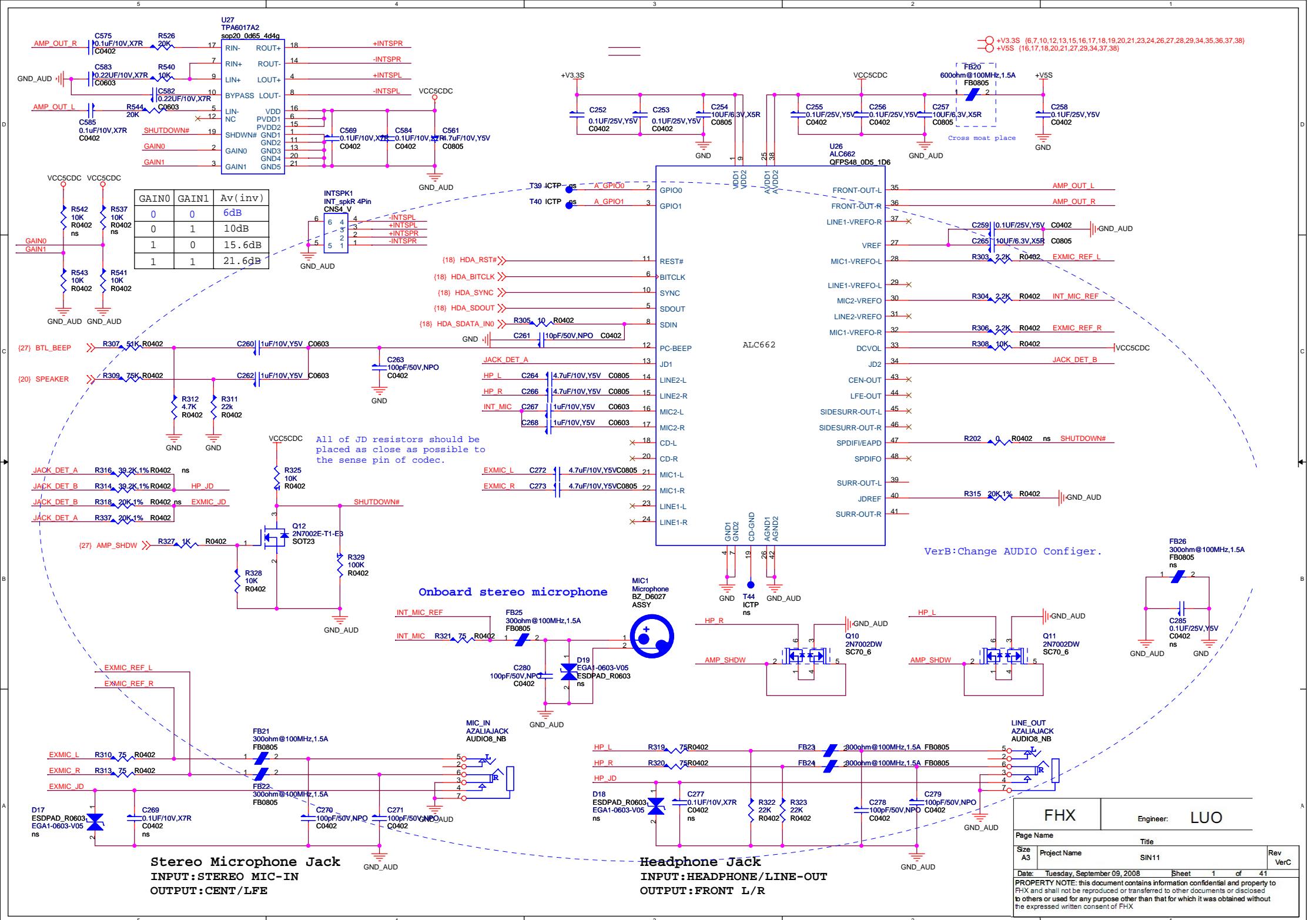
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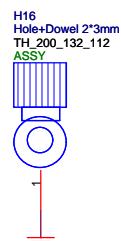
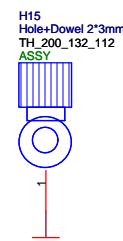
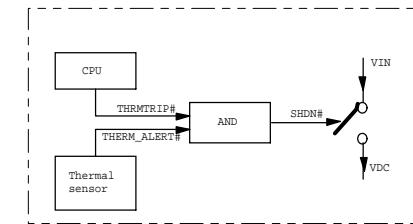
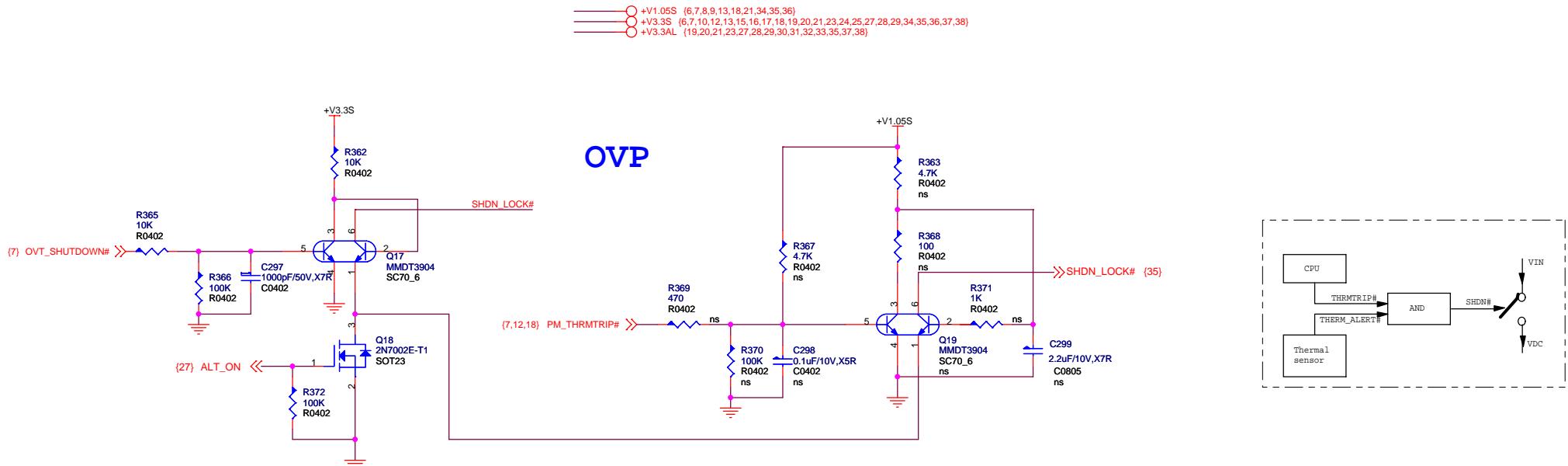




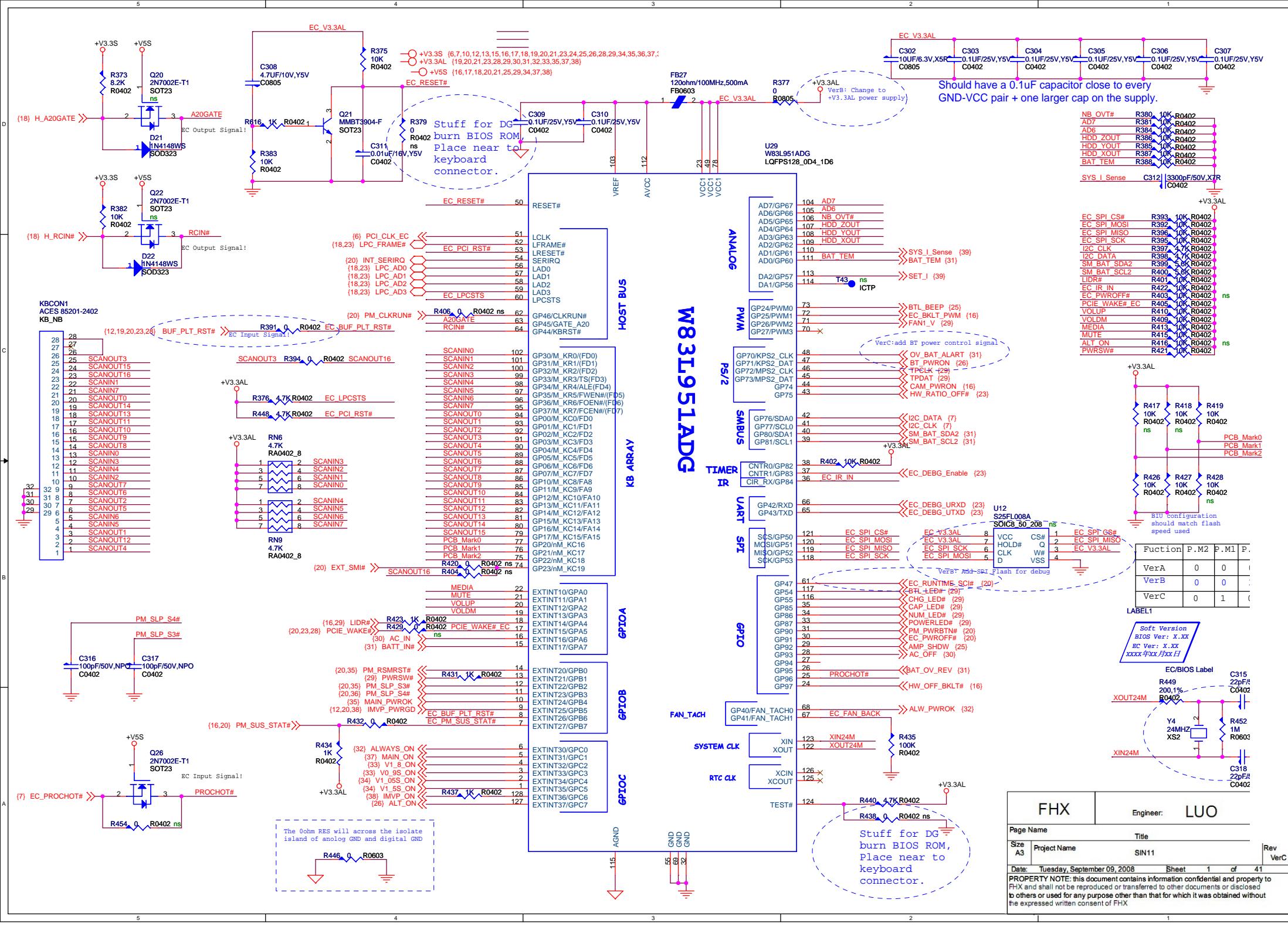


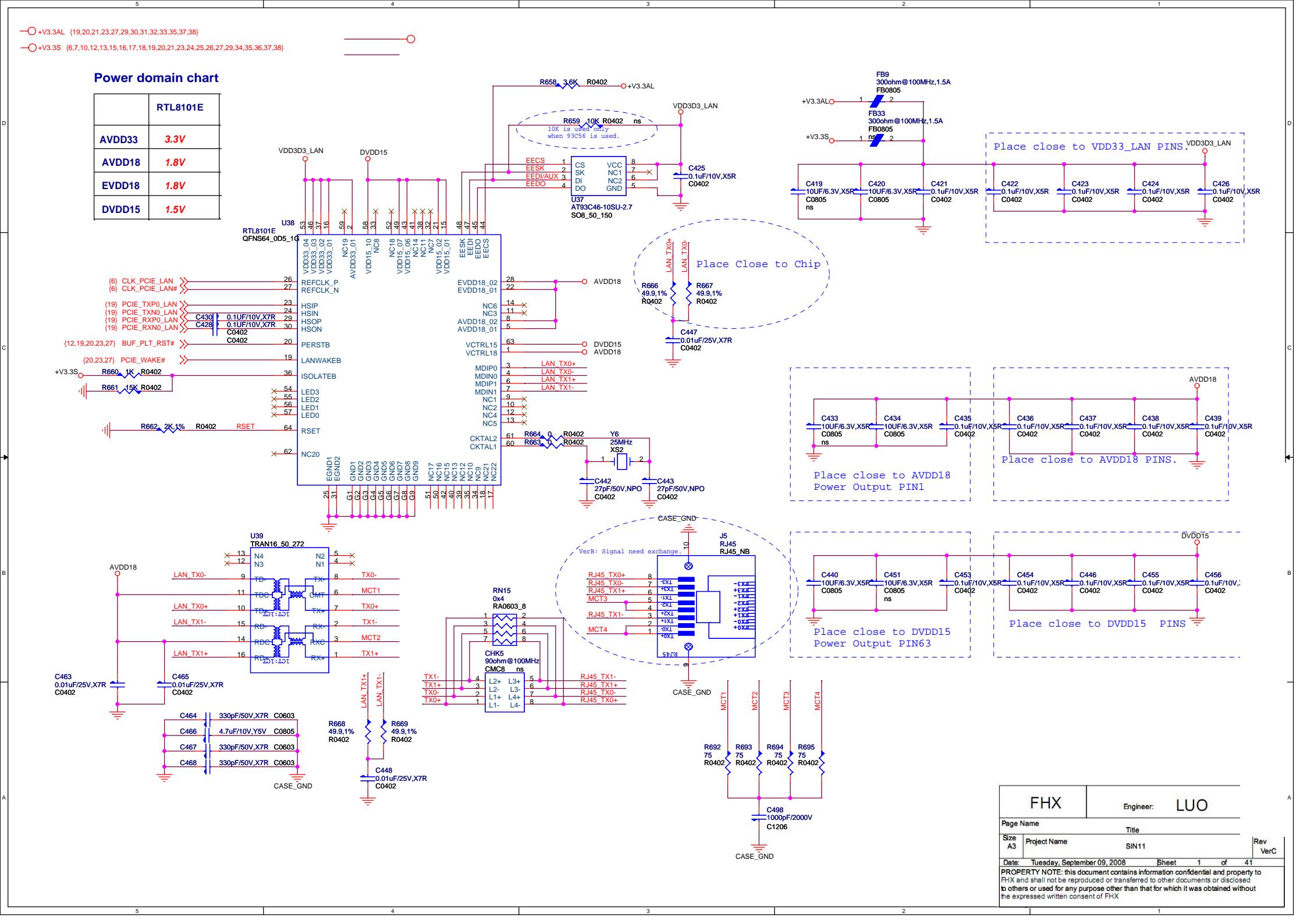
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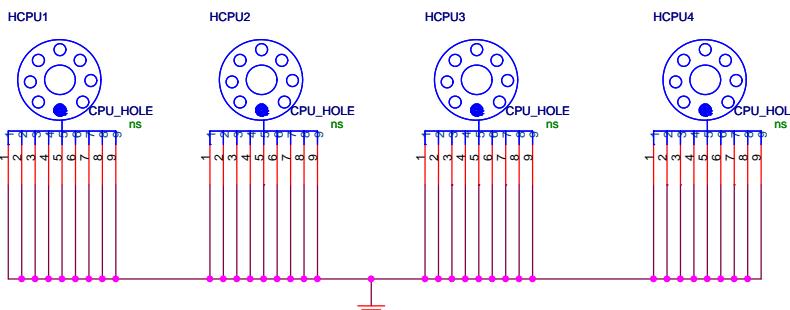
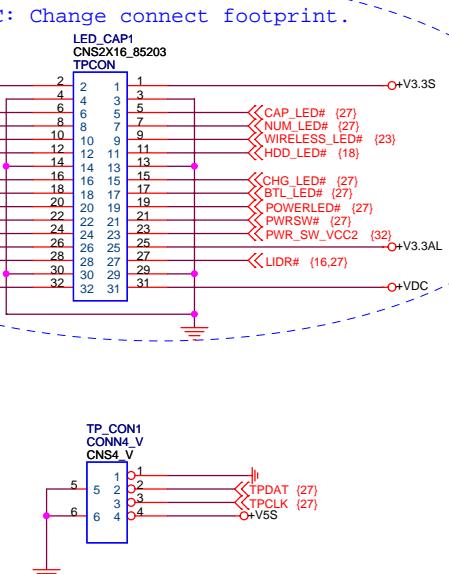
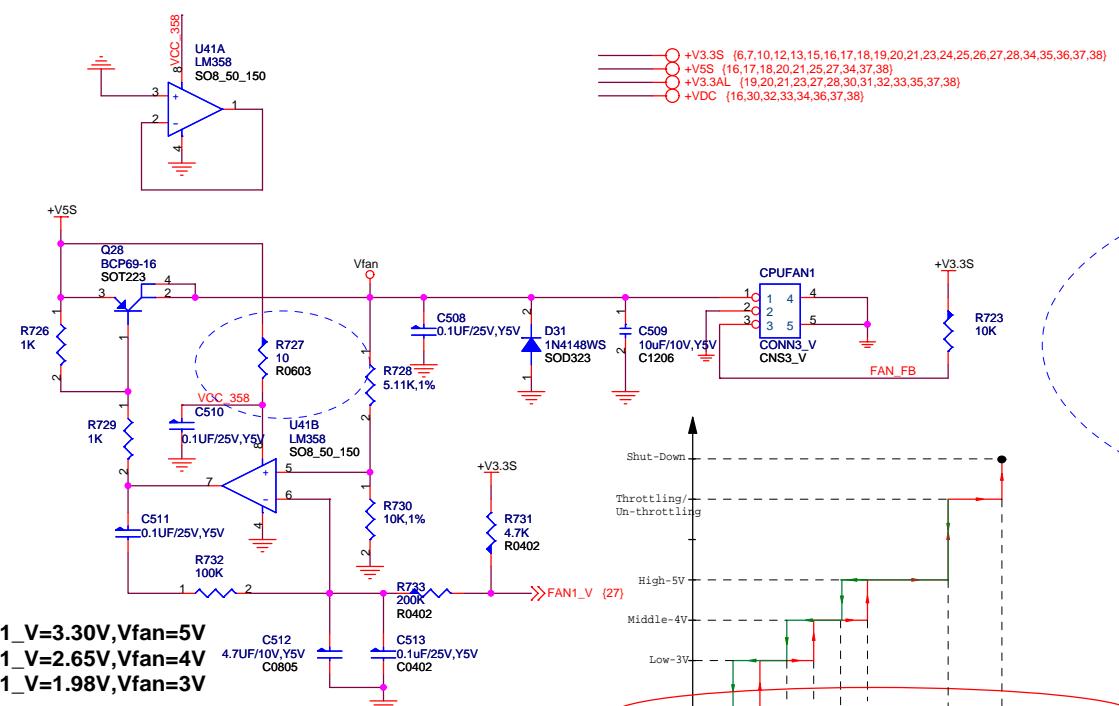




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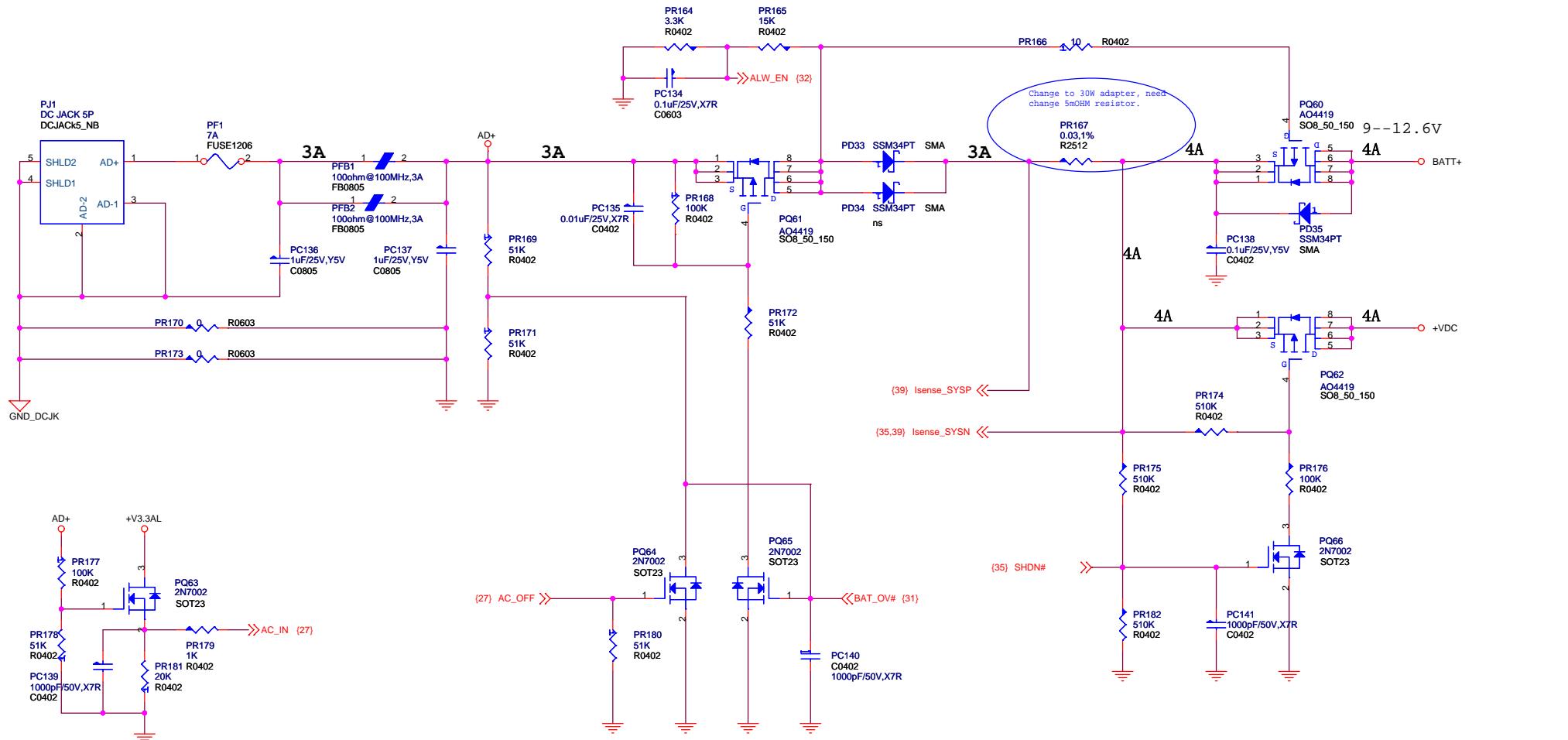




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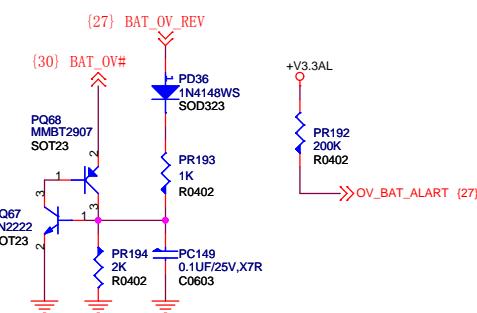
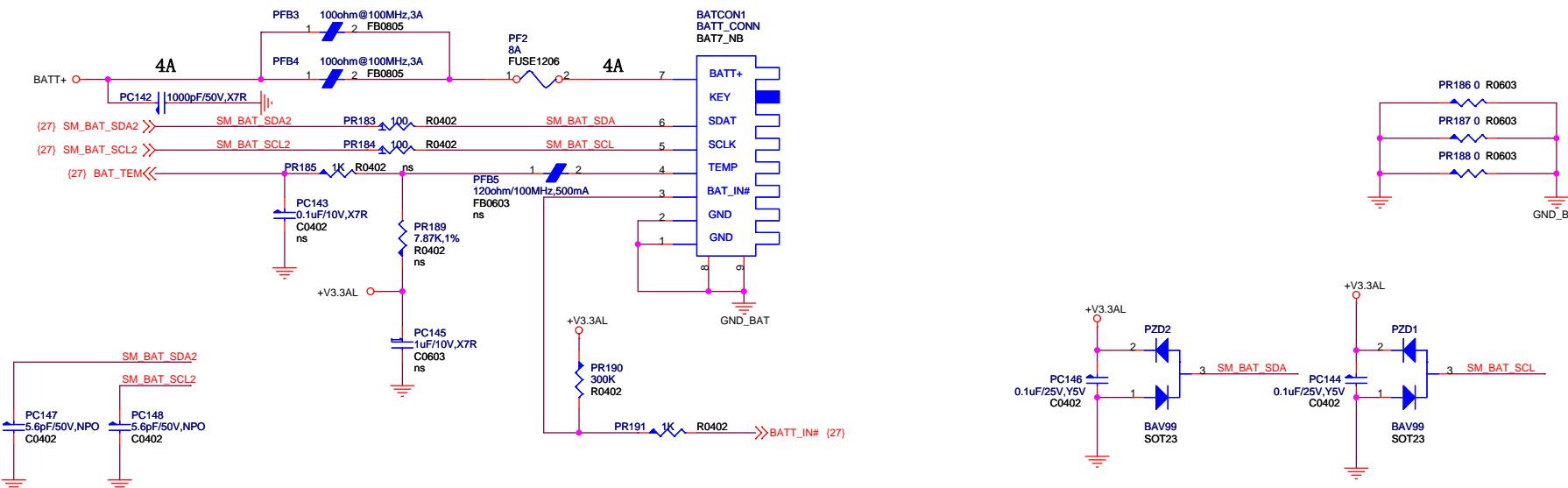
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BATT+ (31,39)
 +VDC (16,29,32,33,34,36,37,38)
 +V3.3AL (19,20,21,23,27,28,29,31,32,33,35,37,38)

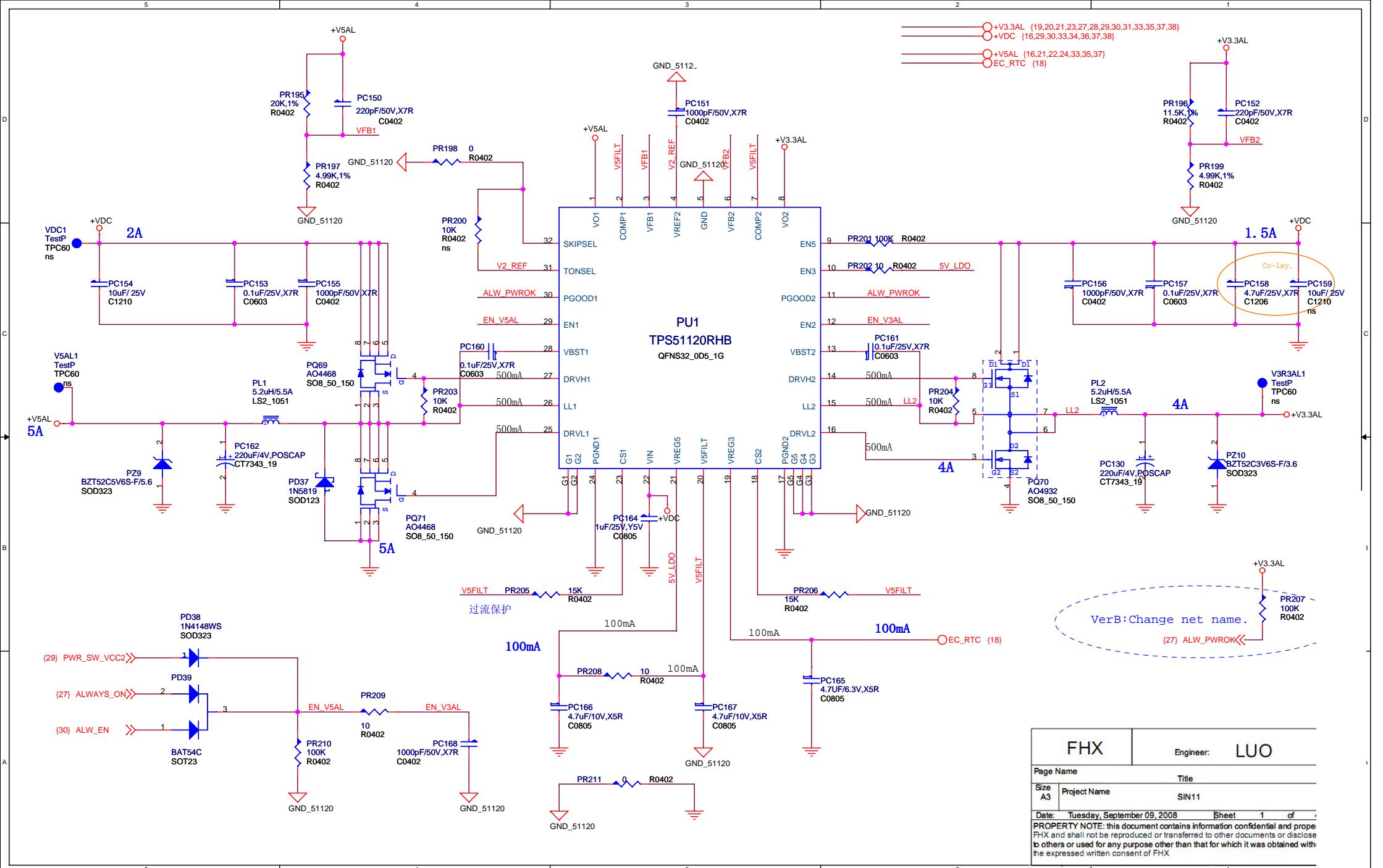


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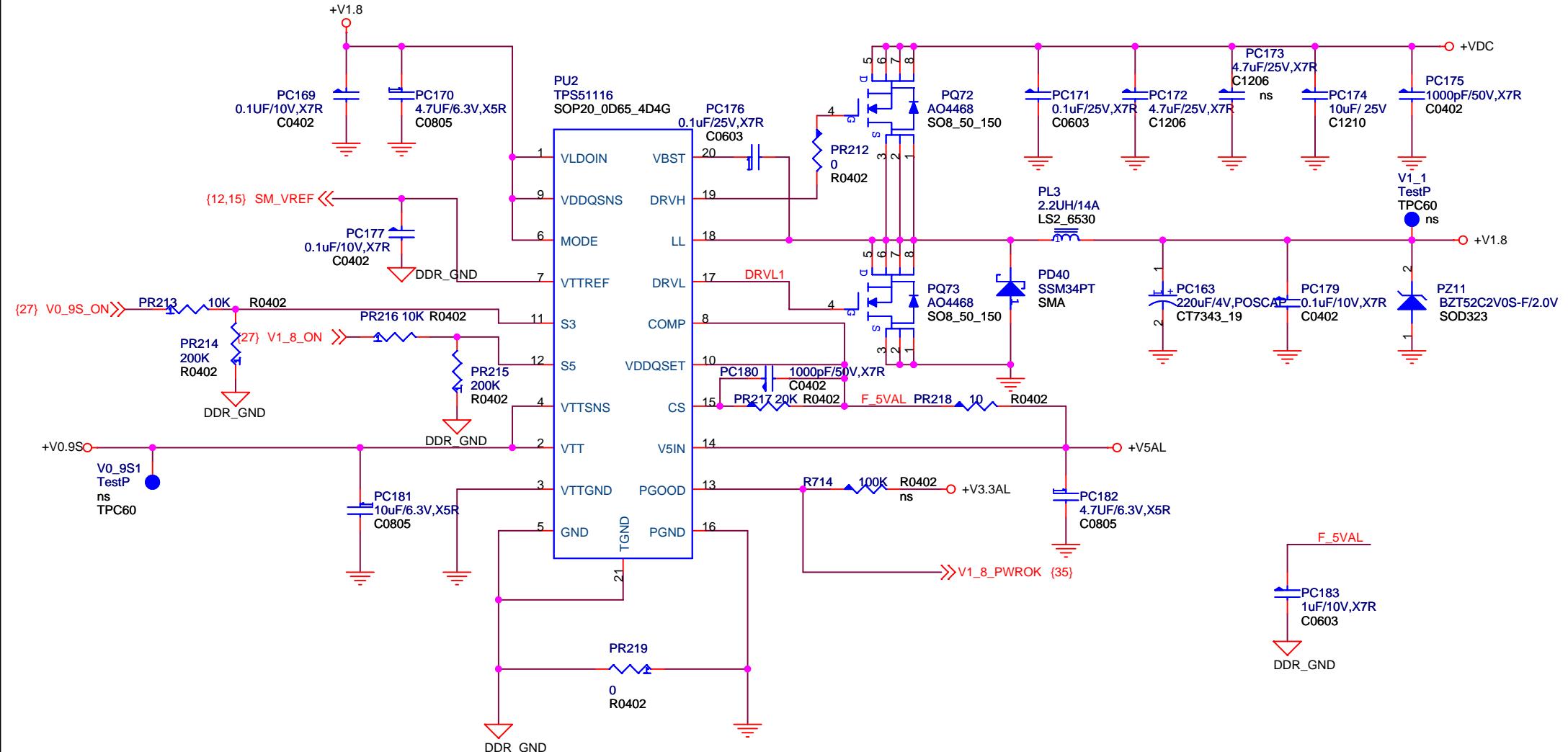
—○ BATT+ {30,39}
—○ +V3.3AL {19,20,21,23,27,28,29,30,32,33,35,37,38}



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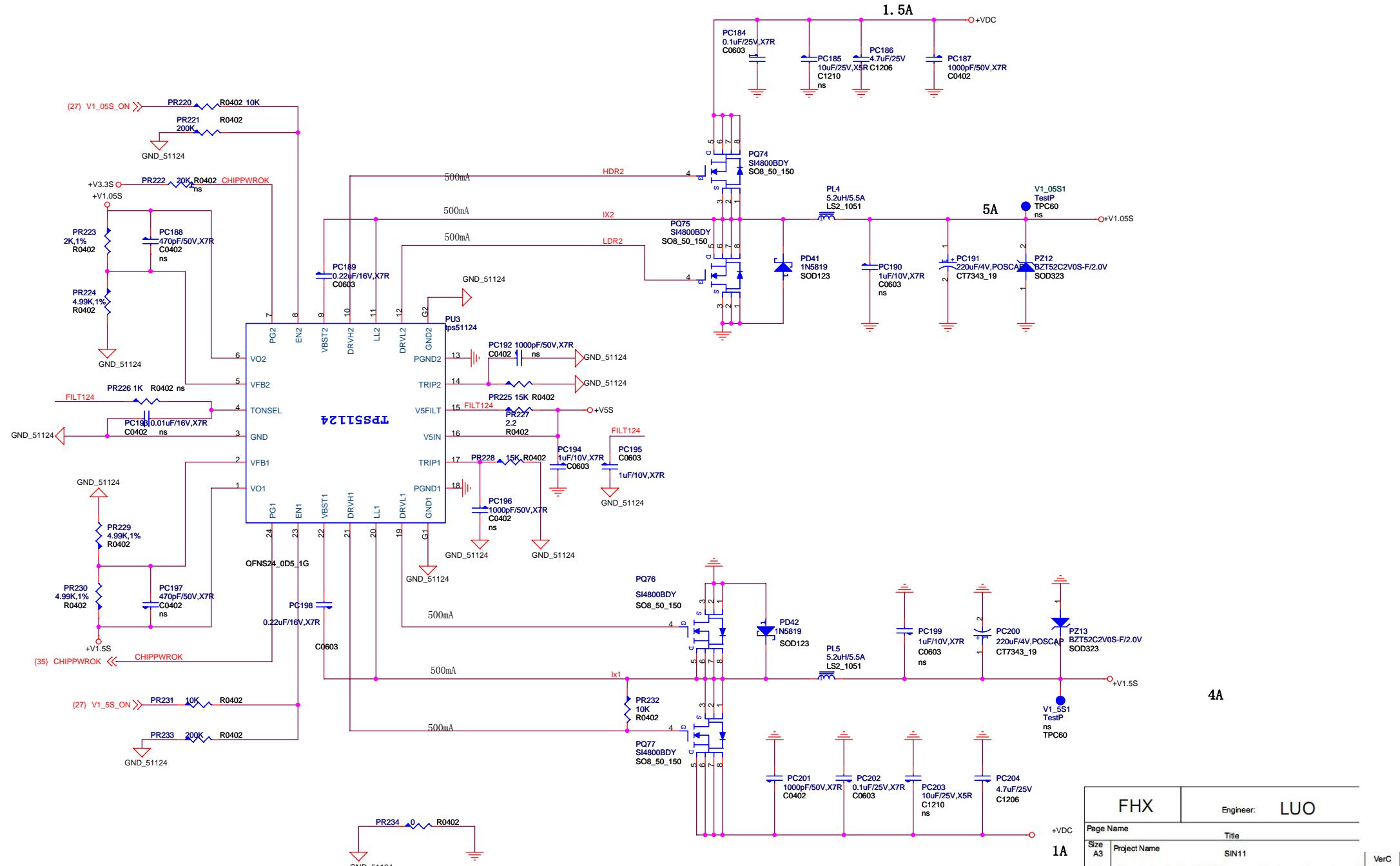


- +V5AL {16,21,22,24,32,35,37}
- +V3.3AL {19,20,21,23,27,28,29,30,31,32,35,37,38}
- +VDC {16,29,30,32,34,36,37,38}
- +V1.8 {12,13,15,35,36}
- +V0.9S {15,36}



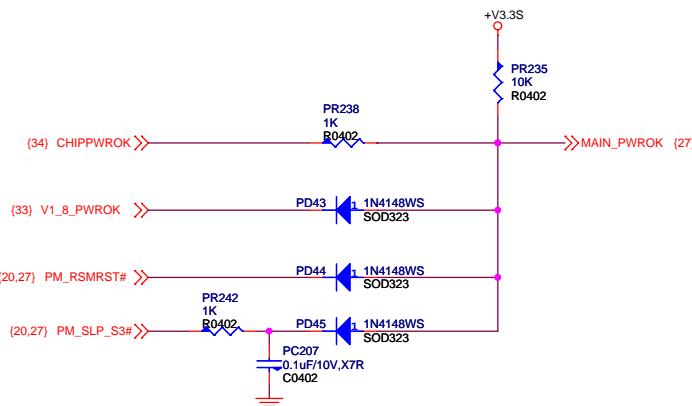
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+V1.05S (6,7,8,9,13,18,21,26,35,36)
 +VDC (16,29,30,32,33,36,37,38)
 +VSS (16,17,18,20,21,25,27,29,37,38)
 +V3.3S (6,7,10,12,13,15,16,17,18,19,20,21,23,24,25,26,27,28,29,35,36,37,38)
 +V1.5S (8,10,13,21,23,35,36)

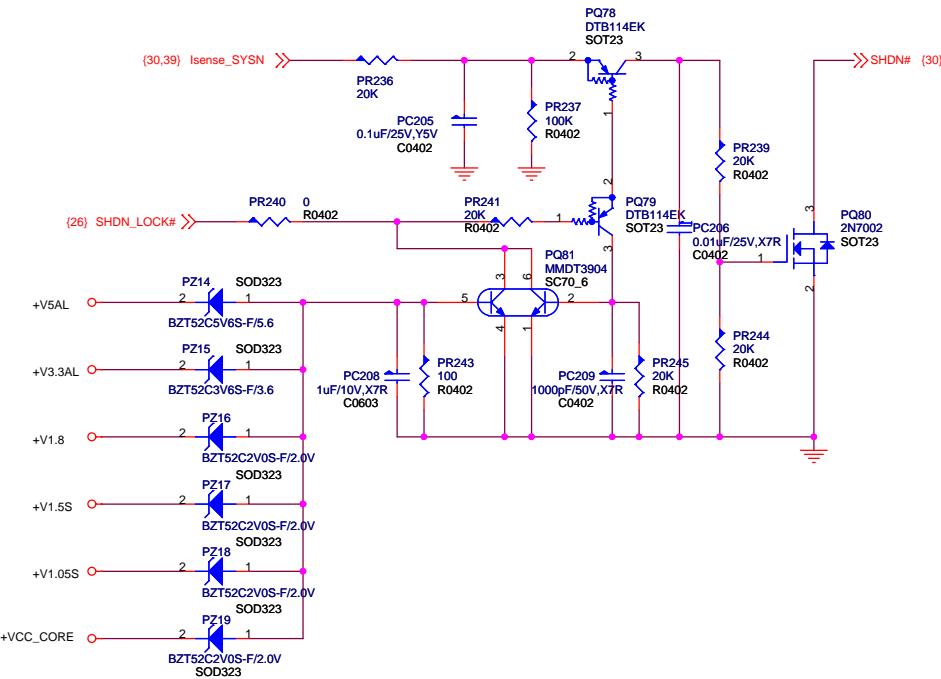


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 +V5AL (16,21,22,24,32,33,37)
 +V3.3AL (19,20,21,23,27,28,29,30,31,32,33,37,38)
 +V1.05S (6,7,8,9,13,18,21,26,34,36)
 +V1.5S (8,10,13,21,23,34,36)
 +VCC_CORE (8,38)
 +V1.8 (12,13,15,33,36)
 +VDC (16,29,30,32,33,34,36,37,38)

Power Good Logic CIRCUIT

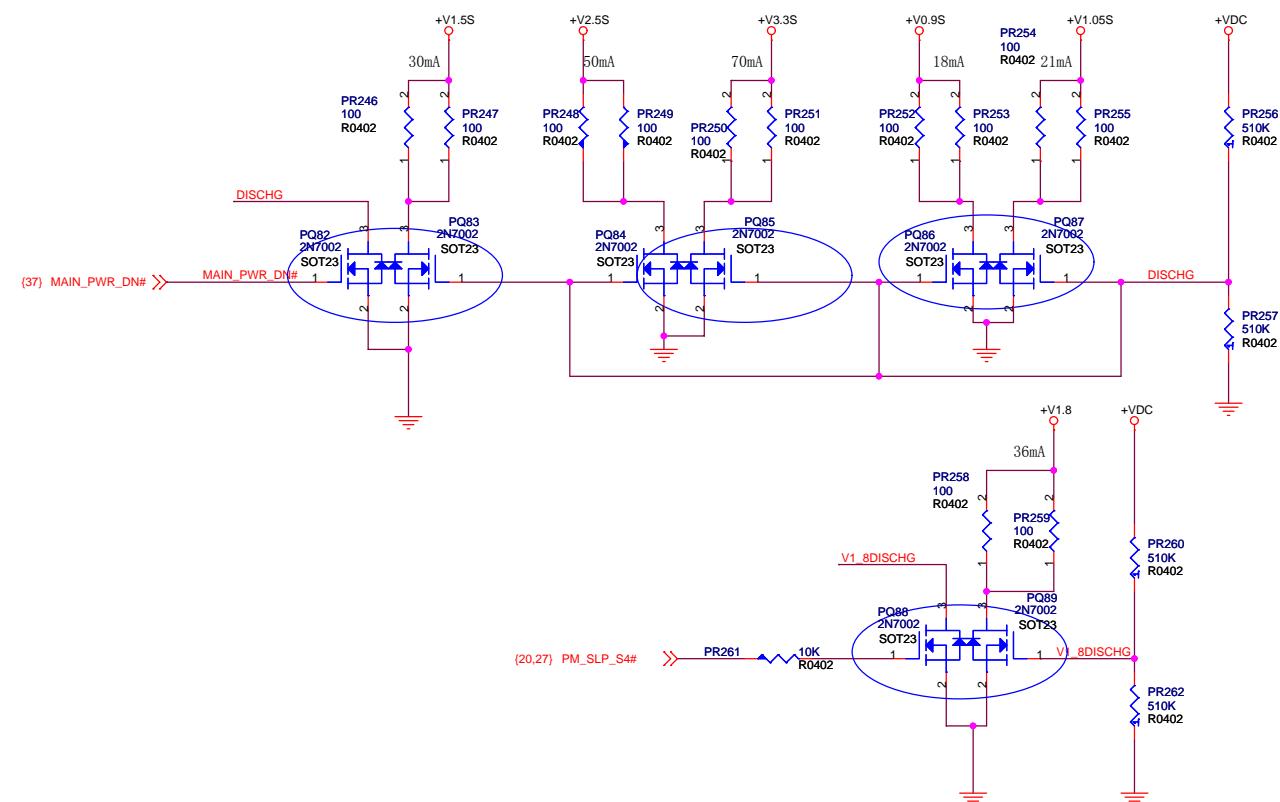


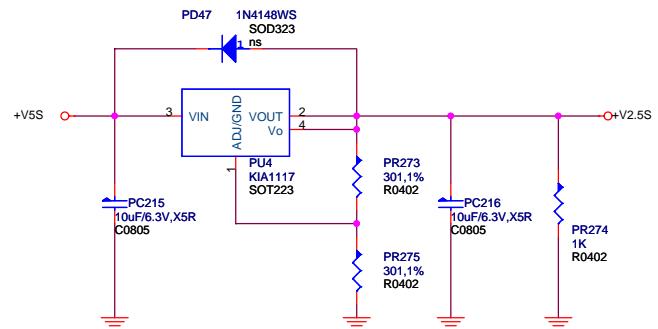
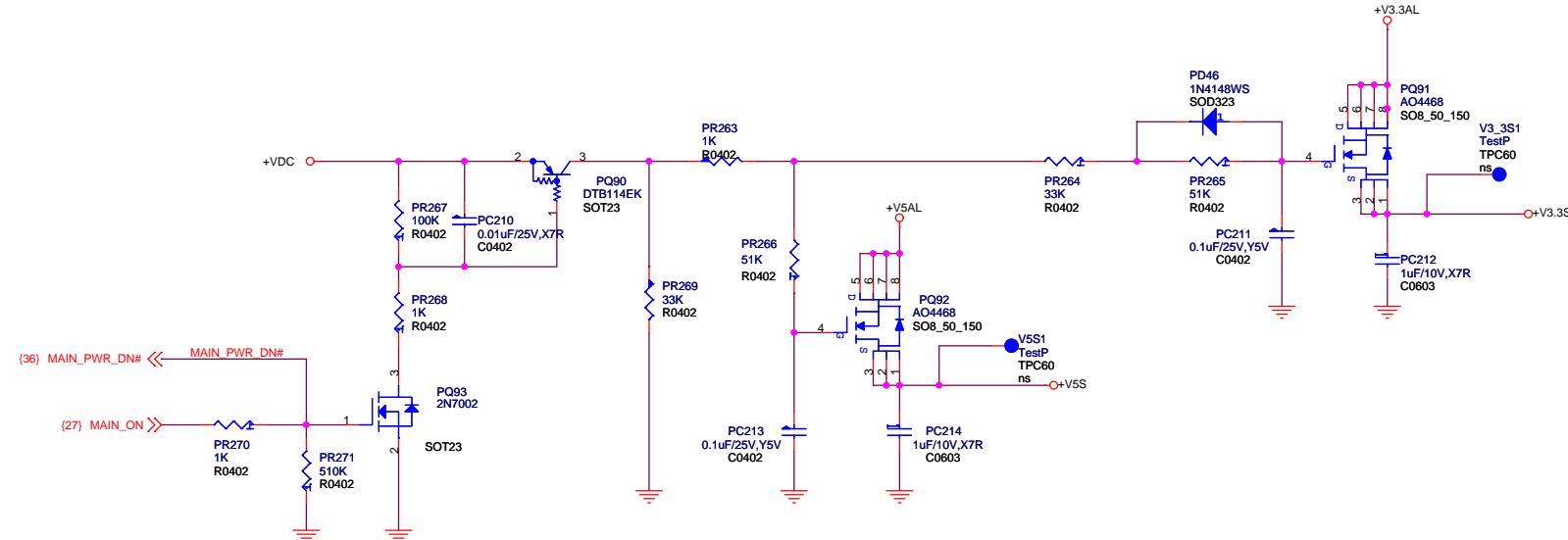
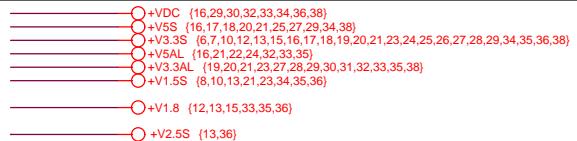
OVP CIRCUIT



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- +V3.3S (6,7,10,12,13,15,16,17,18,19,20,21,23,24,25,26,27,28,29,34,35,37,38)
 +V3.3AL (19,20,21,23,27,28,29,30,31,32,33,35,37,38)
 +V5S (16,17,18,20,21,25,27,29,34,37,38)
 +V5AL (16,21,22,24,32,33,35,37)
 +V1.5S (8,10,13,21,23,34,35)
 +V2.5S (13,37)
 +V0.9S (15,33)
 +V1.05S (6,7,8,9,13,18,21,26,34,35)
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 +V1.8 (12,13,15,33,35)

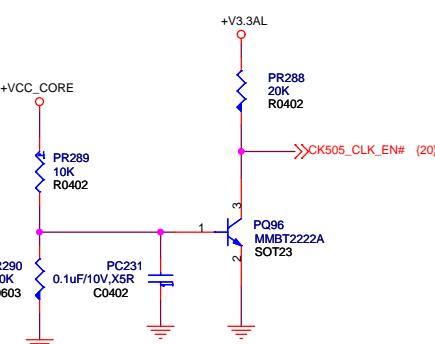
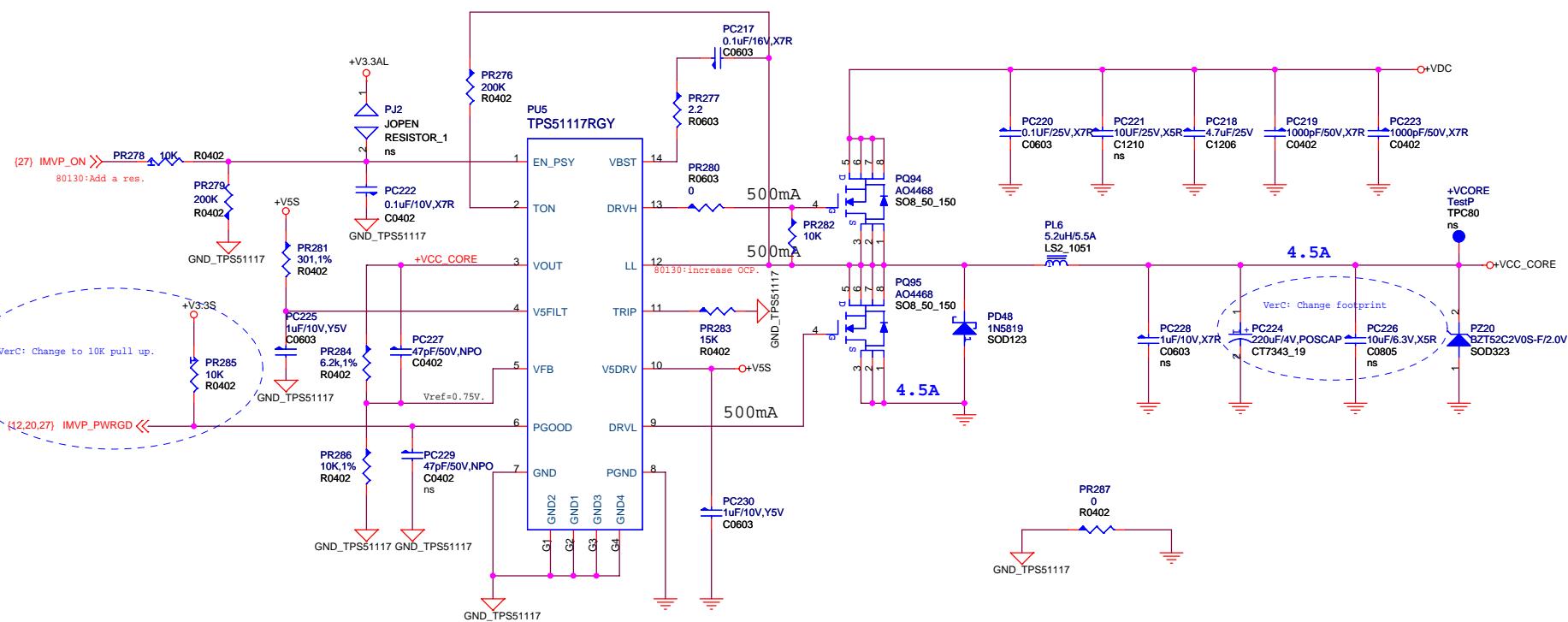




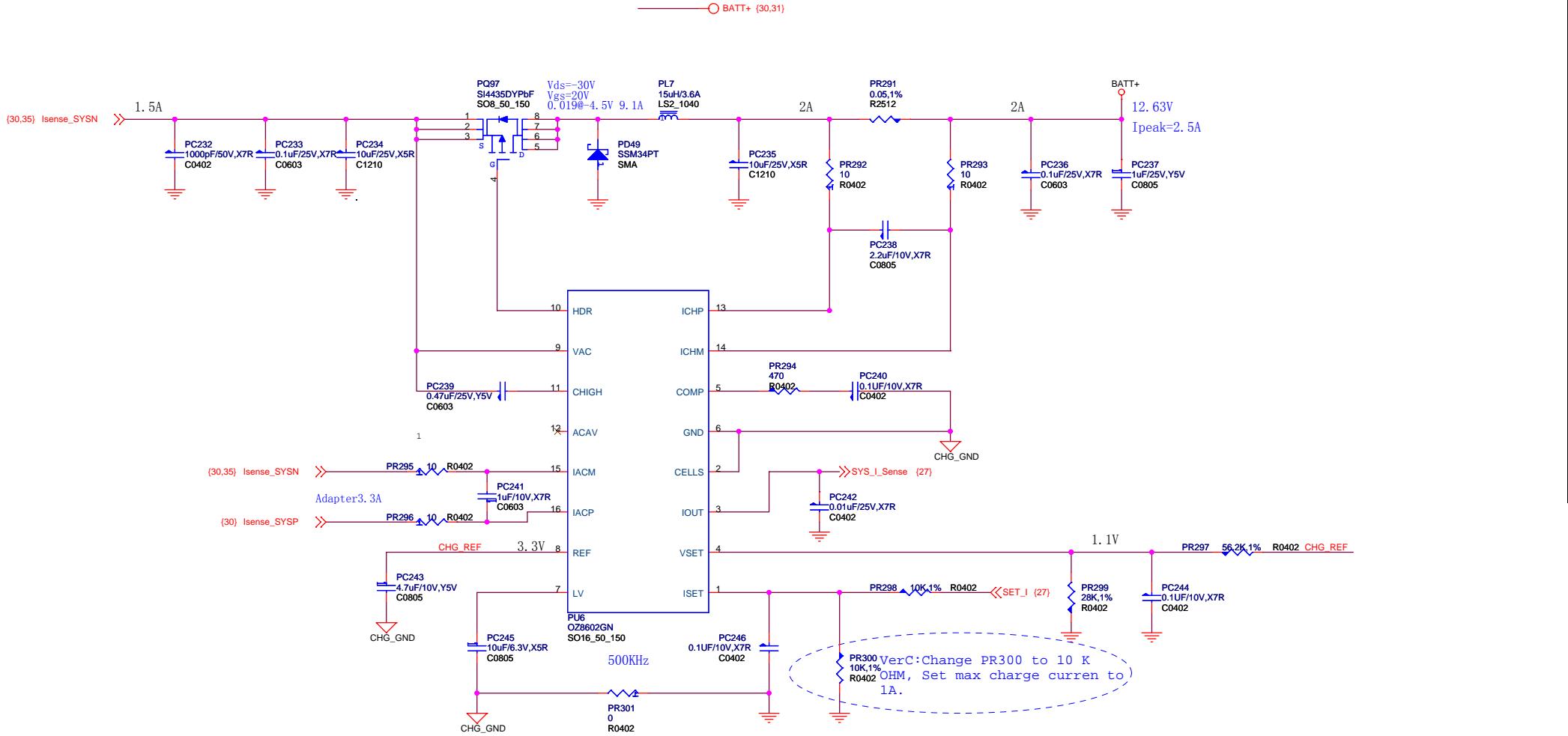
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+VDC (16,29,30,32,33,34,36,37)
 +V5S (16,17,18,20,21,25,27,29,34,37)
 +VCC_CORE (8,35)
 +V3.3S (6,7,10,12,13,15,16,17,18,19,20,21,23,24,25,26,27,28,29,34,35,36,37)
 +V3.3AL (19,20,21,23,27,28,29,30,31,32,33,35,37)

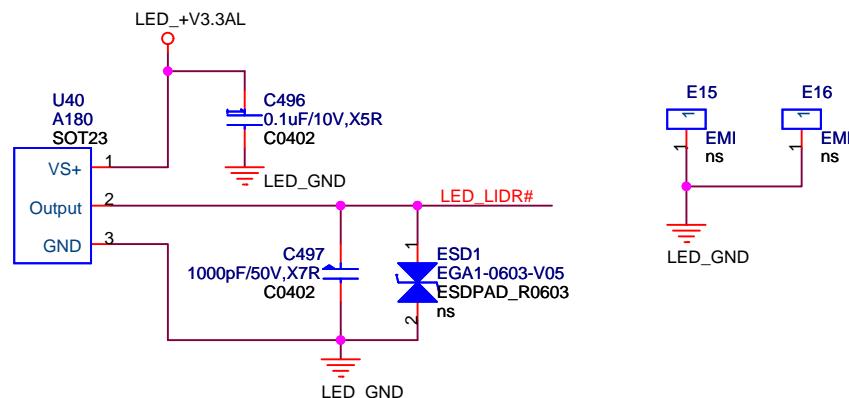
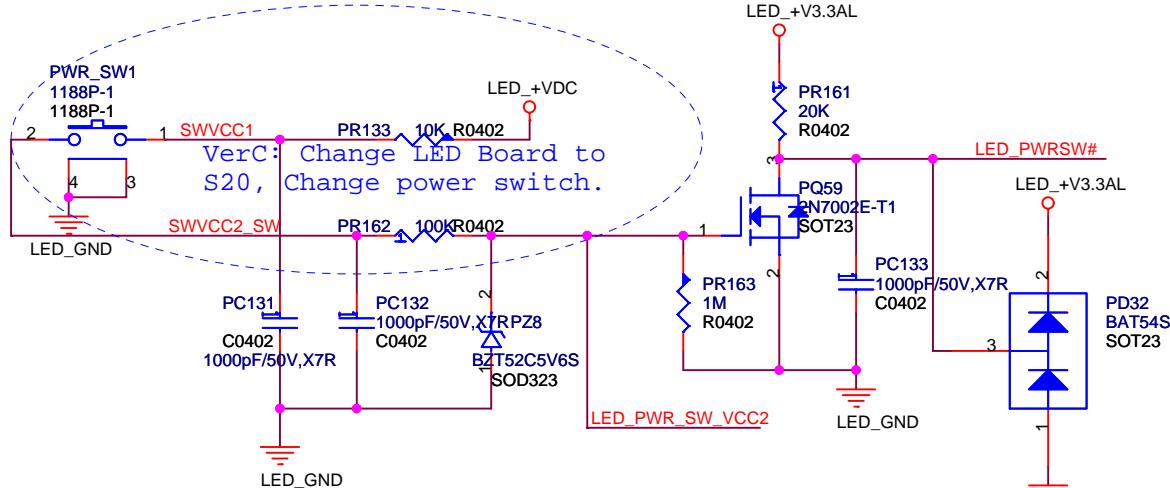
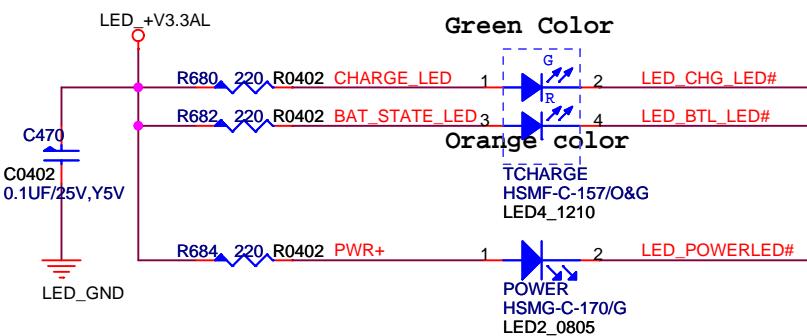
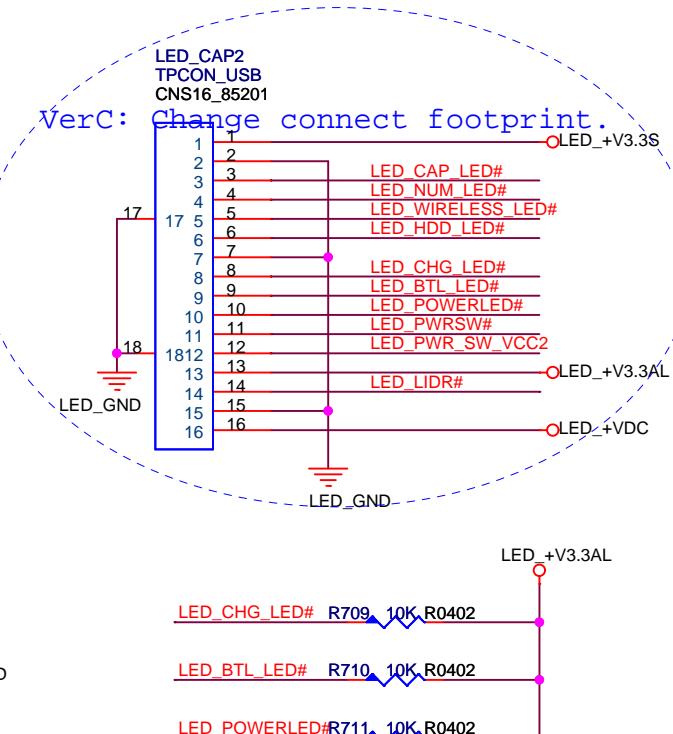
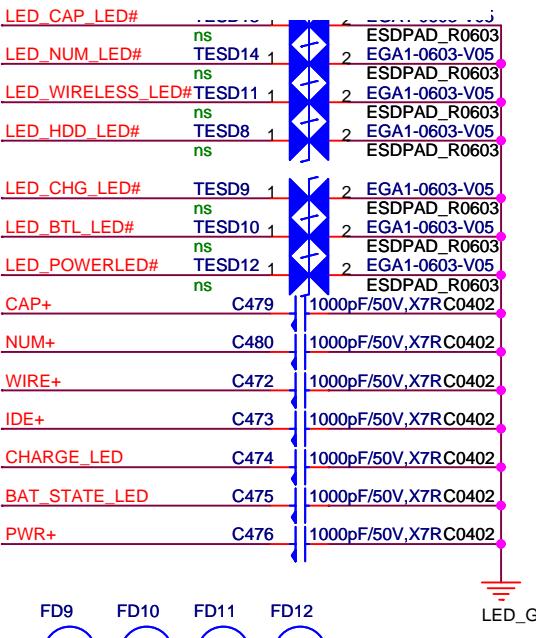
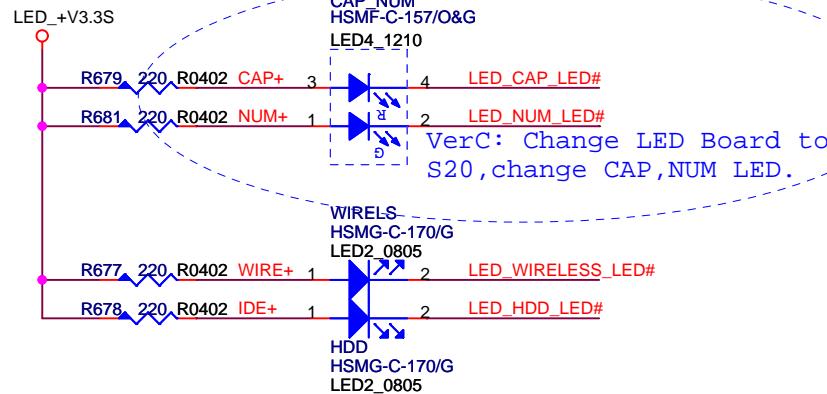


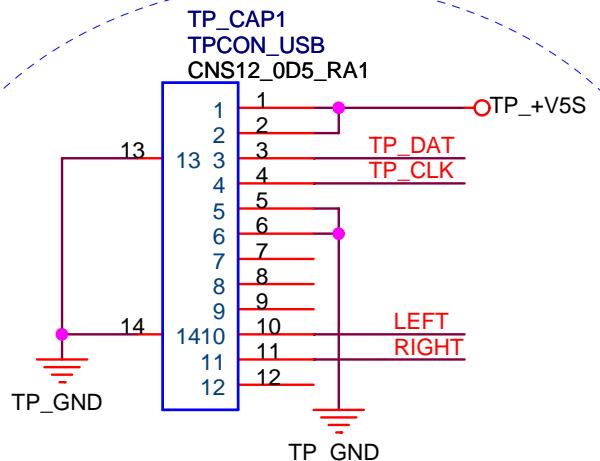
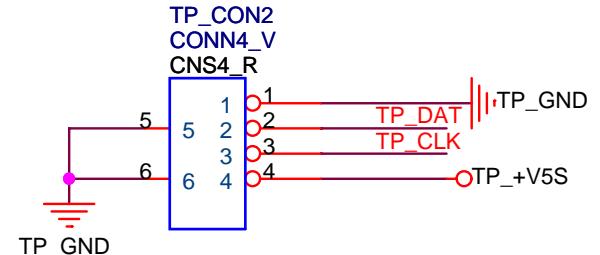
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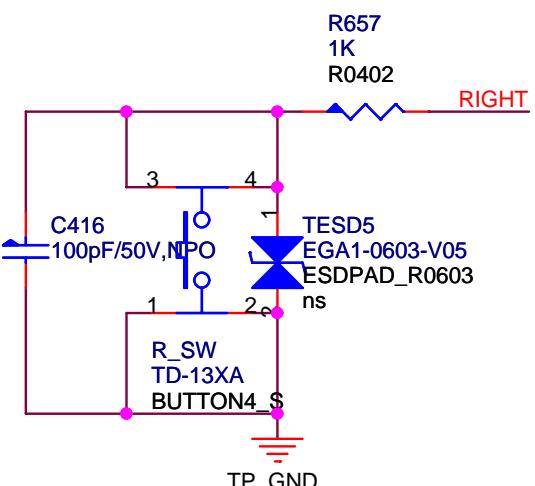
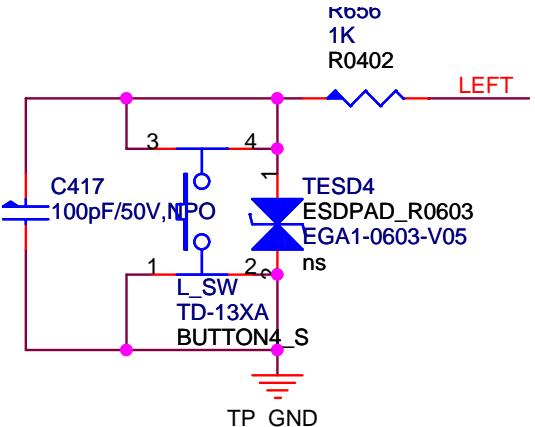
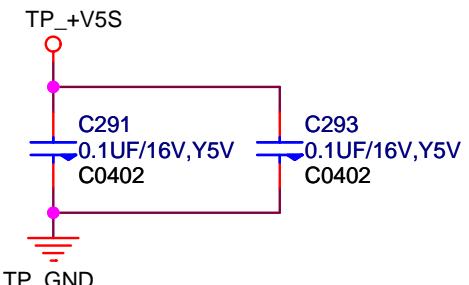
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