

██████████

[illegible]

DfE				
LCD D0	M0	DSP16LCD_D0	DSP16LCD_D16	J64
LCD D1	M1	DSP24LCD_D1	DSP24LCD_D17	J65
LCD D2	L4	DSP5LCD_D2	DSP5LCD_D18	J42
LCD D3	M8	DSP9LCD_D3	DSP22LCD_D19	J43
LCD D4	M2	DSP77LCD_D4	DSP24LCD_D20	J44
LCD D5	M6	DSP8LCD_D5	DSP24LCD_D21	J45
LCD D6	M4	DSP9LCD_D6	DSP26LCD_D22	J46
LCD D7	M8	DSP10LCD_D7	DSP26LCD_D23	J47
LCD D8	L6	DSP11LCD_D8		
LCD D9	K6	DSP24LCD_D9	DSP10LCD_DEN	P5
LCD D10	L4	DSP16LCD_D10	DSP16LCD_LS	N4
LCD D11	L4	DSP4LCD_D11	DSP26LCD_HS	N6
LCD D12	L2	DSP15LCD_D12		
LCD D13	K6	DSP16LCD_D13	DSP277LCD_CLK	G1
LCD D14	J8	DSP77LCD_D14		
LCD D15	J8	DSP18LCD_D15	DSP28	J5
			iNAPx15	
			LCD	
			iNAPx15_D1	

[illegible]

The diagram shows the pin connections for the NAND / SD Interface. It includes a JTAG_MODE pin connected to JTAG_MODE, and a JTAG_MODE pin connected to JTAG_MODE. The iMAPx15 pin is connected to iMAPx15. The NAND / SD pin is connected to NAND / SD. The diagram also shows the connection of the NAND / SD pin to the NAND / SD pin.

Pin	Signal	Direction
1	JTAG_MODE	Input
2	JTAG_MODE	Input
3	JTAG_MODE	Input
4	JTAG_MODE	Input
5	JTAG_MODE	Input
6	JTAG_MODE	Input
7	JTAG_MODE	Input
8	JTAG_MODE	Input
9	JTAG_MODE	Input
10	JTAG_MODE	Input
11	JTAG_MODE	Input
12	JTAG_MODE	Input
13	JTAG_MODE	Input
14	JTAG_MODE	Input
15	JTAG_MODE	Input
16	JTAG_MODE	Input
17	JTAG_MODE	Input
18	JTAG_MODE	Input
19	JTAG_MODE	Input
20	JTAG_MODE	Input
21	JTAG_MODE	Input
22	JTAG_MODE	Input
23	JTAG_MODE	Input
24	JTAG_MODE	Input
25	JTAG_MODE	Input
26	JTAG_MODE	Input
27	JTAG_MODE	Input
28	JTAG_MODE	Input
29	JTAG_MODE	Input
30	JTAG_MODE	Input
31	JTAG_MODE	Input
32	JTAG_MODE	Input
33	JTAG_MODE	Input
34	JTAG_MODE	Input
35	JTAG_MODE	Input
36	JTAG_MODE	Input
37	JTAG_MODE	Input
38	JTAG_MODE	Input
39	JTAG_MODE	Input
40	JTAG_MODE	Input
41	JTAG_MODE	Input
42	JTAG_MODE	Input
43	JTAG_MODE	Input
44	JTAG_MODE	Input
45	JTAG_MODE	Input
46	JTAG_MODE	Input
47	JTAG_MODE	Input
48	JTAG_MODE	Input
49	JTAG_MODE	Input
50	JTAG_MODE	Input
51	JTAG_MODE	Input
52	JTAG_MODE	Input
53	JTAG_MODE	Input
54	JTAG_MODE	Input
55	JTAG_MODE	Input
56	JTAG_MODE	Input
57	JTAG_MODE	Input
58	JTAG_MODE	Input
59	JTAG_MODE	Input
60	JTAG_MODE	Input
61	JTAG_MODE	Input
62	JTAG_MODE	Input
63	JTAG_MODE	Input
64	JTAG_MODE	Input
65	JTAG_MODE	Input
66	JTAG_MODE	Input
67	JTAG_MODE	Input
68	JTAG_MODE	Input
69	JTAG_MODE	Input
70	JTAG_MODE	Input
71	JTAG_MODE	Input
72	JTAG_MODE	Input
73	JTAG_MODE	Input
74	JTAG_MODE	Input
75	JTAG_MODE	Input
76	JTAG_MODE	Input
77	JTAG_MODE	Input
78	JTAG_MODE	Input
79	JTAG_MODE	Input
80	JTAG_MODE	Input
81	JTAG_MODE	Input
82	JTAG_MODE	Input
83	JTAG_MODE	Input
84	JTAG_MODE	Input
85	JTAG_MODE	Input
86	JTAG_MODE	Input
87	JTAG_MODE	Input
88	JTAG_MODE	Input
89	JTAG_MODE	Input
90	JTAG_MODE	Input
91	JTAG_MODE	Input
92	JTAG_MODE	Input
93	JTAG_MODE	Input
94	JTAG_MODE	Input
95	JTAG_MODE	Input
96	JTAG_MODE	Input
97	JTAG_MODE	Input
98	JTAG_MODE	Input
99	JTAG_MODE	Input
100	JTAG_MODE	Input
101	JTAG_MODE	Input
102	JTAG_MODE	Input
103	JTAG_MODE	Input
104	JTAG_MODE	Input
105	JTAG_MODE	Input
106	JTAG_MODE	Input
107	JTAG_MODE	Input
108	JTAG_MODE	Input
109	JTAG_MODE	Input
110	JTAG_MODE	Input
111	JTAG_MODE	Input
112	JTAG_MODE	Input
113	JTAG_MODE	Input
114	JTAG_MODE	Input
115	JTAG_MODE	Input
116	JTAG_MODE	Input
117	JTAG_MODE	Input
118	JTAG_MODE	Input
119	JTAG_MODE	Input
120	JTAG_MODE	Input
121	JTAG_MODE	Input
122	JTAG_MODE	Input
123	JTAG_MODE	Input
124	JTAG_MODE	Input
125	JTAG_MODE	Input
126	JTAG_MODE	Input
127	JTAG_MODE	Input
128	JTAG_MODE	Input
129	JTAG_MODE	Input
130	JTAG_MODE	Input
131		

The diagram shows the pin-to-pin connections for the Audio / CAM Interface. The iM4Px15 module (left) has pins A204, B204, D18, B214, C20, C21, I1D18, I2D20, I1E18, and I1E20. The iM4Px15_01 module (right) has pins E21, E19, F17, F18, F19, F20, F18, F19, G20, G21, G20, G17, H18, H17, J18, J17, and K17. The connections are as follows:

iM4Px15 Pin	iM4Px15_01 Pin	Signal	Notes
A204	E21	AUD10PCM1_CDCLK	
B204	E19	AUD11PCM1_SCLK	
D18	F17	AUD12PCM1_SOUT	
B214	F18	AUD13PCM1_SN	
C20	F19	AUD14PCM1_FSYNC	
C21	F20	AUD15SSPD_RXD	
I1D18	F18	AUD16SSPD_TXD	
I2D20	G20	AUD17SSPD_CLK	
I1E18	G21	AUD18SSPD_CSN	
I1E20	G17	AUD19SSPD_FSYNC	
	H18	AUD20SSP1_TXD	
	H17	AUD21SSP1_CLK	
	J18	AUD22SSP1_CSN	
	J17	AUD23	
	K17	AUD24	

Additional connections shown in the diagram:

- A204 to I1D18: AU_MCLK
- B204 to I2D20: AU_BCLK
- D18 to I1E18: AU_SYNC
- B214 to I1E20: AU_SDI
- C20 to I1E18: AU_SDO
- I1D18 to I1E18: PCM0_SCLK
- I2D20 to I1E18: PCM0_SOUT
- I1E18 to I1E20: PCM0_SIN
- I1E20 to I1E20: PCM0_FSYNC

Other signals and components shown:

- TP57: SPK_MUTE (10)
- R237: CHARGE_STA (11)
- U8NC: CTP_INT (5, 9)
- G-SENSOR-INT (10)
- JACK_DET (10)

PWM / UART / GPS / I2C Interface

CAM AUDIO

PMU

TP

BL_PWM

SYS_OCLK3K

UART

infoTM

OMAP3530

UART

UART_TXD1

UART_RXD1

UART_TXD3

UART_RXD3

UART_TXD0

UART_RXD0

UART_TXD2

UART_RXD2

UART_TXD4

UART_RXD4

UART_TXD5

UART_RXD5

UART_TXD6

UART_RXD6

UART_TXD7

UART_RXD7

UART_TXD8

UART_RXD8

UART_TXD9

UART_RXD9

UART_TXD10

UART_RXD10

UART_TXD11

UART_RXD11

UART_TXD12

UART_RXD12

UART_TXD13

UART_RXD13

UART_TXD14

UART_RXD14

UART_TXD15

UART_RXD15

UART_TXD16

UART_RXD16

UART_TXD17

UART_RXD17

UART_TXD18

UART_RXD18

UART_TXD19

UART_RXD19

UART_TXD20

UART_RXD20

UART_TXD21

UART_RXD21

UART_TXD22

UART_RXD22

UART_TXD23

UART_RXD23

UART_TXD24

UART_RXD24

UART_TXD25

UART_RXD25

UART_TXD26

UART_RXD26

UART_TXD27

UART_RXD27

UART_TXD28

UART_RXD28

UART_TXD29

UART_RXD29

UART_TXD30

UART_RXD30

UART_TXD31

UART_RXD31

UART_TXD32

UART_RXD32

UART_TXD33

UART_RXD33

UART_TXD34

UART_RXD34

UART_TXD35

UART_RXD35

UART_TXD36

UART_RXD36

UART_TXD37

UART_RXD37

UART_TXD38

UART_RXD38

UART_TXD39

UART_RXD39

UART_TXD40

UART_RXD40

UART_TXD41

UART_RXD41

UART_TXD42

UART_RXD42

UART_TXD43

UART_RXD43

UART_TXD44

UART_RXD44

UART_TXD45

UART_RXD45

UART_TXD46

UART_RXD46

UART_TXD47

UART_RXD47

UART_TXD48

UART_RXD48

UART_TXD49

UART_RXD49

UART_TXD50

UART_RXD50

UART_TXD51

UART_RXD51

UART_TXD52

UART_RXD52

UART_TXD53

UART_RXD53

UART_TXD54

UART_RXD54

UART_TXD55

UART_RXD55

UART_TXD56

UART_RXD56

UART_TXD57

UART_RXD57

UART_TXD58

UART_RXD58

UART_TXD59

UART_RXD59

UART_TXD60

UART_RXD60

UART_TXD61

UART_RXD61

UART_TXD62

UART_RXD62

UART_TXD63

UART_RXD63

UART_TXD64

UART_RXD64

UART_TXD65

UART_RXD65

UART_TXD66

UART_RXD66

UART_TXD67

UART_RXD67

UART_TXD68

UART_RXD68

UART_TXD69

UART_RXD69

UART_TXD70

UART_RXD70

UART_TXD71

UART_RXD71

UART_TXD72

UART_RXD72

UART_TXD73

UART_RXD73

UART_TXD74

UART_RXD74

UART_TXD75

UART_RXD75

UART_TXD76

UART_RXD76

UART_TXD77

UART_RXD77

UART_TXD78

UART_RXD78

UART_TXD79

UART_RXD79

UART_TXD80

UART_RXD80

UART_TXD81

UART_RXD81

UART_TXD82

UART_RXD82

UART_TXD83

UART_RXD83

UART_TXD84

UART_RXD84

UART_TXD85

UART_RXD85

UART_TXD86

UART_RXD86

UART_TXD87

UART_RXD87

UART_TXD88

UART_RXD88

UART_TXD89

UART_RXD89

UART_TXD90

UART_RXD90

UART_TXD91

UART_RXD91

UART_TXD92

UART_RXD92

UART_TXD93

UART_RXD93

UART_TXD94

UART_RXD94

UART_TXD95

UART_RXD95

UART_TXD96

UART_RXD96

UART_TXD97

UART_RXD97

UART_TXD98

UART_RXD98

UART_TXD99

UART_RXD99

UART_TXD100

UART_RXD100

UART_TXD101

UART_RXD101

UART_TXD102

UART_RXD102

UART_TXD103

UART_RXD103

UART_TXD104

UART_RXD104

UART_TXD105

UART_RXD105

UART_TXD106

UART_RXD106

UART_TXD107

UART_RXD107

UART_TXD108

UART_RXD108

UART_TXD109

UART_RXD109

UART_TXD110

UART_RXD110

UART_TXD111

UART_RXD111

UART_TXD112

UART_RXD112

UART_TXD113

UART_RXD113

UART_TXD114

UART_RXD114

UART_TXD115

UART_RXD115

UART_TXD116

TIAG/Misc Interface

Pinout diagram for TIAG/Misc Interface of the OMAP3530. The diagram shows connections for pins U1-H, L-V2, L-V3, L-V4, L-V5, L-V6, L-V7, L-V8, L-V9, L-V10, L-V11, L-V12, L-V13, L-V14, L-V15, L-V16, L-V17, L-V18, L-V19, L-V20, L-V21, L-V22, L-V23, L-V24, L-V25, L-V26, L-V27, L-V28, L-V29, L-V30, L-V31, L-V32, L-V33, L-V34, L-V35, L-V36, L-V37, L-V38, L-V39, L-V40, L-V41, L-V42, L-V43, L-V44, L-V45, L-V46, L-V47, L-V48, L-V49, L-V50, L-V51, L-V52, L-V53, L-V54, L-V55, L-V56, L-V57, L-V58, L-V59, L-V60, L-V61, L-V62, L-V63, L-V64, L-V65, L-V66, L-V67, L-V68, L-V69, L-V70, L-V71, L-V72, L-V73, L-V74, L-V75, L-V76, L-V77, L-V78, L-V79, L-V80, L-V81, L-V82, L-V83, L-V84, L-V85, L-V86, L-V87, L-V88, L-V89, L-V90, L-V91, L-V92, L-V93, L-V94, L-V95, L-V96, L-V97, L-V98, L-V99, L-V100. The diagram includes connections for RTC, RESET, TEST, POWER, and MISC functions. A callout box highlights the connection for the POWER_IND pin, which is connected to the 1.8V pin of the OMAP3530.

The diagram illustrates the clock source configuration for the iMAPx15. It features a central box labeled **infoTM** with **iMAPx15** below it. To the left, four clock sources are listed: **SYS_XTALI**, **SYS_XTALO**, **RTC_XTALI**, and **RTC_XTALO**. These are connected to a vertical bus labeled **CLK**. The connections are as follows: **SYS_XTALI** to **K19**, **SYS_XTALO** to **K20**, **RTC_XTALI** to **M19**, and **RTC_XTALO** to **M20**. The **CLK** bus is connected to the **iMAPx15** block. The **infoTM** logo is stylized with a blue 'i' and 'M'.

Crystal

Reset Circuit

VDDRTC33

R1

200K

C2

100nF

0

0nF

0

4

REST_GPD

SYS_RST_0

SYS_RST

PULL Circuit

MS_SREN

R10

100K

R11

100K

4

MEM_SREN

Reset Circuit

VDDRTC33

R1

200K

C2

100nF

0

0nF

0

4

REST_GPD

SYS_RST_0

SYS_RST

PULL Circuit

MS_SREN

R10

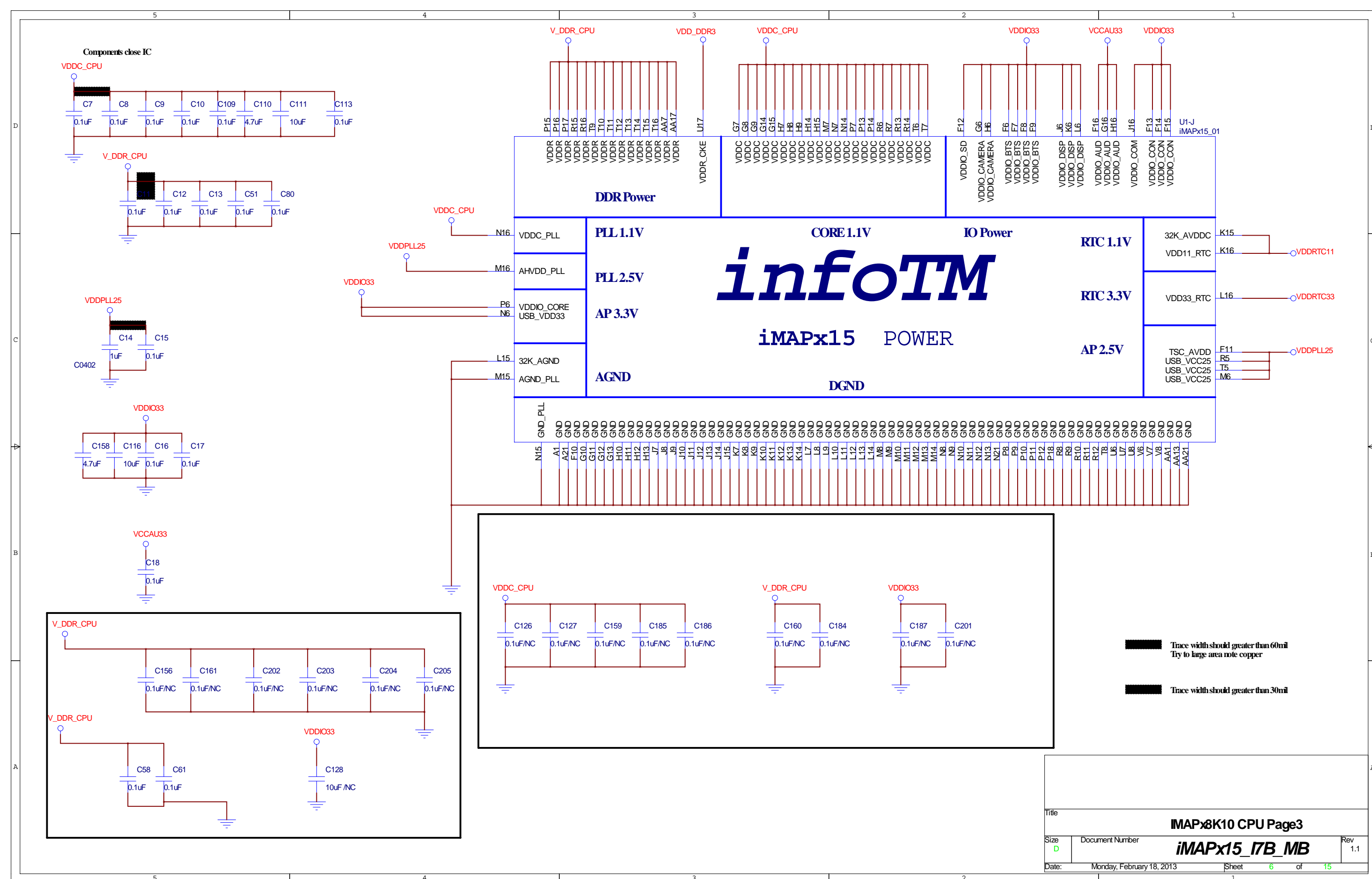
100K

R11

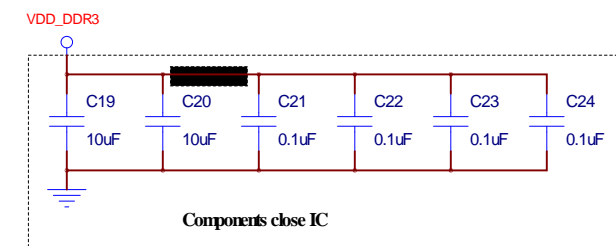
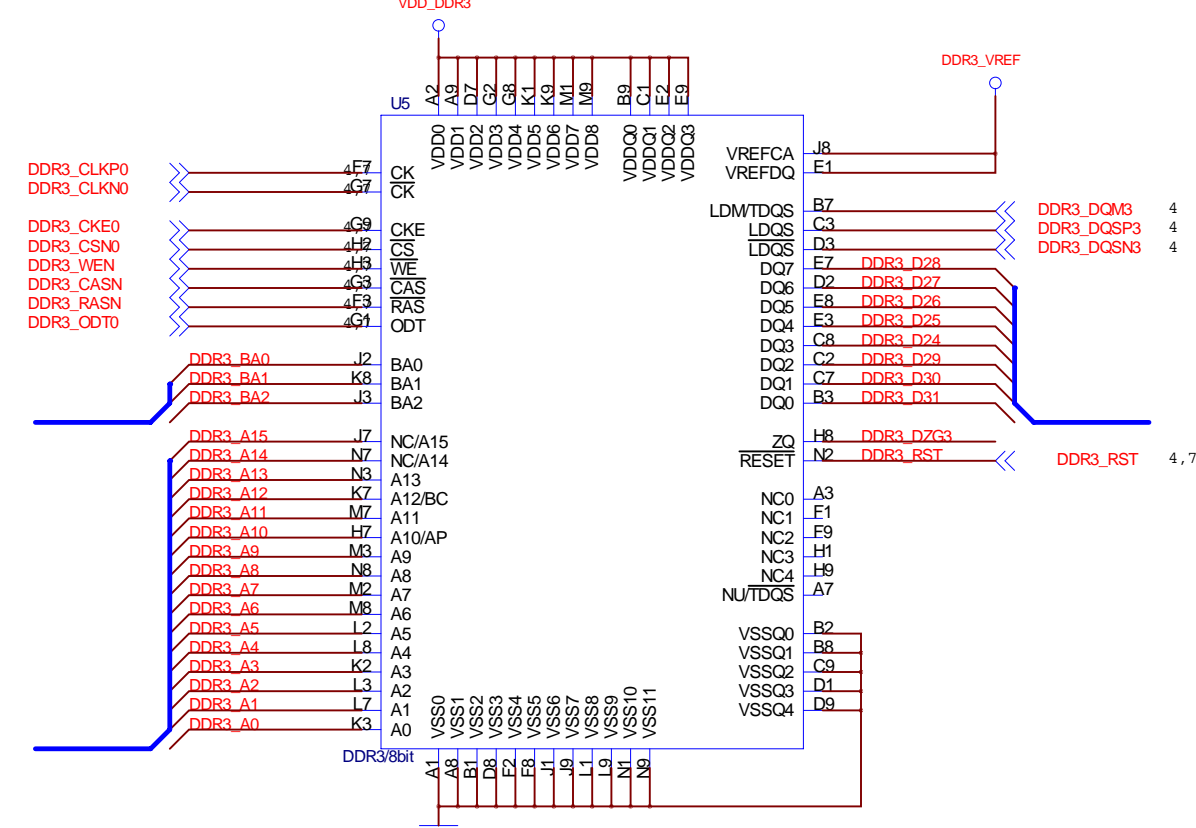
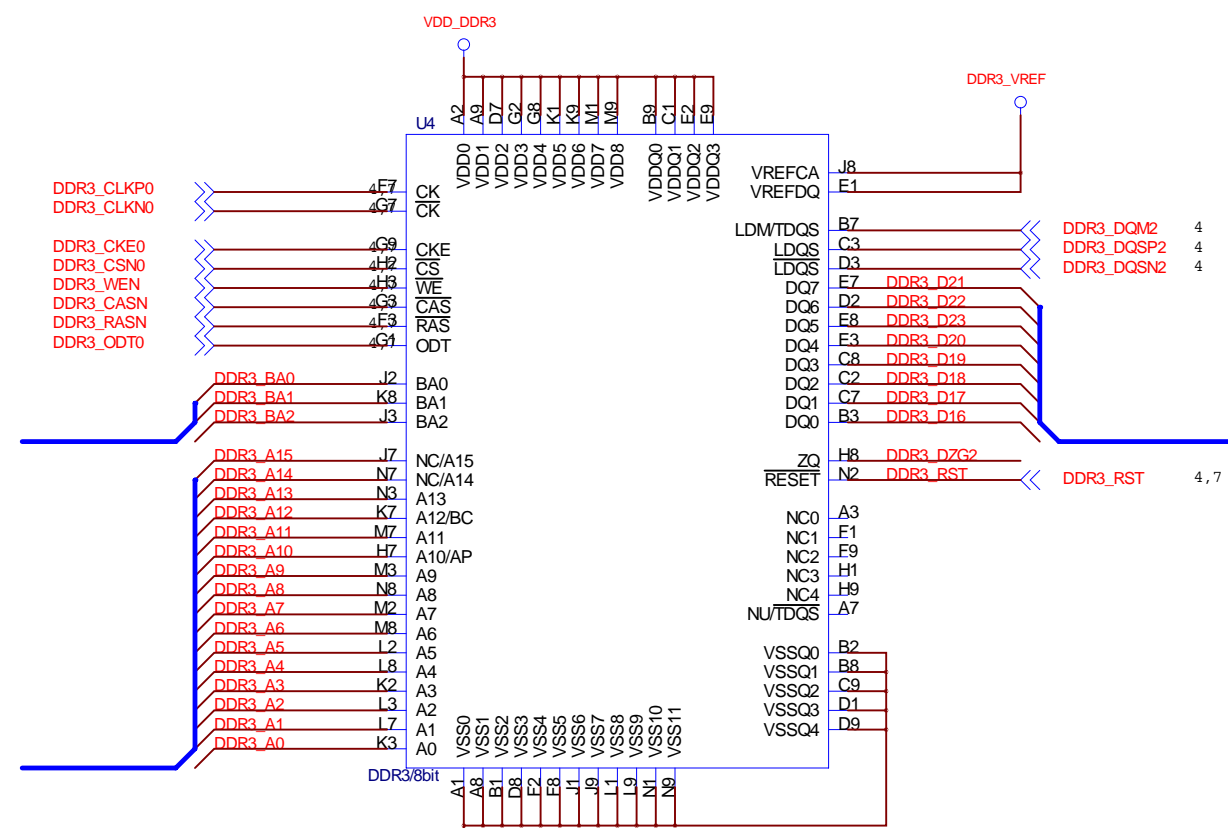
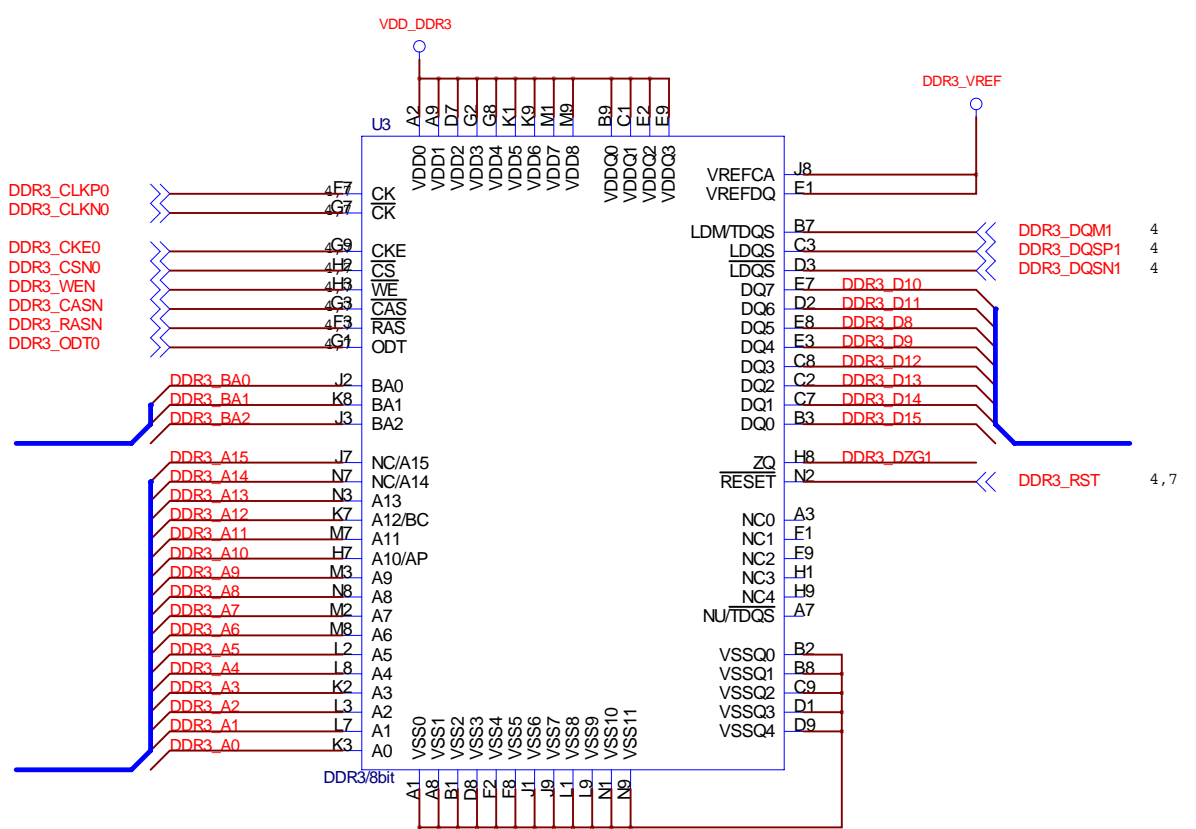
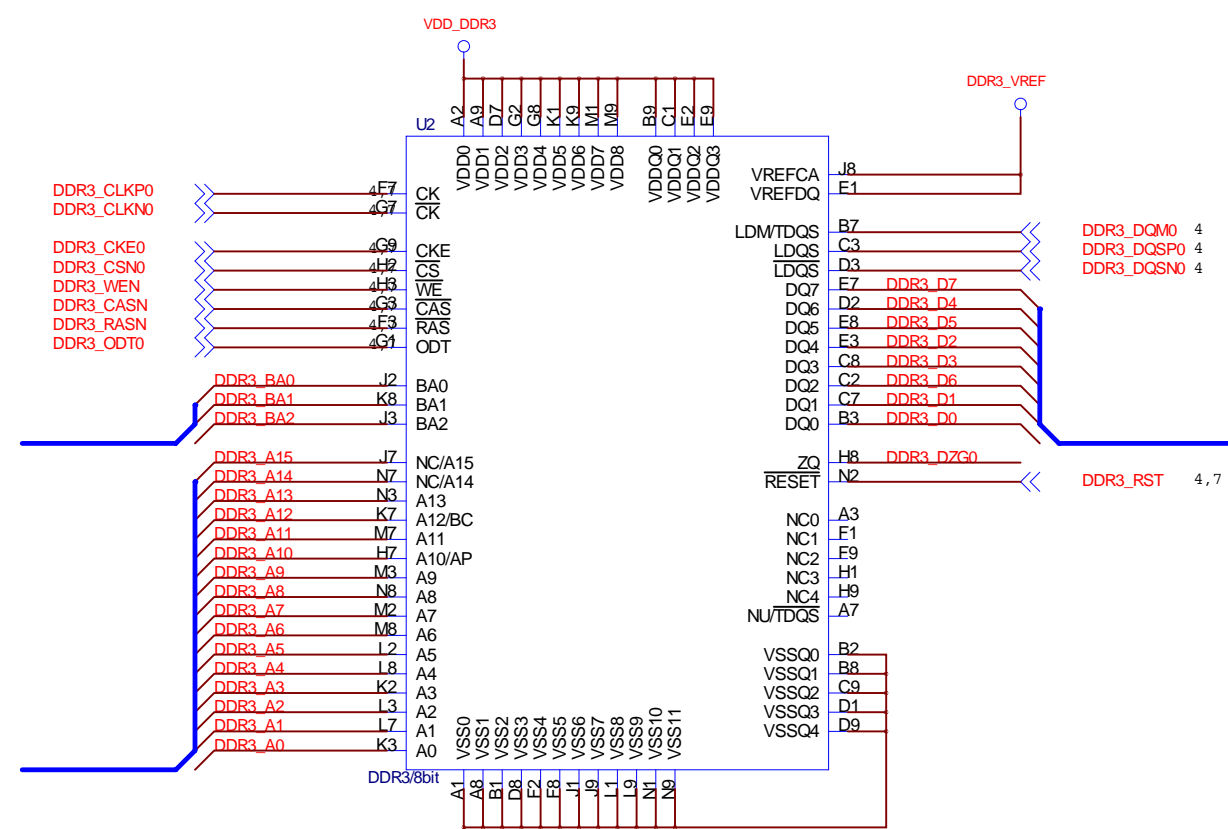
100K

4

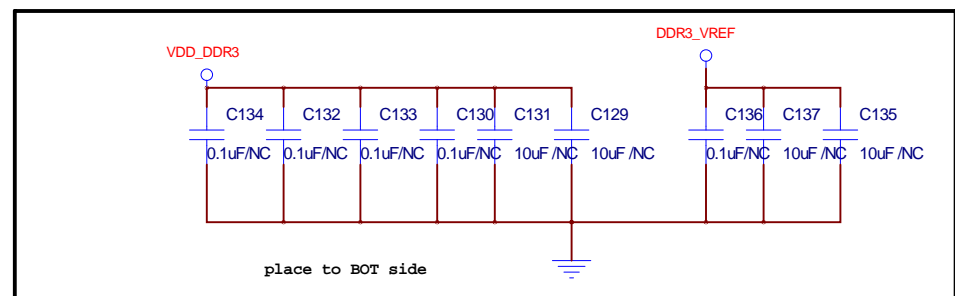
MEM_SREN



DDR3



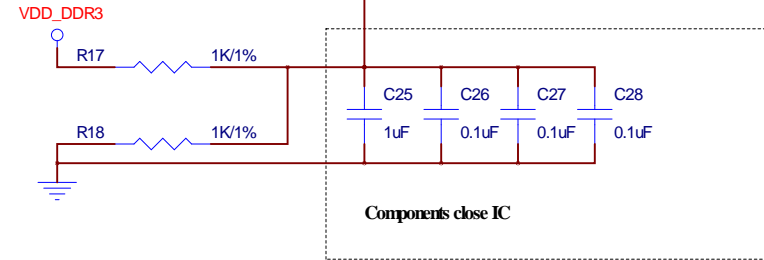
Try to large area ntc copper



place to BOT side



Modify DDR VREF power from V_FBB_CPD to VDD_DDR3



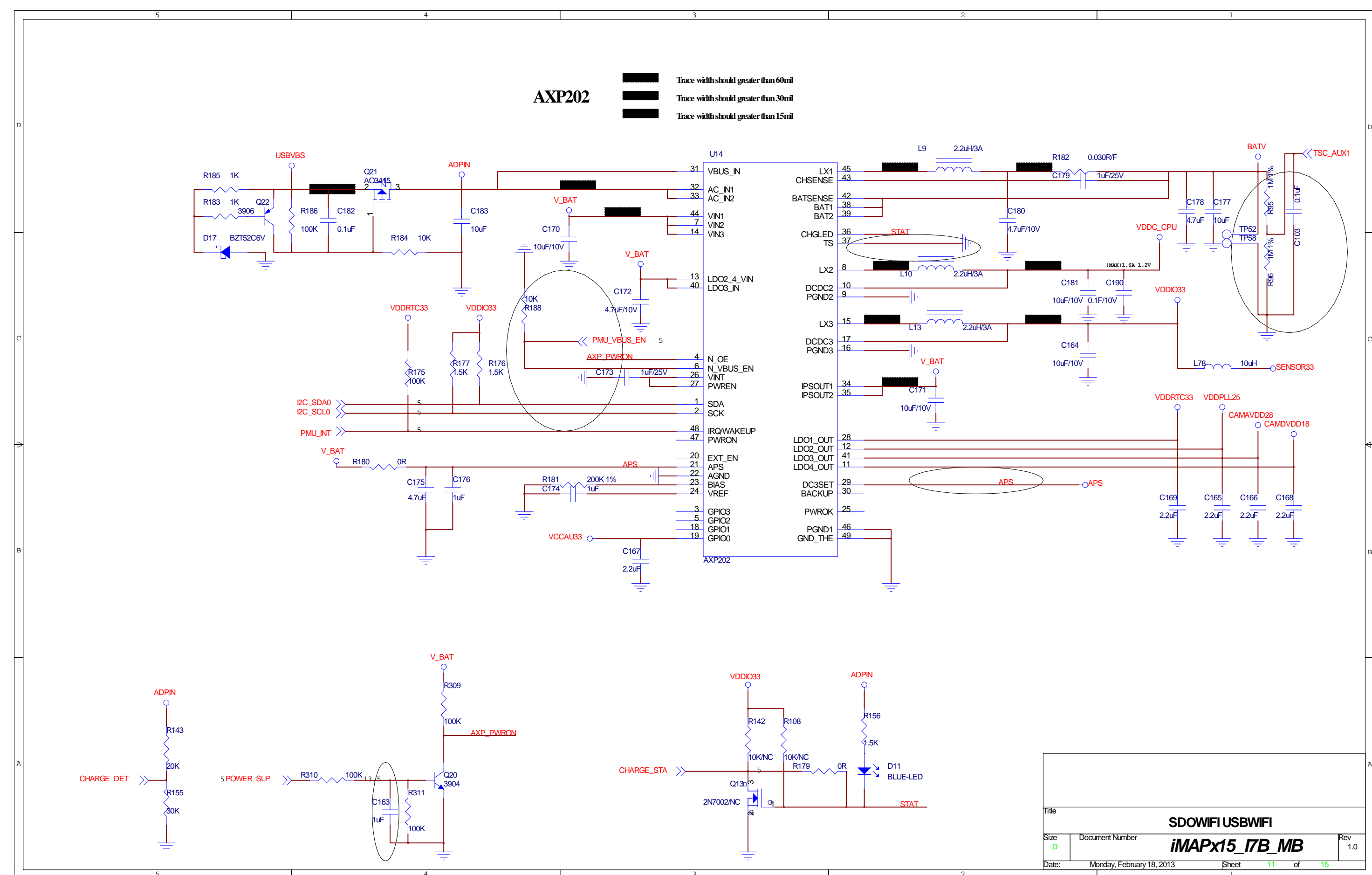
Components close IC

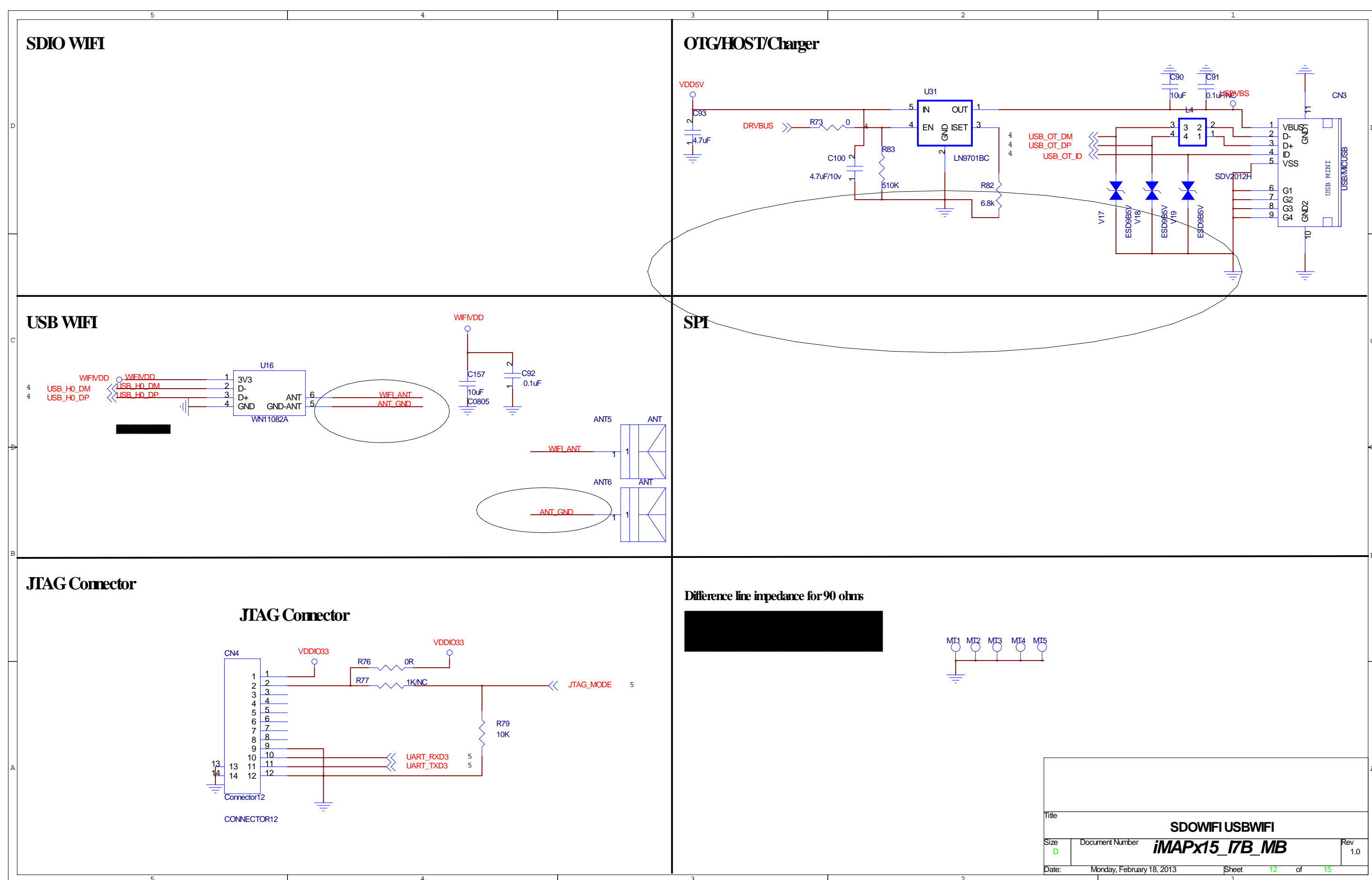
Title		
DDR3 SDRAM		
Doc Number	iMAPx15_I7B_MB	
Date	Monday, February 18, 2013	Rev 1.1
Sheet	7	of 15

The diagram shows a speaker driver circuit. It includes a 5V regulator (U10) and an LM4890 (U11). The speaker is connected to the output of the op-amp. The circuit is powered by a 5V regulator (U10) and an LM4890 (U11). The speaker is connected to the output of the op-amp. The circuit is powered by a 5V regulator (U10) and an LM4890 (U11). The speaker is connected to the output of the op-amp.

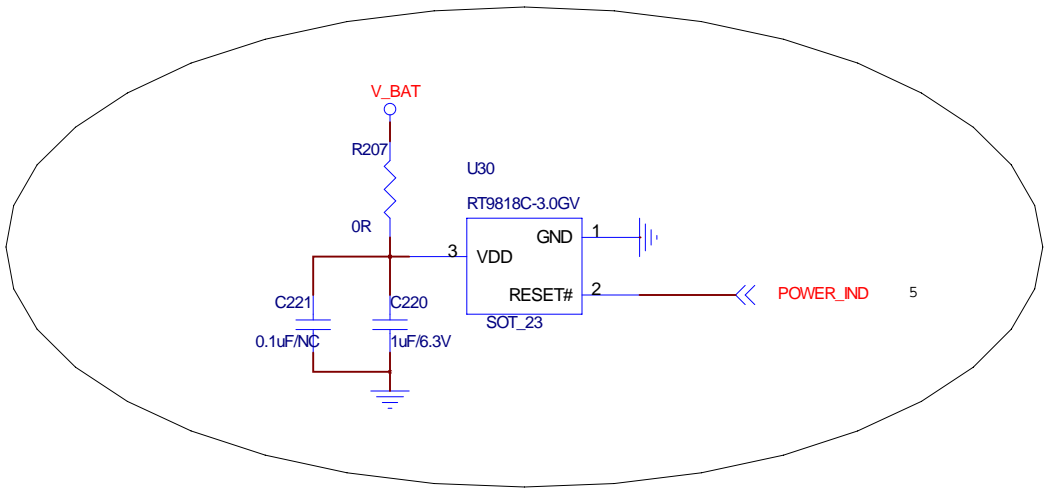
The schematic diagram illustrates the internal circuitry of the EarPhone module. It features two main audio output paths: a left channel (ALL OUT) and a right channel (AUR OUT). Each path consists of a resistor (R132 and R135, both 10K), a capacitor (C66 and C68, both 10uF), and a 1K resistor (R148 and R149) connected to ground. The left channel output is labeled 'L OUT' and the right channel output is labeled 'R OUT'. A jack detection circuit is also present, featuring a 10K resistor (R80) connected to a 'VCCAUX3' input and a 10K resistor (R89) connected to a 'JACK_DET' output. A 0.1uF capacitor (C79) is connected to the 'JACK_DET' output. The module is connected to an 'Audio_Jack' (35) which has pins 1, 2, 3, 4, 5, and 6. Pins 2, 3, 4, and 5 are connected to the audio output lines, while pins 1 and 6 are connected to ground.

[illegible]

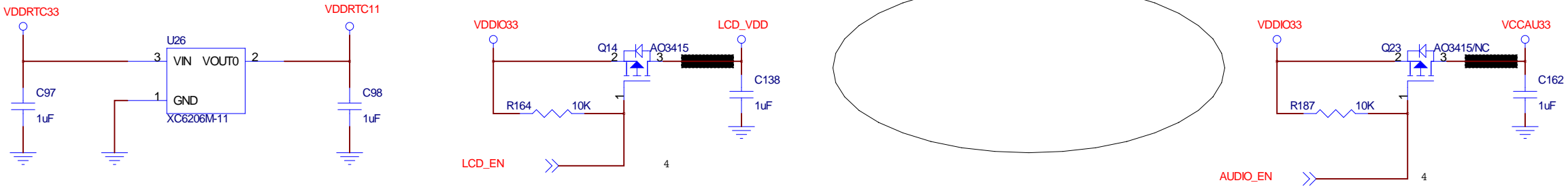




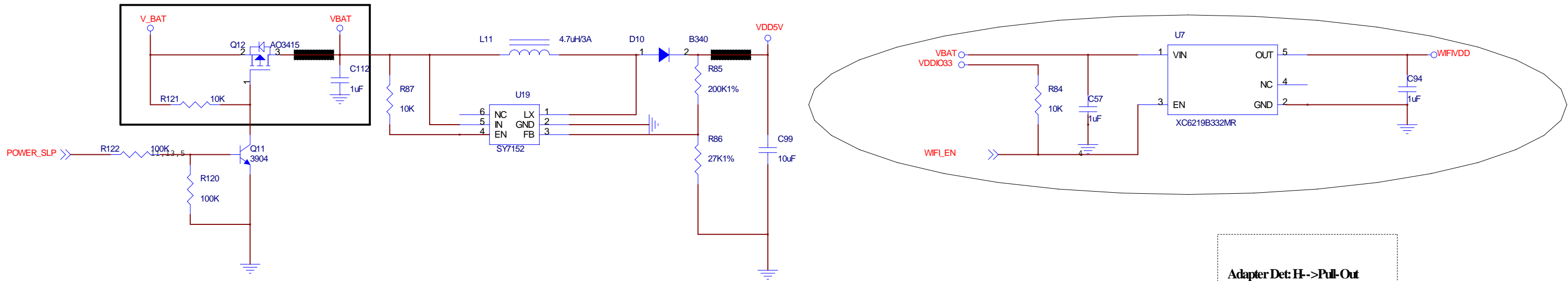
RTC INT



DC Power Input

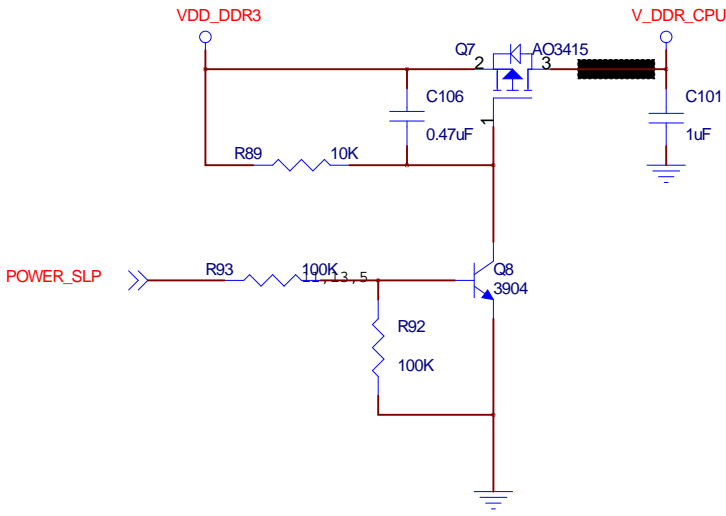


Boost 5V



Trace width should greater than 70mil

V_DDR_CPU

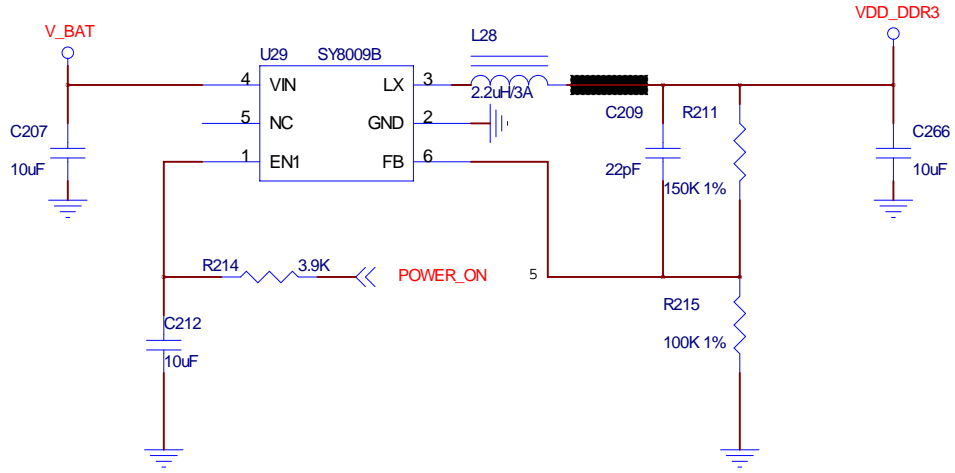


Trace width should greater than 60mil

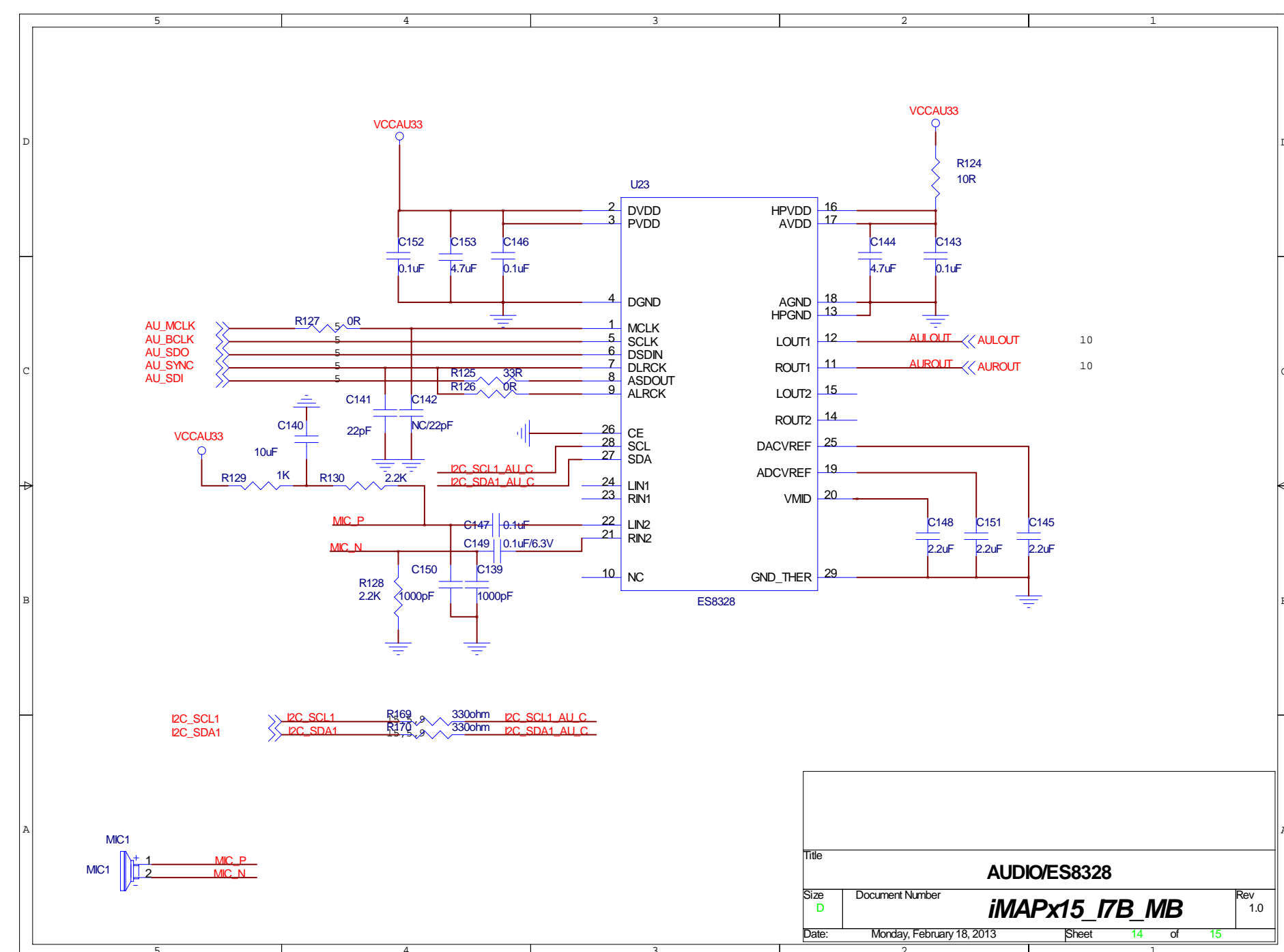
Power-ON and Low-Bat Protector!

battery low voltage for 3.3v

SYSTEM POWER DDR3



Trace width should greater than 80mil



[illegible]

Title				
BT SECTION				
Size	Document Number			Rev
D	<i>IMAPx15_17B_MB</i>			1.0
Date:	Monday, February 18, 2013	Sheet	15	of 15