

AG35 Hardware Design

Automotive Module Series

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About the Document

History

Revision	Date	Author	Description
1.0	2018-03-19	Eden LIU/ Dominic GONG	Initial
			<ol style="list-style-type: none">1. Updated the variants and/or frequency bands of AG35 (Table 1).2. Updated the functional diagram (Figure 1).3. Updated the pin assignment of AG35 (Figure 2).4. Updated the drive current of STATUS pin (Table 4).5. Enabled SHDN_N (pin 176), and added the description of the interface in Chapter 3.7.2.3.6. Enabled an optional audio interface (pins 132~141) for AG35 (Chapter 3.12).7. Updated the pin definition of PCM and I2C interfaces in Chapter 3.13.8. Updated the power domain of SGMII interface (Chapter 3.15).
1.1	2018-12-12	Eden LIU/ Dominic GONG/ Ethan SHAN	<ol style="list-style-type: none">9. Added the description of RTC function (Chapter 3.22).10. Added GNSS performance values of AG35-NA and AG35-J (Chapter 4.2).11. Completed the operating frequency of the module (Chapter 5.1.2),12. Updated the frequency of Galileo and QZSS (Table 34).13. Updated current consumption values of the module (Chapter 6.4).14. Completed the RF output power values of the module (Chapter 6.5).15. Added the RF receiving sensitivity of AG35-E, AG35-NA and AG35-J (Chapter 6.6).

			16. Updated the recommended reflow soldering thermal profile and involved parameters (Chapter 8.2).
1.2	2019-04-30	Eden LIU/ Dominic GONG	<ul style="list-style-type: none"> 1. Removed the optional LTE-FDD B28 from AG35-NA. 2. Enabled HSIC interface (pin 194/195) and added related information thereof (Chapter 2.2, Chapter 2.3, Chapter 3.2, Chapter 3.3 and Chapter 3.23). 3. Added audio interface characteristics (Table 17). 4. Updated the reference circuit for connection with AF20 module (Figure 29). 5. Added AG35-E and AG35-LA GNSS performance parameters (Table 33 and Table 35). 6. Updated AG35-J GNSS performance parameters (Table 36). 7. Updated GNSS frequency (Table 44). 8. Updated current consumption values of the module (Chapter 6.4). 9. Updated RF receiving sensitivity (Chapter 6.6). 10. Updated electrostatic discharge characteristics (Table 69). 11. Updated the recommended stencil thickness and the peak reflow temperature (Chapter 8.2).
1.3	2019-05-20	Eden LIU	Corrected some pin names in the pin assignment figure (Figure 2).

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1 Introduction

This document defines the AG35 module and describes its air interface and hardware interfaces which are connected with customers' applications.

This document can help customers quickly understand module interface specifications, electrical and mechanical details, as well as other related information of the module. Associated with application notes and user guides, customers can use AG35 to design and set up automotive industry mobile applications easily.

Hereby, [Quectel Wireless Solutions Co., Ltd.] declares that the radio equipment type [AG35-LA] is in compliance with Directive 2014/53/EU.

The full text of the EU declaration of conformity is available at the following internet address:
<http://www.quectel.com>



The device could be used with a separation distance of 20cm to the human body.

OEM/Integrators Installation Manual

Important Notice to OEM integrators

1. This module is limited to OEM installation ONLY.
2. This module is limited to installation in mobile or fixed applications, according to Part 2.1091(b).
3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations
4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part 15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are compliant with the transmitter(s) rule(s). The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

Important Note

notice that any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify to Quectel Wireless Solutions Co., Ltd. that they wish to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by the USI, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application.

End Product Labeling

When the module is installed in the host device, the FCC/IC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text: "Contains FCC ID: XMR201905AG35LA"

The FCC ID/IC ID can be used only when all FCC/IC compliance requirements are met.

Antenna Installation

- (1) The antenna must be installed such that 20 cm is maintained between the antenna and users,
- (2) The transmitter module may not be co-located with any other transmitter or antenna.
- (3) Only antennas of the same type and with equal or less gains as shown below may be used with this module. Other types of antennas and/or higher gain antennas may require additional authorization for operation.

Antenna type	GSM850 Gain (dBi)	GSM1900 Gain (dBi)	WCDMA Band II Gain (dBi)	WCDMA Band IV Gain (dBi)	WCDMA Band V Gain (dBi)
Fixed External Antenna	4.50	2.00	2.00	5.00	4.50
Antenna type	LTE Band 2 Gain (dBi)	LTE Band 4 Gain (dBi)	LTE Band 5 Gain (dBi)	LTE Band 7 Gain (dBi)	
Fixed External Antenna	2.00	5.00	4.50	7.00	

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC/IC authorization is no longer considered valid and the FCC ID/IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC/IC authorization.

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in

conjunction with any other antenna or transmitter.

List of applicable FCC rules

This module has been tested and found to comply with part 22, part 24, part 27 requirements for Modular Approval.

The modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuitry), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

This device is intended only for OEM integrators under the following conditions: (For module device use)

- 1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
- 2) The transmitter module may not be co-located with any other transmitter or antenna.

As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

1.1. Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating AG35 module. Manufacturers of the cellular terminal should send the following safety information to users and operating personnel, and incorporate these guidelines into all manuals supplied with the product. If not so, Quectel assumes no liability for customers' failure to comply with these precautions.



Full attention must be given to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.



Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If the device offers an Airplane Mode, then it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on boarding the aircraft.



Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.



Cellular terminals or mobiles operating over radio signals and cellular network cannot be guaranteed to connect in all possible conditions (for example, with unpaid bills or with an invalid (U)SIM card). When emergent help is needed in such conditions, please remember using emergency call. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength.



The cellular terminal or mobile contains a transmitter and receiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV set, radio, computer or other electric equipment.



In locations with potentially explosive atmospheres, obey all posted signs to turn off wireless devices such as your phone or other cellular terminals. Areas with potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, areas where the air contains chemicals or particles such as grain, dust or metal powders, etc.

2 Product Concept

2.1. General Description

AG35 is a series of automotive-grade LTE-FDD/LTE-TDD/WCDMA/TD-SCDMA/EVDO/CDMA/GSM wireless communication module with LTE/WCDMA receive diversity. Engineered to meet the demanding requirements in automotive applications and other harsh operating conditions, it offers a premium solution for high performance automotive and intelligent transportation system (ITS) applications, such as fleet management, onboard vehicle telematics, in-car entertainment systems, emergency calling, and roadside assistance. It provides data connectivity on LTE-FDD, LTE-TDD, DC-HSDPA, HSPA+, HSDPA, HSUPA, WCDMA, TD-SCDMA, EVDO, CDMA, EDGE and GPRS networks. Also it can provide GNSS and voice functionality to meet customers' specific application demands.

AG35 contains five variants: AG35-CE, AG35-E, AG35-NA, AG35-LA and AG35-J. Customers can choose a dedicated type based on the region or operator. The following table shows the frequency bands of AG35 series modules.

Table 1: Frequency Bands of AG35 Series Modules

Network Type	AG35-CE	AG35-E	AG35-NA	AG35-LA	AG35-J
LTE-FDD (with Rx-diversity)	B1/B3/ B5/B8	B1/B3/B5/ B7/B8/B20/ B28	B2/B4/B5/ B7/B12/B13/ B17	B1/B2/B3/ B4/B5/B7/ B8/B28	B1/B3/B5/B8/ B9/B19/B21/ B28
LTE-TDD (with Rx-diversity)	B34/B38/ B39/B40/ B41	B38/B40	N/A	N/A	B41
WCDMA (with Rx-diversity)	B1/B8	B1/B5/B8	B2/B4/B5	B1/B2/B3/ B4/B5/B8	B1/B3/B5/ B6/B8/B19
TD-SCDMA	B34/B39	N/A	N/A	N/A	N/A
EVDO/CDMA	BC0 ¹⁾	N/A	N/A	N/A	N/A
GSM	900/1800MHz	900/1800MHz	850/1900MHz	850/900/ 1800/1900MHz	N/A

GNSS	GPS, GLONASS, BeiDou/ Compass, Galileo, QZSS	GPS, GLONASS, BeiDou/ Compass, Galileo, QZSS	GPS, GLONASS, BeiDou/ Compass, Galileo, QZSS	GPS, GLONASS, BeiDou/ Compass, Galileo, QZSS,SBAS	GPS, GLONASS, BeiDou/ Compass, Galileo, QZSS
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AG35 is an SMD type module which can be embedded in applications through its 299-pin LGA pads. This, coupled with its compact profile of 33.0mm × 37.5mm × 3.0mm, makes AG35 a ruggedized module for the most demanding applications and environments.

NOTES

- 1) EVDO/CDMA BC0 for AG35-CE is optional.
- “*” means under development.

2.2. Key Features

The following table describes the detailed features of AG35 module.

Table 2: AG35 Key Features

Feature	Details
Power Supply	Supply voltage: 3.3V~4.3V Typical supply voltage: 3.8V
Transmitting Power	Class 4 (33dBm±2dB) for GSM850 Class 4 (33dBm±2dB) for EGSM900 Class 1 (30dBm±2dB) for DCS1800 Class 1 (30dBm±2dB) for PCS1900 Class E2 (27dBm±3dB) for GSM850 8-PSK Class E2 (27dBm±3dB) for EGSM900 8-PSK Class E2 (26dBm±3dB) for DCS1800 8-PSK Class E2 (26dBm±3dB) for PCS1900 8-PSK Class 3 (24dBm+2/-1dB) for EVDO/CDMA BC0 Class 3 (24dBm+1/-3dB) for WCDMA bands Class 2 (24dBm+1/-3dB) for TD-SCDMA bands Class 3 (23dBm±2dB) for LTE-FDD bands Class 3 (23dBm±2dB) for LTE-TDD bands
LTE Features	Support up to non-CA Cat 4 FDD and TDD Support 1.4 to 20MHz RF bandwidth

	<p>Support Multiuser MIMO in DL direction</p> <ul style="list-style-type: none"> ● FDD: Max 150Mbps (DL)/50Mbps (UL) ● TDD: Max 130Mbps (DL)/30Mbps (UL)
WCDMA Features	<p>Support 3GPP R8 DC-HSDPA, HSPA+, HSDPA, HSUPA, WCDMA Support QPSK, 16-QAM and 64-QAM modulation</p> <ul style="list-style-type: none"> ● DC-HSDPA: Max 42Mbps (DL) ● HSUPA: Max 5.76Mbps (UL) ● WCDMA: Max 384Kbps (DL)/384Kbps (UL)
TD-SCDMA Features	<p>Support CCSA Release 3 TD-SCDMA</p> <ul style="list-style-type: none"> ● Max 4.2Mbps (DL)/2.2Mbps (UL)
CDMA2000 Features	<p>Support 3GPP2 CDMA2000 1X Advanced, CDMA2000 1x EV-DO Rev.A</p> <ul style="list-style-type: none"> ● EVDO: Max 3.1Mbps (DL)/1.8Mbps (UL) ● 1X Advanced: Max 307.2Kbps (DL)/307.2Kbps (UL)
GSM Features	<p>GPRS: Support GPRS multi-slot class 33 (33 by default) Coding scheme: CS-1, CS-2, CS-3 and CS-4 Max 107Kbps (DL)/85.6Kbps (UL)</p> <p>EDGE: Support EDGE multi-slot class 33 (33 by default) Support GMSK and 8-PSK for different MCS (Modulation and Coding Scheme) Downlink coding schemes: CS 1-4 and MCS 1-9 Uplink coding schemes: CS 1-4 and MCS 1-9 Max 296Kbps (DL)/236.8Kbps (UL)</p>
Internet Protocol Features	<p>Support TCP/UDP/PPP/FTP/HTTP/NTP/PING/QMI/HTTPS/SMTP/MMS/FTPS/SMTPS/SSL protocols</p> <p>Support the protocols PAP (Password Authentication Protocol) and CHAP (Challenge Handshake Authentication Protocol) usually used for PPP connections</p>
SMS	<p>Text and PDU mode Point to point MO and MT SMS cell broadcast SMS storage: ME by default</p>
(U)SIM Interface	<p>Support USIM/SIM card: 1.8V, 3.0V</p>
Audio Features (Optional)	<p>Built-in audio codec with two microphone inputs and one stereo output or two mono outputs GSM: HR/FR/EFR/AMR/AMR-WB WCDMA: AMR/AMR-WB LTE: AMR/AMR-WB Support echo cancellation and noise suppression</p>
PCM Interface	<p>Used for audio function with external codec Support 16-bit linear data format Support long frame synchronization and short frame synchronization</p>

	Support master and slave modes, but must be the master in long frame synchronization
SGMII Interface (Optional)	Support 10/100/1000Mbps
WLAN Interface	Compliant with 802.11, 4-bit, 1.8V WLAN interface
SDIO Interfaces	SDIO1: Compliant with SD 3.0 protocol Used for WLAN function SDIO2: Compliant with SD 3.0 protocol
USB Interface	Compliant with USB 2.0 specification (slave only), and the data transfer rate can reach up to 480Mbps Used for AT command communication, data transmission, GNSS NMEA output, software debugging and firmware upgrade Support USB serial driver under Windows 7/8/8.1/10, Windows CE 5.0/6.0/7.0*, Linux 2.6/3.x/4.1~4.14, Android 4.x/5.x/6.x/7.x/8.x/9.x
HSIC Interface*	High-speed inter-chip USB electrical specification compliant
UART Interfaces	Main UART: Used for AT command communication and data transmission Baud rate reach up to 921600bps, 115200bps by default Support RTS and CTS hardware flow control UART2: Used for BT function* Baud rate reach up to 921600bps, 115200bps by default Support RTS and CTS hardware flow control Debug UART: Used for Linux console and log output 115200bps baud rate
Rx-diversity	Support LTE/WCDMA Rx-diversity
GNSS Features	Gen8C-Lite of Qualcomm Protocol: NMEA 0183 Data update rate: 1Hz by default and maximally up to 10Hz
AT Commands	3GPP TS 27.007/3GPP TS 27.005 AT commands and Quectel enhanced AT commands
Network Indication	Two pins including NET_MODE and NET_STATUS to indicate network connectivity status
Antenna Interface	Including main antenna interface (ANT_MAIN), Rx-diversity antenna interface (ANT_DIV) and GNSS antenna interface (ANT_GNSS)
Physical Characteristics	Size: (33.0±0.15)mm × (37.5±0.15)mm × (3.0±0.2)mm Weight: Approx. 8.1g
Temperature Range	Operation temperature range: -35°C ~ +75°C ¹⁾

	Extended temperature range: -40°C ~ +85°C ²⁾ eCall temperature range: -40°C ~ +90°C ³⁾ Storage temperature range: -40°C ~ +95°C
Firmware Upgrade	USB interface DFOTA
RoHS	All hardware components are fully compliant with EU RoHS directive

NOTES

- 1) Within operation temperature range, the module is 3GPP compliant, and emergency call can be dialed out with a maximum power and data rate.
- 2) Within extended temperature range, the module remains fully functional and retains the ability to establish and maintain a voice, SMS, data transmission, emergency call, etc. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like P_{out} might reduce in their value and exceed the specified tolerances. When the temperature returns to normal operation temperature levels, the module will meet 3GPP specifications again.
- 3) Within eCall temperature range, the emergency call function must be functional until the module is broken. When the ambient temperature is between 75°C and 90°C and the module temperature has reached the threshold value, the module will trigger protective measures (such as reduce power, decrease throughput, unregister the device, etc.) to ensure the full function of emergency call.
4. “*” means under development.

2.3. Functional Diagram

The following figure shows a block diagram of AG35 and illustrates the major functional parts.

- Power management
- Baseband
- DDR+NAND flash
- Radio frequency
- Peripheral interface

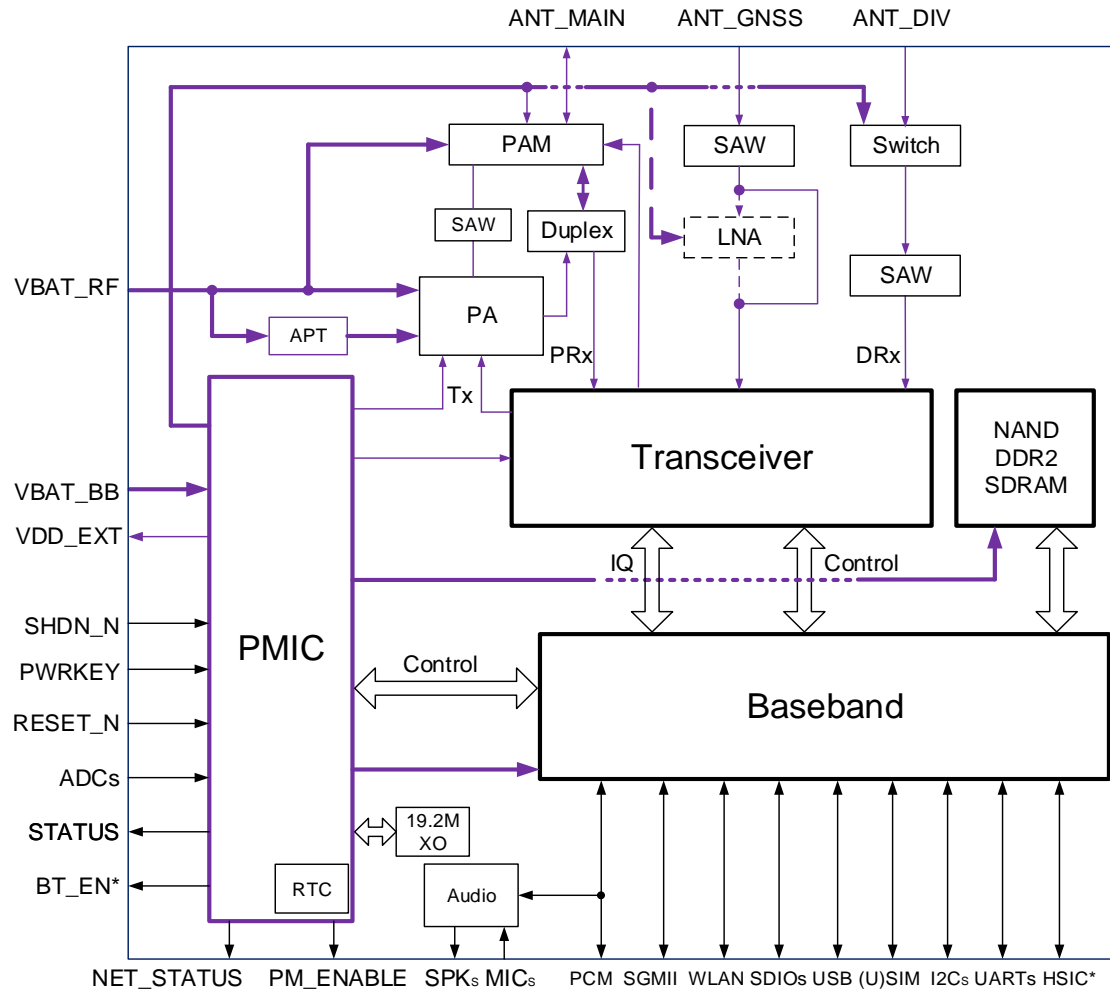


Figure 1: Functional Diagram

NOTE

“*” means under development.

2.4. Evaluation Board

In order to help customers develop applications with AG35 conveniently, Quectel supplies the evaluation board (EVB), USB data cable, earphone, antenna and other peripherals to control or test the module. For more details, please refer to **document [3]**.

3 Application Interfaces

3.1. General Description

AG35 is equipped with 299-pin LGA pads that can be connected to cellular application platform. Sub-interfaces included in these pads are described in detail in the following sub-chapters:

- Power supply
- (U)SIM interface
- USB interface
- UART interfaces
- Audio interface (optional)
- PCM and I2C interfaces
- SDIO interfaces
- SGMII interface (optional)
- Wireless connectivity interfaces
- ADC interfaces
- Status indication interfaces
- USB_BOOT interface
- HSIC interface*

NOTE

“*” means under development.

3.2. Pin Assignment

The following figure shows the pin assignment of AG35 module.

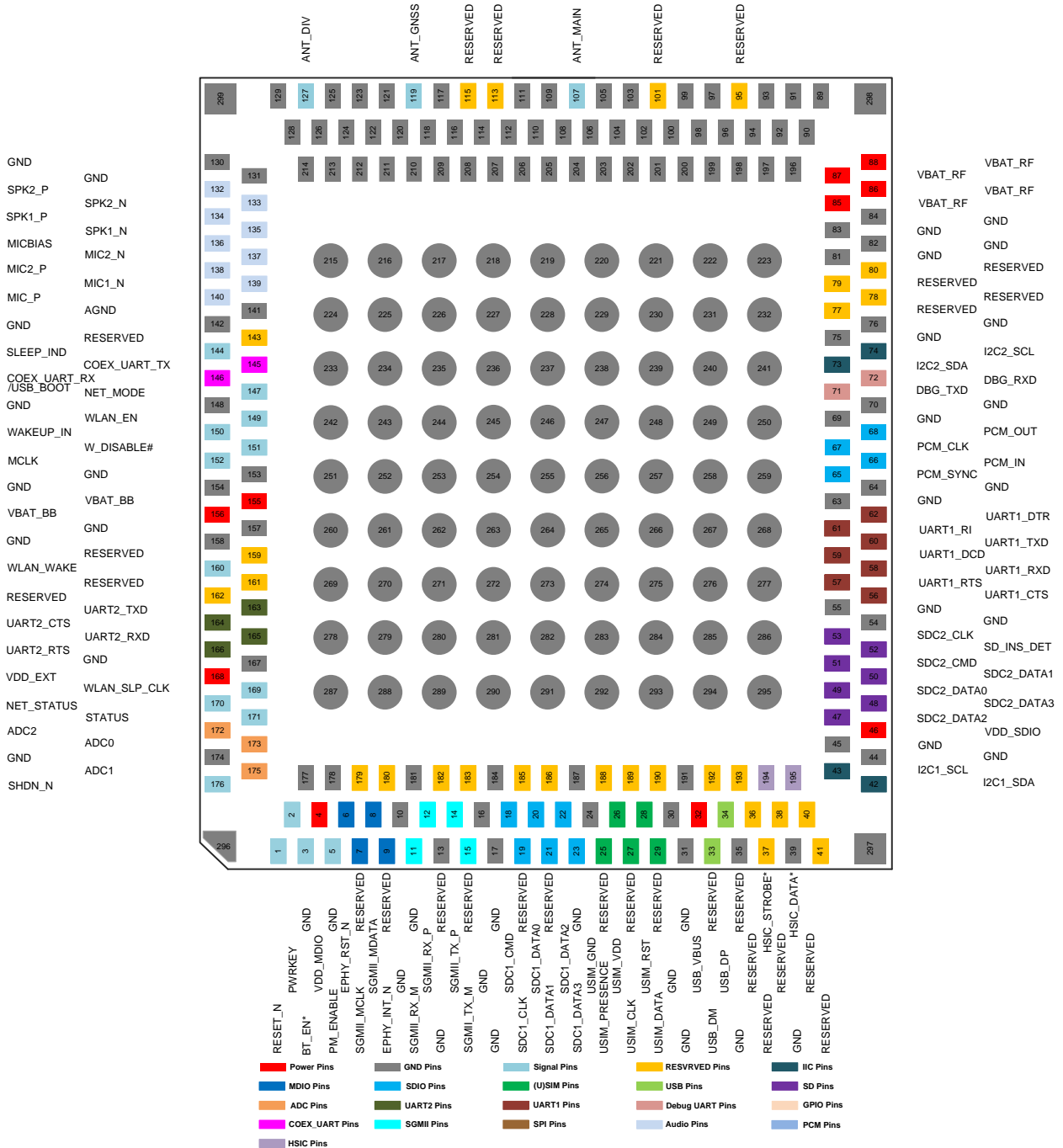


Figure 2: Pin Assignment (Top View)

NOTES

1. Pins 59, 65, 67, 144~147 and 149 cannot be pulled up before power-up.
2. PWRKEY (pin 2) output voltage is 0.8V because of the diode drop in the Qualcomm chipset.
3. GND pins 215~299 should be connected to ground in the design.
4. Keep all RESERVED pins and unused pins unconnected.
5. “*” means under development.

3.3. Pin Description

The following tables show the pin definition and description of AG35.

Table 3: I/O Parameters Definition

Type	Description
AI	Analog input
AO	Analog output
DI	Digital input
DO	Digital output
IO	Bidirectional
PI	Power input
PO	Power output

Table 4: Pin Description

Power Supply					
Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
VBAT_BB	155, 156	PI	Power supply for module's baseband part	Vmax=4.3V Vmin=3.3V Vnorm=3.8V	It must be able to provide sufficient current up to 0.8A.
VBAT_RF	85, 86, 87, 88	PI	Power supply for module's RF part	Vmax=4.3V Vmin=3.3V Vnorm=3.8V	It must be able to provide sufficient current up to 1.8A in a

					transmitting burst.
VDD_EXT	168	PO	Provide 1.8V for external circuit	Vnorm=1.8V Iomax=50mA	Power supply for external GPIO's pull up circuits.
	10, 13, 16, 17, 30, 31, 35, 39, 44, 45, 54, 55, 63, 64, 69, 70, 75, 76, 81~84, 89~94, 96~100, 102~106, 108~112,				
GND	114, 116~118, 120~126, 128~131, 142, 148, 153, 154, 157, 158, 167, 174, 177, 178, 181, 184, 187, 191, 196~299		Ground		

Turn on/off

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
PWRKEY	2	DI	Turn on/off the module	V _{IH} max=2.1V V _{IH} min=1.3V V _{IL} max=0.5V	The output voltage is 0.8V because of the diode drop in the Qualcomm chipset.
RESET_N	1	DI	Reset the module	V _{IH} max=2.1V V _{IH} min=1.3V V _{IL} max=0.5V	Internally pulled up to 1.8V. Active low.
SHDN_N	176	DI	Emergency shutdown for the module	V _{IH} max=2.1V V _{IH} min=1.3V V _{IL} max=0.5V	

Status Indication

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
STATUS	171	OD	Indicate the module's operation status	The drive current should be less than 0.15mA.	Require external pull-up. If unused, keep it open.
NET_MODE	147	DO	Indicate the module's network registration status	V _{OH} min=1.35V V _{OL} max=0.45V	1.8V power domain. If unused, keep it open.
NET_STATUS	170	DO	Indicate the module's network activity status	V _{OH} min=1.35V V _{OL} max=0.45V	1.8V power domain. If unused, keep it open.

USB Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
USB_VBUS	32	PI	USB connection detection	V _{max} =5.25V V _{min} =3.0V V _{norm} =5.0V	Maximum Current: 1mA
USB_DM	33	IO	USB differential data bus (-)	Compliant with USB 2.0 standard specification.	Require differential impedance of 90Ω.
USB_DP	34	IO	USB differential data bus (+)	Compliant with USB 2.0 standard specification.	Require differential impedance of 90Ω.

HSIC Interface*

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
HSIC_STROBE*	194	IO	High speed inter chip interface - strobe	V _{IL} max=0.4V V _{IH} min=0.8V V _{OL} max=0.3V	1.2V power domain. If unused, keep them open.
HSIC_DATA*	195	IO	High speed inter chip interface - data	V _{OH} min=0.9V	

(U)SIM Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
USIM_GND	24		Specified ground for (U)SIM card		Connect to ground of (U)SIM card connector.
USIM_PRESENCE	25	DI	(U)SIM card insertion detection	V _{IL} min=-0.3V V _{IL} max=0.6V V _{IH} min=1.2V V _{IH} max=2.0V	1.8V power domain. If unused, keep it open.

USIM_VDD	26	PO	Power supply for (U)SIM card	For 1.8V (U)SIM: $V_{max}=1.9V$ $V_{min}=1.7V$ For 3.0V (U)SIM: $V_{max}=3.05V$ $V_{min}=2.7V$ $I_{Omax}=50mA$	Either 1.8V or 3V is supported by the module automatically.
USIM_CLK	27	DO	Clock signal of (U)SIM card	For 1.8V USIM: $V_{OLmax}=0.45V$ $V_{OHmin}=1.35V$ For 3.0V USIM: $V_{OLmax}=0.45V$ $V_{OHmin}=2.55V$	
USIM_RST	28	DO	Reset signal of (U)SIM card	For 1.8V USIM: $V_{OLmax}=0.45V$ $V_{OHmin}=1.35V$ For 3.0V USIM: $V_{OLmax}=0.45V$ $V_{OHmin}=2.55V$	
USIM_DATA	29	IO	Data signal of (U)SIM card	For 1.8V USIM: $V_{ILmax}=0.6V$ $V_{IHmin}=1.2V$ $V_{OLmax}=0.45V$ $V_{OHmin}=1.35V$ For 3.0V USIM: $V_{ILmax}=1.0V$ $V_{IHmin}=1.95V$ $V_{OLmax}=0.45V$ $V_{OHmin}=2.55V$	

Main UART Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
UART1_CTS	56	DO	DTE clear to send	$V_{OLmax}=0.45V$ $V_{OHmin}=1.35V$	1.8V power domain. If unused, keep it open.
UART1_RTS	57	DI	DTE request to send	$V_{ILmin}=-0.3V$ $V_{ILmax}=0.6V$ $V_{IHmin}=1.2V$ $V_{IHmax}=2.0V$	1.8V power domain. If unused, keep it open.

UART1_RXD	58	DI	Receive data	$V_{ILmin}=-0.3V$ $V_{ILmax}=0.6V$ $V_{IHmin}=1.2V$ $V_{IHmax}=2.0V$	1.8V power domain. If unused, keep it open.
UART1_DCD	59	DO	Data carrier detection	$V_{OLmax}=0.45V$ $V_{OHmin}=1.35V$	1.8V power domain. If unused, keep it open.
UART1_TXD	60	DO	Transmit data	$V_{OLmax}=0.45V$ $V_{OHmin}=1.35V$	1.8V power domain. If unused, keep it open.
UART1_RI	61	DO	Ring indicator	$V_{OLmax}=0.45V$ $V_{OHmin}=1.35V$	1.8V power domain. If unused, keep it open.
UART1_DTR	62	DI	Data terminal ready. Sleep mode control	$V_{ILmin}=-0.3V$ $V_{ILmax}=0.6V$ $V_{IHmin}=1.2V$ $V_{IHmax}=2.0V$	1.8V power domain. Pulled up by default. Low level wakes up the module. If unused, keep it open.

UART2 Interface (for BT Function*)

UART2_TXD	163	DO	Transmit data	$V_{OLmax}=0.45V$ $V_{OHmin}=1.35V$	1.8V power domain. If unused, keep it open.
UART2_CTS	164	DO	DTE clear to send	$V_{OLmax}=0.45V$ $V_{OHmin}=1.35V$	1.8V power domain. If unused, keep it open.
UART2_RXD	165	DI	Receive data	$V_{ILmin}=-0.3V$ $V_{ILmax}=0.6V$ $V_{IHmin}=1.2V$ $V_{IHmax}=2.0V$	1.8V power domain. If unused, keep it open.
UART2_RTS	166	DI	DTE request to send	$V_{ILmin}=-0.3V$ $V_{ILmax}=0.6V$ $V_{IHmin}=1.2V$ $V_{IHmax}=2.0V$	1.8V power domain. If unused, keep it open.

Debug UART Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
DBG_TXD	71	DO	Transmit data	$V_{OLmax}=0.45V$ $V_{OHmin}=1.35V$	1.8V power domain. If unused, keep it open.
DBG_RXD	72	DI	Receive data	$V_{ILmin}=-0.3V$ $V_{ILmax}=0.6V$	1.8V power domain. If unused, keep it

$V_{IHmin}=1.2V$
 $V_{IHmax}=2.0V$

open.

ADC Interfaces

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
ADC2	172	AI	General purpose analog to digital converter interface	Voltage Range: 0.1V to 1.7V	If unused, keep it open.
ADC0	173	AI	General purpose analog to digital converter interface	Voltage Range: 0.3V to VBAT_BB	If unused, keep it open.
ADC1	175	AI	General purpose analog to digital converter interface	Voltage Range: 0.3V to VBAT_BB	If unused, keep it open.

Audio Interface (Optional)

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
SPK2_P	132	AO	Earphone analog output 2 (+)		If unused, keep it open.
SPK2_N	133	AO	Earphone analog output 2 (-)		If unused, keep it open.
SPK1_P	134	AO	Earphone analog output 1 (+)		If unused, keep it open.
SPK1_N	135	AO	Earphone analog output 1 (-)		If unused, keep it open.
MICBIAS	136	AO	Bias voltage output for microphone	$V_{max}=1.55V$ $V_{min}=1.5V$ $V_{norm}=1.525V$	If unused, keep it open.
MIC2_N	137	AI	Microphone analog input 2 (-)		If unused, keep it open.
MIC2_P	138	AI	Microphone analog input 2 (+)		If unused, keep it open.
MIC1_N	139	AI	Microphone analog input 1 (-)		If unused, keep it open.
MIC1_P	140	AI	Microphone analog input 1 (+)		If unused, keep it open.
AGND	141		Analog ground		If unused, keep it open.

PCM Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
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PCM_SYNC	65	IO	PCM data frame synchronization signal	$V_{OLmax}=0.45V$ $V_{OHmin}=1.35V$ $V_{ILmin}=-0.3V$ $V_{ILmax}=0.6V$ $V_{IHmin}=1.2V$ $V_{IHmax}=2.0V$	1.8V power domain. In master mode, it is an output signal. In slave mode, it is an input signal. If unused, keep it open.
PCM_IN	66	DI	PCM data input	$V_{ILmin}=-0.3V$ $V_{ILmax}=0.6V$ $V_{IHmin}=1.2V$ $V_{IHmax}=2.0V$	1.8V power domain. If unused, keep it open.
PCM_CLK	67	IO	PCM clock	$V_{OLmax}=0.45V$ $V_{OHmin}=1.35V$ $V_{ILmin}=-0.3V$ $V_{ILmax}=0.6V$ $V_{IHmin}=1.2V$ $V_{IHmax}=2.0V$	1.8V power domain. In master mode, it is an output signal. In slave mode, it is an input signal. If unused, keep it open.
PCM_OUT	68	DO	PCM data output	$V_{OLmax}=0.45V$ $V_{OHmin}=1.35V$	1.8V power domain. If unused, keep it open.
MCLK	152	DO	Output 12.288MHz	$V_{OLmax}=0.45V$ $V_{OHmin}=1.35V$	1.8V power domain. If unused, keep it open.

I2C1 Interface (for Codec Configuration by Default)

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
I2C1_SDA	42	IO	I2C1 serial data. Used for external codec.	$V_{OLmax}=0.45V$ $V_{OHmin}=1.35V$ $V_{ILmin}=-0.3V$ $V_{ILmax}=0.6V$ $V_{IHmin}=1.2V$ $V_{IHmax}=2.0V$	External pull-up resistor is required. 1.8V only. If unused, keep it open.
I2C1_SCL	43	DO	I2C1 serial clock. Used for external codec.	$V_{OLmax}=0.45V$ $V_{OHmin}=1.35V$	External pull-up resistor is required. 1.8V only. If unused, keep it open.

I2C2 Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
I2C2_SDA	73	IO	I2C2 serial data	$V_{OLmax}=0.45V$ $V_{OHmin}=1.35V$	External pull-up resistor is required.

				$V_{ILmin}=-0.3V$ $V_{ILmax}=0.6V$ $V_{IHmin}=1.2V$ $V_{IHmax}=2.0V$	1.8V only. If unused, keep it open.
I2C2_SCL	74	DO	I2C2 serial data	$V_{OLmax}=0.45V$ $V_{OHmin}=1.35V$	External pull-up resistor is required. 1.8V only. If unused, keep it open.

SDIO2 Interface (for SD Card)

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
VDD_SDIO	46	PO	SDIO pull up power source for SD card	$I_{Omax}=50mA$	1.8V/2.85V configurable power output. If unused, keep it open.
SDC2_DATA2	47	IO	SDIO data signal (bit 2)	For 1.8V signaling: $V_{OLmax}=0.45V$ $V_{OHmin}=1.4V$ $V_{ILmin}=-0.3V$ $V_{ILmax}=0.58V$ $V_{IHmin}=1.27V$ $V_{IHmax}=2.0V$	SDIO signal level can be selected according to the one supported by SD card. Please refer to SD 3.0 protocol for more details. If unused, keep it open.
SDC2_DATA3	48	IO	SDIO data signal (bit 3)		
SDC2_DATA0	49	IO	SDIO data signal (bit 0)		
SDC2_DATA1	50	IO	SDIO data signal (bit 1)		
SDC2_CMD	51	IO	SDIO command signal	For 3.0V signaling: $V_{OLmax}=0.38V$ $V_{OHmin}=2.01V$ $V_{ILmin}=-0.3V$ $V_{ILmax}=0.76V$ $V_{IHmin}=1.72V$ $V_{IHmax}=3.34V$	
SD_INS_DET	52	DI	Insertion detection for SD card	$V_{OLmax}=0.45V$ $V_{OHmin}=1.35V$ $V_{ILmin}=-0.3V$ $V_{ILmax}=0.6V$ $V_{IHmin}=1.2V$ $V_{IHmax}=2.0V$	1.8V power domain. If unused, keep it open.
SDC2_CLK	53	DO	SDIO bus clock	For 1.8V Signaling: $V_{OLmax}=0.45V$ $V_{OHmin}=1.4V$ For 3.0V Signaling: $V_{OLmax}=0.38V$	SDIO signal level can be selected according to the one supported by SD card. Please refer to SD 3.0 protocol for more

$V_{OHmin}=2.01V$

details.
If unused, keep it open.

MDIO Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
VDD_MDIO	4	PO	SGMII_MDATA pull-up power source		1.8V/2.85V configurable power output. If unused, keep it open.
EPHY_RST_N	6	DO	Ethernet PHY reset	1.8V: $V_{OLmax}=0.45V$ $V_{OHmin}=1.35V$ 2.85V: $V_{OLmax}=0.35V$ $V_{OHmin}=2.14V$	1.8V/2.85V power domain. If unused, keep it open.
SGMII_MCLK	7	DO	SGMII MDIO (Management Data Input/Output) clock	1.8V: $V_{OLmax}=0.45V$ $V_{OHmin}=1.35V$ 2.85V: $V_{OLmax}=0.35V$ $V_{OHmin}=2.14V$	1.8V/2.85V power domain. If unused, keep it open.
SGMII_MDATA	8	IO	SGMII MDIO (Management Data Input/Output) data	1.8V: $V_{ILmax}=0.58V$ $V_{IHmin}=1.27V$ $V_{OLmax}=0.45V$ $V_{OHmin}=1.4V$ 2.85V: $V_{ILmax}=1.0V$ $V_{IHmin}=1.95V$ $V_{OLmax}=0.45V$ $V_{OHmin}=2.55V$	1.8V/2.85V power domain. External 1.5K resistor pulled up to VDD_MDIO is required. If unused, keep it open.
EPHY_INT_N	9	DI	Ethernet PHY interrupt	$V_{ILmin}=-0.3V$ $V_{ILmax}=0.6V$ $V_{IHmin}=1.2V$ $V_{IHmax}=2.0V$	1.8V power domain. If unused, keep it open.

SGMII Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
SGMII_RX_M	11	AI	SGMII receiving (-)		If unused, keep it open.
SGMII_RX_P	12	AI	SGMII receiving (+)		If unused, keep it

					open.
SGMII_TX_P	14	AO	SGMII transmission (+)		If unused, keep it open.
SGMII_TX_M	15	AO	SGMII transmission (-)		If unused, keep it open.
WLAN Interface (SDIO1 and WLAN Control Interfaces)					
Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
SDC1_CMD	18	IO	WLAN SDIO command signal	$V_{OLmax}=0.45V$ $V_{OHmin}=1.35V$	1.8V power domain. If unused, keep it open.
SDC1_CLK	19	DO	WLAN SDIO clock signal	$V_{OLmax}=0.45V$ $V_{OHmin}=1.35V$	1.8V power domain. If unused, keep it open.
SDC1_DATA0	20	IO	WLAN SDIO data bus (bit 0)	$V_{OLmax}=0.45V$ $V_{OHmin}=1.35V$ $V_{ILmin}=-0.3V$ $V_{ILmax}=0.6V$ $V_{IHmin}=1.2V$ $V_{IHmax}=2.0V$	1.8V power domain. If unused, keep it open.
SDC1_DATA1	21	IO	WLAN SDIO data bus (bit 1)	$V_{OLmax}=0.45V$ $V_{OHmin}=1.35V$ $V_{ILmin}=-0.3V$ $V_{ILmax}=0.6V$ $V_{IHmin}=1.2V$ $V_{IHmax}=2.0V$	1.8V power domain. If unused, keep it open.
SDC1_DATA2	22	IO	WLAN SDIO data bus (bit 2)	$V_{OLmax}=0.45V$ $V_{OHmin}=1.35V$ $V_{ILmin}=-0.3V$ $V_{ILmax}=0.6V$ $V_{IHmin}=1.2V$ $V_{IHmax}=2.0V$	1.8V power domain. If unused, keep it open.
SDC1_DATA3	23	IO	WLAN SDIO data bus (bit 3)	$V_{OLmax}=0.45V$ $V_{OHmin}=1.35V$ $V_{ILmin}=-0.3V$ $V_{ILmax}=0.6V$ $V_{IHmin}=1.2V$ $V_{IHmax}=2.0V$	1.8V power domain. If unused, keep it open.
PM_ENABLE	5	DO	External power enable control	$V_{OLmax}=0.45V$ $V_{OHmin}=1.35V$	1.8V power domain. If unused, keep it open.

WLAN_EN	149	DO	WLAN function enable control via Wi-Fi module	V _{OL} max=0.45V V _{OH} min=1.35V	1.8V power domain. If unused, keep it open.
WLAN_WAKE	160	DI	Wake up the module via WLAN	V _{IL} min=-0.3V V _{IL} max=0.6V V _{IH} min=1.2V V _{IH} max=2.0V	1.8V power domain. If unused, keep it open.
WLAN_SLP_CLK	169	DO	WLAN sleep clock	V _{OL} max=0.45V V _{OH} min=1.35V	1.8V power domain. If unused, keep it open.
COEX_UART_RX/USB_BOOT	146	DI	LTE/WLAN&BT coexistence signal./ Force the module to enter into emergency download mode.	V _{IL} min=-0.3V V _{IL} max=0.6V V _{IH} min=1.2V V _{IH} max=2.0V	If unused, keep it open.
COEX_UART_TX	145	DO	LTE/WLAN&BT coexistence signal	V _{OL} max=0.45V V _{OH} min=1.35V	If unused, keep it open.

RF Interfaces

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
ANT_MAIN	107	IO	Main antenna interface		50Ω impedance.
ANT_GNSS	119	AI	GNSS antenna interface		50Ω impedance. If unused, keep it open.
ANT_DIV	127	AI	Receive diversity antenna interface		50Ω impedance. If unused, keep it open.

Other Interfaces

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
BT_EN*	3	DO	Bluetooth enable control	V _{OL} max=0.45V V _{OH} min=1.35V	
SLEEP_IND	144	DO	Sleep indication	V _{OL} max=0.45V V _{OH} min=1.35V	
WAKEUP_IN	150	DI	Sleep mode control	V _{IL} min=-0.3V V _{IL} max=0.6V V _{IH} min=1.2V V _{IH} max=2.0V	1.8V power domain. Pulled up by default. Low level wakes up the module. If unused, keep it open.

W_DISABLE#	151	DI	Airplane mode control	$V_{ILmin}=-0.3V$ $V_{ILmax}=0.6V$ $V_{IHmin}=1.2V$ $V_{IHmax}=2.0V$	1.8V power domain. Pulled up by default. In low voltage level, module can enter into airplane mode. If unused, keep it open.
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RESERVED Pins

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
RESERVED	36~38, 40, 41, 95, 101, 113, 115, 77~80, 143, 159 161, 162, 179, 180, 182, 183, 185, 186, 188~190, 192~193		Reserved		Keep these pins unconnected.

NOTES

1. “*” means under development.
2. Keep all RESERVED pins and unused pins unconnected.

3.4. Operating Modes

The table below briefly summarizes the various operating modes referred in the following chapters.

Table 5: Overview of Operating Modes

Mode	Details	
Normal Operation	Idle	Software is active. The module has registered on the network, and it is ready to send and receive data.
	Talk/Data	Network connection is ongoing. In this mode, the power consumption is decided by network setting and data transfer rate.
Minimum Functionality	AT+CFUN=0 can set the module to a minimum functionality mode without removing the power supply. In this case, both RF function and (U)SIM card will be invalid.	

Mode	
Airplane Mode	AT+CFUN=4 or W_DISABLE# pin can set the module to airplane mode. In this case, RF function will be invalid.
Sleep Mode	In this mode, the current consumption of the module will be reduced to the minimal level. During this mode, the module can still receive paging message, SMS, voice call and TCP/UDP data from the network normally.
Power down Mode	In this mode, the power management unit shuts down the power supply. Software is not active. The serial interfaces are not accessible. Operating voltage (connected to VBAT_RF and VBAT_BB) remains applied.

3.5. Power Saving

3.5.1. Sleep Mode

AG35 is able to reduce its current consumption to a minimum value during the sleep mode. This chapter mainly introduces some ways to enter into or exit from sleep mode. The diagram below illustrates the current consumption of AG35 during sleep mode.

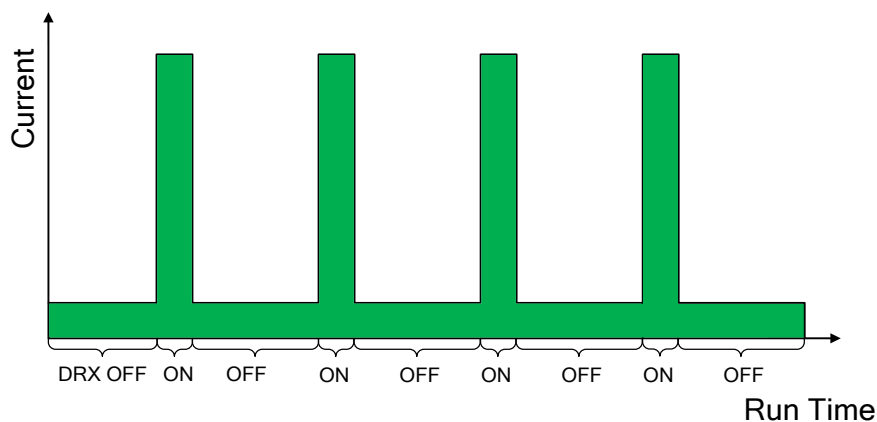


Figure 3: Sleep Mode Current Consumption Diagram

NOTE

DRX cycle index values are broadcasted by the wireless network.

3.5.1.1. UART Application

If the host communicates with module via UART interface, the following preconditions can let the module enter into sleep mode.

- Execute **AT+QSClk=1** command to enable sleep mode.
- Drive DTR to high level.

The following figure shows the connection between the module and the host.

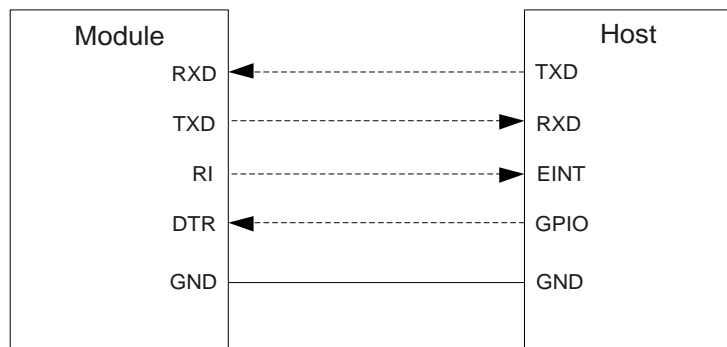


Figure 4: Sleep Mode Application via UART

- Driving the host DTR to low level will wake up the module.
- When AG35 has URC to report, RI signal will wake up the host. Please refer to Chapter 3.20 for details about RI behavior.

3.5.1.2. USB Application with USB Remote Wakeup Function

If the host supports USB suspend/resume and remote wakeup functions, the following three preconditions must be met to let the module enter into sleep mode.

- Execute **AT+QSClk=1** command to enable sleep mode.
- Ensure the DTR is held in high level or keep it open.
- The host's USB bus, which is connected with the module's USB interface, enters into suspended state.

The following figure shows the connection between the module and the host.

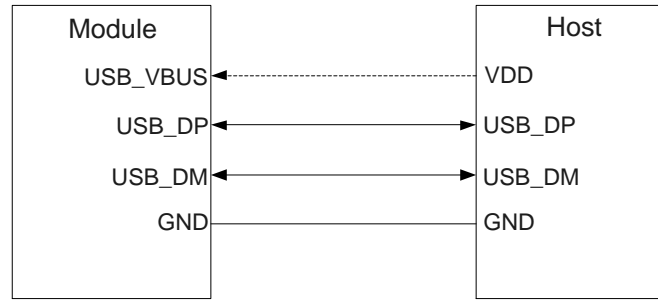


Figure 5: Sleep Mode Application with USB Remote Wakeup

- Sending data to AG35 through USB will wake up the module.
- When AG35 has URC to report, the module will send remote wake-up signals via USB bus so as to wake up the host.

3.5.1.3. USB Application with USB Suspend/Resume and RI Functions

If the host supports USB suspend/resume, but does not support remote wake-up function, the RI signal is needed to wake up the host.

There are three preconditions to let the module enter into sleep mode.

- Execute **AT+QSClk=1** command to enable sleep mode.
- Ensure the DTR is held in high level or keep it open.
- The host's USB bus, which is connected with the module's USB interface, enters into suspended state.

The following figure shows the connection between the module and the host.

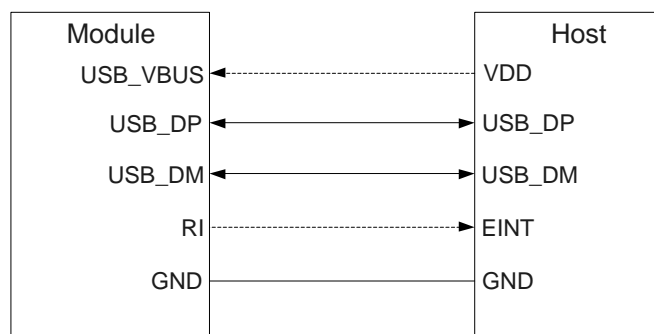


Figure 6: Sleep Mode Application with RI

- Sending data to AG35 through USB will wake up the module.
- When AG35 has URC to report, RI signal will wake up the host.

3.5.1.4. USB Application without USB Suspend Function

If the host does not support USB suspend function, USB_VBUS should be disconnected via an external control circuit to let the module enter into sleep mode.

- Execute **AT+QSClk=1** command to enable sleep mode.
- Ensure the DTR is held in high level or keep it open.
- Disconnect USB_VBUS.

The following figure shows the connection between the module and the host.

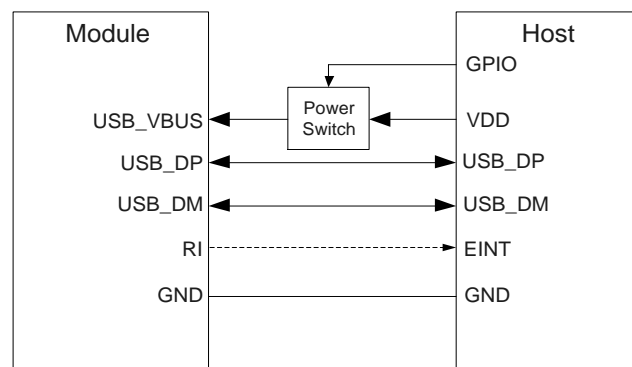


Figure 7: Sleep Mode Application without Suspend Function

Switching on the power switch to supply power to USB_VBUS will wake up the module.

NOTE

Please pay attention to the level match shown in dotted line between the module and the host. Refer to **document [1]** for more details about the module's power management application.

3.5.2. Airplane Mode

When the module enters into airplane mode, the RF function does not work, and all AT commands correlative with RF function will be inaccessible. This mode can be set via the following ways.

Hardware:

The W_DISABLE# pin is pulled up by default. Driving it to low level will let the module enter into airplane mode.

Software:

AT+CFUN command provides choices of the functionality level, through setting **<fun>** into 0, 1, or 4.

- **AT+CFUN=0**: Minimum functionality mode. Both (U)SIM and RF functions are disabled.
- **AT+CFUN=1**: Full functionality mode (by default).
- **AT+CFUN=4**: Airplane mode. RF function is disabled.

NOTES

1. Airplane mode control via W_DISABLE# is disabled in firmware by default. It can be enabled by **AT+QCFG="airplanecontrol"** command. Please refer to **document [2]** for more details.
2. The execution of **AT+CFUN** command will not affect GNSS function.

3.6. Power Supply

3.6.1. Power Supply Pins

AG35 provides six VBAT pins for connection with the external power supply. There are two separate voltage domains for VBAT.

- Four VBAT_RF pins for module's RF part
- Two VBAT_BB pins for module's baseband part

The following table shows the details of VBAT pins and ground pins.

Table 6: VBAT and GND Pins

Pin Name	Pin No.	Description	Min.	Typ.	Max.	Unit
VBAT_RF	85, 86, 87, 88	Power supply for module's RF part	3.3	3.8	4.3	V
VBAT_BB	155, 156	Power supply for module's baseband part	3.3	3.8	4.3	V
GND	10, 13, 16, 17, 30, 31, 35, 39, 44, 45, 54, 55, 63, 64, 69, 70, 75, 76, 81~84, 89~94, 96~100, 102~106, 108~112, 114, 116~118, 120~126, 128~131, 142, 148, 153, 154,	Ground	-	0	-	V

157, 158, 167, 174,
177, 178, 181, 184,
187, 191, 196~299

3.6.2. Decrease Voltage Drop

The power supply range of the module is from 3.3V to 4.3V. Please make sure the input voltage will never drop below 3.3V. The following figure shows the voltage drop during burst transmission in 2G network. The voltage drop will be less in 3G and 4G networks.

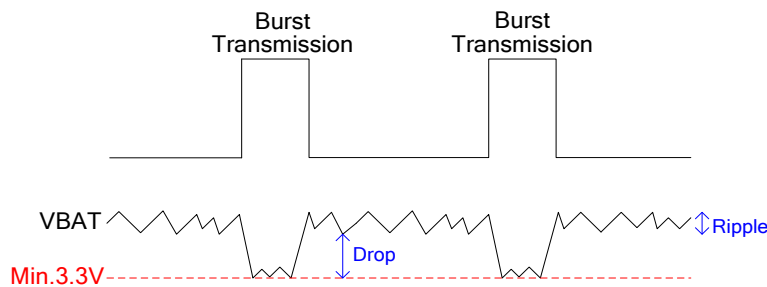


Figure 8: Power Supply Limits during Burst Transmission

To decrease voltage drop, a bypass capacitor of about 100μF with low ESR should be used, and a multi-layer ceramic chip capacitor (MLCC) array should also be reserved due to its low ESR. It is recommended to use three ceramic capacitors (100nF, 33pF, 10pF) for composing the MLCC array, and place these capacitors close to VBAT pins. The main power supply from an external application has to be a single voltage source and can be expanded to two sub paths with star structure. The width of VBAT_BB trace should be no less than 1mm, and the width of VBAT_RF trace should be no less than 2mm. In principle, the longer the VBAT trace is, the wider it will be.

In addition, in order to get a stable power source, it is suggested to use a power TVS (e.g. WS4.5DPF-B, $V_{RWM}=4.5V$, $P_{pp}=450W$) and a zener diode with dissipation power more than 0.5W, and place them as close to the VBAT pins as possible. The following figure shows the star structure of the power supply.

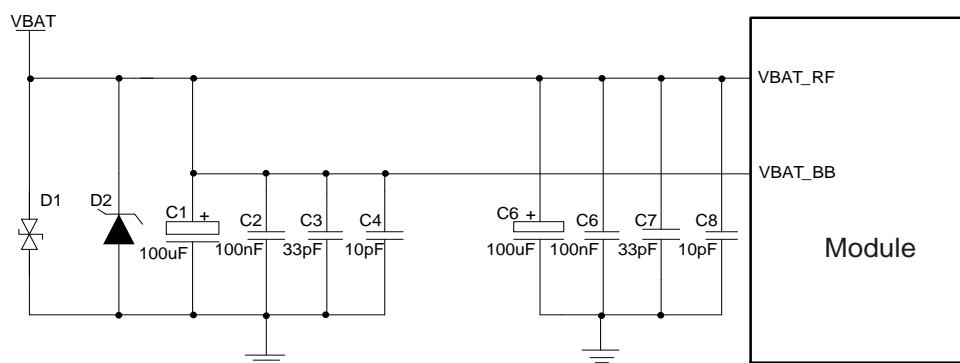


Figure 9: Star Structure of the Power Supply

3.6.3. Reference Design for Power Supply

Power design for the module is very important, as the performance of the module largely depends on the power source. The power supply of AG35 should be able to provide sufficient current up to 2A at least. If the voltage drop between the input and output is not too high, it is recommended to use an LDO to supply power for the module. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is preferred to be used as the power supply.

The following figure shows a reference design for +12V/+24V input power source. The designed output for the power supply is about 3.8V and the maximum rated current is 5A.

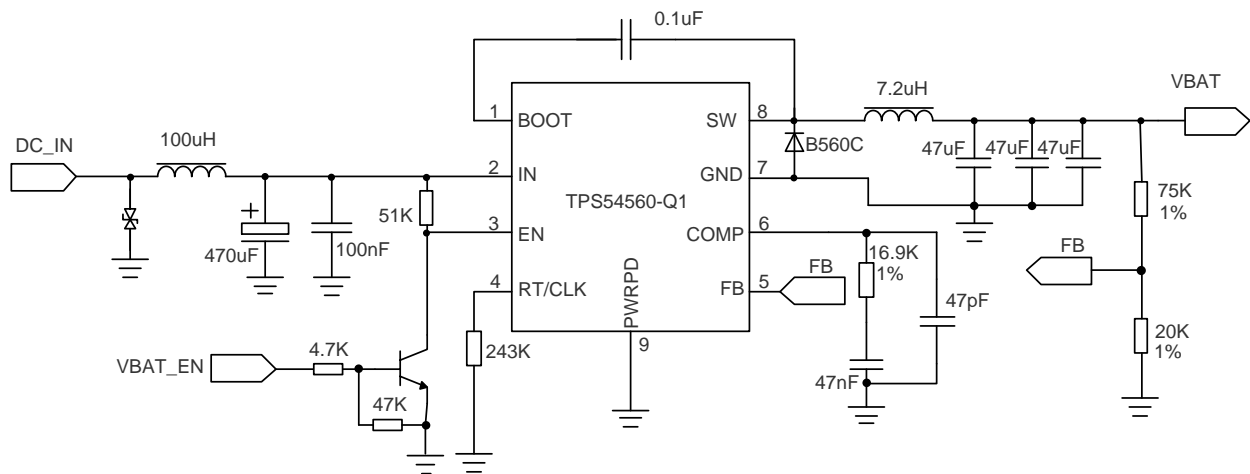


Figure 10: Reference Circuit of Power Supply

3.6.4. Monitor the Power Supply

AT+CBC command can be used to monitor the VBAT_BB voltage value. For more details, please refer to [document \[2\]](#).

3.7. Turn on and off Scenarios

3.7.1. Turn on Module Using the PWRKEY

The following table shows the pin definition of PWRKEY.

Table 7: PWRKEY Pin Description

Pin Name	Pin No.	Description	DC Characteristics	Comment
PWRKEY	2	Turn on/off the module	$V_{IHmax}=2.1V$ $V_{IHmin}=1.3V$ $V_{ILmax}=0.5V$	The output voltage is 0.8V because of the diode drop in the Qualcomm chipset.

When AG35 is in power down mode, it can be turned on by driving the PWRKEY pin to a low level for at least 500ms. It is recommended to use an open drain/collector driver to control the PWRKEY. After STATUS pin (require external pull-up) outputting a low level, PWRKEY pin can be released. A simple reference circuit is illustrated in the following figure.

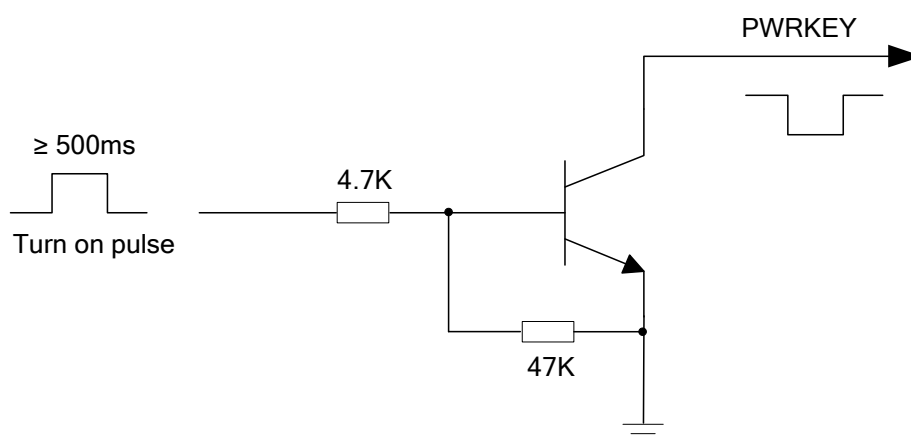


Figure 11: Turn on the Module Using Driving Circuit

Another way to control the PWRKEY is using a button directly. When pressing the key, electrostatic strike may generate from finger. Therefore, a TVS component is indispensable to be placed nearby the button for ESD protection. A reference circuit is shown in the following figure.

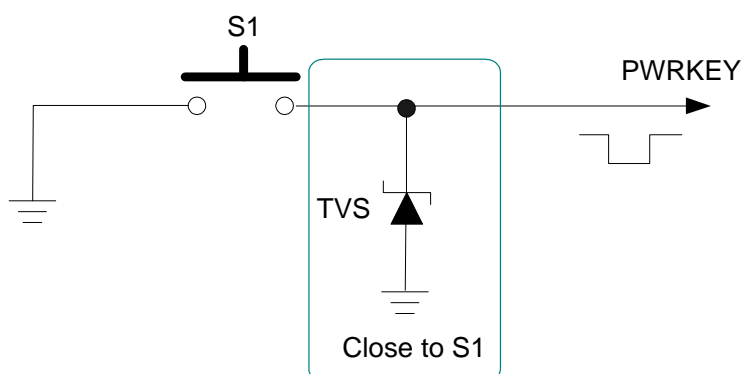


Figure 12: Turn on the Module Using Keystroke

The turn on scenario is illustrated in the following figure.

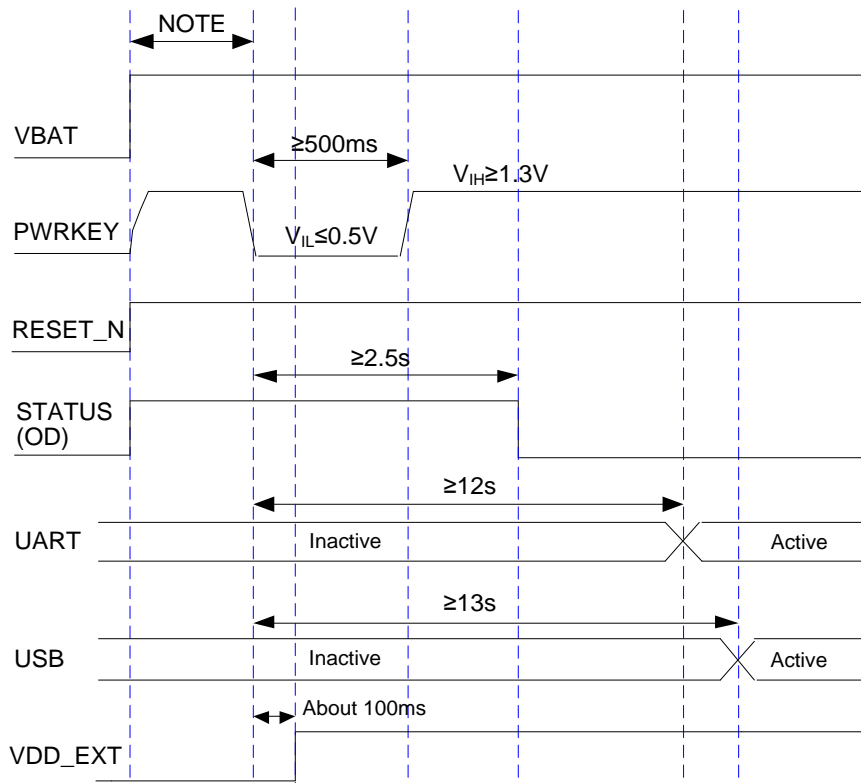


Figure 13: Timing of Turning on Module

NOTE

Please make sure that VBAT is stable before pulling down PWRKEY pin. The time between them is no less than 30ms.

3.7.2. Turn off Module

Either of the following methods can be used to turn off the module:

- Normal power down procedure: Turn off the module using the PWRKEY pin.
- Normal power down procedure: Turn off the module using **AT+QPOWD** command.

3.7.2.1. Turn off Module Using the PWRKEY Pin

Driving the PWRKEY pin to a low level voltage for at least 650ms, the module will execute power-down procedure after PWRKEY is released. The power-down scenario is illustrated in the following figure.

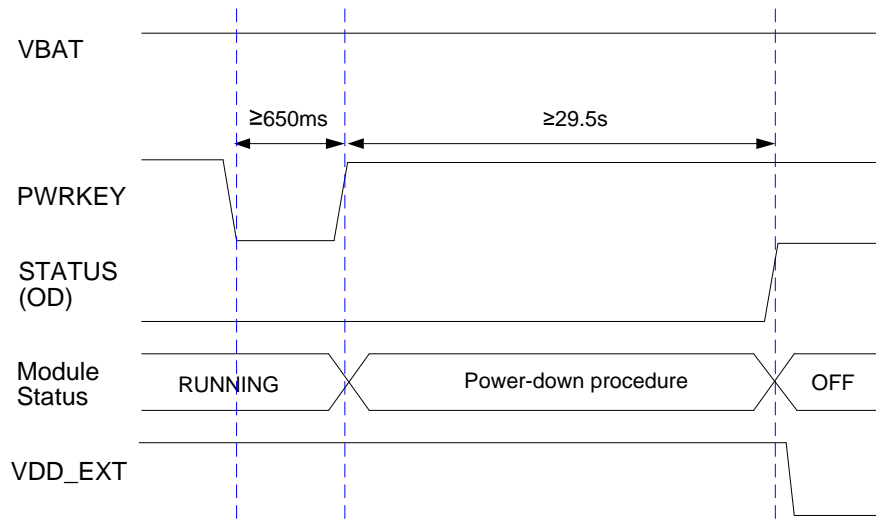


Figure 14: Timing of Turning off Module

3.7.2.2. Turn off Module Using AT Command

It is also a safe way to use **AT+QPOWD** command to turn off the module, which is similar to turning off the module via PWRKEY Pin.

Please refer to **document [2]** for details about the **AT+QPOWD** command.

NOTES

1. In order to avoid damaging the internal flash, please do not switch off the power supply when the module works normally. Only after the module is shut down by PWRKEY or AT command, the power supply can be cut off.
2. When turn off module with AT command, please keep PWRKEY at high level after the execution of power-off command. Otherwise the module will be turned on again after successfully turn-off.

3.7.2.3. Turn off Module Using SHDN_N

The following table shows the pin definition of SHDN_N.

Table 8: Pin Definition of SHDN_N

Pin Name	Pin No.	Description	DC Characteristics	Comment
SHDN_N	176	Emergency shutdown	$V_{IHmax}=2.1V$	

for the module

$V_{IHmin}=1.3V$

$V_{ILmax}=0.5V$

Driving the SHDN_N pin to a low level voltage and then releasing it will make the module shut down unconditionally. The shut-down scenario is illustrated in the following figure.

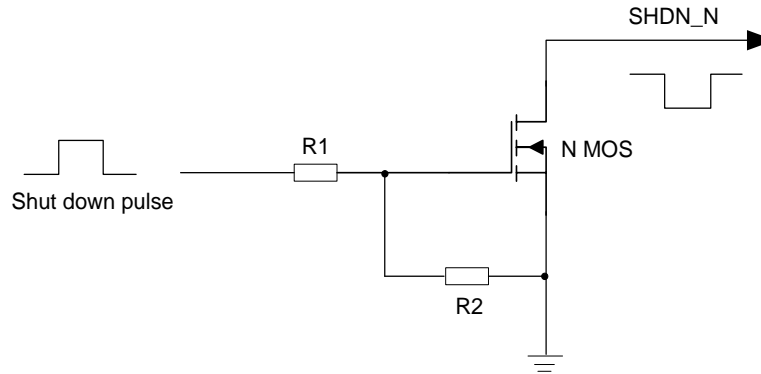


Figure 15: Shut Down the Module Using Driving Circuit

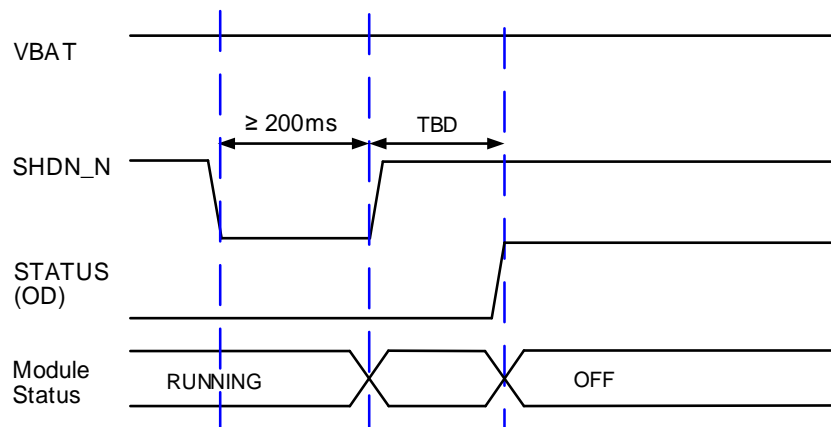


Figure 16: Timing of Turning off Module via SHDN_N

NOTES

1. Pulling down SHDN_N for module shutdown is an emergency option when there are failures in turning off the module by PWRKEY or AT command. And it is recommended to use an external OD circuit to control the SHDN_N pin.
2. Never pull up SHDN_N pin.

3.8. Reset the Module

The RESET_N can be used to reset the module. The module can be reset by driving the RESET_N to a low level voltage for 150~460ms. As the RESET_N pin is sensitive to interference, the routing trace on the interface board of the module is recommended to be as short as possible and totally ground shielded.

Table 9: RESET_N Pin Description

Pin Name	Pin No.	Description	DC Characteristics	Comment
RESET_N	1	Reset the module	$V_{IHmax}=2.1V$ $V_{IHmin}=1.3V$ $V_{ILmax}=0.5V$	Pull-up to 1.8V internally. Active low.

The recommended circuit is similar to the PWRKEY control circuit. An open drain/collector driver or button can be used to control the RESET_N.

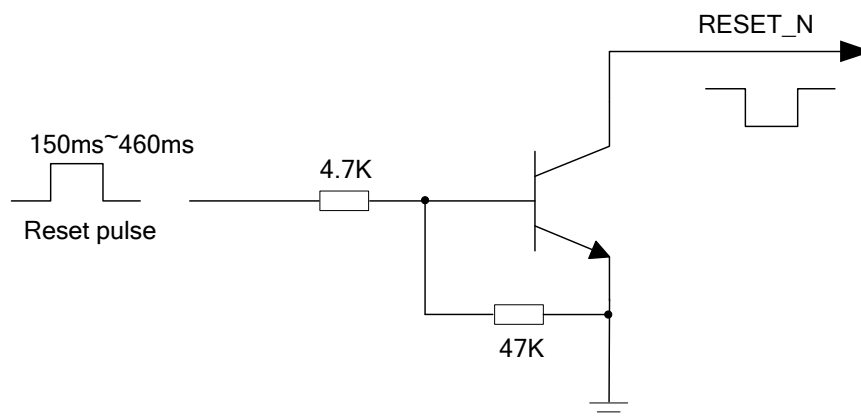


Figure 17: Reference Circuit of RESET_N by Using Driving Circuit

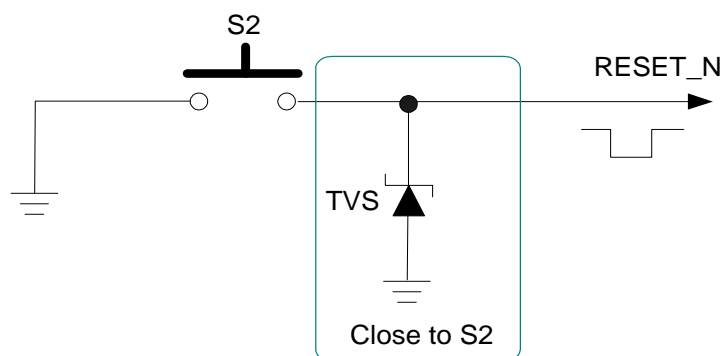


Figure 18: Reference Circuit of RESET_N by Using Button

The reset scenario is illustrated in the following figure.

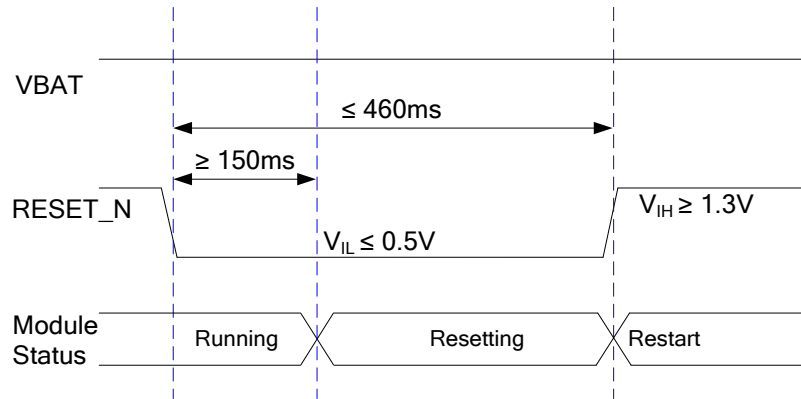


Figure 19: Timing of Resetting Module

NOTES

1. Use RESET_N only when turning off the module by **AT+QPOWD** command and PWRKEY pin both failed.
2. Please assure that there is no large capacitance on PWRKEY and RESET_N pins.

3.9. (U)SIM Interface

The (U)SIM interface circuitry meets ETSI and IMT-2000 requirements. Both 1.8V and 3.0V (U)SIM cards are supported.

Table 10: Pin Definition of (U)SIM Interface

Pin Name	Pin No.	I/O	Description	Comment
USIM_VDD	26	PO	Power supply for (U)SIM card	Either 1.8V or 3.0V is supported by the module automatically.
USIM_DATA	29	IO	Data signal of (U)SIM card	
USIM_CLK	27	DO	Clock signal of (U)SIM card	
USIM_RST	28	DO	Reset signal of (U)SIM card	
USIM_PRESENCE	25	DI	(U)SIM card insertion detection	
USIM_GND	24		Specified ground for (U)SIM card	

AG35 supports (U)SIM card hot-plug via the USIM_PRESENCE pin. The function supports low level and high level detections, and is disabled by default. Please refer to **document [2]** about **AT+QSIMDET** command for details.

The following figure shows a reference design of (U)SIM interface with an 8-pin (U)SIM card connector.

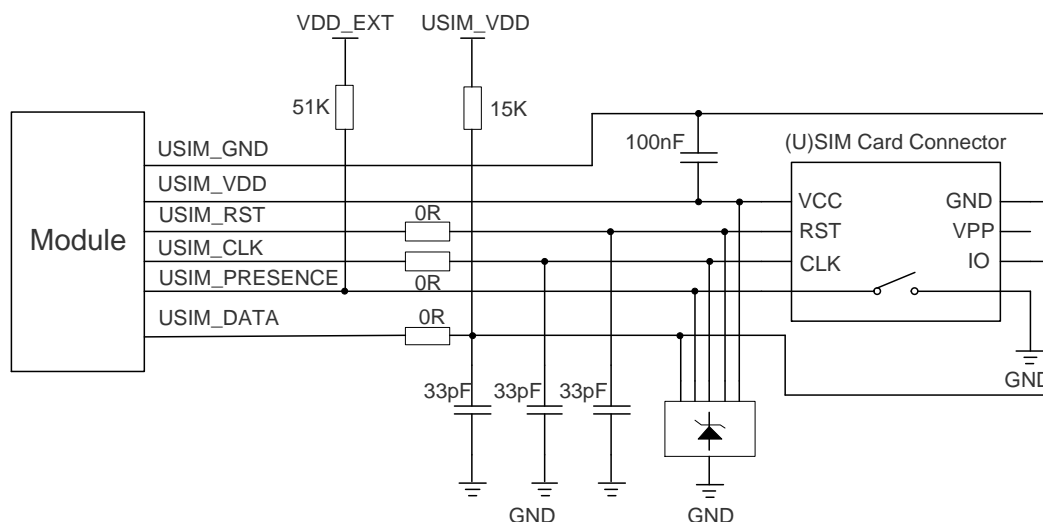


Figure 20: Reference Circuit of (U)SIM Interface with an 8-Pin (U)SIM Card Connector

If (U)SIM card detection function is not needed, please keep USIM_PRESENCE unconnected. A reference circuit for (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

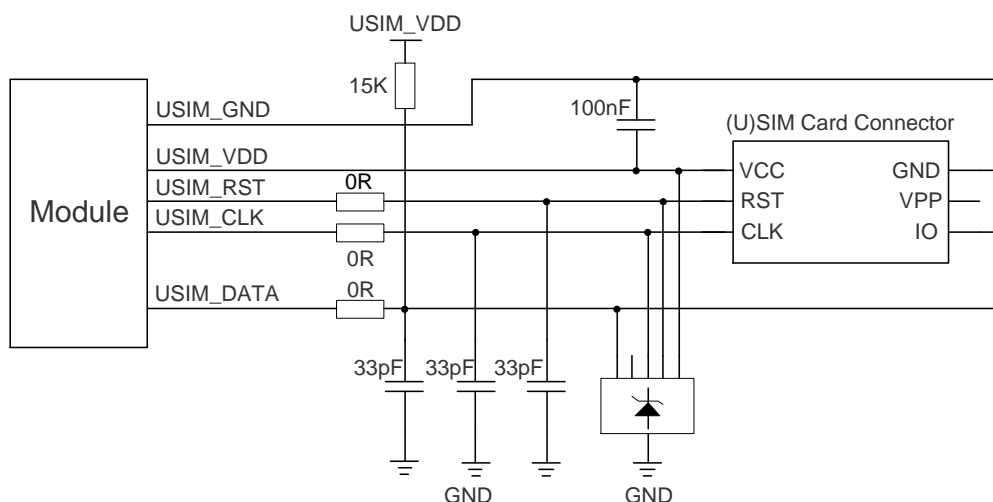


Figure 21: Reference Circuit of (U)SIM Interface with a 6-Pin (U)SIM Card Connector

In order to enhance the reliability and availability of the (U)SIM card in customers' applications, please follow the criteria below in the (U)SIM circuit design:

- Keep the placement of (U)SIM card connector as close as possible to the module. Keep the trace length as less than 200mm as possible.
- Keep (U)SIM card signals away from RF and VBAT traces.
- Assure the ground between the module and the (U)SIM card connector short and wide. Keep the trace width of ground and USIM_VDD no less than 0.5mm to maintain the same electric potential.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.
- In order to offer good ESD protection, it is recommended to add a TVS diode array with parasitic capacitance not exceeding 10pF. The 0Ω resistors should be added in series between the module and the (U)SIM card connector so as to suppress EMI spurious transmission and enhance ESD protection. The 33pF capacitors are used for filtering interference of EGSM900. Please note that the (U)SIM peripheral circuit should be close to the (U)SIM card connector.
- The pull-up resistor on USIM_DATA line can improve anti-jamming capability when long layout trace and sensitive occasions are applied, and should be placed close to the (U)SIM card connector.

NOTE

The load capacitance of (U)SIM interface will affect rise and fall time of data exchange.

3.10. USB Interface

AG35 contains one integrated Universal Serial Bus (USB) interface which complies with the USB 2.0 specification and supports high-speed (480Mbps) and full-speed (12Mbps) modes. The USB interface is used for AT command communication, data transmission, GNSS NMEA sentences output, software debugging, firmware upgrade and voice over USB*. The following table shows the pin definition of USB interface.

Table 11: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	32	PI	USB connection detection	Typical 5.0V Maximum current: 1mA
USB_DM	33	IO	USB differential data bus (-)	Require differential impedance of 90Ω
USB_DP	34	IO	USB differential data bus (+)	
GND	30		Ground	

For more details about USB 2.0 specifications, please visit <http://www.usb.org/home>.

The USB interface is recommended to be reserved for firmware upgrade in application design. The following figure shows a reference circuit of USB interface.

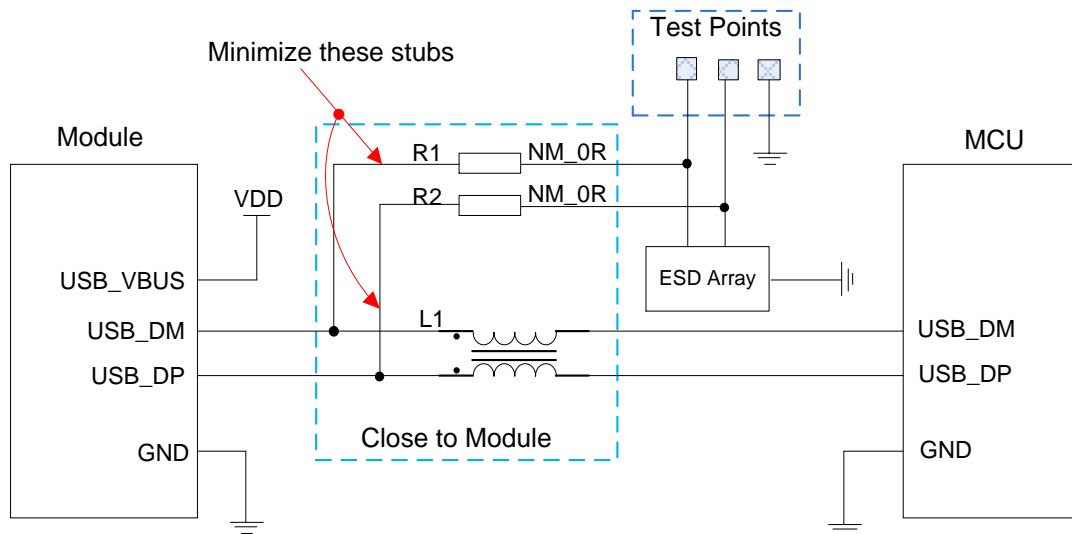


Figure 22: Reference Circuit of USB Application

In order to ensure signal integrity of USB data lines, components R1, R2 and L1 must be placed close to the module, and also these resistors should be placed close to each other. The extra stubs of trace must be as short as possible.

The following principles should be complied with when design the USB interface, so as to meet USB 2.0 specification.

- It is important to route the USB signal traces as differential pairs with total grounding. The impedance of USB differential trace is 90Ω.
- Do not route signal traces under crystals, oscillators, magnetic devices or RF signal traces. It is important to route the USB differential traces in inner-layer with ground shielding on not only upper and lower layers but also right and left sides.
- Pay attention to the influence of junction capacitance of ESD protection components on USB data lines. Typically, the capacitance value should be less than 2pF.
- Keep the ESD protection components as close to the USB connector as possible.

NOTES

1. AG35 can be used as a slave device only.
2. “*” means under development.

3.11. UART Interfaces

The module provides three UART interfaces: main UART interface, UART2 interface and debug UART interface. The following are the features of these UART interfaces.

- The main UART interface supports 9600bps, 19200bps, 38400bps, 57600bps, 115200bps, 230400bps, 460800bps and 921600bps baud rates, and the default is 115200bps. The interface is used for data transmission and AT command communication.
- The UART2 interface supports 9600bps, 19200bps, 38400bps, 57600bps, 115200bps, 230400bps, 460800bps and 921600bps baud rates, and the default is 115200bps. The interface is designed for BT function*.
- The debug UART interface supports 115200bps baud rate. It is used for Linux console and log output.

The following tables show the pin definition of the three UART interfaces.

Table 12: Pin Definition of Main UART Interface

Pin Name	Pin No.	I/O	Description	Comment
UART1_RI	61	DO	Ring indicator	1.8V power domain
UART1_DCD	59	DO	Data carrier detection	1.8V power domain
UART1_CTS	56	DO	Clear to send	1.8V power domain
UART1_RTS	57	DI	Request to send	1.8V power domain
UART1_DTR	62	DI	Sleep mode control	1.8V power domain
UART1_TXD	60	DO	Transmit data	1.8V power domain
UART1_RXD	58	DI	Receive data	1.8V power domain

Table 13: Pin Definition of UART2 Interface (for BT Function*)

Pin Name	Pin No.	I/O	Description	Comment
UART2_TXD	163	DO	Transmit data	1.8V power domain
UART2_CTS	164	DO	Clear to send	1.8V power domain
UART2_RXD	165	DI	Receive data	1.8V power domain

UART2_RTS	166	DI	Request to send	1.8V power domain
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Table 14: Pin Definition of Debug UART Interface

Pin Name	Pin No.	I/O	Description	Comment
DBG_TXD	71	DO	Transmit data	1.8V power domain
DBG_RXD	72	DI	Receive data	1.8V power domain

The logic levels are described in the following table.

Table 15: Logic Levels of Digital I/O

Parameter	Min.	Max.	Unit
V_{IL}	-0.3	0.6	V
V_{IH}	1.2	2.0	V
V_{OL}	0	0.45	V
V_{OH}	1.35	1.8	V

The module provides 1.8V UART interfaces. A level translator should be used if customers' application is equipped with a 3.3V UART interface. A level translator TXS0108E-Q1 provided by *Texas Instruments* is recommended. The following figure shows a reference design.

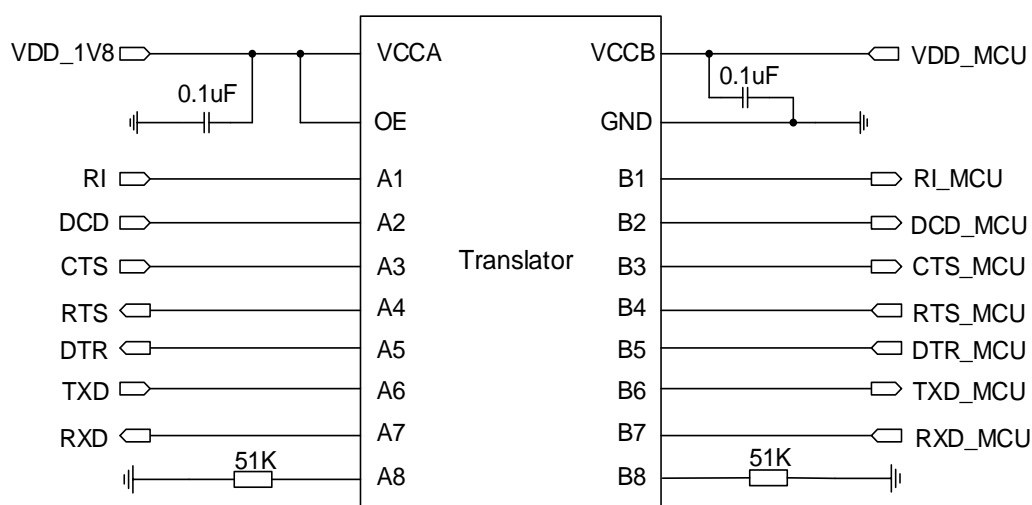


Figure 23: Reference Circuit with Translator Chip

Please visit <http://www.ti.com> for more information.

Another example with transistor translation circuit is shown as below. The circuit design of dotted line section can refer to the design of solid line section, in terms of both module input and output circuit designs. But please pay attention to the direction of connection.

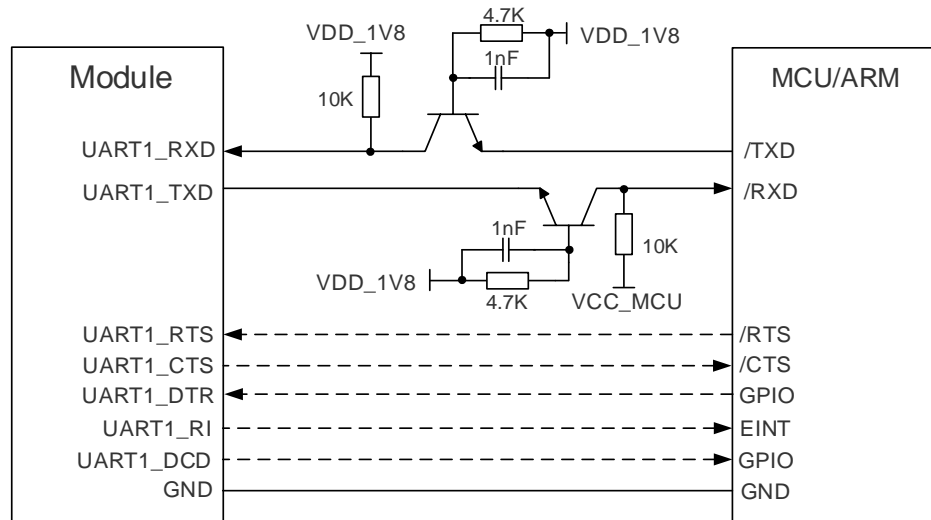


Figure 24: Reference Circuit with Transistor Circuit

NOTES

1. The above is a reference circuit of UART1 interface, which is similar to that of other UART interfaces.
2. Transistor circuit solution is not suitable for applications with high baud rates exceeding 460Kbps.
3. When the module enters into sleep mode, it is recommended to switch off the power supply for VDD_1V8 so as to reduce power consumption.
4. “*” means under development.

3.12. Audio Interface (Optional)

AG35 is designed with an optional built-in audio codec to enable analog audio function. The following table shows the pin definition of analog audio interface.

Table 16: Pin Definition of Analog Audio Interface

Pin Name	Pin No.	I/O	Description	Comment
SPK2_P	132	AO	Earphone analog output 2 (+)	

SPK2_N	133	AO	Earphone analog output 2 (-)
SPK1_P	134	AO	Earphone analog output 1 (+)
SPK1_N	135	AO	Earphone analog output 1 (-)
MICBIAS	136	AO	Bias voltage output for microphone
MIC2_N	137	AI	Microphone analog input 2 (-)
MIC2_P	138	AI	Microphone analog input 2 (+)
MIC1_N	139	AI	Microphone analog input 1 (-)
MIC1_P	140	AI	Microphone analog input 1 (+)
AGND	141		Analog ground

Table 17: Audio Interface Characteristics

Parameter	Condition	Min	Typ.	Max	Unit
MIC1_P/N					
Full-Scale Input	$AV_{LINE}=0dB$ $f=1kHz$			1.0	Vp-p
Noise	$AV_{LINE}=0dB$ $f=1kHz$		-80		dB
SPK1_P/N					
Max power output	Differential mode $R_L=32\Omega$ $f=1kHz$			462.5	mV
THD+N	Output Gain=0dB $f=1kHz$		0.28%		

NOTES

1. The built-in codec uses the same signals as the module's PCM interface (pins 65~68) for external digital audio design. Therefore, when the built-in codec is utilized, the PCM interface cannot be used for other purposes (that is, keep pins 65~68 unconnected or set the interface to high impedance state).
2. The built-in audio codec (analog audio function) is optional.
3. MOS ≥ 3.8 .

3.13. PCM and I2C Interfaces

AG35 provides one Pulse Code Modulation (PCM) digital interface for audio design. The interface supports the following modes:

- Primary mode (short frame synchronization, works as both master and slave)
- Auxiliary mode (long frame synchronization, works as master only)

In primary mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC falling edge represents the MSB. In this mode, the PCM interface supports 256kHz, 512kHz, 1024kHz or 2048kHz PCM_CLK at 8kHz PCM_SYNC, and also supports 4096kHz PCM_CLK at 16kHz PCM_SYNC.

In auxiliary mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC rising edge represents the MSB. In this mode, the PCM interface operates with a 256kHz, 512kHz, 1024kHz or 2048kHz PCM_CLK and an 8kHz, 50% duty cycle PCM_SYNC.

AG35 supports 16-bit linear data format. The following figures show the primary mode's timing relationship with 8kHz PCM_SYNC and 2048kHz PCM_CLK, as well as the auxiliary mode's timing relationship with 8kHz PCM_SYNC and 256kHz PCM_CLK.

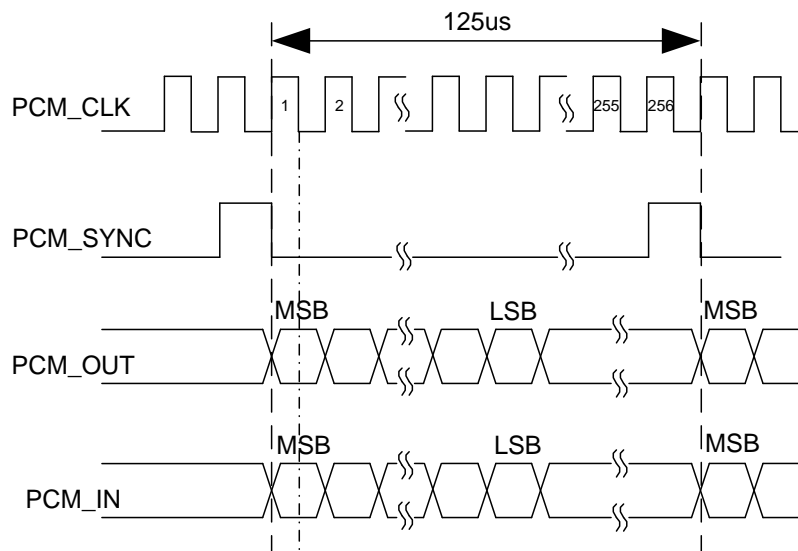


Figure 25: Primary Mode Timing

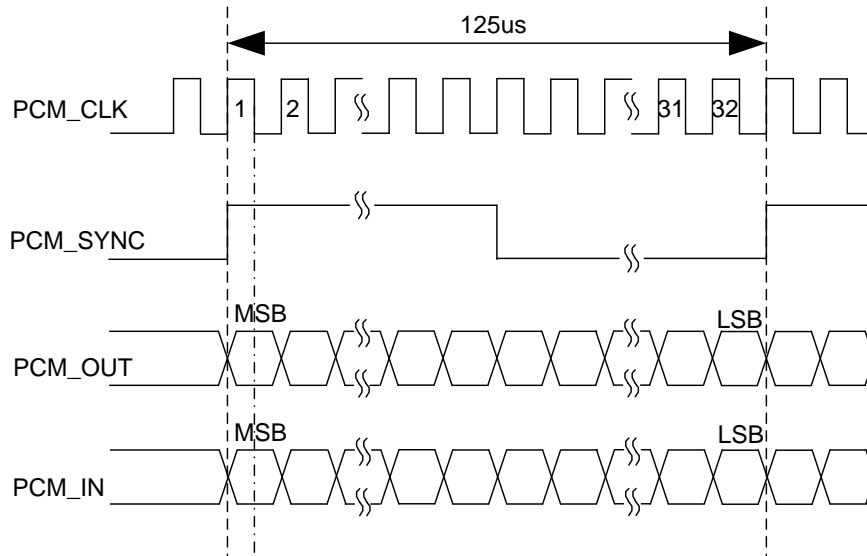


Figure 26: Auxiliary Mode Timing

The following table shows the pin definition of PCM and I2C interfaces which can be applied on audio codec design.

Table 18: Pin Definition of PCM Interface

Pin Name	Pin No.	I/O	Description	Comment
PCM_IN	66	DI	PCM data input	1.8V power domain
PCM_OUT	68	DO	PCM data output	1.8V power domain
PCM_SYNC	65	IO	PCM data frame sync signal	1.8V power domain
PCM_CLK	67	IO	PCM data bit clock	1.8V power domain
MCLK	152	DO	Output 12.288MHz	1.8V power domain

Table 19: Pin Definition of I2C Interfaces

Pin Name	Pin No.	I/O	Description	Comment
I2C1_SDA	42	IO	I2C1 serial data	Require external pull-up to 1.8V
I2C1_SCL	43	DO	I2C1 serial clock	Require external pull-up to 1.8V
I2C2_SDA	73	IO	I2C2 serial data	Require external pull-up to 1.8V

I2C2_SCL	74	DO	I2C2 serial clock	Require external pull-up to 1.8V
----------	----	----	-------------------	----------------------------------

NOTES

1. By default, I2C1 is used for codec configuration while I2C2 is not available with any codec configuration driver.
2. When the built-in codec is used, its 8-bit address is 0x31 when reading and 0x30 when writing. In order to avoid conflicts, please avoid using I2C1 peripherals with the same addresses.
3. When the built-in codec is used, pin 152 and pins 65~68 will not be used.

Clock and mode can be configured by AT command, and the default configuration is master mode using short frame synchronization format with 2048kHz PCM_CLK and 8kHz PCM_SYNC. Please refer to **document [2]** about **AT+QDAI** command for details.

The following figure shows a reference design of PCM interface with external codec IC.

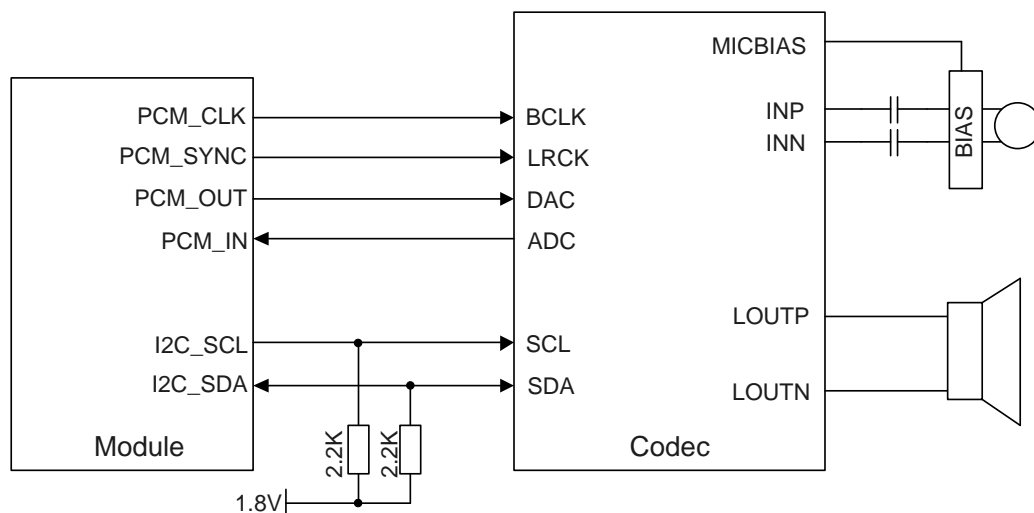


Figure 27: Reference Circuit of PCM Application with Audio Codec

NOTES

1. It is recommended to reserve an RC (R=22Ω, C=22pF) circuit on the PCM lines, especially for PCM_CLK.
2. AG35 works as a master device pertaining to I2C interface.

3.14. SDIO Interfaces

AG35 provides two SDIO interfaces which support SD 3.0 protocol.

3.14.1. SDIO1 Interface

SDIO1 interface is used for WLAN function. More details are provided in **Chapter 3.16**.

3.14.2. SDIO2 Interface

SDIO2 interface supports SD card.

The following tables show the pin definition of SDIO2 interface.

Table 20: Pin Definition of SDIO2 Interface

Pin Name	Pin No.	I/O	Description	Comment
SDC2_DATA3	48	IO	SDIO data signal (bit 3)	SDIO signal level can be selected according to the one supported by SD card. Please refer to SD 3.0 protocol for more details.
SDC2_DATA2	47	IO	SDIO data signal (bit 2)	
SDC2_DATA1	50	IO	SDIO data signal (bit 1)	
SDC2_DATA0	49	IO	SDIO data signal (bit 0)	
SDC2_CLK	53	DO	SDIO bus clock	
SDC2_CMD	51	IO	SDIO command signal	1.8V/2.85V configurable output. Cannot be used for SD card power supply.
VDD_SDIO	46	PO	SDIO pull up power source	
SD_INS_DET	52	DI	Insertion detection for SD card	

The following figure shows a reference design of SD card interface.

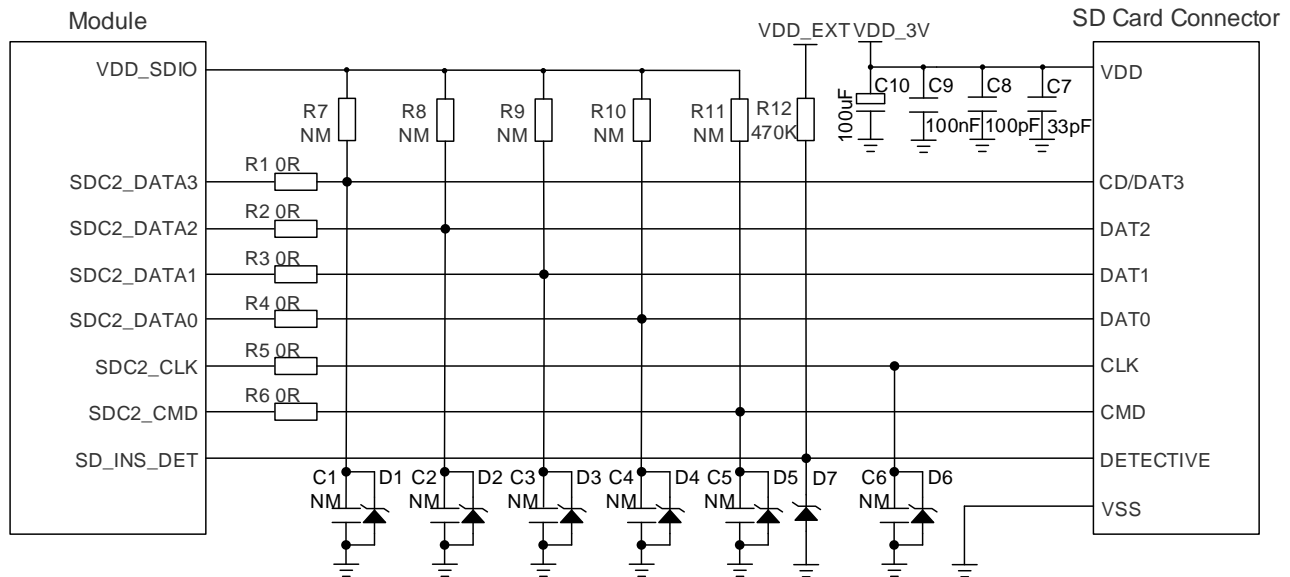


Figure 28: Reference Circuit of SD Card Application

Please follow the principles below in the SD card circuit design:

- The voltage range of SD card power supply VDD_3V is 2.7~3.6V and a sufficient current up to 0.8A should be provided. As the maximum output current of VDD_SDIO is 50mA which can only be used for SDIO pull-up resistors, an externally power supply is needed for SD card.
- To avoid jitter of bus, resistors R7~R11 are needed to pull up the SDIO to VDD_SDIO. Value of these resistors is among 10~100kohm and the recommended value is 100kohm.
- In order to improve signal quality, it is recommended to add 0Ω resistors R1~R6 in series between the module and the SD card. The bypass capacitors C1~C6 are reserved and not mounted by default. All resistors and bypass capacitors should be placed close to the module.
- In order to offer good ESD protection, it is recommended to add TVS with capacitance value less than 2pF on SD card pins.
- It is important to route the SDIO signal traces with total grounding. The impedance of SDIO data trace is 50Ω (±10%).
- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, analog signals, etc., as well as noisy signals such as clock signals, DCDC signals, etc.
- It is recommended to keep the trace length difference between CLK and DATA/CMD less than 1mm and the total routing length less than 50mm. The total trace length inside the module is 23mm, so the exterior total trace length should be less than 27mm.
- Make sure the adjacent trace spacing is two times of the trace width and the load capacitance of SDIO bus should be less than 40pF.

3.15. SGMII Interface (Optional)

AG35 includes an integrated Ethernet MAC with an SGMII interface and two management interfaces. Key features of the SGMII interface are shown below:

- IEEE802.3 compliance
- Half/full duplex for 10/100/1000Mbps
- Support VLAN tagging
- Support IEEE1588 and Precision Time Protocol (PTP)
- Can be connected to an external Ethernet PHY like AR8033, or an external switch
- Management interfaces support dual power domains: 1.8V and 2.85V.

The following table shows the pin definition of SGMII interface.

Table 21: Pin Definition of SGMII Interface

Pin Name	Pin No.	I/O	Description	Comment
MDIO Interface				
EPHY_RST_N	6	DO	Ethernet PHY reset	1.8V/2.85V power domain
EPHY_INT_N	9	DI	Ethernet PHY interrupt	1.8V power domain
SGMII_MDATA	8	IO	SGMII MDIO (Management Data Input/Output) data	1.8V/2.85V power domain
SGMII_MCLK	7	DO	SGMII MDIO (Management Data Input/Output) clock	1.8V/2.85V power domain
VDD_MDIO	4	PO	SGMII MDIO pull-up power source	1.8V/2.85V power domain. External pull-up power source for SGMII MDIO pins.
SGMII Signal Part				
SGMII_TX_M	15	AO	SGMII transmission (-)	Connect with a 0.1uF capacitor, close to the PHY side.
SGMII_TX_P	14	AO	SGMII transmission (+)	Connect with a 0.1uF capacitor, close to the PHY side.
SGMII_RX_P	12	AI	SGMII receiving (+)	
SGMII_RX_M	11	AI	SGMII receiving (-)	

The following figure shows the simplified block diagram for Ethernet application.

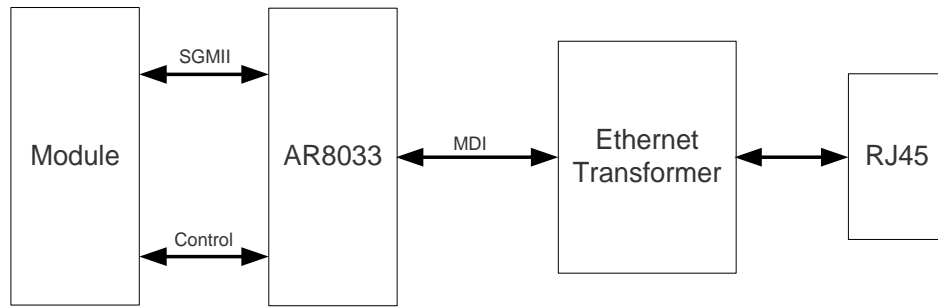


Figure 25: Simplified Block Diagram for Ethernet Application

The following figure shows a reference design of SGMII interface with PHY AR8033 application.

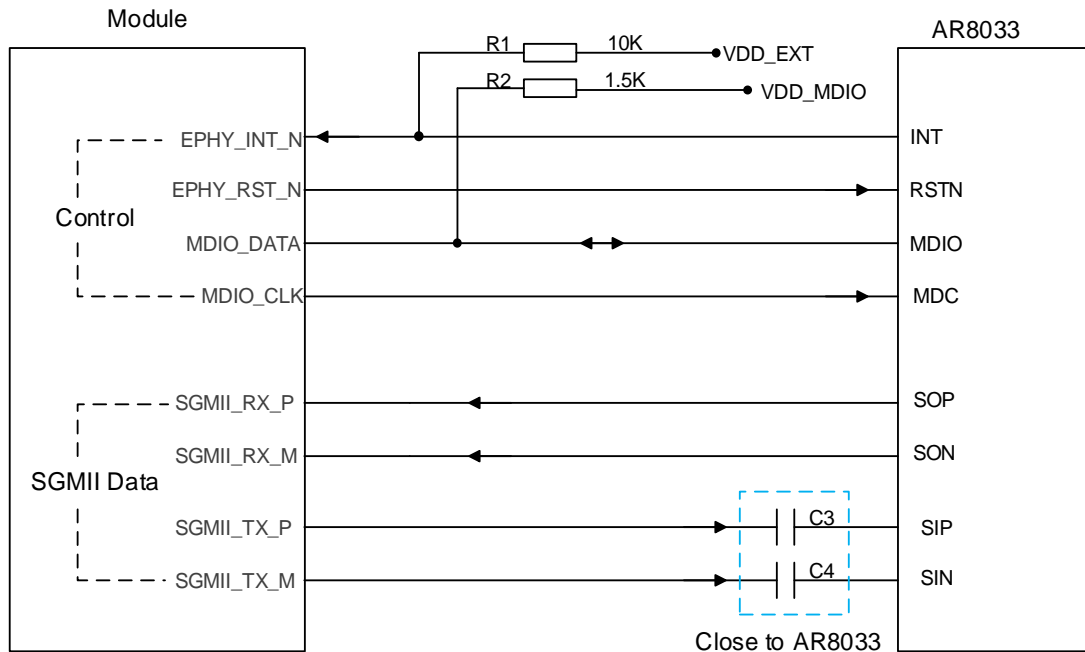


Figure 26: Reference Circuit of SGMII Interface with PHY AR8033 Application

In order to enhance the reliability and availability of customers' application, please follow the criteria below in the Ethernet PHY circuit design:

- Keep SGMII data and control signals away from RF and VBAT traces.
- Keep the maximum trace length less than 10 inches and keep skew on the differential pairs less than 20 mils.
- The differential impedance of SGMII data trace is $100\Omega \pm 10\%$.
- To minimize crosstalk, the distance between separate adjacent pairs that are on the same layer must be equal to or larger than 40 mils.

3.16. Wireless Connectivity Interfaces

AG35 supports a low-power SDIO 3.0 interface (SDIO1 interface) for WLAN function, and UART2 & PCM interfaces for BT function*.

The following table shows the pin definition of wireless connectivity interfaces.

Table 22: Pin Definition of Wireless Connectivity Interfaces

Pin Name	Pin No.	I/O	Description	Comment
WLAN Power Supply				
PM_ENABLE	5	DO	WLAN power enable	1.8V power domain
WLAN Interface				
SDC1_DATA3	23	IO	SDIO data bus (bit 3)	1.8V power domain
SDC1_DATA2	22	IO	SDIO data bus (bit 2)	1.8V power domain
SDC1_DATA1	21	IO	SDIO data bus (bit 1)	1.8V power domain
SDC1_DATA0	20	IO	SDIO data bus (bit 0)	1.8V power domain
SDC1_CLK	19	DO	SDIO clock signal	1.8V power domain
SDC1_CMD	18	IO	SDIO command signal	1.8V power domain
WLAN_EN	149	DO	WLAN function control via Wi-Fi module. Active high.	1.8V power domain
WLAN_WAKE	160	DI	Wake up the host (AG35 module) by Wi-Fi module	1.8V power domain
WLAN_SLP_CLK	169	DO	WLAN sleep clock	1.8V power domain
Coexistence Interface				
COEX_UART_RX/ USB_BOOT	146	DI	LTE/WLAN&BT coexistence signal	1.8V power domain
COEX_UART_TX	145	DO	LTE/WLAN&BT coexistence signal	1.8V power domain
BT Interface*				
BT_EN*	3	DO	Bluetooth enable control	V _{OL} max=0.45V

V _{OHmin} =1.35V				
UART2_TXD	163	DO	Transmit data	1.8V power domain
UART2_CTS	164	DO	DTE clear to send	1.8V power domain
UART2_RXD	165	DI	Receive data	1.8V power domain
UART2_RTS	166	DI	DTE request to send	1.8V power domain
PCM_IN	66	DI	PCM data input	1.8V power domain
PCM_OUT	68	DO	PCM data output	1.8V power domain
PCM_SYNC	65	IO	PCM data frame sync signal	1.8V power domain
PCM_CLK	67	IO	PCM data bit clock	1.8V power domain

The following figure shows a reference design for the connection between wireless connectivity interfaces and Quectel AF20 module.

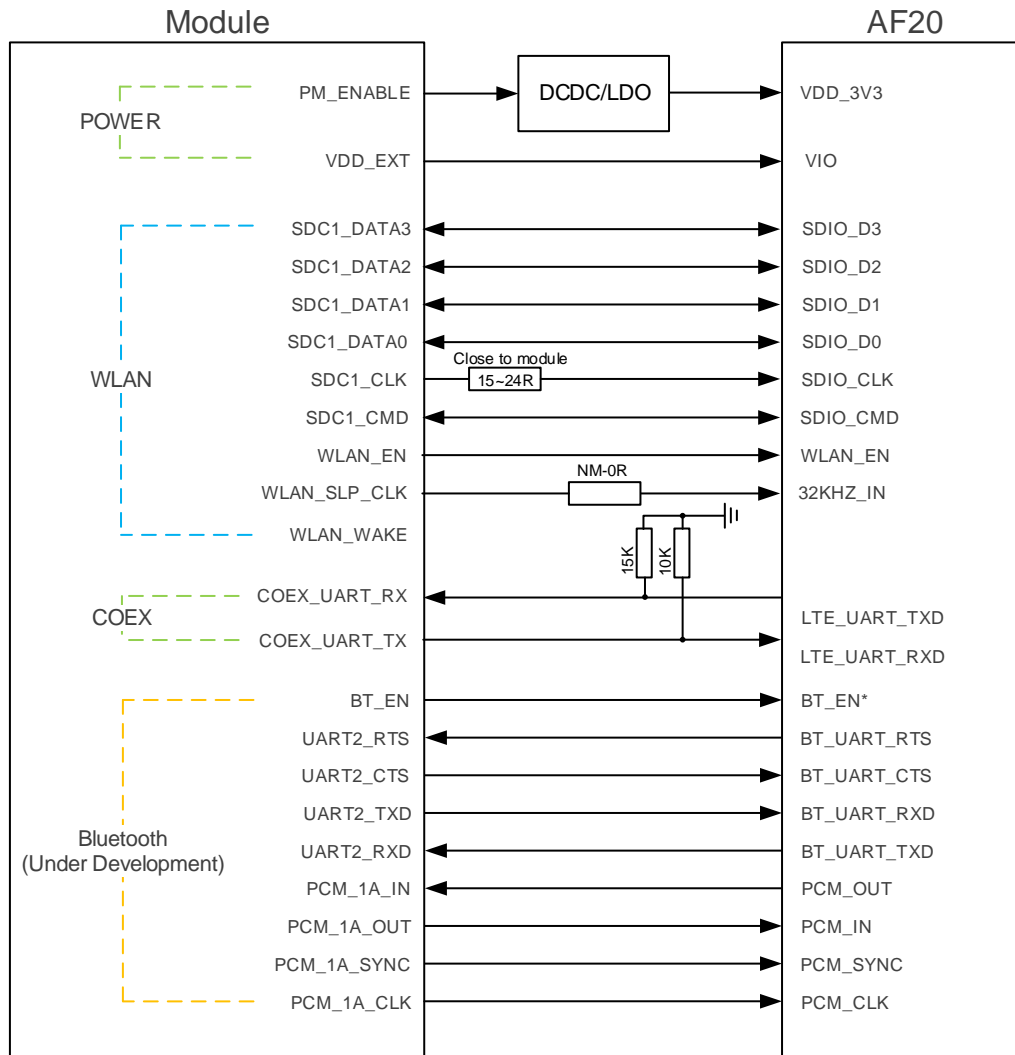


Figure 29: Reference Circuit for Connection with AF20 Module

3.16.1. WLAN Interface

AG35 provides a low power SDIO 3.0 interface and a control interface for WLAN design.

The WLAN interface (SDIO interface) supports the following modes:

- Single data rate (SDR) mode (up to 208MHz)
- Double data rate (DDR) mode (up to 50MHz)

As SDIO signals are very high-speed signals, in order to ensure the SDIO interface design corresponds with the SDIO 3.0 specification, please comply with the following principles:

- It is important to route the SDIO signal traces with total grounding. The impedance of SDIO signal

trace is 50Ω (±10%).

- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, analog signals, etc., as well as noisy signals such as clock signals, DCDC signals, etc.
- It is recommended to keep the trace length difference between CLK and DATA/CMD less than 1mm and the total routing length less than 50mm. The total length of SDIO signal traces inside AG35 module is 12mm and that inside AF20 is 10mm, so the exterior total trace length should be less than 28mm.
- Keep termination resistors within 15~24Ω on clock lines near the module and keep the route distance from the module clock pins to termination resistors less than 5mm.
- Make sure the adjacent trace spacing is two times of the trace width and the bus capacitance is less than 40pF.

3.16.2. BT Interface*

More information about BT interface will be added in the future version of this document.

NOTE

“*” means under development.

3.17. ADC Interfaces

The module provides three analog-to-digital converter (ADC) interfaces. The voltage value on ADC pins can be read via **AT+QADC=<port>** command, through setting <port> into 0, 1 or 2. For more details about the AT command, please refer to **document [2]**.

- **AT+QADC=0**: read the voltage value on ADC0
- **AT+QADC=1**: read the voltage value on ADC1
- **AT+QADC=2**: read the voltage value on ADC2

In order to improve the accuracy of ADC, the trace of ADC interfaces should be surrounded by ground.

Table 23: Pin Definition of ADC Interfaces

Pin Name	Pin No.	Description
ADC2	172	General purpose analog to digital converter interface
ADC0	173	General purpose analog to digital converter interface

ADC1	175	General purpose analog to digital converter interface
------	-----	---

The following table describes the characteristics of ADC interfaces.

Table 24: Characteristics of ADC Interfaces

Parameter	Min.	Typ.	Max.	Unit
ADC2 Voltage Range	0.1		1.7	V
ADC0 Voltage Range	0.3		VBAT_BB	V
ADC1 Voltage Range	0.3		VBAT_BB	V
ADC Resolution		15		bits
ADC Sample Rate		2.4		MHz

NOTES

1. The input voltage for each ADC interface must not exceed its corresponding voltage range.
2. It is prohibited to supply any voltage to ADC pins when VBAT is removed.
3. It is recommended to use resistor divider circuit for ADC application.

3.18. Network Status Indication

The network indication pins can be used to drive network status indication LEDs. The module provides two network indication pins: NET_MODE and NET_STATUS. The following tables describe the pin definition and logic level changes in different network status.

Table 25: Pin Definition of Network Connection Status /Activity Indicator

Pin Name	Pin No.	I/O	Description	Comment
NET_MODE	147	DO	Indicate the module's network registration status	1.8V power domain
NET_STATUS	170	DO	Indicate the module's network activity status	1.8V power domain

Table 26: Working State of the Network Connection Status /Activity Indicator

Pin Name	Logic Level Changes	Network Status
NET_MODE	Always High	Registered on LTE network
	Always Low	Others
NET_STATUS	Flicker slowly (200ms High/1800ms Low)	Network searching
	Flicker slowly (1800ms High/200ms Low)	Idle
	Flicker quickly (125ms High/125ms Low)	Data transfer is ongoing
	Always High	Voice calling

A reference circuit is shown in the following figure.

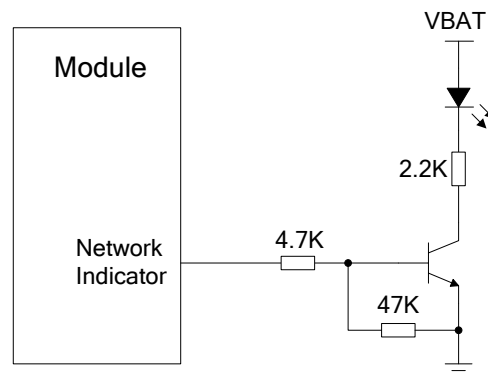


Figure 30: Reference Circuit of the Network Indicator

3.19. STATUS

The STATUS pin is an open drain output for indicating the module's operation status. It can be connected to a GPIO of DTE with a pull up resistor, or as an LED indication circuit as shown below. When the module is turned on normally, the STATUS pin will present a low level state. Otherwise, it will present high-impedance state.

Table 27: Pin Definition of STATUS

Pin Name	Pin No.	I/O	Description	Comment
STATUS	171	OD	Indicate the module's operation status	Require external pull-up

The following figure shows different design circuits of STATUS, and customers can choose either one according to application demands.

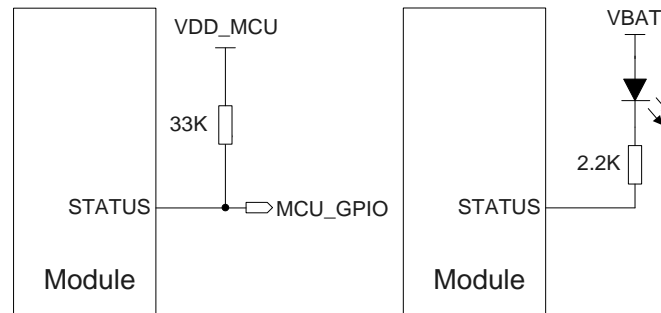


Figure 31: Reference Circuit of the STATUS

NOTES

1. In sleep state, STATUS will still output a low voltage to drive the LED, causing an extra current consumption on VBAT. So it is recommended to replace VBAT with an external controllable power supply, and use it to switch off the power source during sleep state so as to reduce power consumption.
2. It is not recommended to use level translator circuit for STATUS.

3.20. Behaviors of RI

AT+QCFG="risignalttype", "physical" command can be used to configure RI behavior.

No matter on which port URC is presented, URC will trigger the behavior of RI pin.

NOTE

URC can be outputted from UART port, USB AT port and USB modem port by **AT+QURCCFG** command. The default port is USB AT port.

The default behaviors of RI are shown as below.

Table 28: Default Behaviors of RI

State	Response
Idle	RI keeps in high level
URC	RI outputs 120ms low pulse when new URC returns

The default RI behaviors can be configured flexibly by **AT+QCFG="urc/ri/ring"** command. Please refer to **document [2]** for more details.

3.21. USB_BOOT Interface

AG35 provides a USB_BOOT pin which is multiplexed with COEX_UART_RX. Developers can pull up USB_BOOT to VDD_EXT before powering on the module, thus the module will enter into emergency download mode when powered on. In this mode, the module supports firmware upgrade over USB interface.

Table 29: Pin Definition of USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	Comment
COEX_ UART_RX/ USB_BOOT	146	DI	Force the module to enter into emergency download mode	1.8V power domain. Active high. If unused, keep it open.

The following figure shows a reference circuit design of USB_BOOT interface.

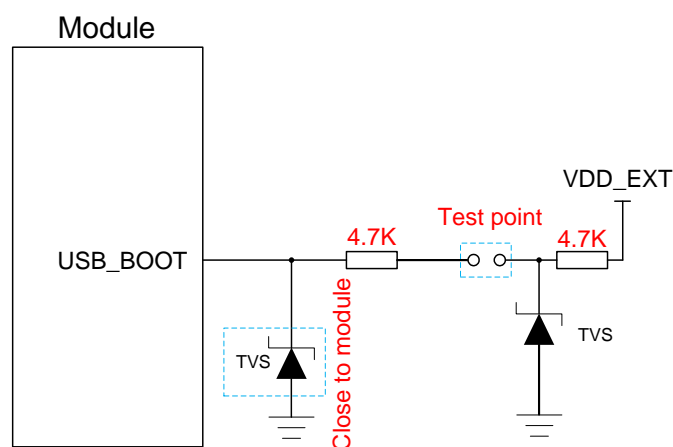


Figure 32: Reference Circuit of USB_BOOT Interface

3.22. RTC

AG35 has a real time clock within the PMIC, but has no dedicated RTC power supply pin.

The RTC is powered by VBAT_BB. If VBAT_BB is removed, the RTC will not be maintained.

NOTE

If RTC needs to be maintained, then VBAT_BB must be powered all the time.

3.23. HSIC Interface*

AG35 provides a HSIC interface for EAVB. HSIC is a 2-signal source synchronous serial interface which uses 240MHz DDR signaling to provide High-Speed 480Mbps USB transfers which are 100% host driver compatible with traditional USB cable-connected topologies. The HSIC interface supports the following features:

- High-Speed 480Mbps data rate only
- No power consumed unless a transfer in progress
- Signals driven at 1.2V standard LVCMOS levels.

The following table shows the pin definition of HSIC interface.

Table 30: Pin Definition of HSIC Interface

Pin Name	Pin No.	I/O	Description	Comment
HSIC_STROBE	194	IO	High speed inter chip interface - strobe	1.2V power domain.
HSIC_DATA	195	IO	High speed inter chip interface - data	If unused, keep them open.

The following table shows the layout guidelines of HSIC interface.

Table 31: Design Guidelines for HSIC

Designs	Guidelines
General	Data rate 480Mbps

	Impedance	45Ω ~ 55Ω
Length matching	Intra-pair match	< 2.5mm (15ps)
	Maximum trace length	8cm
Spacing	HSIC to all other signals	> 3 × line width
	HSIC_DATA to HSIC_STROBE	> 3 × line width

NOTES

1. “*” means under development.
2. More details will be provided in a future release of this document.

4 GNSS Receiver

4.1. General Description

AG35 includes a fully integrated global navigation satellite system solution that supports Gen8C-Lite of Qualcomm (GPS, GLONASS, BeiDou, Galileo and QZSS).

AG35 supports standard NMEA-0183 protocol, and outputs NMEA sentences at 1Hz data update rate via USB interface by default.

By default, AG35 GNSS engine is switched off. It has to be switched on with AT command. For more details about GNSS engine technology and configurations, please refer to **document [4]**.

4.2. GNSS Performance

The following table shows the GNSS performance of AG35.

Table 32: AG35-CE GNSS Performance

Parameter	Description	Conditions	Typ.	Unit
Sensitivity (GNSS)	Cold start	Autonomous	-146	dBm
	Reacquisition	Autonomous	-158	dBm
	Tracking	Autonomous	-162	dBm
TTFF (GNSS)	Cold start @open sky	Autonomous	35	s
		XTRA enabled	18	s
	Warm start @open sky	Autonomous	26	s
		XTRA enabled	2.2	s

	Hot start @open sky	Autonomous	2.5	s
		XTRA enabled	1.8	s
Accuracy (GNSS)	CEP-50	Autonomous @open sky	< 2.5	m

Table 33: AG35-E GNSS Performance

Parameter	Description	Conditions	Typ.	Unit
Sensitivity (GNSS)	Cold start	Autonomous	-146	dBm
	Reacquisition	Autonomous	-158	dBm
	Tracking	Autonomous	-162	dBm
TTFF (GNSS)	Cold start @open sky	Autonomous	35	s
		XTRA enabled	18	s
	Warm start @open sky	Autonomous	26	s
		XTRA enabled	2.2	s
	Hot start @open sky	Autonomous	2.5	s
		XTRA enabled	1.8	s
Accuracy (GNSS)	CEP-50	Autonomous @open sky	< 2.5	m

Table 34: AG35-NA GNSS Performance

Parameter	Description	Conditions	Typ.	Unit
Sensitivity (GNSS)	Cold start	Autonomous	-146	dBm
	Reacquisition	Autonomous	-158	dBm
	Tracking	Autonomous	-162	dBm
TTFF (GNSS)	Cold start @open sky	Autonomous	35	s
		XTRA enabled	18	s
	Warm start	Autonomous	26	s

	@open sky	XTRA enabled	2.2	s
	Hot start	Autonomous	2.5	s
	@open sky	XTRA enabled	1.8	s
Accuracy (GNSS)	CEP-50	Autonomous @open sky	< 2.5	m

Table 35: AG35-LA GNSS Performance

Parameter	Description	Conditions	Typ.	Unit
Sensitivity (GNSS)	Cold start	Autonomous	-146	dBm
	Reacquisition	Autonomous	-158	dBm
	Tracking	Autonomous	-162	dBm
TTFF (GNSS)	Cold start @open sky	Autonomous	35	s
		XTRA enabled	18	s
	Warm start @open sky	Autonomous	26	s
		XTRA enabled	2.2	s
	Hot start @open sky	Autonomous	2.5	s
		XTRA enabled	1.8	s
Accuracy (GNSS)	CEP-50	Autonomous @open sky	< 2.5	m

Table 36: AG35-J GNSS Performance

Parameter	Description	Conditions	Typ.	Unit
Sensitivity (GNSS)	Cold start	Autonomous	-146	dBm
	Reacquisition	Autonomous	-158	dBm
	Tracking	Autonomous	-162	dBm
TTFF (GNSS)	Cold start @open sky	Autonomous	35	s
		XTRA enabled	18	s

	Warm start @open sky	Autonomous	26	s
		XTRA enabled	2.2	s
	Hot start @open sky	Autonomous	2.5	s
		XTRA enabled	1.8	s
Accuracy (GNSS)	CEP-50	Autonomous @open sky	< 2.5	m

NOTES

1. Tracking sensitivity: the lowest GNSS signal value at the antenna port on which the module can keep on positioning for 3 minutes.
2. Reacquisition sensitivity: the lowest GNSS signal value at the antenna port on which the module can fix position again within 3 minutes after loss of lock.
3. Cold start sensitivity: the lowest GNSS signal value at the antenna port on which the module fixes position within 3 minutes after executing cold start command.

4.3. Layout Guidelines

The following layout guidelines should be taken into account in application design.

- Maximize the distance among GNSS antenna, main antenna and Rx-diversity antenna.
- Digital circuits such as (U)SIM card, USB interface, camera module, display connector and SD card should be kept away from the antennas.
- Use ground vias around the GNSS trace and sensitive analog signal traces to provide coplanar isolation and protection.
- Keep the characteristic impedance for ANT_GNSS trace as 50Ω.

Please refer to **Chapter 5** for GNSS antenna reference design and antenna installation information.

5 Antenna Interfaces

AG35 includes a main antenna interface, an Rx-diversity antenna interface which is used to resist the fall of signals caused by high speed movement and multipath effect, and a GNSS antenna interface. The antenna ports have an impedance of 50Ω.

5.1. Main/Rx-diversity Antenna Interface

5.1.1. Pin Definition

The pin definition of main antenna and Rx-diversity antenna interfaces are shown below.

Table 37: Pin Definition of RF Antenna Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	107	IO	Main antenna interface	50Ω impedance
ANT_DIV	127	AI	Receive diversity antenna interface	50Ω impedance

5.1.2. Operating Frequency

Table 38: AG35-CE Operating Frequencies

3GPP Band	Transmit	Receive	Unit
EGSM900	880~915	925~960	MHz
DCS1800	1710~1785	1805~1880	MHz
WCDMA B1	1920~1980	2110~2170	MHz
WCDMA B8	880~915	925~960	MHz
EVDO/CDMA BC0 ¹⁾	824~849	869~894	MHz
TD-SCDMA B34	2010~2025	2010~2025	MHz

TD-SCDMA B39	1880~1920	1880~1920	MHz
LTE-FDD B1	1920~1980	2110~2170	MHz
LTE-FDD B3	1710~1785	1805~1880	MHz
LTE-FDD B5	824~849	869~894	MHz
LTE-FDD B8	880~915	925~960	MHz
LTE-TDD B34	2010~2025	2010~2025	MHz
LTE-TDD B38	2570~2620	2570~2620	MHz
LTE-TDD B39	1880~1920	1880~1920	MHz
LTE-TDD B40	2300~2400	2300~2400	MHz
LTE-TDD B41	2555~2655	2555~2655	MHz

Table 39: AG35-E Operating Frequencies

3GPP Band	Transmit	Receive	Unit
EGSM900	880~915	925~960	MHz
DCS1800	1710~1785	1805~1880	MHz
WCDMA B1	1920~1980	2110~2170	MHz
WCDMA B5	824~849	869~894	MHz
WCDMA B8	880~915	925~960	MHz
LTE-FDD B1	1920~1980	2110~2170	MHz
LTE-FDD B3	1710~1785	1805~1880	MHz
LTE-FDD B5	824~849	869~894	MHz
LTE-FDD B7	2500~2570	2620~2690	MHz
LTE-FDD B8	880~915	925~960	MHz
LTE-FDD B20	832~862	791~821	MHz
LTE-FDD B28	703~748	758~803	MHz

LTE-TDD B38	2570~2620	2570~2620	MHz
LTE-TDD B40	2300~2400	2300~2400	MHz

Table 40: AG35-NA Operating Frequencies

3GPP Band	Transmit	Receive	Unit
GSM850	824~849	869~894	MHz
PCS1900	1850~1910	1930~1990	MHz
WCDMA B2	1850~1910	1930~1990	MHz
WCDMA B4	1710~1755	2110~2155	MHz
WCDMA B5	824~849	869~894	MHz
LTE-FDD B2	1850~1910	1930~1990	MHz
LTE-FDD B4	1710~1755	2110~2155	MHz
LTE-FDD B5	824~849	869~894	MHz
LTE-FDD B7	2500~2570	2620~2690	MHz
LTE-FDD B12	699~716	729~746	MHz
LTE-FDD B13	777~787	746~756	MHz
LTE-FDD B17	704~716	734~746	MHz

Table 41: AG35-LA Operating Frequencies

3GPP Band	Transmit	Receive	Unit
GSM850	824~849	869~894	MHz
EGSM900	880~915	925~960	MHz
DCS1800	1710~1785	1805~1880	MHz
PCS1900	1850~1910	1930~1990	MHz
WCDMA B1	1920~1980	2110~2170	MHz

WCDMA B2	1850~1910	1930~1990	MHz
WCDMA B3	1710~1785	1805~1880	MHz
WCDMA B4	1710~1755	2110~2155	MHz
WCDMA B5	824~849	869~894	MHz
WCDMA B8	880~915	925~960	MHz
LTE-FDD B1	1920~1980	2110~2170	MHz
LTE-FDD B2	1850~1910	1930~1990	MHz
LTE-FDD B3	1710~1785	1805~1880	MHz
LTE-FDD B4	1710~1755	2110~2155	MHz
LTE-FDD B5	824~849	869~894	MHz
LTE-FDD B7	2500~2570	2620~2690	MHz
LTE-FDD B8	880~915	925~960	MHz
LTE FDD B28	703~748	758~803	MHz

Table 42: AG35-J Operating Frequencies

3GPP Band	Transmit	Receive	Unit
WCDMA B1	1920~1980	2110~2170	MHz
WCDMA B3	1710~1785	1805~1880	MHz
WCDMA B5	824~849	869~894	MHz
WCDMA B6	830~840	875~885	MHz
WCDMA B8	880~915	925~960	MHz
WCDMA B19	830~845	875~890	MHz
LTE-FDD B1	1920~1980	2110~2170	MHz
LTE-FDD B3	1710~1785	1805~1880	MHz
LTE-FDD B5	824~848.9	869~893.9	MHz

LTE-FDD B8	880~915	925~960	MHz
LTE-FDD B9	1749.9~1784.8	1844.9~1879.8	MHz
LTE-FDD B19	830~845	875~890	MHz
LTE-FDD B21	1747.9~1462.8	1495.9~1510.8	MHz
LTE FDD B28	703~748	758~803	MHz
LTE TDD B41	2535~2655	2535~2655	MHz

NOTE

¹⁾ EVDO/CDMA BC0 for AG35-CE is optional.

5.1.3. Reference Design of RF Antenna Interfaces

A reference design of main and Rx-diversity antenna interfaces is shown as below. It is recommended to reserve a π -type matching circuit for better RF performance, and the π -type matching components (R1/C1/C2 and R2/C3/C4) should be placed as close to the antennas as possible. The capacitors are not mounted by default.

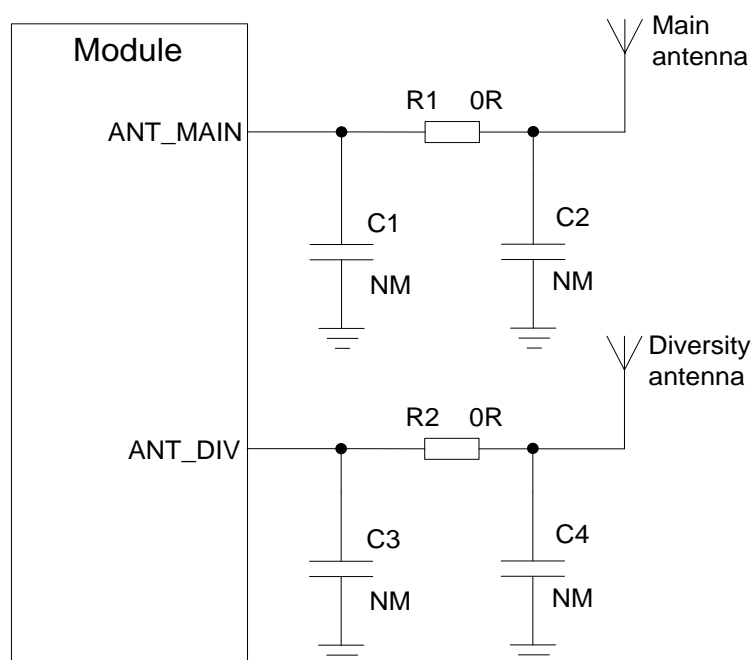


Figure 33: Reference Circuit of RF Antenna Interfaces

NOTES

1. Keep a proper distance between the main antenna and the Rx-diversity antenna to improve receiving sensitivity.
2. ANT_DIV function is enabled by default. **AT+QCFG="diversity",0** command can be used to disable receive diversity. Please refer to **document [2]** for details.

5.1.4. Reference Design of RF Layout

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, height from the reference ground to the signal layer (H), and the clearance between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

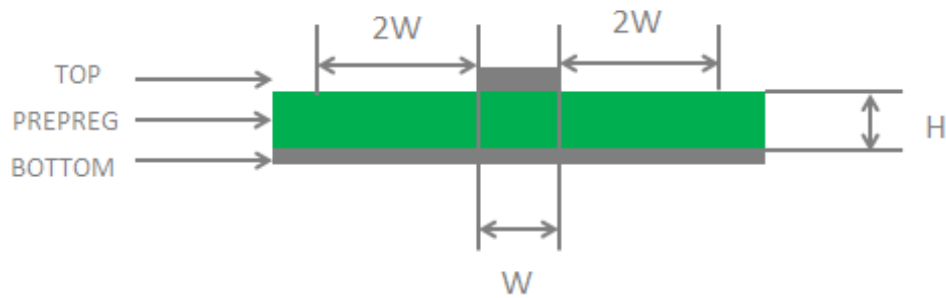


Figure 34: Microstrip Design on a 2-layer PCB

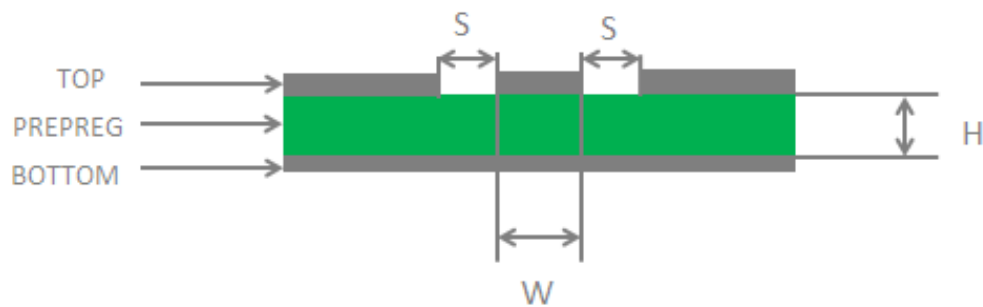


Figure 35: Coplanar Waveguide Design on a 2-layer PCB

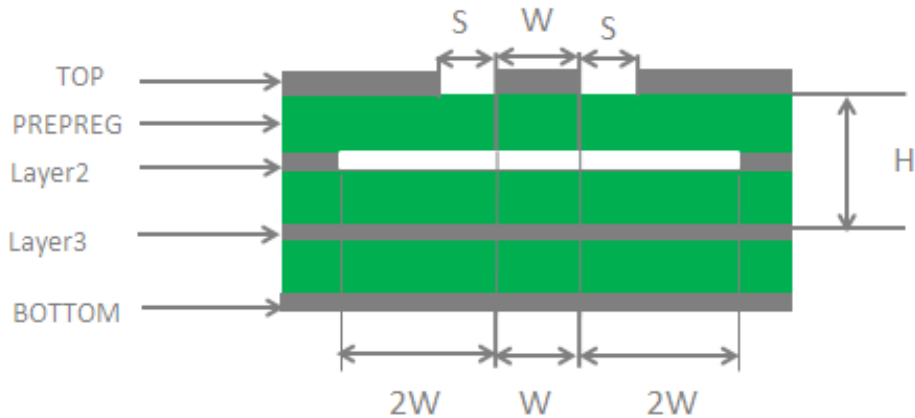


Figure 36: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

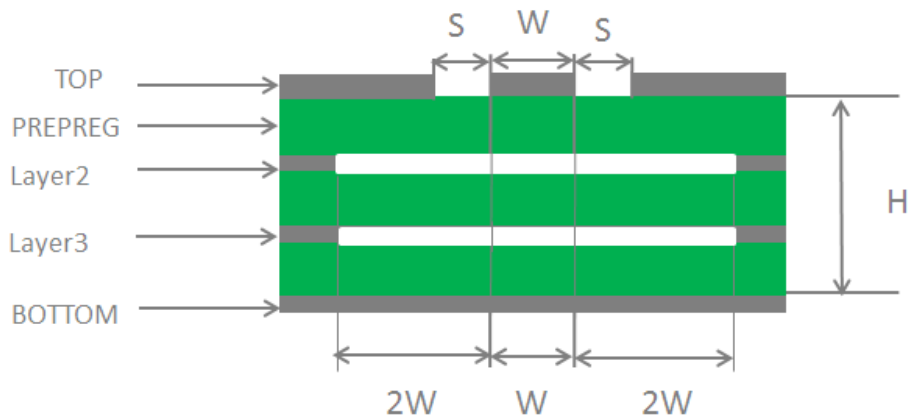


Figure 37: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

In order to ensure RF performance and reliability, the following principles should be complied with in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces as to 50Ω .
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible, and all the right-angle traces should be changed to curved ones.
- There should be clearance area under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be no less than two times as wide as the width of RF signal traces ($2*W$).

For more details about RF layout, please refer to **document [5]**.

5.2. GNSS Antenna Interface

The following tables show the pin definition and frequency specification of GNSS antenna interface.

Table 43: Pin Definition of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	119	AI	GNSS antenna interface	50Ω impedance

Table 44: GNSS Frequency

Type	Frequency	Unit
GPS	1575.42±1.023	MHz
GLONASS	1597.5~1605.8	MHz
Galileo	1575.42±2.046	MHz
BeiDou	1561.098±2.046	MHz
QZSS	1575.42	MHz

A reference design of GNSS antenna interface is shown as below.

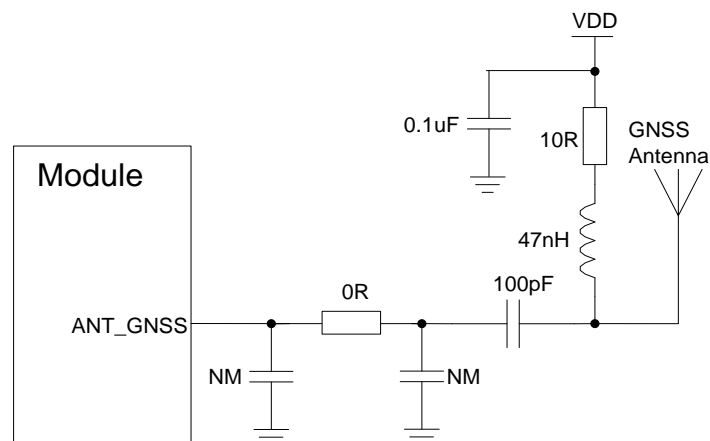


Figure 38: Reference Circuit of GNSS Antenna

NOTES

1. An external LDO can be selected to supply power according to the active antenna requirement.
2. If the module is designed with a passive antenna, then the VDD circuit is not needed.

5.3. Antenna Installation

5.3.1. Antenna Requirements

The following table shows the requirements on main antenna, Rx-diversity antenna and GNSS antenna.

Table 45: Antenna Requirements

Antenna Type	Requirements
GNSS ¹⁾	<p>Frequency range: 1559MHz~1609MHz</p> <p>Polarization: RHCP or linear</p> <p>VSWR: < 2 (Typ.)</p> <p>Passive antenna gain: > 0dBi</p> <p>Active antenna noise figure: < 1.5dB</p> <p>Active antenna gain: > 0dBi</p> <p>Active antenna embedded LNA gain: < 17dB</p>
GSM/EVDO/CDMA/UMTS/ TD-SCDMA/LTE	<p>VSWR: ≤ 2</p> <p>Efficiency: > 30%</p> <p>Max input power: 50W</p> <p>Input impedance: 50Ω</p> <p>Cable insertion loss: < 1dB</p> <p>(GSM850/EGSM900, WCDMA B5/B6/B8/B19, LTE-FDD B5/B8/B12/B13/B17/B19/B20/B28, EVDO/CDMA BC0)</p> <p>Cable insertion loss: < 1.5dB</p> <p>(DCS1800/PCS900, WCDMA B1/B2/B3/B4, LTE-FDD B1/B2/B3/B4/B9/B11/B21, LTE-TDD B34/B39, TD-SCDMA B34/B39)</p> <p>Cable insertion loss: < 2dB</p> <p>(LTE-FDD B7, LTE-TDD B38/B40/B41)</p>

NOTE

- ¹⁾ It is recommended to use a passive GNSS antenna when LTE B13 or B14 is supported, as the use of active antenna may generate harmonics which will affect the GNSS performance.

5.3.2. Recommended RF Connector for Antenna Installation

If RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT connector provided by *HIROSE*.

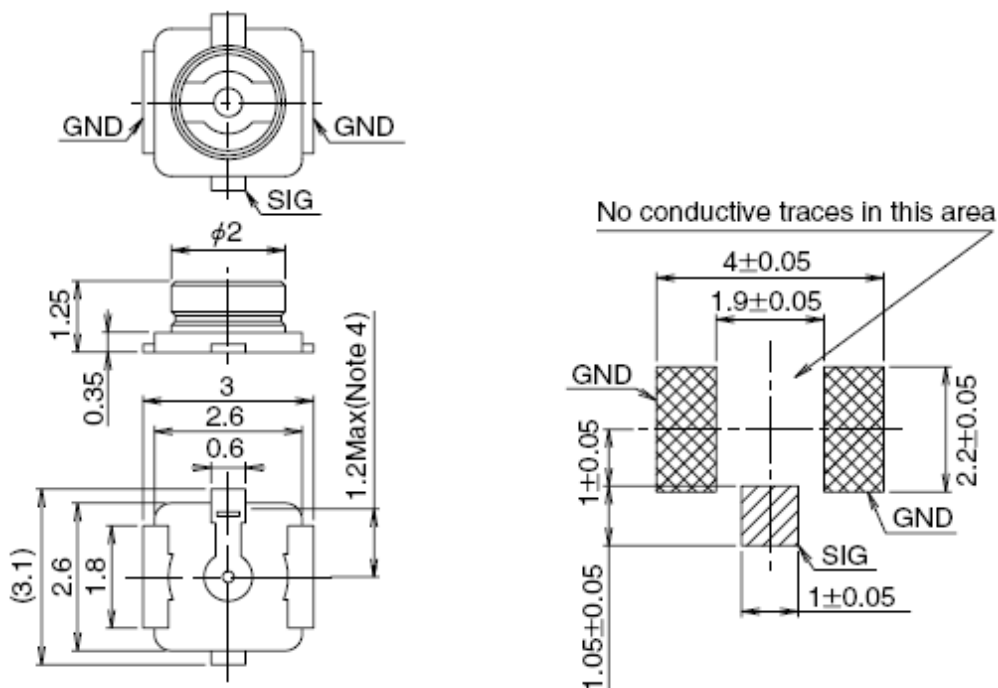


Figure 39: Dimensions of the U.FL-R-SMT Connector (Unit: mm)

U.FL-LP serial connectors listed in the following figure can be used to match the U.FL-R-SMT.

Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 40: Mechanicals of U.FL-LP Connectors

The following figure describes the space factor of mated connector.

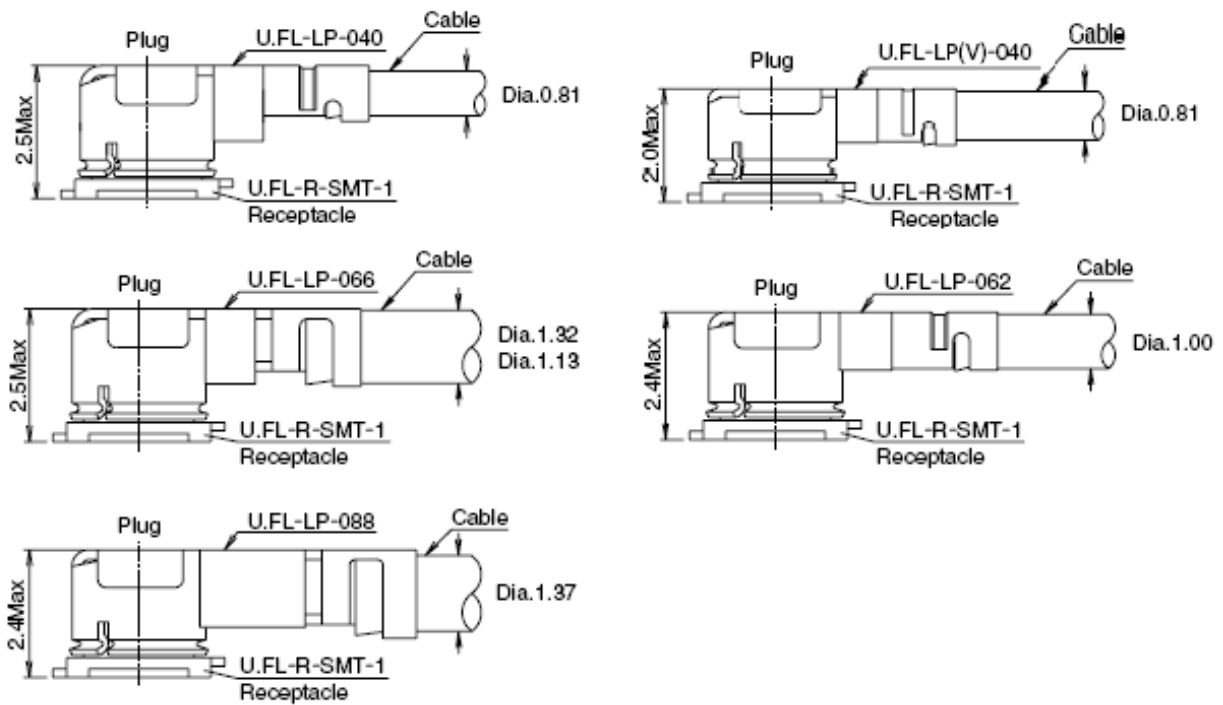


Figure 41: Space Factor of Mated Connector (Unit: mm)

For more details, please visit <https://www.hirose.com>.

6 Electrical, Reliability and Radio Characteristics

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 46: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_RF/VBAT_BB	-0.3	4.7	V
USB_VBUS	-0.3	5.5	V
Peak Current of VBAT_BB	0	0.8	A
Peak Current of VBAT_RF	0	1.8	A
Voltage at Digital Pins	-0.3	2.3	V
Voltage at ADC0	0.3	VBAT_BB	V
Voltage at ADC1	0.3	VBAT_BB	V
Voltage at ADC2	0.1	1.7	V

6.2. Power Supply Ratings

Table 47: Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltages must stay between the minimum and maximum values.	3.3	3.8	4.3	V
	Voltage drop during burst transmission	Maximum power control level on EGSM900.			400	mV
I _{VBAT}	Peak supply current (during transmission slot)	Maximum power control level on EGSM900.		1.8	2.0	A
USB_VBUS	USB connection detection		3.0	5.0	5.25	V

6.3. Operation and Storage Temperatures

Table 48: Operation and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operation Temperature Range ¹⁾	-35	25	+75	°C
Extended Temperature Range ²⁾	-40		+85	°C
eCall Temperature Range ³⁾	-40		+90	°C
Storage Temperature Range	-40		+95	°C

NOTES

- ¹⁾ Within operation temperature range, the module is 3GPP compliant, and emergency call can be dialed out with a maximum power and data rate.
- ²⁾ Within extended temperature range, the module remains fully functional and retains the ability to establish and maintain a voice, SMS, data transmission, emergency call, etc. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like P_{out} might reduce in their value and exceed the specified

tolerances. When the temperature returns to normal operation temperature levels, the module will meet 3GPP specifications again.

3. ³⁾ Within eCall temperature range, the emergency call function must be functional until the module is broken. When the ambient temperature is between 75°C and 90°C and the module temperature has reached the threshold value, the module will trigger protective measures (such as reduce power, decrease throughput, unregister the device, etc.) to ensure the full function of emergency call.

6.4. Current Consumption

Table 49: AG35-CE Current Consumption (25°C, 3.8V Power Supply)

Parameter	Description	Conditions	Typ.	Unit
I _{VBAT}	OFF state	Power down	20	uA
		AT+CFUN=0 (USB disconnected)	1.2	mA
		EGSM900 DRX=2 (USB disconnected)	2.3	mA
		EGSM900 DRX=5 (USB disconnected)	1.9	mA
		EGSM900 DRX=5 (USB suspend)	2.2	mA
		EGSM900 DRX=9 (USB disconnected)	1.6	mA
		DCS1800 DRX=2 (USB disconnected)	1.8	mA
		DCS1800 DRX=5 (USB disconnected)	1.4	mA
	Sleep state	DCS1800 DRX=5 (USB suspend)	1.8	mA
		DCS1800 DRX=9 (USB disconnected)	1.1	mA
		TD-SCDMA B34 DRX=6 (USB disconnected)	2.0	mA
		TD-SCDMA B34 DRX=6 (USB suspend)	2.1	mA
		TD-SCDMA B34 DRX=7 (USB disconnected)	1.8	mA
		TD-SCDMA B34 DRX=8 (USB disconnected)	1.6	mA
		TD-SCDMA B34 DRX=9 (USB disconnected)	1.5	mA

	WCDMA PF=64 (USB disconnected)	2.0	mA
	WCDMA PF=64 (USB suspend)	2.4	mA
	WCDMA PF=128 (USB disconnected)	1.8	mA
	WCDMA PF=256 (USB disconnected)	1.5	mA
	WCDMA PF=512 (USB disconnected)	1.4	mA
	BC0 SCI=1 (USB disconnected)	3.5	mA
	BC0 SCI=1 (USB suspend)	3.7	mA
	LTE-FDD PF=32 (USB disconnected)	3.8	mA
	LTE-FDD PF=64 (USB disconnected)	2.7	mA
	LTE-FDD PF=64 (USB suspend)	3.3	mA
	LTE-FDD PF=128 (USB disconnected)	2.2	mA
	LTE-FDD PF=256 (USB disconnected)	1.9	mA
	LTE-TDD PF=32 (USB disconnected)	3.8	mA
	LTE-TDD PF=64 (USB disconnected)	3.1	mA
	LTE-TDD PF=64 (USB suspend)	3.2	mA
	LTE-TDD PF=128 (USB disconnected)	2.4	mA
	LTE-TDD PF=256 (USB disconnected)	1.7	mA
Idle state	GSM DRX=5 (USB connected)	20.0	mA
	GSM DRX=5 (USB disconnected)	34.0	mA
	WCDMA PF=64 (USB connected)	35.0	mA
	WCDMA PF=64 (USB disconnected)	22.0	mA
	BC0 SCI=1 (USB disconnected)	22.0	mA
	BC0 SCI=1 (USB connected)	34.0	mA
	LTE-FDD PF=64 (USB connected)	35.0	mA
	LTE-FDD PF=64 (USB disconnected)	22.0	mA

	LTE-TDD PF=64 (USB connected)	35.0	mA
	LTE-TDD PF=64 (USB disconnected)	23.0	mA
GPRS data transfer (GNSS OFF)	EGSM900 4DL/1UL @32.66dBm	249.2	mA
	EGSM900 3DL/2UL @32.51dBm	421.6	mA
	EGSM900 2DL/3UL @30.65dBm	495.0	mA
	EGSM900 1DL/4UL @29.37dBm	568.9	mA
	DCS1800 4DL/1UL @29.21dBm	174.1	mA
	DCS1800 3DL/2UL @29.03dBm	276.1	mA
	DCS1800 2DL/3UL @28.95dBm	374.9	mA
	DCS1800 1DL/4UL @28.81dBm	476.8	mA
	EDGE data transfer (GNSS OFF)	EGSM900 4DL/1UL @27.02dBm	155.2
EGSM900 3DL/2UL @27.05dBm		256.9	mA
EGSM900 2DL/3UL @26.82dBm		350.0	mA
EGSM900 1DL/4UL @26.69dBm		446.0	mA
DCS1800 4DL/1UL @25.21dBm		146.0	mA
DCS1800 3DL/2UL @25.11dBm		226.7	mA
DCS1800 2DL/3UL @25.01dBm		312.0	mA
DCS1800 1DL/4UL @24.84dBm		401.6	mA
EVDO/CDMA data transfer (GNSS OFF)	BC0 ¹⁾ @23.71dBm	609.06	mA
TD-SCDMA data transfer (GNSS OFF)	B34 @22.73dBm	131.51	mA
	B39 @22.94dBm	132.77	mA
WCDMA data transfer (GNSS OFF)	WCDMA B1 HSDPA @21.95dBm	540.18	mA
	WCDMA B8 HSDPA @22.32dBm	481.27	mA
	WCDMA B1 HSUPA @21.52dBm	532.06	mA
	WCDMA B8 HSUPA @21.49dBm	466.51	mA

LTE data transfer (GNSS OFF)	LTE-FDD B1 @23.01dBm	698.07	mA
	LTE-FDD B3 @23.24dBm	708.78	mA
	LTE-FDD B5 @23.28dBm	629.16	mA
	LTE-FDD B8 @23.27dBm	597.21	mA
	LTE-TDD B34 @22.73dBm	334.99	mA
	LTE-TDD B38 @22.85dBm	430.39	mA
	LTE-TDD B39 @22.97dBm	330.62	mA
	LTE-TDD B40 @22.94dBm	405.78	mA
	LTE-TDD B41 @22.91dBm	456.63	mA
GSM voice call	EGSM900, PCL=5 @32.3dBm	230.4	mA
	EGSM900, PCL=12 @19.3dBm	103.2	mA
	EGSM900, PCL=19 @5.3dBm	73.0	mA
	DCS1800, PCL=0 @29.26dBm	155.5	mA
	DCS1800, PCL=7 @16.52dBm	117.3	mA
	DCS1800, PCL=15 @0.3dBm	97	mA
EVDO/CDMA voice call	BC0 ¹⁾ @23.78dBm	592.7	mA
	BC0 ¹⁾ @-60.55dBm	112.7	mA
WCDMA voice call	WCDMA B1 @23.15dBm	502.2	mA
	WCDMA B8 @23.24dBm	525.6	mA

Table 50: AG35-E Current Consumption

Parameter	Description	Conditions	Typ.	Unit
I _{BAT}	OFF state	Power down	20	uA
	Sleep state	AT+CFUN=0 (USB disconnected)	1.2	mA
		GSM DRX=2 (USB disconnected)	2.3	mA

	GSM DRX=5 (USB disconnected)	1.7	mA
	GSM DRX=5 (USB suspend)	1.9	mA
	GSM DRX=9 (USB disconnected)	1.6	mA
	WCDMA PF=64 (USB disconnected)	2.0	mA
	WCDMA PF=64 (USB suspend)	2.4	mA
	WCDMA PF=128 (USB disconnected)	1.7	mA
	WCDMA PF=256 (USB disconnected)	1.5	mA
	WCDMA PF=512 (USB disconnected)	1.4	mA
	LTE-FDD PF=32 (USB disconnected)	3.7	mA
	LTE-FDD PF=64 (USB disconnected)	2.5	mA
	LTE-FDD PF=64 (USB suspend)	2.8	mA
	LTE-FDD PF=128 (USB disconnected)	2.1	mA
	LTE-FDD PF=256 (USB disconnected)	1.8	mA
	LTE-TDD PF=32 (USB disconnected)	3.6	mA
	LTE-TDD PF=64 (USB disconnected)	2.5	mA
	LTE-TDD PF=64 (USB suspend)	2.7	mA
	LTE-TDD PF=128 (USB disconnected)	1.9	mA
	LTE-TDD PF=256 (USB disconnected)	1.7	mA
Idle state	GSM DRX=5 (USB connected)	17.5	mA
	GSM DRX=5(USB disconnected)	29.2	mA
	WCDMA PF=64 (USB connected)	29.4	mA
	WCDMA PF=64 (USB disconnected)	18.4	mA
	LTE-FDD PF=64 (USB connected)	28.3	mA
	LTE-FDD PF=64 (USB disconnected)	18.5	mA
	LTE-TDD PF=64 (USB connected)	29.5	mA

	LTE-TDD PF=64 (USB disconnected)	17.5	mA
GPRS data transfer (GNSS OFF)	EGSM900 4DL/1UL @33.02dBm	235	mA
	EGSM900 3DL/2UL @32.85dBm	405	mA
	EGSM900 2DL/3UL @30.4dBm	445	mA
	EGSM900 1DL/4UL @29.2dBm	515	mA
	DCS1800 4DL/1UL @29.7dBm	175	mA
	DCS1800 3DL/2UL @29.6dBm	275	mA
	DCS1800 2DL/3UL @29dBm	370	mA
	DCS1800 1DL/4UL @28dBm	440	mA
EDGE data transfer (GNSS OFF)	EGSM900 4DL/1UL @27.5dBm	158	mA
	EGSM900 3DL/2UL @27.5dBm	251	mA
	EGSM900 2DL/3UL @26.9dBm	331	mA
	EGSM900 1DL/4UL @25.3dBm	385	mA
	DCS1800 4DL/1UL @26.2dBm	150	mA
	DCS1800 3DL/2UL @26dBm	232	mA
	DCS1800 2DL/3UL @25dBm	307	mA
WCDMA data transfer (GNSS OFF)	DCS1800 1DL/4UL @24.6dBm	386	mA
	WCDMA B1 HSDPA @22.2dBm	552	mA
	WCDMA B5 HSDPA @22.8dBm	435	mA
	WCDMA B8 HSDPA @22.2dBm	495	mA
	WCDMA B1 HSUPA @21.9dBm	569	mA
	WCDMA B5 HSUPA @22.2dBm	432	mA
	WCDMA B8 HSUPA @22dBm	512	mA
LTE data transfer (GNSS OFF)	LTE-FDD B1 @23.5dBm	730	mA
	LTE-FDD B3 @23.8dBm	750	mA

		LTE-FDD B5 @23.18dBm	530	mA
		LTE-FDD B7 @23.7dBm	710	mA
		LTE-FDD B8 @23.6dBm	600	mA
		LTE-FDD B20 @23.8dBm	600	mA
		LTE-FDD B28A @23.3dBm	780	mA
		LTE-FDD B28B @23.5dBm	700	mA
		LTE-TDD B38 @23.3dBm	385	mA
		LTE-TDD B40 @22.95dBm	370	mA
	GSM voice call	EGSM900 @PCL=5	246	mA
		EGSM900 @PCL=12	116	mA
		EGSM900 @PCL=19	88	mA
		DCS1800 @PCL=0	177	mA
		DCS1800 @PCL=7	128	mA
		DCS1800 @PCL=15	109	mA
WCDMA voice call		WCDMA B1 (max power) @23.07dBm	640	mA
		WCDMA B5 (max power) @23.24dBm	450	mA
		WCDMA B8 (max power) @23.1dBm	550	mA

Table 51: AG35-NA Current Consumption

Parameter	Description	Conditions	Typ.	Unit
I _{BAT}	OFF state	Power down	20	uA
		AT+CFUN=0 (USB disconnected)	1.2	mA
	Sleep state	GSM DRX=2 (USB disconnected)	2.3	mA
		GSM DRX=5 (USB disconnected)	2.0	mA
		GSM DRX=5 (USB suspend)	2.3	mA

	GSM DRX=9 (USB disconnected)	1.7	mA
	WCDMA PF=64 (USB disconnected)	2.2	mA
	WCDMA PF=64 (USB suspend)	2.5	mA
	WCDMA PF=128 (USB disconnected)	1.8	mA
	WCDMA PF=256 (USB disconnected)	1.6	mA
	WCDMA PF=512 (USB disconnected)	1.5	mA
	LTE-FDD PF=32 (USB disconnected)	3.6	mA
	LTE-FDD PF=64 (USB disconnected)	2.6	mA
	LTE-FDD PF=64 (USB suspend)	2.8	mA
	LTE-FDD PF=128 (USB disconnected)	2.0	mA
	LTE-FDD PF=256 (USB disconnected)	1.7	mA
Idle state	GSM DRX=5 (USB disconnected)	14.0	mA
	GSM DRX=5 (USB connected)	25.0	mA
	WCDMA PF=64 (USB connected)	31.0	mA
	WCDMA PF=64 (USB disconnected)	19.0	mA
	LTE-FDD PF=64 (USB connected)	31.0	mA
	LTE-FDD PF=64 (USB disconnected)	19.0	mA
GPRS data transfer (GNSS OFF)	GSM850 4DL/1UL @32.66dBm	256	mA
	GSM850 3DL/2UL @32.51dBm	425	mA
	GSM850 2DL/3UL @30.65dBm	510	mA
	GSM850 1DL/4UL @29.37dBm	580	mA
	PCS1900 4DL/1UL @29.21dBm	185	mA
	PCS1900 3DL/2UL @29.03dBm	296	mA
	PCS1900 2DL/3UL @28.95dBm	390	mA
	PCS1900 1DL/4UL @28.81dBm	480	mA

EDGE data transfer (GNSS OFF)	GSM850 4DL/1UL @27.02dBm	160	mA
	GSM850 3DL/2UL @27.05dBm	265	mA
	GSM850 2DL/3UL @26.82dBm	355	mA
	GSM850 1DL/4UL @26.69dBm	456	mA
	PCS1900 4DL/1UL @25.21dBm	155	mA
	PCS1900 3DL/2UL @25.11dBm	230	mA
	PCS1900 2DL/3UL @25.01dBm	320	mA
	PCS1900 1DL/4UL @24.84dBm	410	mA
WCDMA data transfer (GNSS OFF)	WCDMA B2 HSDPA (max power) @22.32dBm	560	mA
	WCDMA B4 HSDPA (max power) @22.32dBm	570	mA
	WCDMA B5 HSDPA (max power) @22.48dBm	560	mA
	WCDMA B2 HSUPA (max power) @22.09dBm	520	mA
	WCDMA B4 HSUPA (max power) @22.32dBm	560	mA
	WCDMA B5 HSUPA (max power) @22.28dBm	550	mA
LTE data transfer (GNSS OFF)	LTE-FDD B2 (max power) @22.85dBm	650	mA
	LTE-FDD B4 (max power) @23.08dBm	640	mA
	LTE-FDD B5 (max power) @23.18dBm	650	mA
	LTE-FDD B7 (max power) @23dBm	710	mA
	LTE-FDD B12 (max power) @23dBm	660	mA
	LTE-FDD B13 (max power) @23.19dBm	650	mA
	LTE-FDD B17 (max power) @23.2dBm	670	mA
GSM voice call	GSM850 @PCL=5	80	mA
	GSM850 @PCL=12	190	mA
	GSM850 @PCL=19	110	mA

	PCS1900 @PCL=0	90	mA
	PCS1900 @PCL=7	590	mA
	PCS1900 @PCL=15	595	mA
WCDMA voice call	WCDMA B2 (max power) @22.96dBm	580	mA
	WCDMA B4 (max power) @22.96dBm	560	mA
	WCDMA B5 (max power) @23.15dBm	570	mA

Table 52: AG35-LA Current Consumption

Parameter	Description	Conditions	Typ.	Unit
I _{BAT}	OFF state	Power down	10	uA
	Sleep state	AT+CFUN=0 (USB disconnected)	1.0	mA
		GSM DRX=2 (USB disconnected)	1.9	mA
		GSM DRX=5 (USB disconnected)	1.5	mA
		GSM DRX=9 (USB disconnected)	1.3	mA
		WCDMA PF=64 (USB disconnected)	2.0	mA
		WCDMA PF=128 (USB disconnected)	1.6	mA
		WCDMA PF=256 (USB disconnected)	1.5	mA
		WCDMA PF=512 (USB disconnected)	1.4	mA
		LTE-FDD PF=32 (USB disconnected)	3.4	mA
		LTE-FDD PF=64 (USB disconnected)	2.3	mA
		LTE-FDD PF=128 (USB disconnected)	1.8	mA
		LTE-FDD PF=256 (USB disconnected)	1.6	mA
	Idle state	GSM DRX=5 (USB connected)	30	mA
		GSM DRX=5 (USB disconnected)	20	mA
		WCDMA PF=64 (USB connected)	30	mA

GPRS data transfer (GNSS OFF)	WCDMA PF=64 (USB disconnected)	20	mA
	LTE-FDD PF=64 (USB connected)	31	mA
	LTE-FDD PF=64 (USB disconnected)	21	mA
	GSM850 4DL/1UL @32.62dBm	228	mA
	GSM850 3DL/2UL @32.0dBm	369	mA
	GSM850 2DL/3UL @30.12dBm	435	mA
	GSM850 1DL/4UL @29.38dBm	527	mA
	EGSM900 4DL/1UL @32.96dBm	241	mA
	EGSM900 3DL/2UL @32.51dBm	364	mA
	EGSM900 2DL/3UL @30.55dBm	459	mA
	EGSM900 1DL/4UL @29.77dBm	558	mA
	DCS1800 4DL/1UL @29.52dBm	177	mA
	DCS1800 3DL/2UL @29.28dBm	283	mA
	DCS1800 2DL/3UL @28.15dBm	353	mA
	DCS1800 1DL/4UL @27.32dBm	432	mA
	PCS1900 4DL/1UL @30.05dBm	177	mA
	PCS1900 3DL/2UL @29.02dBm	263	mA
	PCS1900 2DL/3UL @26.84dBm	317	mA
	PCS1900 1DL/4UL @26.01dBm	384	mA
EDGE data transfer (GNSS OFF)	GSM850 4DL/1UL @26.3dBm	139	mA
	GSM850 3DL/2UL @25.52dBm	217	mA
	GSM850 2DL/3UL @23.45dBm	266	mA
	GSM850 1DL/4UL @22.86dBm	332	mA
	EGSM900 4DL/1UL @26.67dBm	148	mA
	EGSM900 3DL/2UL @25.33dBm	219	mA

	EGSM900 2DL/3UL @23.71dBm	274	mA
	EGSM900 1DL/4UL @22.85dBm	333	mA
	DCS1800 4DL/1UL @25.86dBm	147	mA
	DCS1800 3DL/2UL @25.24dBm	226	mA
	DCS1800 2DL/3UL @23.54dBm	293	mA
	DCS1800 1DL/4UL @22.56dBm	367	mA
	PCS1900 4DL/1UL @25.41dBm	138	mA
	PCS1900 3DL/2UL @25.21dBm	220	mA
	PCS1900 2DL/3UL @23.28dBm	286	mA
	PCS1900 1DL/4UL @22.21dBm	359	mA
WCDMA data transfer (GNSS OFF)	WCDMA B1 HSDPA @22.56dBm	517	mA
	WCDMA B2 HSDPA @22.62dBm	489	mA
	WCDMA B3 HSDPA @22.43dBm	539	mA
	WCDMA B4 HSDPA @22.49dBm	558	mA
	WCDMA B5 HSDPA @23.32dBm	481	mA
	WCDMA B8 HSDPA @22.69dBm	523	mA
	WCDMA B1 HSUPA @22.47dBm	525	mA
	WCDMA B2 HSUPA @22.57dBm	505	mA
	WCDMA B3 HSUPA @21.85dBm	525	mA
	WCDMA B4 HSUPA @22.0dBm	579	mA
LTE data transfer (GNSS OFF)	WCDMA B5 HSUPA @22.51dBm	471	mA
	WCDMA B8 HSUPA @22.45dBm	527	mA
	LTE-FDD B1 @23.1dBm	632	mA
	LTE-FDD B2 @23.5dBm	632	mA
	LTE-FDD B3 @23.24dBm	692	mA

	LTE-FDD B4 @23.5dBm	675	mA
	LTE-FDD B5 @23.55dBm	555	mA
	LTE-FDD B7 @23.61dBm	654	mA
	LTE-FDD B8 @23.59dBm	629	mA
	LTE-FDD B28A @23.5dBm	709	mA
	LTE-FDD B28B @23.64dBm	722	mA
GSM voice call	GSM850 @PCL=5	236	mA
	GSM850 @PCL=12	112	mA
	GSM850 @PCL=19	87	mA
	EGSM900 @PCL=5	243	mA
	EGSM900 @PCL=12	115	mA
	EGSM900 @PCL=19	88	mA
	DCS1800 @PCL=0	180	mA
	DCS1800 @PCL=7	128	mA
	DCS1800 @PCL=15	109	mA
	PCS1900 @PCL=0	182	mA
	PCS1900 @PCL=7	128	mA
	PCS1900 @PCL=15	108	mA
WCDMA voice call	WCDMA B1 (max power) @23.2dBm	559	mA
	WCDMA B2 (max power) @23.21dBm	536	mA
	WCDMA B3 (max power) @23.06dBm	593	mA
	WCDMA B4 (max power) @23.15dBm	593	mA
	WCDMA B5 (max power) @23.42dBm	493	mA
	WCDMA B8 (max power) @23.34dBm	570	mA

Table 53: AG35-J Current Consumption

Parameter	Description	Conditions	Typ.	Unit
I _{VBAT}	OFF state	Power down	20	uA
		AT+CFUN=0 (USB disconnected)	1.1	mA
	Sleep state	WCDMA PF=64 (USB disconnected)	1.9	mA
		WCDMA PF=64 (USB suspend)	2.2	mA
		WCDMA PF=128 (USB disconnected)	1.6	mA
		WCDMA PF=256 (USB disconnected)	1.4	mA
		WCDMA PF=512 (USB disconnected)	1.3	mA
		LTE-FDD PF=32 (USB disconnected)	3.4	mA
		LTE-FDD PF=64 (USB disconnected)	2.3	mA
		LTE-FDD PF=64 (USB suspend)	2.6	mA
		LTE-FDD PF=128 (USB disconnected)	1.8	mA
		LTE-FDD PF=256 (USB disconnected)	1.5	mA
		LTE-TDD PF=32 (USB disconnected)	3.5	mA
		LTE-TDD PF=64 (USB disconnected)	2.4	mA
		LTE-TDD PF=64 (USB suspend)	2.7	mA
		LTE-TDD PF=128 (USB disconnected)	1.9	mA
		LTE-TDD PF=256 (USB disconnected)	1.6	mA
	Idle state	WCDMA PF=64 (USB connected)	29	mA
		WCDMA PF=64 (USB disconnected)	19	mA
		LTE-FDD PF=64 (USB connected)	30	mA
		LTE-FDD PF=64 (USB disconnected)	19	mA
		LTE-TDD PF=64 (USB connected)	29	mA
		LTE-TDD PF=64 (USB disconnected)	19	mA

WCDMA data transfer (GNSS OFF)	WCDMA B1 HSDPA @22.32dBm	550	mA
	WCDMA B3 HSDPA @22.32dBm	590	mA
	WCDMA B5 HSDPA @22.32dBm	530	mA
	WCDMA B6 HSDPA @22.32dBm	536	mA
	WCDMA B8 HSDPA @22.48dBm	580	mA
	WCDMA B19 HSDPA @22.32dBm	550	mA
	WCDMA B1 HSUPA @22.09dBm	565	mA
	WCDMA B3 HSUPA @22.09dBm	596	mA
	WCDMA B5 HSUPA @22.32dBm	550	mA
	WCDMA B6 HSUPA @22.28dBm	545	mA
	WCDMA B8 HSUPA @22.28dBm	578	mA
	WCDMA B19 HSUPA @22.28dBm	565	mA
LTE data transfer (GNSS OFF)	LTE-FDD B1 @22.85dBm	660	mA
	LTE-FDD B3 @23.08dBm	680	mA
	LTE-FDD B5 @23.08dBm	670	mA
	LTE-FDD B8 @23.18dBm	630	mA
	LTE-FDD B9 @23dBm	629	mA
	LTE-FDD B19 @23.19dBm	645	mA
	LTE-FDD B21 @23dBm	600	mA
	LTE-FDD B28 @23dBm	700	mA
	LTE-TDD B41 @23dBm	430	mA
WCDMA voice call	WCDMA B1 (max power) @22.96dBm	590	mA
	WCDMA B3 (max power) @22.96dBm	630	mA
	WCDMA B5 (max power) @22.96dBm	600	mA
	WCDMA B6 (max power) @22.96dBm	596	mA

WCDMA B8 (max power) @22.96dBm	598	mA
WCDMA B19 (max power) @23.15dBm	590	mA

Table 54: AG35-CE GNSS Current Consumption

Parameter	Description	Conditions	Typ.	Unit
I _{VBAT} (GNSS)	Searching (AT+CFUN=0)	Cold Start @Passive Antenna	47.5	mA
		Hot Start @Passive Antenna	45.2	mA
		Lost State @Passive Antenna	44.1	mA
	Tracking (AT+CFUN=0)	Open Sky @Passive Antenna	28.8	mA

Table 55: AG35-E GNSS Current Consumption

Parameter	Description	Conditions	Typ.	Unit
I _{VBAT} (GNSS)	Searching (AT+CFUN=0)	Cold Start @Passive Antenna	45.5	mA
		Hot Start @Passive Antenna	45.6	mA
		Lost State @Passive Antenna	46.1	mA
	Tracking (AT+CFUN=0)	Open Sky @Passive Antenna	28.7	mA

Table 56: AG35-NA GNSS Current Consumption

Parameter	Description	Conditions	Typ.	Unit
I _{VBAT} (GNSS)	Searching (AT+CFUN=0)	Cold Start @Passive Antenna	47.9	mA
		Hot Start @Passive Antenna	51.5	mA
		Lost State @Passive Antenna	46.1	mA
	Tracking (AT+CFUN=0)	Open Sky @Passive Antenna	25.2	mA

Table 57: AG35-LA GNSS Current Consumption

Parameter	Description	Conditions	Typ.	Unit
I _V BAT (GNSS)	Searching (AT+CFUN=0)	Cold Start @Passive Antenna	46.8	mA
		Hot Start @Passive Antenna	47.1	mA
		Lost State @Passive Antenna	47.1	mA
	Tracking (AT+CFUN=0)	Open Sky @Passive Antenna	32.3	mA

Table 58: AG35-J GNSS Current Consumption

Parameter	Description	Conditions	Typ.	Unit
I _V BAT (GNSS)	Searching (AT+CFUN=0)	Cold Start @Passive Antenna	46.1	mA
		Hot Start @Passive Antenna	45.1	mA
		Lost State @Passive Antenna	45.2	mA
	Tracking (AT+CFUN=0)	Open Sky @Passive Antenna	31.9	mA

NOTE

¹⁾ EVDO/CDMA BC0 for AG35-CE is optional.

6.5. RF Output Power

The following table shows the RF output power of AG35 module.

Table 59: AG35-CE RF Output Power

Frequency	Max.	Min.
EGSM900	33dBm±2dB	5dBm±5dB
DCS1800	30dBm±2dB	0dBm±5dB
WCDMA B1	24dBm+1/-3dB	<-49dBm

WCDMA B8	24dBm+1/-3dB	<-49dBm
EVDO/CDMA BC0 ¹⁾	24dBm+2/-1dB	<-49dBm
TD-SCDMA B34	24dBm+1/-3dB	<-49dBm
TD-SCDMA B39	24dBm+1/-3dB	<-49dBm
LTE-FDD B1	23dBm±2dB	<-39dBm
LTE-FDD B3	23dBm±2dB	<-39dBm
LTE-FDD B5	23dBm±2dB	<-39dBm
LTE-FDD B8	23dBm±2dB	<-39dBm
LTE-TDD B34	23dBm±2dB	<-39dBm
LTE-TDD B38	23dBm±2dB	<-39dBm
LTE-TDD B39	23dBm±2dB	<-39dBm
LTE-TDD B40	23dBm±2dB	<-39dBm
LTE-TDD B41	23dBm±2dB	<-39dBm

Table 60: AG35-E RF Output Power

Frequency	Max.	Min.
EGSM900	33dBm±2dB	5dBm±5dB
DCS1800	30dBm±2dB	0dBm±5dB
WCDMA B1	24dBm+1/-3dB	<-49dBm
WCDMA B5	24dBm+1/-3dB	<-49dBm
WCDMA B8	24dBm+1/-3dB	<-49dBm
LTE-FDD B1	23dBm±2dB	<-39dBm
LTE-FDD B3	23dBm±2dB	<-39dBm
LTE-FDD B5	23dBm±2dB	<-39dBm
LTE-FDD B7	23dBm±2dB	<-39dBm

LTE-FDD B8	23dBm±2dB	<-39dBm
LTE-FDD B20	23dBm±2dB	<-39dBm
LTE-FDD B28	23dBm±2dB	<-39dBm
LTE-TDD B38	23dBm±2dB	<-39dBm
LTE-TDD B40	23dBm±2dB	<-39dBm

Table 61: AG35-NA RF Output Power

Frequency	Max.	Min.
GSM850	33dBm±2dB	5dBm±5dB
PCS1900	30dBm±2dB	0dBm±5dB
WCDMA B2	24dBm+1/-3dB	<-49dBm
WCDMA B4	24dBm+1/-3dB	<-49dBm
WCDMA B5	24dBm+1/-3dB	<-49dBm
LTE-FDD B2	23dBm±2dB	<-39dBm
LTE-FDD B4	23dBm±2dB	<-39dBm
LTE-FDD B5	23dBm±2dB	<-39dBm
LTE-FDD B7	23dBm±2dB	<-39dBm
LTE-FDD B12	23dBm±2dB	<-39dBm
LTE-FDD B13	23dBm±2dB	<-39dBm
LTE-FDD B17	23dBm±2dB	<-39dBm

Table 62: AG35-LA RF Output Power

Frequency	Max.	Min.
GSM850	33dBm±2dB	5dBm±5dB
EGSM900	33dBm±2dB	5dBm±5dB

DCS1800	30dBm±2dB	0dBm±5dB
PCS1900	30dBm±2dB	0dBm±5dB
WCDMA B1	24dBm+1/-3dB	<-49dBm
WCDMA B2	24dBm+1/-3dB	<-49dBm
WCDMA B3	24dBm+1/-3dB	<-49dBm
WCDMA B4	24dBm+1/-3dB	<-49dBm
WCDMA B5	24dBm+1/-3dB	<-49dBm
WCDMA B8	24dBm+1/-3dB	<-49dBm
LTE-FDD B1	23dBm±2dB	<-39dBm
LTE-FDD B2	23dBm±2dB	<-39dBm
LTE-FDD B3	23dBm±2dB	<-39dBm
LTE-FDD B4	23dBm±2dB	<-39dBm
LTE-FDD B5	23dBm±2dB	<-39dBm
LTE-FDD B7	23dBm±2dB	<-39dBm
LTE-FDD B8	23dBm±2dB	<-39dBm
LTE-FDD B28	23dBm±2dB	<-39dBm

Table 63: AG35-J RF Output Power

Frequency	Max.	Min.
WCDMA B1	24dBm+1/-3dB	<-49dBm
WCDMA B3	24dBm+1/-3dB	<-49dBm
WCDMA B5	24dBm+1/-3dB	<-49dBm
WCDMA B6	24dBm+1/-3dB	<-49dBm
WCDMA B8	24dBm+1/-3dB	<-49dBm
WCDMA B19	24dBm+1/-3dB	<-49dBm

LTE-FDD B1	23dBm±2dB	<-39dBm
LTE-FDD B3	23dBm±2dB	<-39dBm
LTE-FDD B5	23dBm±2dB	<-39dBm
LTE-FDD B8	23dBm±2dB	<-39dBm
LTE-FDD B9	23dBm±2dB	<-39dBm
LTE-FDD B19	23dBm±2dB	<-39dBm
LTE-FDD B21	23dBm±2dB	<-39dBm
LTE-FDD B28	23dBm±2dB	<-39dBm
LTE-TDD B41	23dBm±2dB	<-39dBm

NOTES

- ¹⁾ EVDO/CDMA BC0 for AG35-CE is optional.
- In GPRS 4 slots TX mode, the max output power is reduced by 3.0dB. This design conforms to the GSM specification as described in **Chapter 13.16** of 3GPP TS 51.010-1.

6.6. RF Receiving Sensitivity

Table 64: AG35-CE RF Receiving Sensitivity

Frequency	Receive Sensitivity (Typ.) (Unit: dBm)			
	Primary	Diversity	SIMO	3GPP (SIMO)
EGSM900	-109	/	/	-102
DCS1800	-109	/	/	-102
WCDMA B1	-109	-110	-112	-106.7
WCDMA B8	-110	-110	-112.5	-103.7
EVDO/CDMA BC0 ¹⁾	-109	/	/	-104
TD-SCDMA B34	-109	/	/	-108
TD-SCDMA B39	-110	/	/	-108

LTE-FDD B1 (10M)	-98	-99	-102	-96.3
LTE-FDD B3 (10M)	-98.6	-99	-102	-93.3
LTE-FDD B5 (10M)	-98.5	-100	-102.5	-94.3
LTE-FDD B8 (10M)	-98.5	-100	-102.5	-93.3
LTE-TDD B34 (10M)	-98.1	-99	-101.7	-96.3
LTE-TDD B38 (10M)	-98.5	-98	-101	-94.3
LTE-TDD B39 (10M)	-98.4	-99	-102	-96.3
LTE-TDD B40 (10M)	-98.3	-99	-101.5	-96.3
LTE-TDD B41 (10M)	-97.6	-98	-100.5	-94.3

Table 65: AG35-E RF Receiving Sensitivity

Frequency	Receive Sensitivity (Typ.) (Unit: dBm)			
	Primary	Diversity	SIMO	3GPP (SIMO)
EGSM900	-108.5	/	/	-102
DCS1800	-108.7	/	/	-102
WCDMA B1	-110	-110	-112	-106.7
WCDMA B5	-110.5	-111	-112.5	-104.7
WCDMA B8	-110	-110.5	-112	-103.7
LTE-FDD B1 (10M)	-98.1	-99	-101.5	-96.3
LTE-FDD B3 (10M)	-98.5	-99	-101.7	-93.3
LTE-FDD B5 (10M)	-99.5	-100.5	-102.5	-94.3
LTE-FDD B7 (10M)	-97	-99	-101.1	-94.3
LTE-FDD B8 (10M)	-98.5	-99.8	-101.7	-93.3
LTE-FDD B20 (10M)	-98.2	-99.2	-101.5	-93.3
LTE-FDD B28 (10M)	-98.5	-99.2	-101.8	-94.8
LTE-TDD B38 (10M)	-96.5	-98.6	-100.8	-94.3

LTE-TDD B40 (10M)	-98	-98.3	-101.3	-96.3
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Table 66: AG35-NA RF Receiving Sensitivity

Frequency	Receive Sensitivity (Typ.) (Unit: dBm)			
	Primary	Diversity	SIMO	3GPP (SIMO)
GSM850	-108.5	NA	NA	-102
PCS1900	-108.2	NA	NA	-102
WCDMA B2	-109.5	-110.2	-110.4	-104.7
WCDMA B4	-109.8	-109.5	-110.9	-106.7
WCDMA B5	-110	-109.5	-110.8	-104.7
LTE-FDD B2 (10M)	-98	-98.5	-100.6	-94.3
LTE-FDD B4 (10M)	-97.9	-98.2	-100.3	-96.3
LTE-FDD B5 (10M)	-98.5	-99	-100.8	-94.3
LTE-FDD B7 (10M)	-97.3	-97.6	-99.9	-94.3
LTE-FDD B12 (10M)	-98.5	-99	-99.9	-93.3
LTE-FDD B13 (10M)	-98	-99.6	-100	-93.3
LTE-FDD B17 (10M)	-98.3	-98.5	-100.3	-93.3

Table 67: AG35-LA RF Receiving Sensitivity

Frequency	Receive Sensitivity (Typ.) (Unit: dBm)			
	Primary	Diversity	SIMO	3GPP (SIMO)
GSM850	-109.5	/	/	-102
EGSM900	-108.5	/	/	-102
DCS1800	-108.5	/	/	-102
PCS1900	-108.5	/	/	-102
WCDMA B1	-110	-111	-112	-106.7
WCDMA B2	-110	-111	-112	-104.7

WCDMA B3	-109	-110	-111	-103.7
WCDMA B4	-109.5	-110	-111	-106.7
WCDMA B5	-110	-111.5	-112	-104.7
WCDMA B8	-109.5	-111	-111.5	-103.7
LTE-FDD B1 (10M)	-98.2	-99.1	-101.8	-96.3
LTE-FDD B2 (10M)	-98.6	-99.8	-102.4	-94.3
LTE-FDD B3 (10M)	-98.6	-98.9	-102	-93.3
LTE-FDD B4 (10M)	-97.4	-99	-101.3	-96.3
LTE-FDD B5 (10M)	-99.2	-100.2	-102.5	-94.3
LTE-FDD B7 (10M)	-97.4	-98.4	-101	-94.3
LTE-FDD B8 (10M)	-98.3	-99.7	-102.3	-93.3
LTE-FDD B28 (10M)	-98.3	-98.7	-101.8	-94.8

Table 68: AG35-J RF Receiving Sensitivity

Frequency	Receive Sensitivity (Typ.) (Unit: dBm)			
	Primary	Diversity	SIMO	3GPP (SIMO)
WCDMA B1	-109	-109.8	-110.2	-106.7
WCDMA B3	-110	-109.5	-110.3	-103.7
WCDMA B5	-109.6	-109.5	-110.6	-104.7
WCDMA B6	-109.2	-109.8	-110.3	-106.7
WCDMA B8	-110	-109.9	-110.9	-103.7
WCDMA B19	-109.8	-109.7	-110.3	-106.7
LTE-FDD B1 (10M)	-97.8	-98.2	-99.8	-96.3
LTE-FDD B3 (10M)	-97.2	-98.5	-99.3	-93.3
LTE-FDD B5 (10M)	-98.2	-98	-99.9	-94.3
LTE-FDD B8 (10M)	-98.5	-98.6	-100	-93.3

LTE-FDD B9 (10M)	-98.2	-98	-100	-95.3
LTE-FDD B19 (10M)	-97.9	-98	-99.8	-96.3
LTE-FDD B21 (10M)	-98	-98.5	-100	-96.3
LTE-FDD B28 (10M)	-98.5	-98.5	-100.9	-94.8
LTE-TDD B41 (10M)	-97.9	-98	-99.5	-94.3

NOTE

¹⁾ EVDO/CDMA BC0 for AG35-CE is optional.

6.7. Electrostatic Discharge

The module is not protected against electrostatic discharge (ESD) in general. Consequently, it is subject to ESD handling precautions that typically apply to ESD sensitive components. Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates the module.

The following table shows the module electrostatic discharge characteristics.

Table 69: Electrostatic Discharge Characteristics

Tested Points	Contact Discharge	Air Discharge	Unit
VBAT, GND	±8	±10	kV
All Antenna Interfaces	±8	±10	kV
Other Interfaces	±0.5	±1	kV

6.8. Thermal Consideration

In order to achieve better performance of the module, it is recommended to comply with the following principles for thermal consideration:

- On customers' PCB design, please keep placement of the module away from heating sources, especially high power components such as ARM processor, audio power amplifier, power supply, etc.
- Do not place components on the opposite side of the PCB area where the module is mounted, in order to facilitate adding of heatsink when necessary.
- Do not apply solder mask on the opposite side of the PCB area where the module is mounted, so as to ensure better heat dissipation performance.
- The reference ground of the area where the module is mounted should be complete, and add ground vias as many as possible for better heat dissipation. Through-holes will create better heat dissipation performance.
- Make sure the ground pads of the module and PCB are fully connected.
- According to customers' application demands, the heatsink can be mounted on the top of the module, or the opposite side of the PCB area where the module is mounted, or both of them.
- The heatsink should be designed with as many fins as possible to increase heat dissipation area. Meanwhile, a thermal pad with high thermal conductivity should be used between the heatsink and module/PCB.

The following shows two kinds of heatsink designs for reference and customers can choose one or both of them according to their application structure.

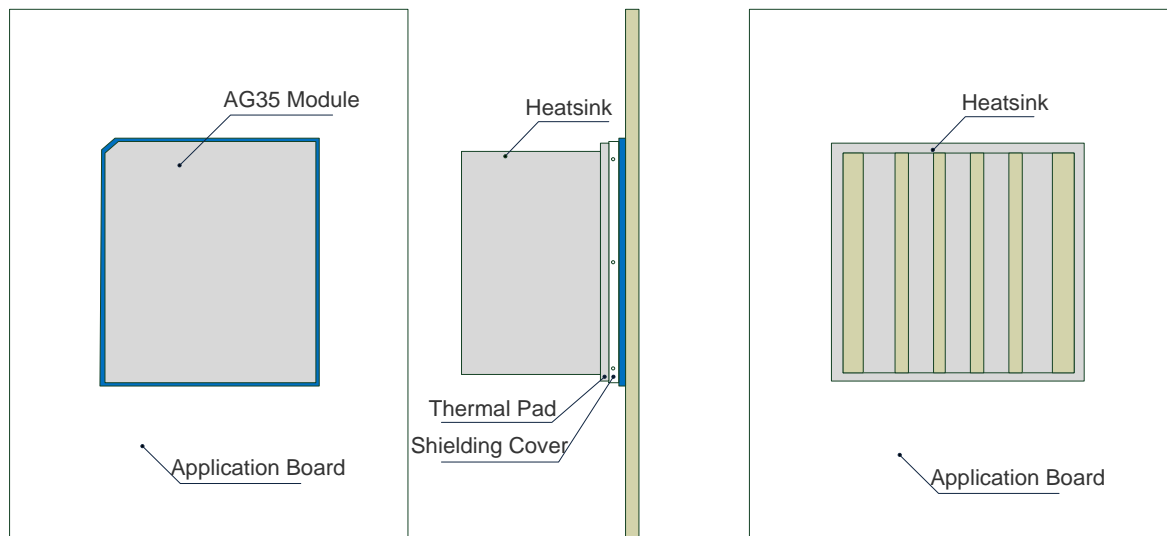


Figure 42: Referenced Heatsink Design (Heatsink at the Top of the Module)

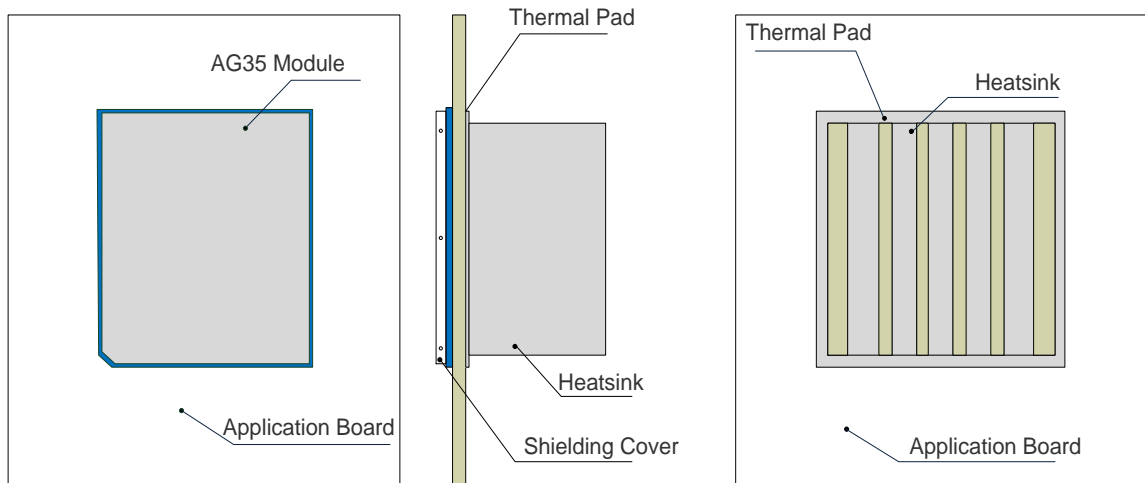


Figure 43: Referenced Heatsink Design (Heatsink at the Backside of Customers' PCB)

NOTES

1. For better performance, the maximum temperature of the internal BB chip should be kept below 105°C. When the maximum temperature of the BB chip reaches or exceeds 105°C, the module works normal but provides reduced performance (such as RF output power, data rate, etc.). When the maximum BB chip temperature reaches or exceeds 118°C, the module will disconnect from the network, and it will recover to network connected state after the maximum temperature falls below 118°C. Therefore, the thermal design should be maximally optimized to make sure the maximum BB chip temperature always maintains below 105°C. Customers can execute **AT+QTEMP** command and get the maximum BB chip temperature from the first returned value.
2. For more detailed introduction on thermal design, please refer to **document [7]**.

7 Mechanical Dimensions

This chapter describes the mechanical dimensions of the module. All dimensions are measured in mm, and the tolerances for dimensions without tolerance values are $\pm 0.05\text{mm}$.

7.1. Mechanical Dimensions of the Module

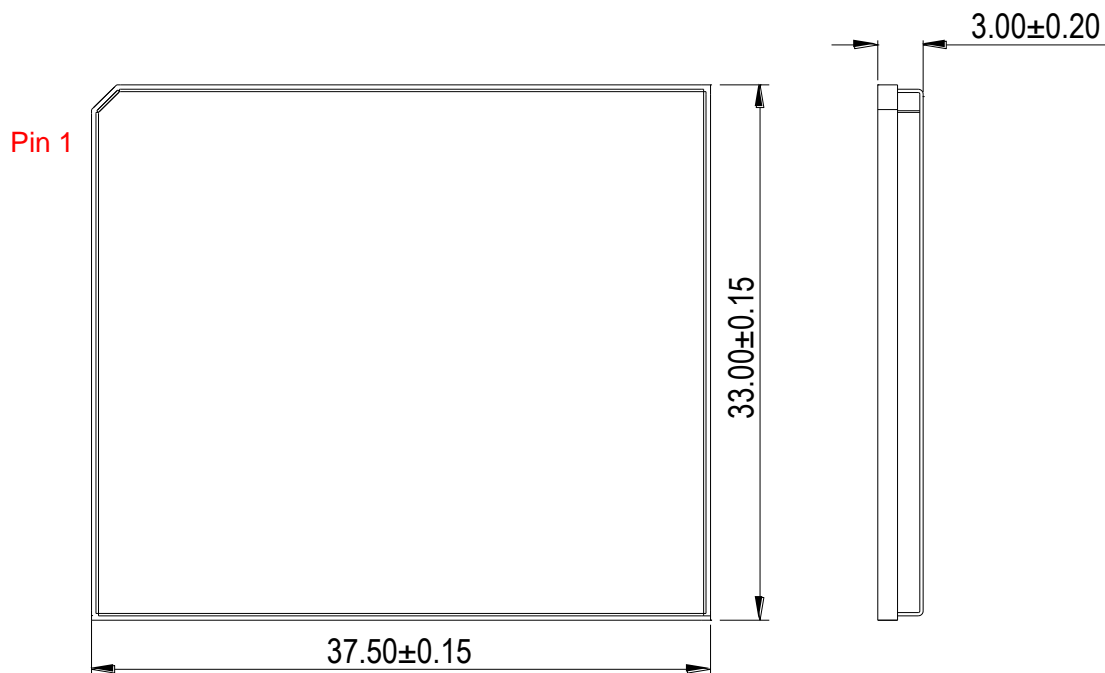


Figure 44: Module Top and Side Dimensions

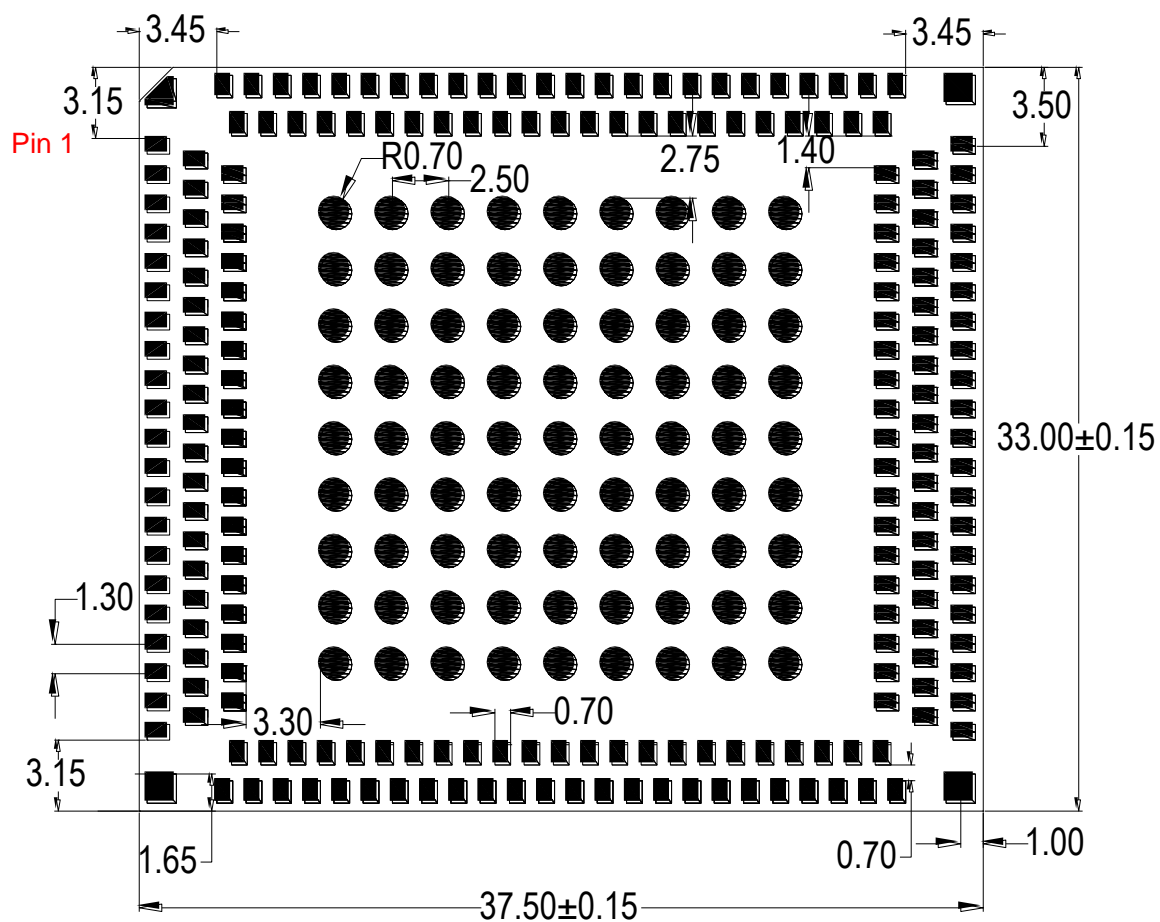


Figure 45: Module Bottom Dimensions (Top View)

7.2. Recommended Footprint

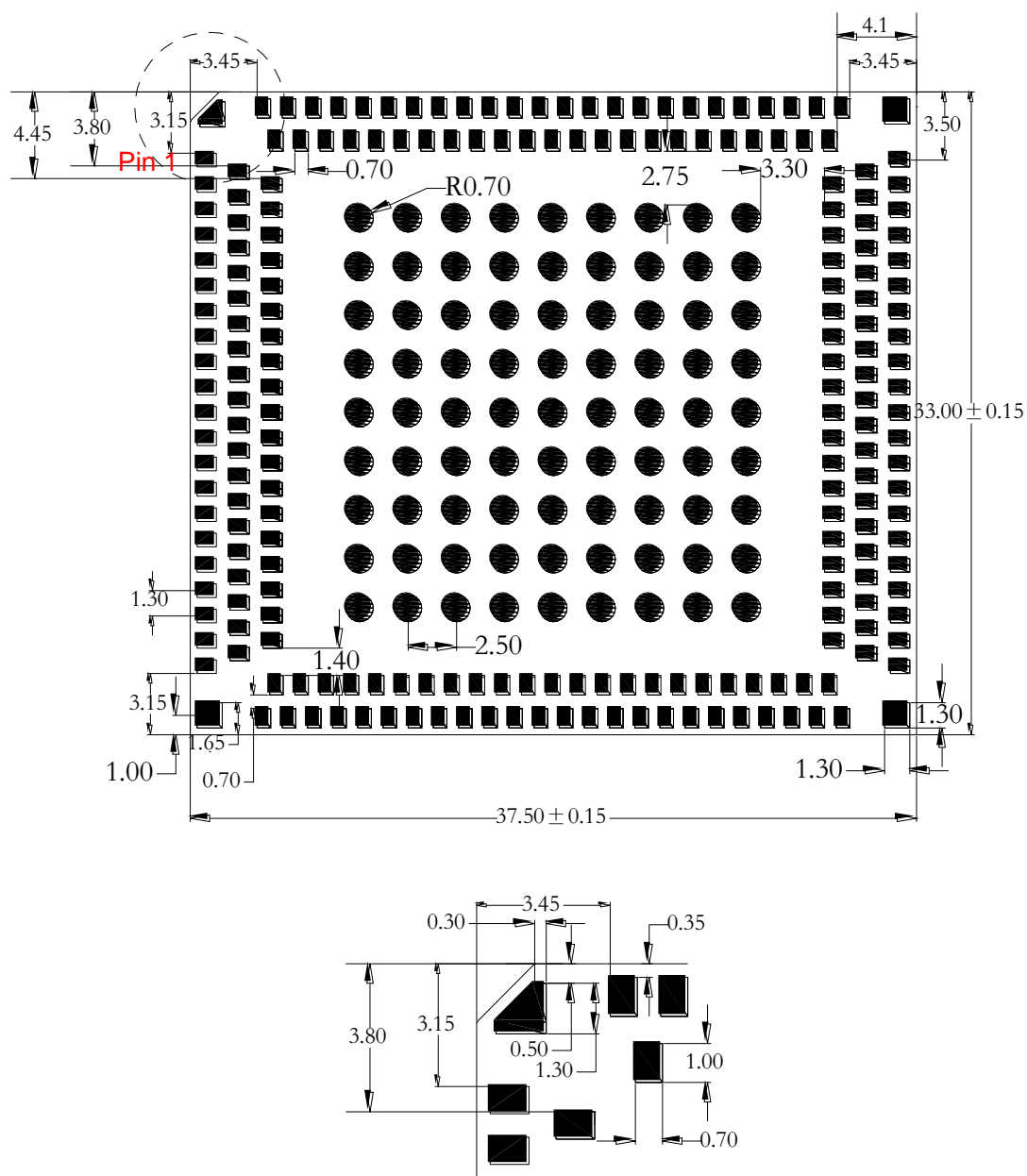


Figure 46: Module Bottom Dimensions (Top View)

NOTE

For convenient maintenance of the module, please keep about 3mm between the module and other components on the host PCB.

7.3. Design Effect Drawings of the Module



Figure 47: Top View of the Module

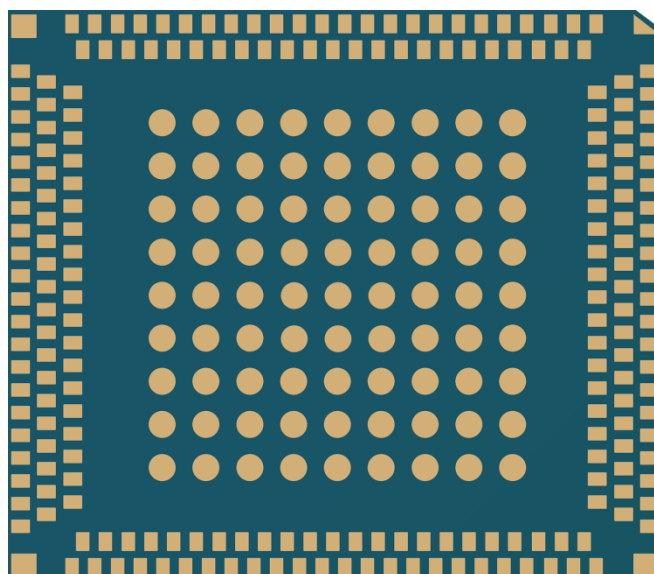


Figure 48: Bottom View of the Module

NOTE

These are renderings of AG35 module. For authentic appearance, please refer to the module that you receive from Quectel.

8 Storage, Manufacturing and Packaging

8.1. Storage

AG35 is stored in a vacuum-sealed bag. It is rated at MSL 3, and its storage restrictions are shown as below.

1. Shelf life in the vacuum-sealed bag: 12 months at $< 40^{\circ}\text{C}/90\%\text{RH}$.
2. After the vacuum-sealed bag is opened, devices that will be subjected to reflow soldering or other high temperature processes must be:
 - Mounted within 168 hours at the factory environment of $\leq 30^{\circ}\text{C}/60\%\text{RH}$.
 - Stored at $<10\% \text{ RH}$.
3. Devices require baking before mounting, if any circumstance below occurs:
 - When the ambient temperature is $23^{\circ}\text{C}\pm 5^{\circ}\text{C}$ and the humidity indicator card shows the humidity is $>10\%$ before opening the vacuum-sealed bag.
 - Device mounting cannot be finished within 168 hours at factory conditions of $\leq 30^{\circ}\text{C}/60\% \text{ RH}$.
4. If baking is required, devices may be baked for 8 hours at $120^{\circ}\text{C}\pm 5^{\circ}\text{C}$.

NOTE

As the plastic package cannot be subjected to high temperature, it should be removed from devices before high temperature (120°C) baking. If shorter baking time is desired, please refer to *IPC/JEDECJ-STD-033* for baking procedure.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. The force on the squeegee should be adjusted properly so as to produce a clean stencil surface on a single pass. To ensure the module soldering quality, the thickness of stencil for the module is recommended to be 0.13mm~0.15mm. For more details, please refer to **document [6]**.

It is suggested that the peak reflow temperature is 238~245°C, and the absolute maximum reflow temperature is 245°C. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

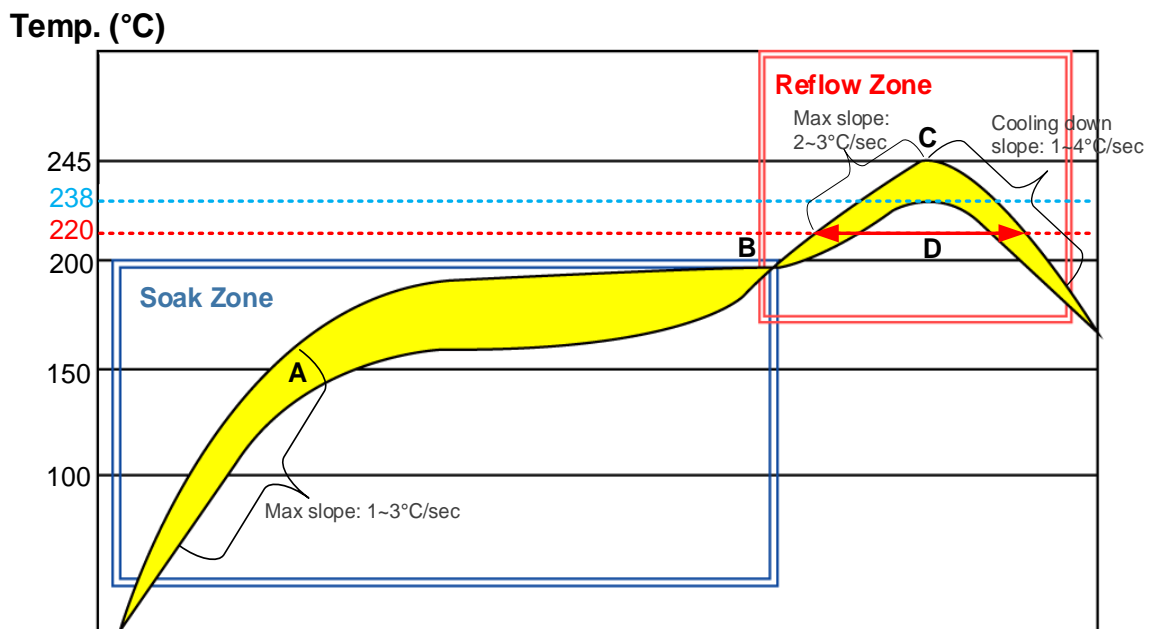


Figure 49: Recommended Reflow Soldering Thermal Profile

Table 70: Recommended Thermal Profile Parameters

Factor	Recommendation
Soak Zone	
Max slope	1 to 3°C/sec
Soak time (between A and B: 150°C and 200°C)	60 to 120 sec

Reflow Zone	
Max slope	2 to 3°C/sec
Reflow time (D: over 220°C)	40 to 60 sec
Max temperature	238°C ~ 245°C
Cooling down slope	1 to 4°C/sec
Reflow Cycle	
Max reflow cycle	1

8.3. Packaging

AG35 is packaged in tape and reel carriers. One reel is 10.56 meters long and contains 220 modules. The figures below show the package details, measured in mm.

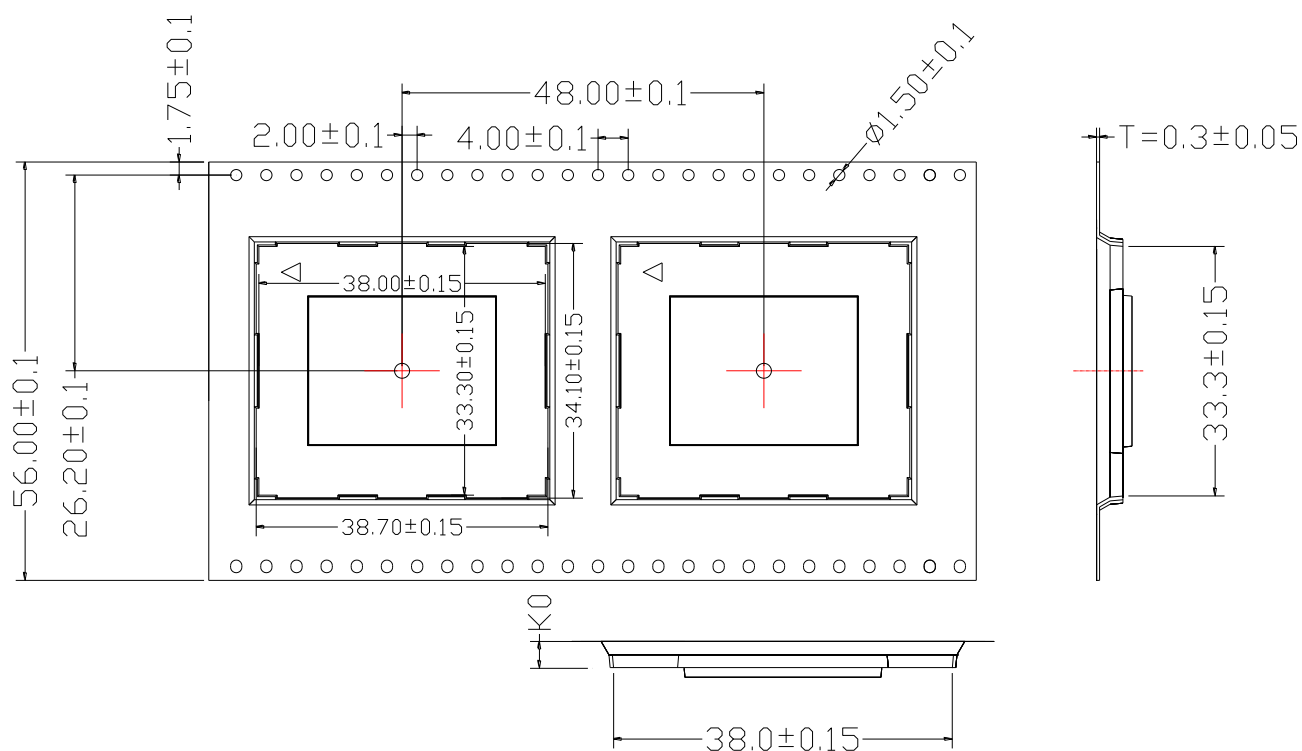


Figure 50: Tape Specifications

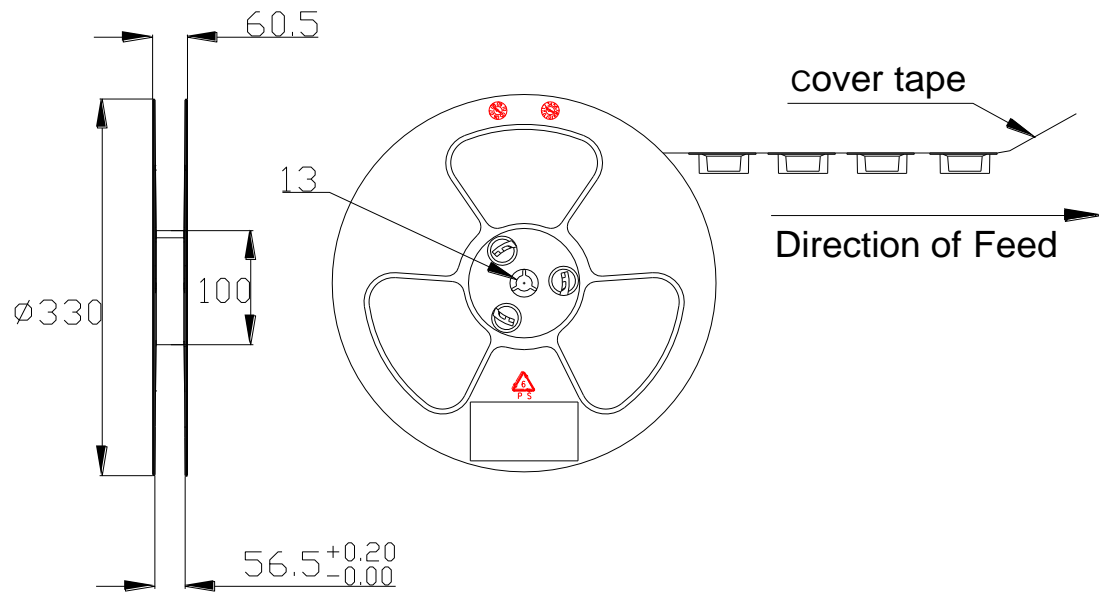


Figure 51: Reel Specifications

9 Appendix A References

Table 71: Related Documents

SN	Document Name	Remark
[1]	Quectel_AG35_Power_Management_Application_Note	AG35 Power Management Application Note
[2]	Quectel_AG35_AT_Commands_Manual	AG35 AT Commands Manual
[3]	Quectel_UMTS<E_EVB_User_Guide	UMTS<E EVB User Guide
[4]	Quectel_AG35_GNSS_AT_Commands_Manual	AG35 GNSS AT Commands Manual
[5]	Quectel_RF_Layout_Application_Note	RF Layout Application Note
[6]	Quectel_Module_Secondary_SMT_User_Guide	Module Secondary SMT User Guide
[7]	Quectel_LTE_Module_Thermal_Design_Guide	Thermal Design Guide for Quectel LTE (LTE/LTE-A/Automotive) modules

Table 72: Terms and Abbreviations

Abbreviation	Description
AMR	Adaptive Multi-rate
bps	Bits Per Second
CHAP	Challenge Handshake Authentication Protocol
CS	Coding Scheme
CSD	Circuit Switched Data
CTS	Clear To Send
DC-HSPA+	Dual-carrier High Speed Packet Access
DFOTA	Delta Firmware Upgrade Over The Air

DL	Downlink
DTR	Data Terminal Ready
DTX	Discontinuous Transmission
EAVB	Ethernet Audio Video Bridging
EFR	Enhanced Full Rate
ESD	Electrostatic Discharge
EVDO	Evolution-Data Optimized
FDD	Frequency Division Duplex
FR	Full Rate
GLONASS	GLObalnaya NAVigatsionnaya Sputnikovaya Sistema, the Russian Global Navigation Satellite System
GMSK	Gaussian Minimum Shift Keying
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
GSM	Global System for Mobile Communications
HR	Half Rate
HSPA	High Speed Packet Access
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
I/O	Input/Output
LED	Light Emitting Diode
LNA	Low Noise Amplifier
LTE	Long Term Evolution
LVC MOS	Low Voltage Complementary Metal Oxide Semiconductor
MIMO	Multiple Input Multiple Output
MO	Mobile Originated

MOS	Mean Opinion Score
MS	Mobile Station (GSM engine)
MT	Mobile Terminated
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PDU	Protocol Data Unit
PPP	Point-to-Point Protocol
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RHCP	Right Hand Circularly Polarized
Rx	Receive
SIM	Subscriber Identification Module
SMS	Short Message Service
TDD	Time Division Duplexing
TDMA	Time Division Multiple Access
TD-SCDMA	Time Division-Synchronous Code Division Multiple Access
TX	Transmitting Direction
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
(U)SIM	(Universal) Subscriber Identity Module
Vmax	Maximum Voltage Value
Vnorm	Normal Voltage Value
Vmin	Minimum Voltage Value

V_{IHmax}	Maximum Input High Level Voltage Value
V_{IHmin}	Minimum Input High Level Voltage Value
V_{ILmax}	Maximum Input Low Level Voltage Value
V_{ILmin}	Minimum Input Low Level Voltage Value
V_{Imax}	Absolute Maximum Input Voltage Value
V_{Imin}	Absolute Minimum Input Voltage Value
V_{Oax}	Maximum Output High Level Voltage Value
V_{Oin}	Minimum Output High Level Voltage Value
V_{OLmax}	Maximum Output Low Level Voltage Value
V_{OLmin}	Minimum Output Low Level Voltage Value
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access

10 Appendix B GPRS Coding Schemes

Table 73: Description of Different Coding Schemes

Scheme	CS-1	CS-2	CS-3	CS-4
Code Rate	1/2	2/3	3/4	1
USF	3	3	3	3
Pre-coded USF	3	6	6	12
Radio Block excl.USF and BCS	181	268	312	428
BCS	40	16	16	16
Tail	4	4	4	-
Coded Bits	456	588	676	456
Punctured Bits	0	132	220	-
Data Rate Kb/s	9.05	13.4	15.6	21.4

11 Appendix C GPRS Multi-slot Classes

Twenty-nine classes of GPRS multi-slot modes are defined for MS in GPRS specification. Multi-slot classes are product dependent, and determine the maximum achievable data rates in both the uplink and downlink directions. Written as 3+1 or 2+2, the first number indicates the amount of downlink timeslots, while the second number indicates the amount of uplink timeslots. The active slots determine the total number of slots the GPRS device can use simultaneously for both uplink and downlink communications.

The description of different multi-slot classes is shown in the following table.

Table 74: GPRS Multi-slot Classes

Multislot Class	Downlink Slots	Uplink Slots	Active Slots
1	1	1	2
2	2	1	3
3	2	2	3
4	3	1	4
5	2	2	4
6	3	2	4
7	3	3	4
8	4	1	5
9	3	2	5
10	4	2	5
11	4	3	5
12	4	4	5
13	3	3	NA
14	4	4	NA

15	5	5	NA
16	6	6	NA
17	7	7	NA
18	8	8	NA
19	6	2	NA
20	6	3	NA
21	6	4	NA
22	6	4	NA
23	6	6	NA
24	8	2	NA
25	8	3	NA
26	8	4	NA
27	8	4	NA
28	8	6	NA
29	8	8	NA
30	5	1	6
31	5	2	6
32	5	3	6
33	5	4	6

12 Appendix D EDGE Modulation and Coding Schemes

Table 75: EDGE Modulation and Coding Schemes

Coding Scheme	Modulation	Coding Family	1 Timeslot	2 Timeslot	4 Timeslot
CS-1:	GMSK	/	9.05kbps	18.1kbps	36.2kbps
CS-2:	GMSK	/	13.4kbps	26.8kbps	53.6kbps
CS-3:	GMSK	/	15.6kbps	31.2kbps	62.4kbps
CS-4:	GMSK	/	21.4kbps	42.8kbps	85.6kbps
MCS-1	GMSK	C	8.80kbps	17.60kbps	35.20kbps
MCS-2	GMSK	B	11.2kbps	22.4kbps	44.8kbps
MCS-3	GMSK	A	14.8kbps	29.6kbps	59.2kbps
MCS-4	GMSK	C	17.6kbps	35.2kbps	70.4kbps
MCS-5	8-PSK	B	22.4kbps	44.8kbps	89.6kbps
MCS-6	8-PSK	A	29.6kbps	59.2kbps	118.4kbps
MCS-7	8-PSK	B	44.8kbps	89.6kbps	179.2kbps
MCS-8	8-PSK	A	54.4kbps	108.8kbps	217.6kbps
MCS-9	8-PSK	A	59.2kbps	118.4kbps	236.8kbps