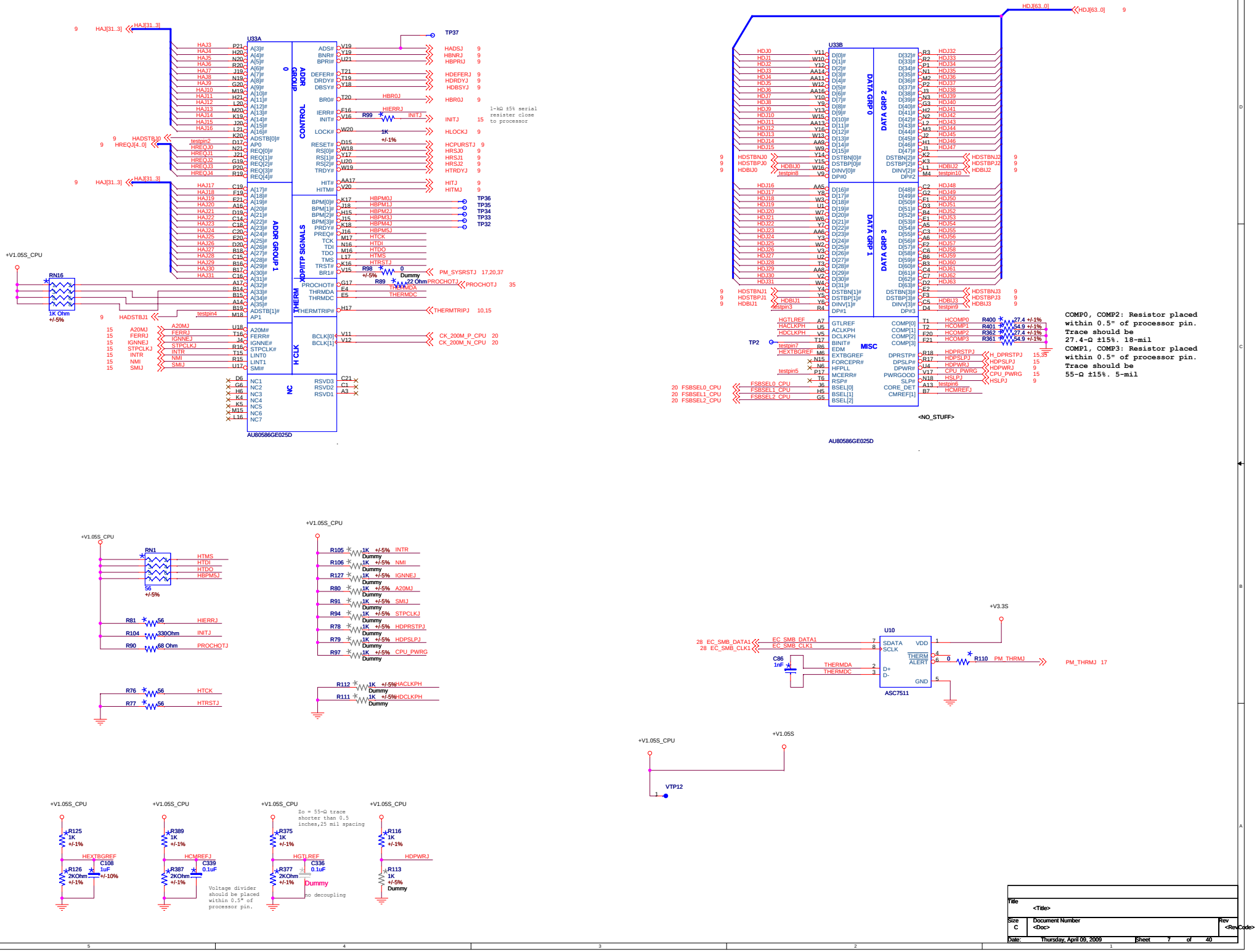
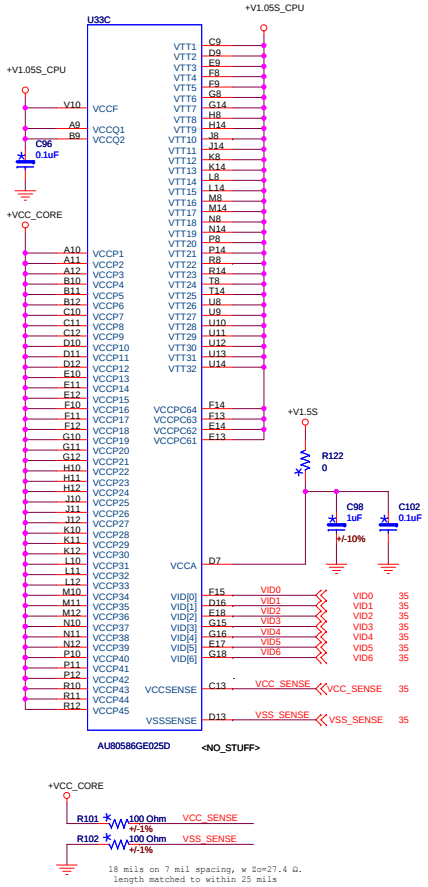
Schematic Diagram

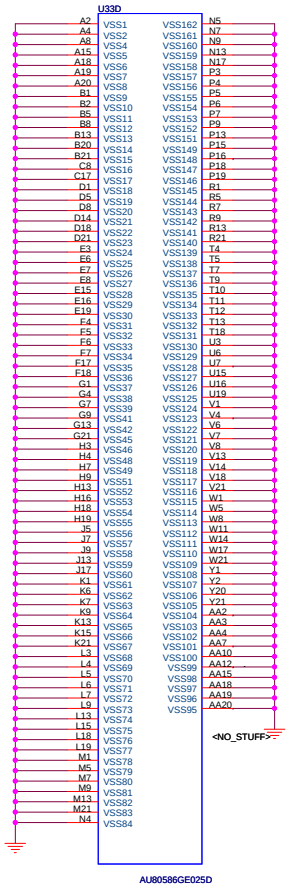
Page Index

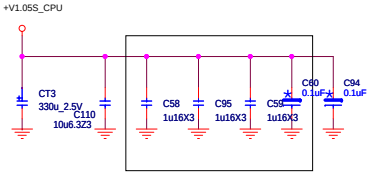
01. Index Page	21. AUDIO
02. CPU-1	22. MODEM
03. CPU-2	23. USB
04. GMCH-1	24. CARD READER
05. GMCH-2	25. EC-1
06. GMCH-3	26. EC-2
07. GMCH-4	27. DC RAIL
08. GMCH-5	28. SYSTEM CHARGE
09. SO-DIMM	29. SYSTEM VR
10. ICH7M-1	30. CHIP VR
11. ICH7M-2	31. DDR VR
12. ICH7M-3	32. CPU VR
13. ICH7M-4	33. OTHER VR
14. ICH7M-5	34. MODIFY HISTORY
15. CLOCK GEN	.
16. VGA	
17. LVDS	
18. SSD	
19. MINI PCIE	
20. LAN	

Title: <Title>		
Size: C	Document Number: <Doc>	Rev: <RevCode>
Date: Wednesday, February 18, 2009	Sheet 1 of 40	

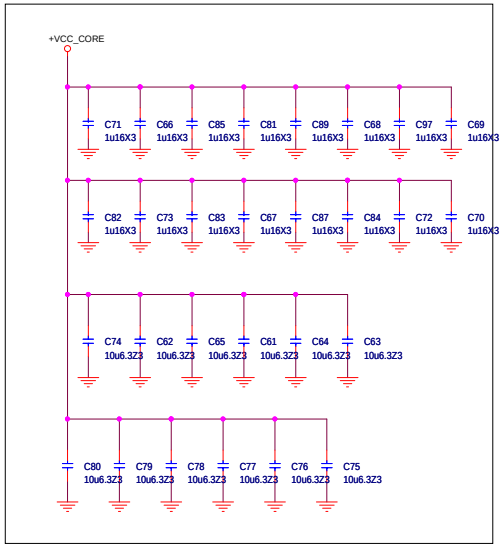

U33A
ADDR GROUP 0
ADDR GROUP 1
CONTROL
HDPITP SIGNALS
THERM
H CLK
NC
AU80586GE025D
TP37
TP36
TP35
TP34
TP33
TP32
RN16
1K Ohm
+/-5%
testpin2
testpin4
HADSTBJ0
HREQJ[4..0]
HADSTBJ1
HAJ[31..3]
1-kΩ ±5% serial resister close to processor
R99
INITJ
R98
0
Dummy
22 Ohm
PM_SYSRSTJ 17,20,37
PROCHOTJ
PROCHOTJ 35
TMMDA
THERMDC
THERMTRIPJ 10,15
CK_200M_P_CPU 20
CK_200M_N_CPU 20
+V1.05S_CPU
U33B
DATA GRP 0
DATA GRP 2
DATA GRP 1
DATA GRP 3
HDJ[63..0]
HDJ[63..0] 9
HDSTBNJ0
HDSTBPJ0
HDBIJ0
testpin8
HDSTBNJ2
HDSTBPJ2
HDBIJ2
testpin10
HDSTBNJ1
HDSTBPJ1
HDBIJ1
testpin3
HDSTBNJ3
HDSTBPJ3
HDBIJ3
testpin9
MISC
TP2
testpin7
HEXTBGREF
testpin5
FSBSEL0_CPU
FSBSEL1_CPU
FSBSEL2_CPU
HCOMP0
HCOMP1
HCOMP2
HCOMP3
R400 27.4 +/-1%
R401 54.9 +/-1%
R362 27.4 +/-1%
R361 54.9 +/-1%
HDPRSTPJ
HDPSLPJ
HDPWRJ
CPU_PWRG
HSLPJ
H_DPRSTPJ 15,35
HDPSLPJ 15
HDPWRJ 9
CPU_PWRG 15
HSLPJ 9
<NO_STUFF>
AU80586GE025D
COMP0, COMP2: Resistor placed within 0.5" of processor pin. Trace should be 27.4-Ω ±15%. 18-mil
COMP1, COMP3: Resistor placed within 0.5" of processor pin. Trace should be 55-Ω ±15%. 5-mil
RN1
56
+/-5%
HTMS
HTDI
HTDO
HBPM5J
R81 56 HIERRJ
R104 330Ohm INITJ
R90 68 Ohm PROCHOTJ
R76 56 HTCK
R77 56 HTRSTJ
R105 1K +/-5% Dummy INTR
R106 1K +/-5% Dummy NMI
R127 1K +/-5% Dummy IGNNEJ
R80 1K +/-5% Dummy A20MJ
R91 1K +/-5% Dummy SMIJ
R94 1K +/-5% Dummy STPCLKJ
R78 1K +/-5% Dummy HDPRSTPJ
R79 1K +/-5% Dummy HDPSLPJ
R97 1K +/-5% Dummy CPU_PWRG
R112 1K +/-5% Dummy HACLKPH
R111 1K +/-5% Dummy HDCLKPH
+V3.3S
U10
ASC7511
SDATA
SCLK
THERM
ALERT
VDD
GND
D+
D-
EC_SMB_DATA1
EC_SMB_CLK1
C86 1nF
THERMDA
THERMDC
R110 0 PM_THRMJ
PM_THRMJ 17
+V1.05S
VTP12
R125 1K +/-1%
R126 2KOhm +/-1%
C108 1uF +/-10%
HEXTBGREF
R389 1K +/-1%
R387 2KOhm +/-1%
C339 0.1uF
HCMREFJ
Voltage divider should be placed within 0.5" of processor pin.
R375 1K +/-1%
R377 2KOhm +/-1%
C336 0.1uF Dummy
HGTLREF
Zo = 55-Ω trace shorter than 0.5 inches,25 mil spacing
no decoupling
R116 1K +/-1%
R113 1K +/-5% Dummy
HDPWRJ
Title
<Title>
Size C
Document Number <Doc>
Rev <RevCode>
Date: Thursday, April 09, 2009
Sheet 7 of 40



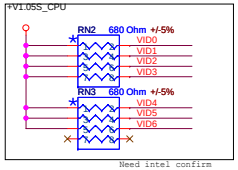




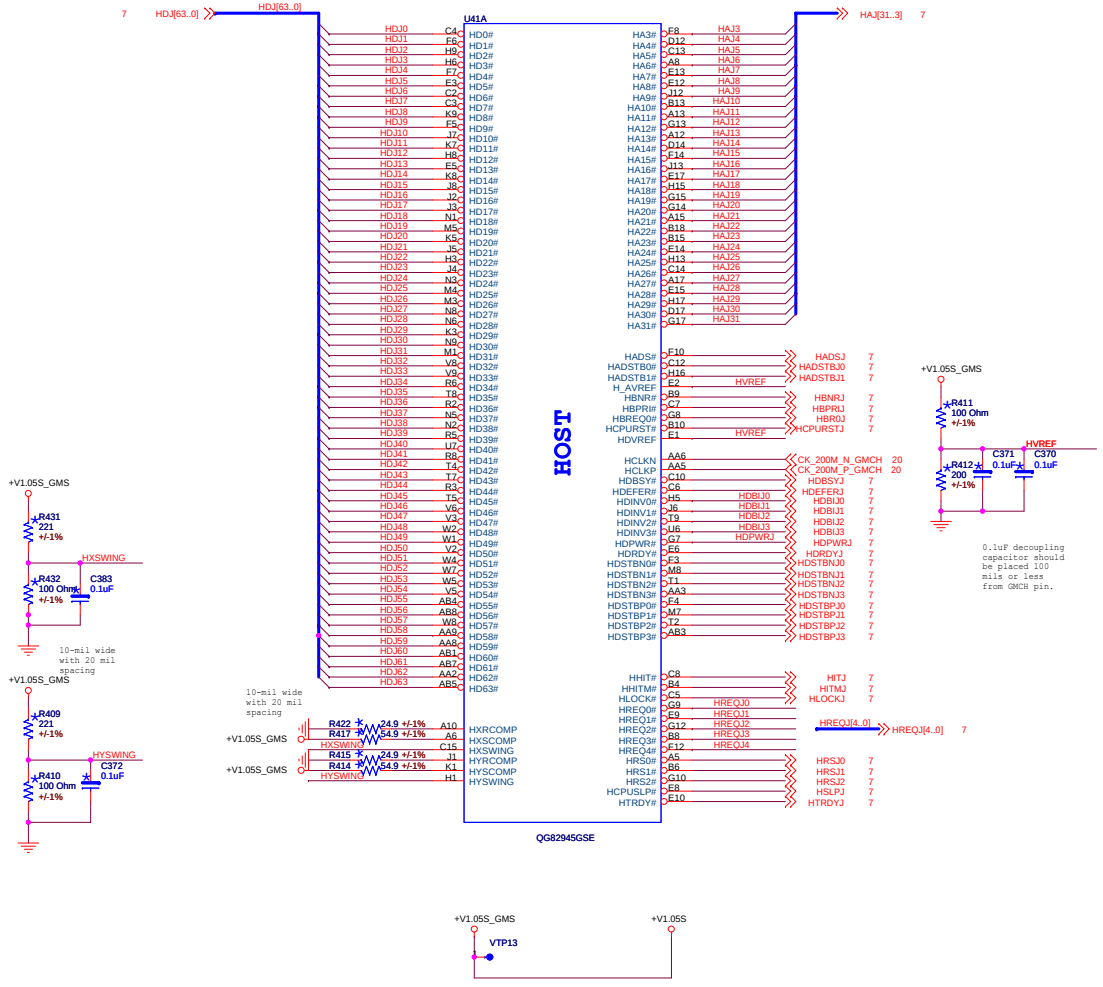
PLACE IN CAVITY,bottom



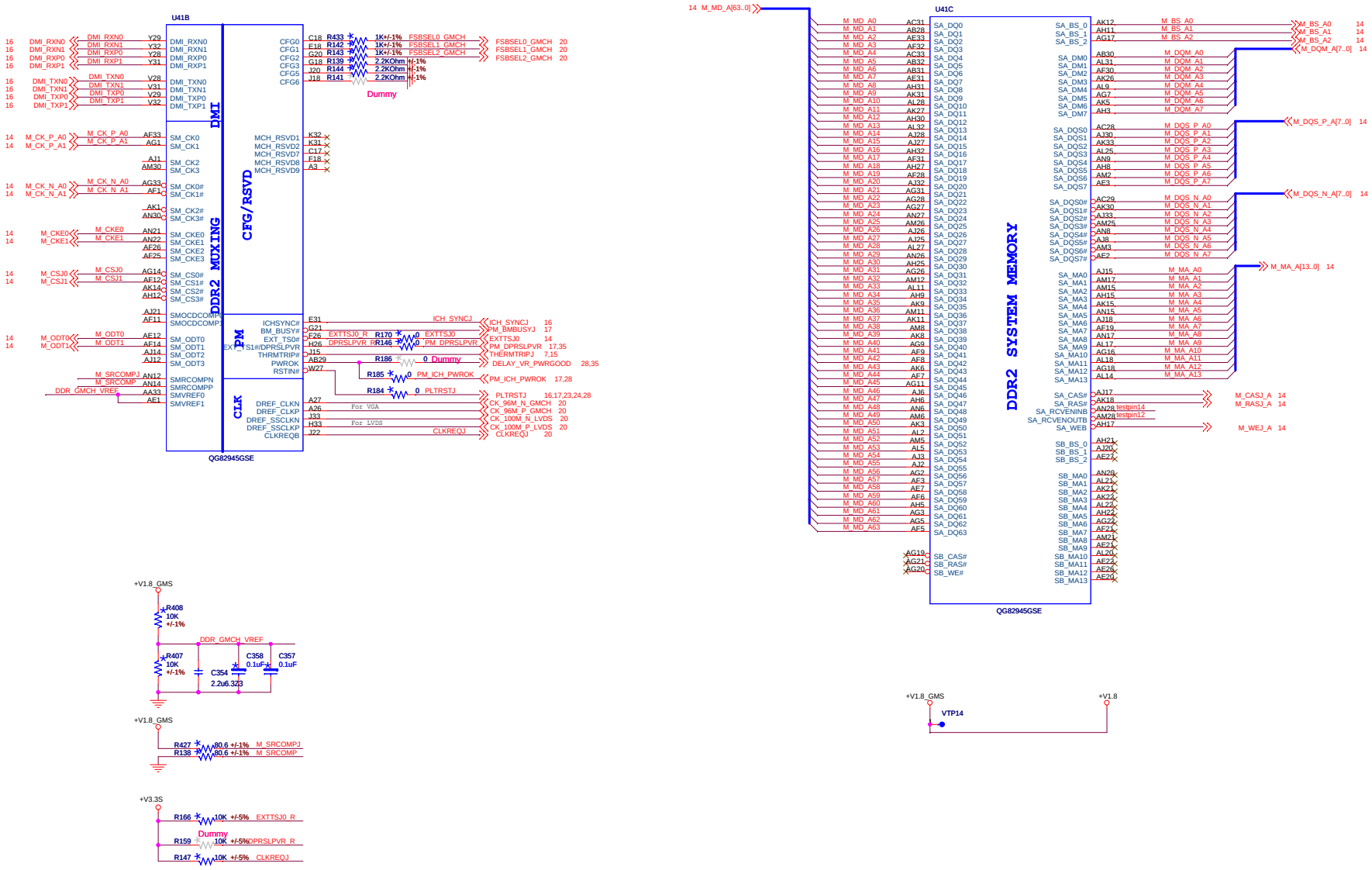
PLACE IN CAVITY



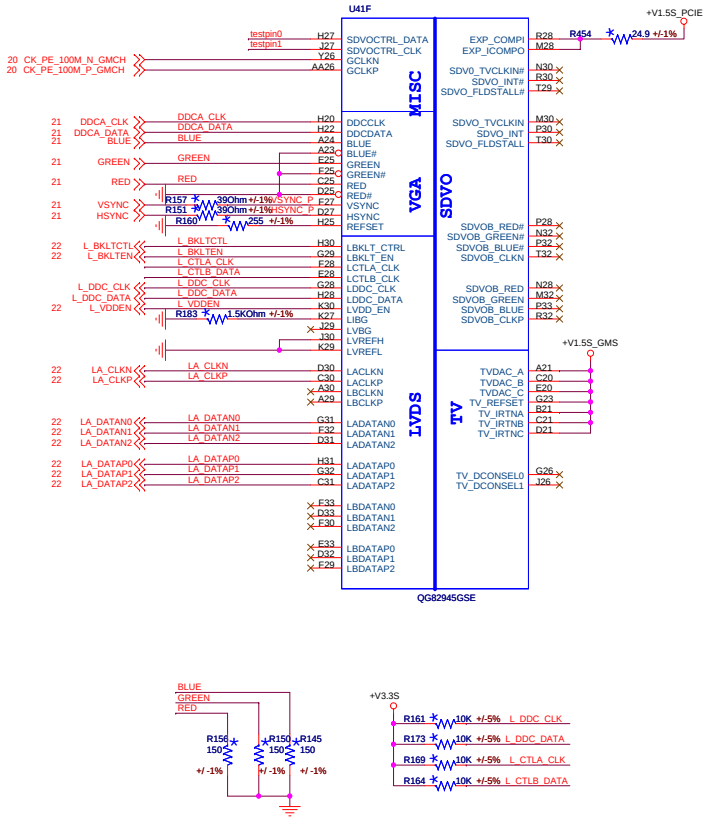
Title	<Title>	
Size C	Document Number <Doc>	Rev <RevCode>
Date: Saturday, March 28, 2009	Sheet 8 of 40	



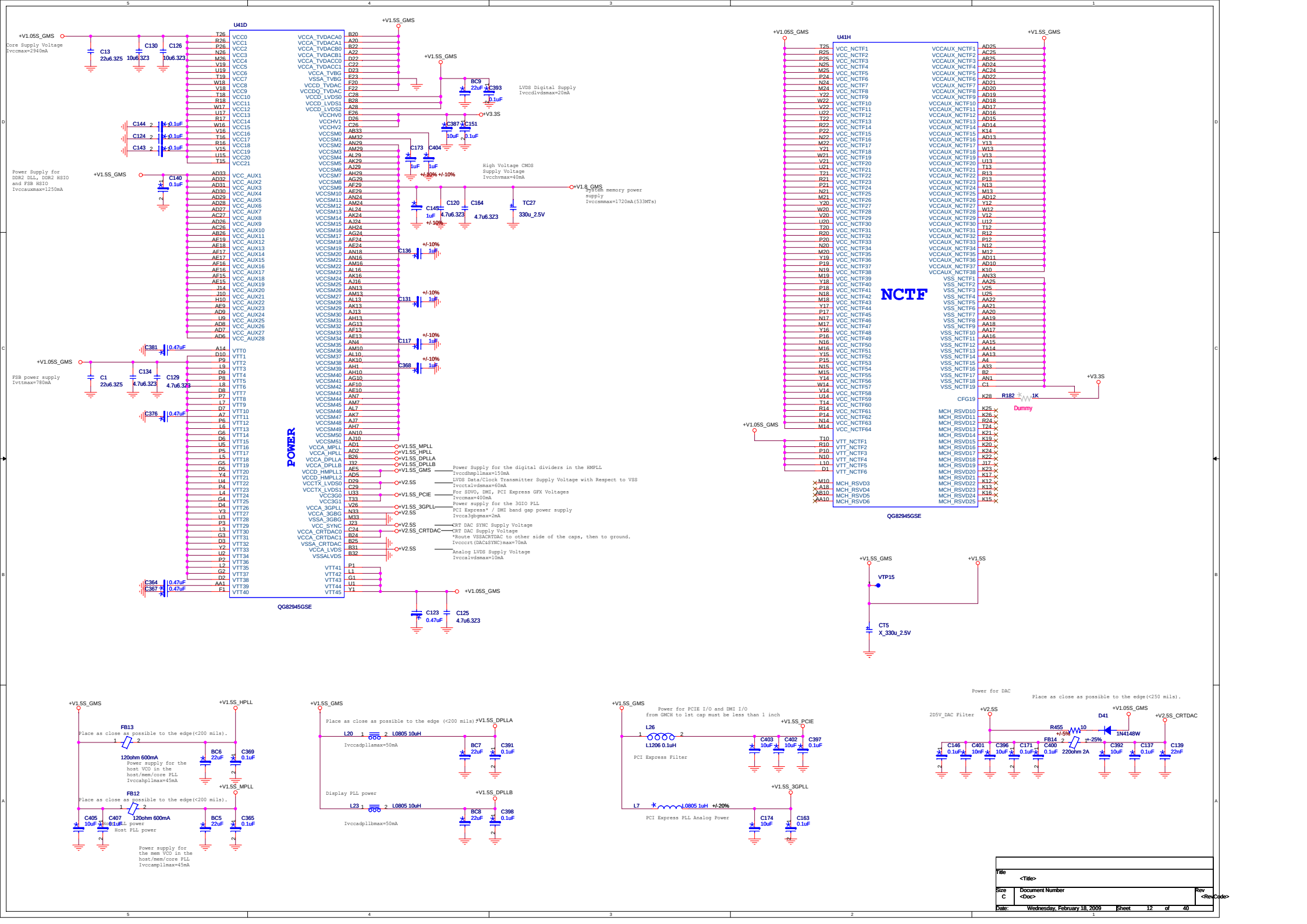
Title	<Title>		
Size C	Document Number <Doc>		Rev <RevCode>
Date: Saturday, March 28, 2009	Sheet 9 of 40		

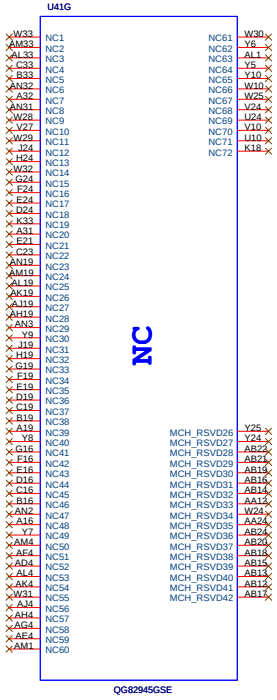


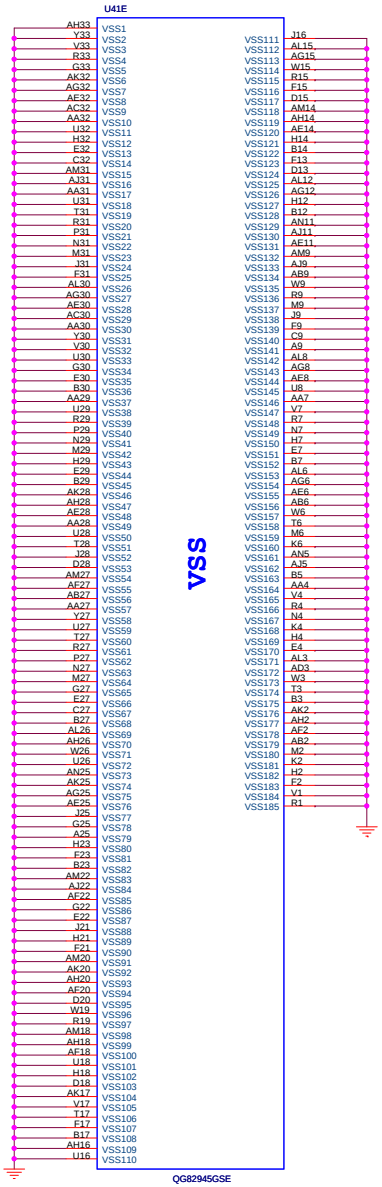
Title	<Title>		
Size C	Document Number <Doc>		Rev <RevCode>
Date: Saturday, March 28, 2009	Sheet 10 of 40		



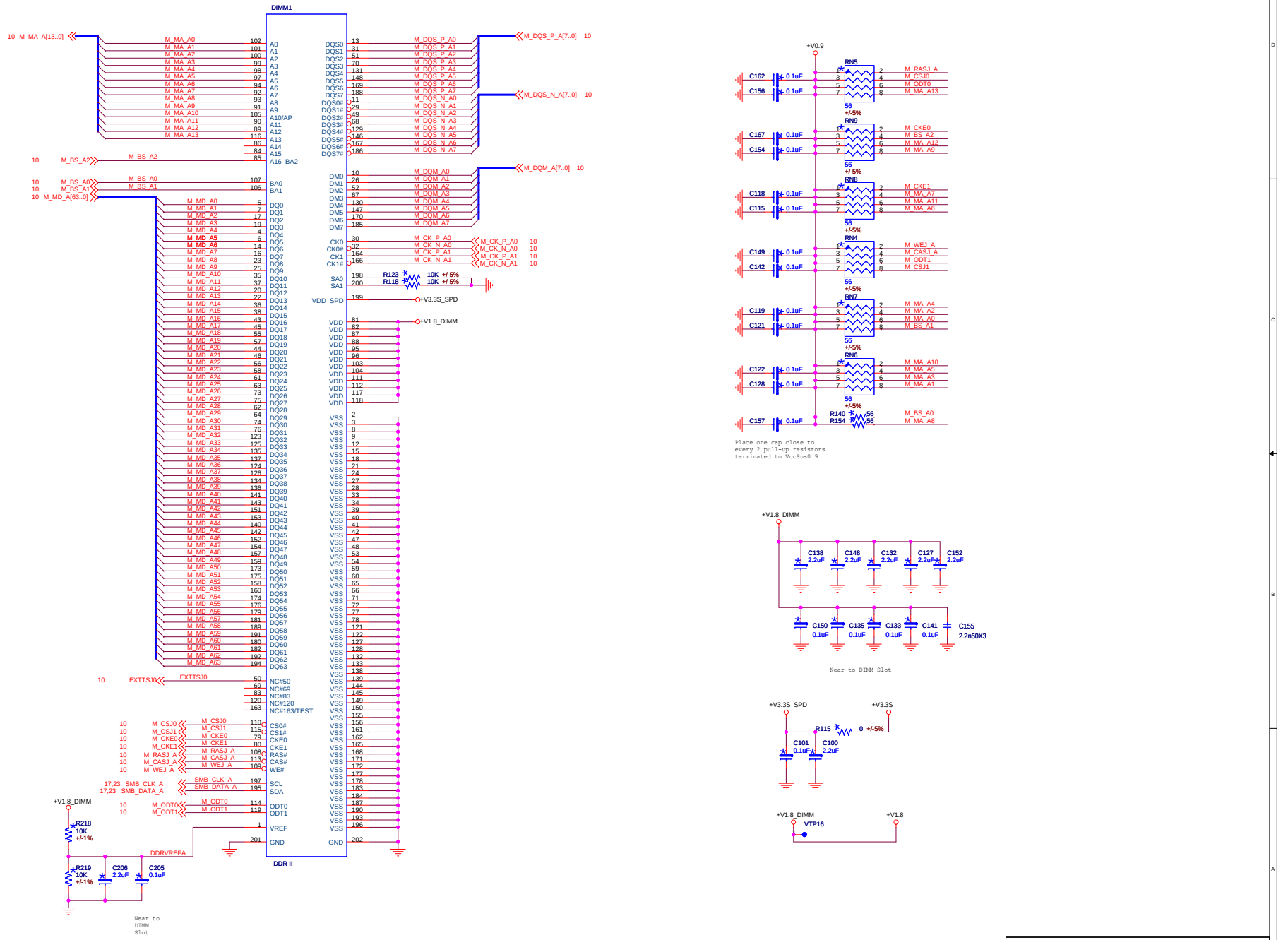
Title	<Title>	
Size C	Document Number <Doc>	Rev <RevCode>
Date: Saturday, March 28, 2009	Sheet 11 of 40	


U41D
POWER
QG82945GSE
+V1.05S_GMS
+V1.5S_GMS
+V3.3S
+V1.8_GMS
+V1.5S_MPLL
+V1.5S_HPLL
+V1.5S_DPLLA
+V1.5S_DPLLB
+V1.5S_PCIE
+V1.5S_3GPLL
+V2.5S
+V2.5S_CRTDAC
+V1.05S_GMS
Core Supply Voltage
Ivccmax=2940mA
Power Supply for DDR2 DLL, DDR2 HSIO and FSB HSIO
Ivccauxmax=1250mA
FSB power supply
Ivttmax=780mA
LVDS Digital Supply
Ivccdlvdsmax=20mA
High Voltage CMOS Supply Voltage
Ivcchvmax=40mA
System memory power supply
Ivccsmmax=1720mA(533MTs)
Power Supply for the digital dividers in the HMPLL
Ivccdhmpllmax=150mA
LVDS Data/Clock Transmitter Supply Voltage with Respect to VSS
Ivcctxlvdsmax=60mA
For SDVO, DMI, PCI Express GFX Voltages
Ivccmax=400mA
Power supply for the 3GIO PLL
PCI Express* / DMI band gap power supply
Ivcca3gbgmax=2mA
CRT DAC SYNC Supply Voltage
CRT DAC Supply Voltage
*Route VSSACRTDAC to other side of the caps, then to ground.
Ivcccrt(DAC&SYNC)max=70mA
Analog LVDS Supply Voltage
Ivccalvdsmax=10mA
U41H
NCTF
QG82945GSE
Dummy
Power supply for the host VCO in the host/mem/core PLL
Ivccahpllmax=45mA
Host PLL power
Power supply for the mem VCO in the host/mem/core PLL
Ivccamp1lmax=45mA
Place as close as possible to the edge (<200 mils).
Display PLL power
Ivccadp11bmax=50mA
Power for PCIE I/O and DMI I/O
from GMCH to 1st cap must be less than 1 inch
PCI Express Filter
PCI Express PLL Analog Power
Power for DAC
Place as close as possible to the edge(<250 mils).
2D5V_DAC Filter
Title
<Title>
Size C
Document Number
<Doc>
Rev
<RevCode>
Date: Wednesday, February 18, 2009
Sheet 12 of 40

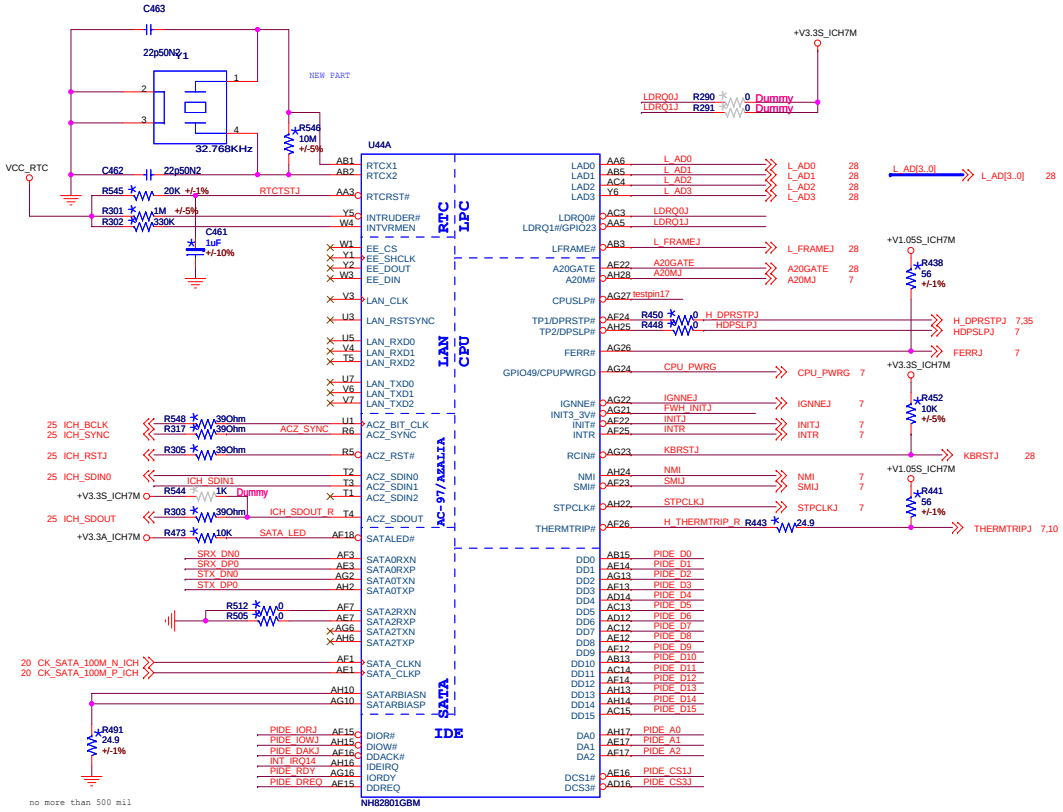


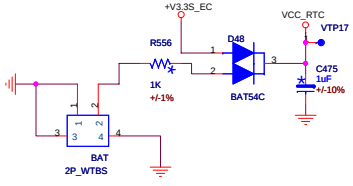


Title	<Title>		
Size: C	Document Number: <Doc>		Rev: <RevCode>
Date: Wednesday, February 18, 2009	Sheet 13 of 40		



Title	<Title>	
Size C	Document Number <Doc>	Rev <RevCode>
Date: Saturday, March 28, 2009	Sheet 14 of 40	



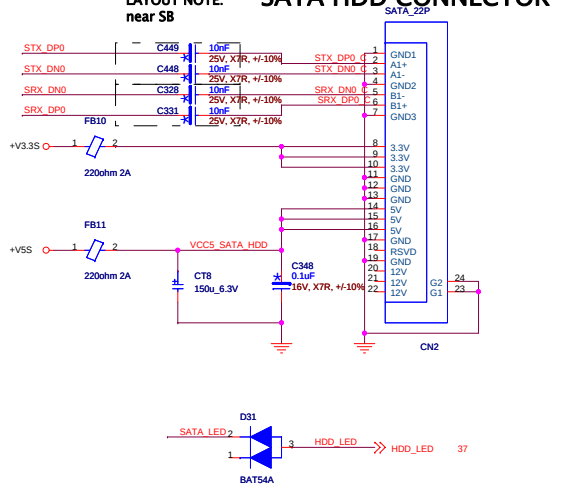


check with battary if 1 2 pin is correct
check with ME's sample

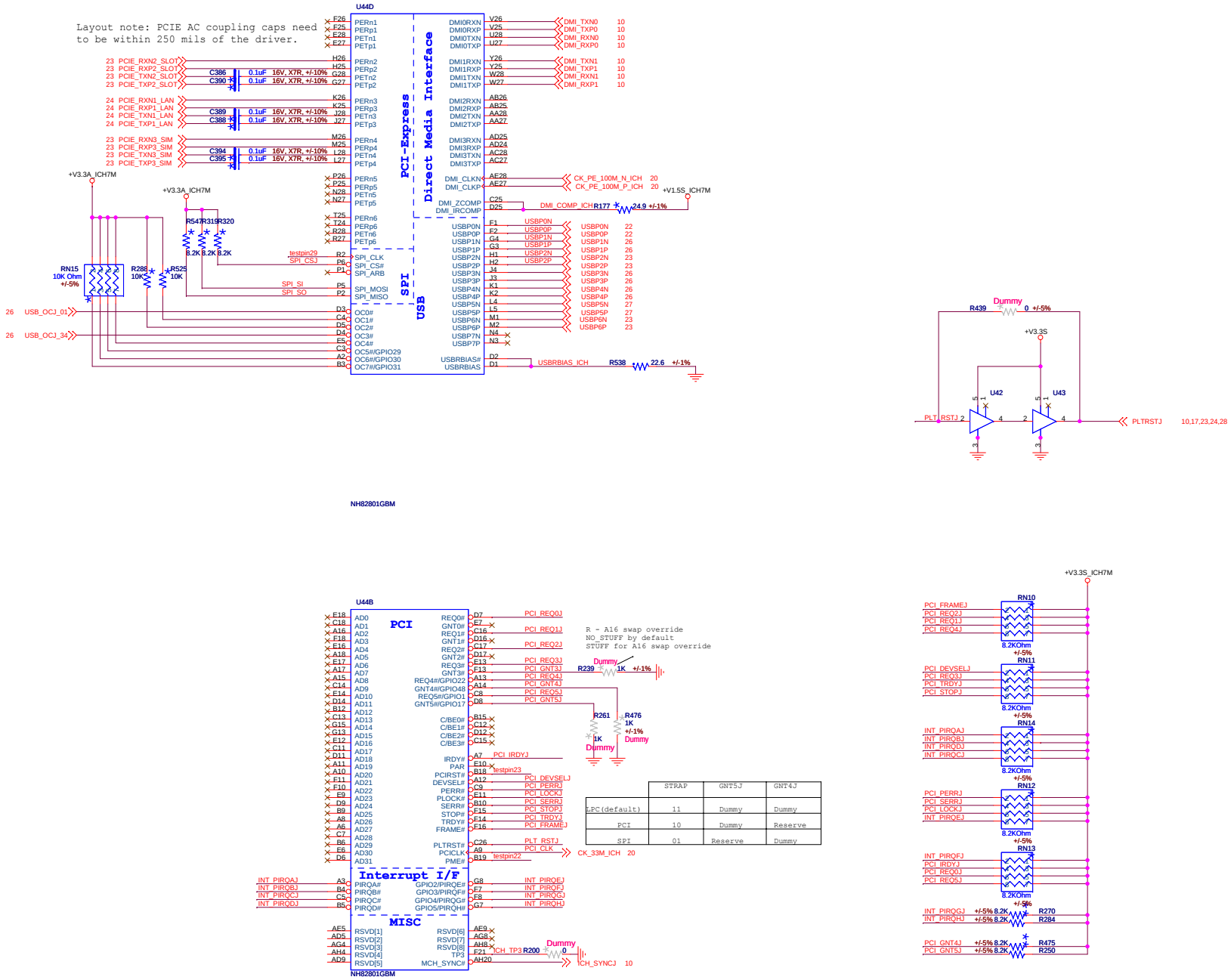
LAYOUT NOTE:
near connector

LAYOUT NOTE:
near SB

SATA HDD CONNECTOR

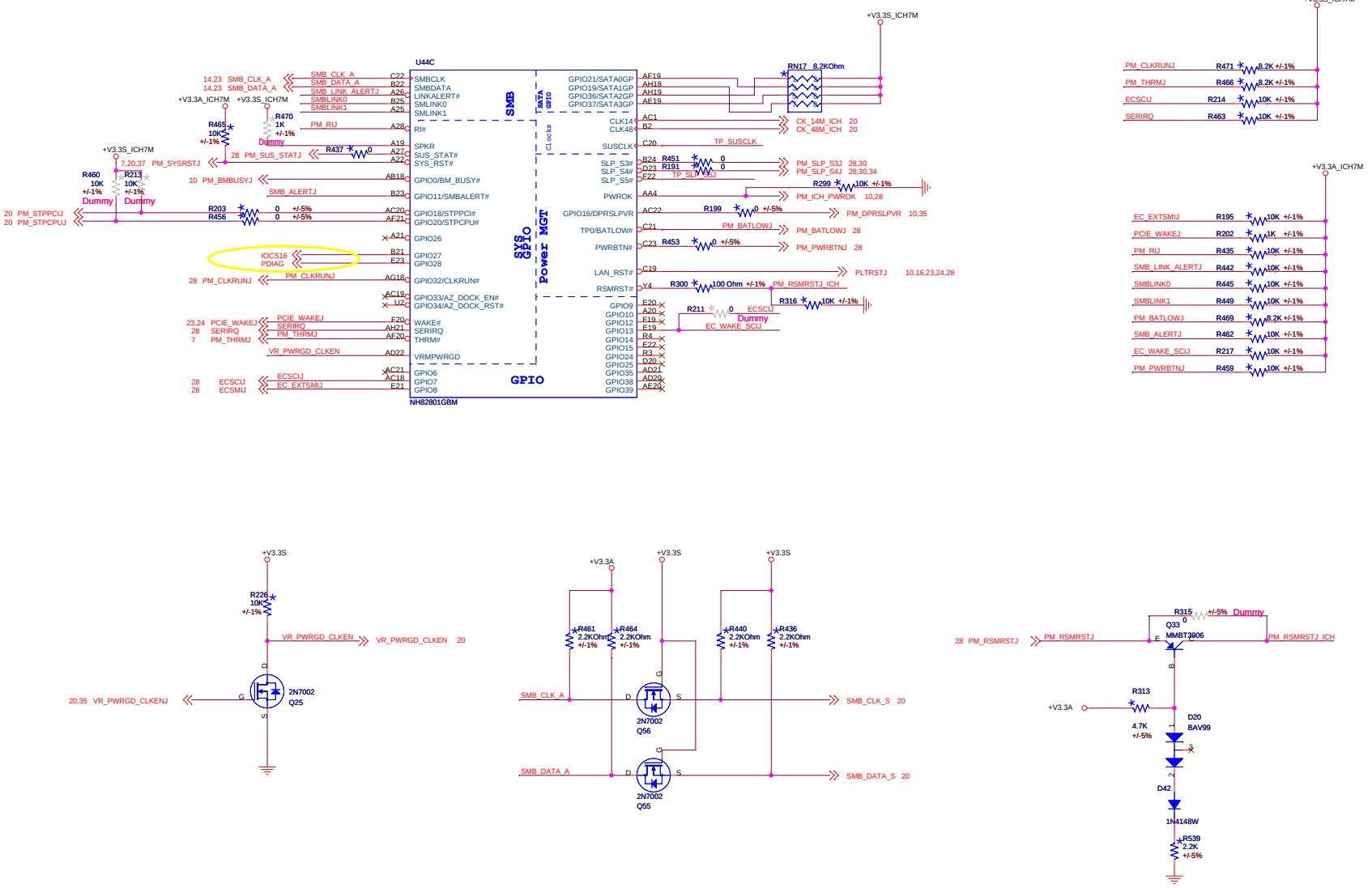


Title	<Title>		
Size C	Document Number <Doc>		Rev <RevCode>
Date: Saturday, March 28, 2009	Sheet 15 of 40		

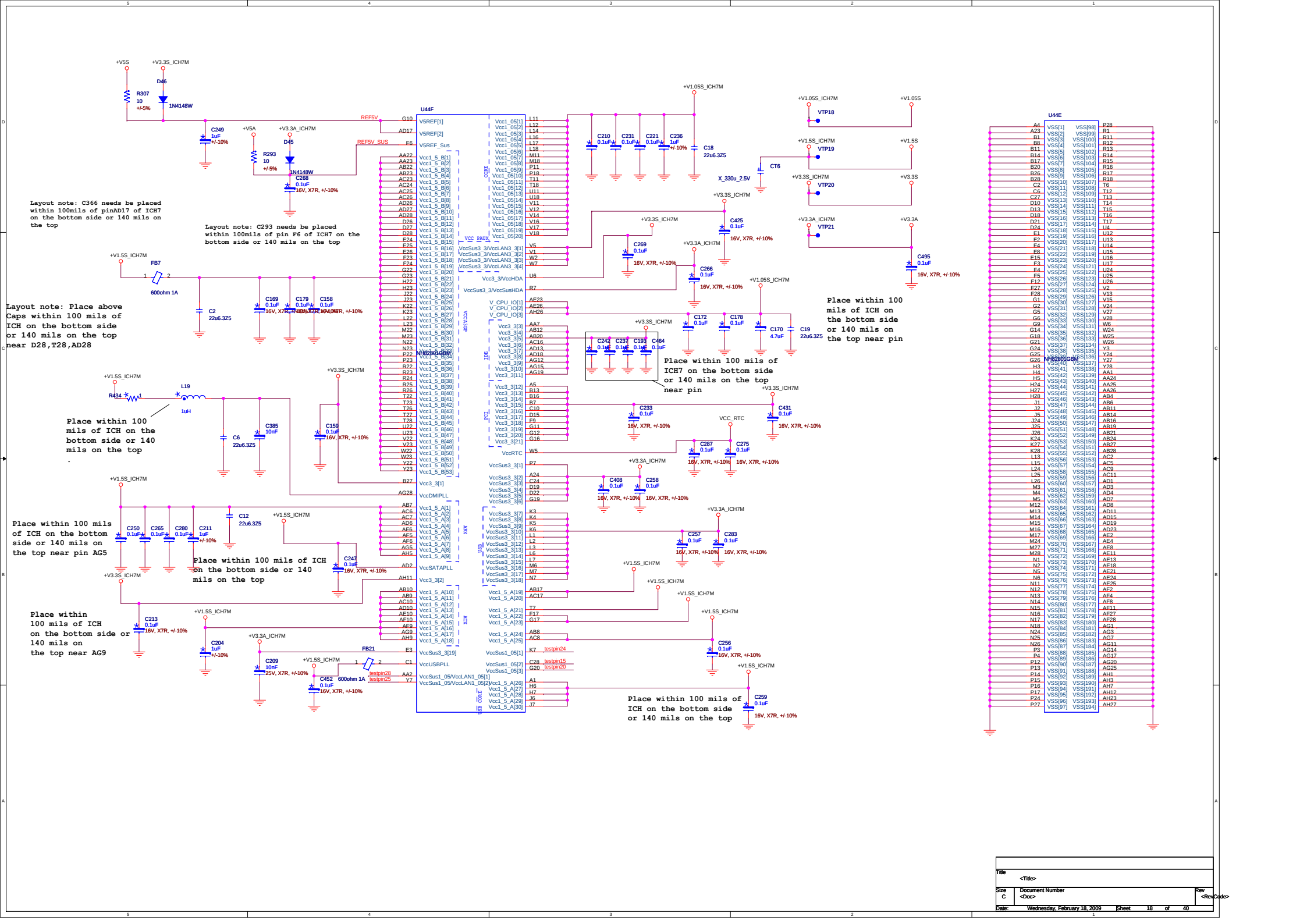


	STRAP	GNT5J	GNT4J
LPC(default)	11	Dummy	Dummy
PCI	10	Dummy	Reserve
SPI	01	Reserve	Dummy

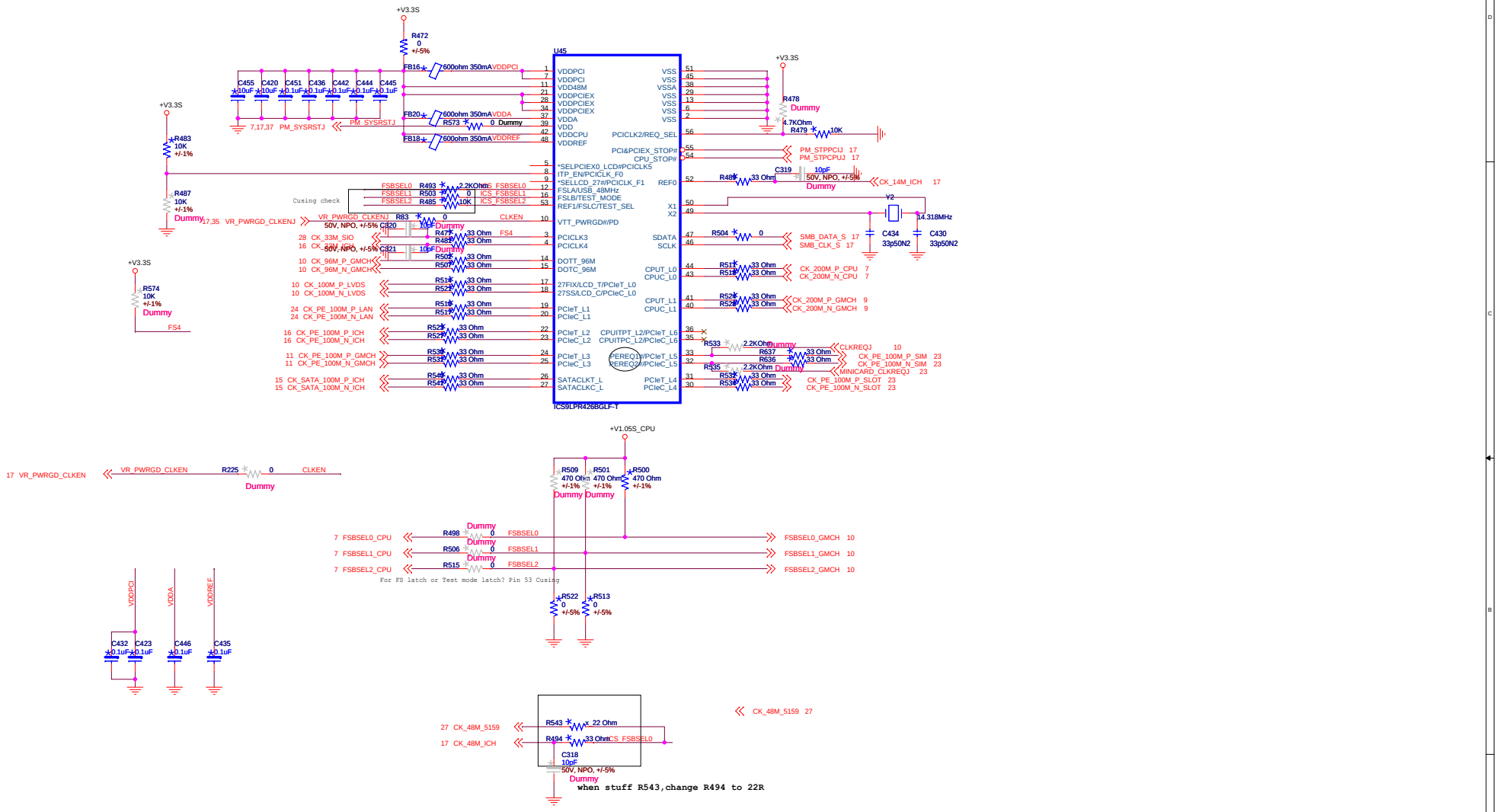
Title	<Title>		
Size C	Document Number <Doc>		Rev <RevCode>
Date: Saturday, March 28, 2009	Sheet 16 of 40		



Title	<Title>	
Size C	Document Number <Doc>	Rev <RevCode>
Date: Saturday, March 28, 2009	Sheet 17 of 40	

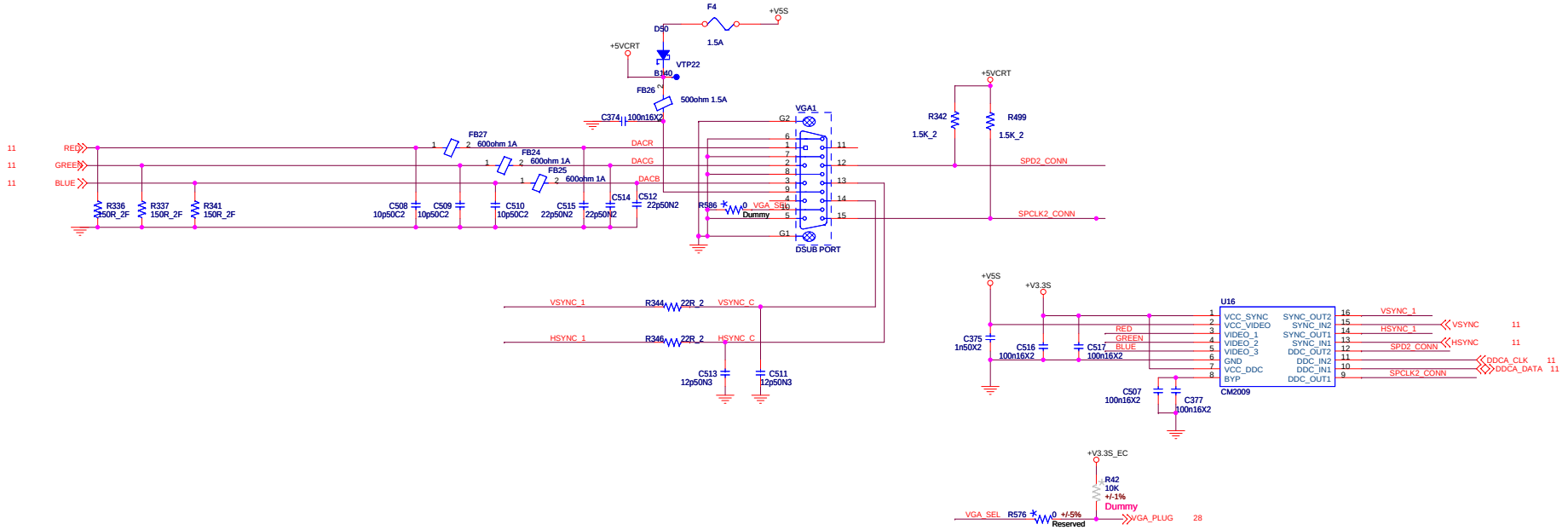

U44F
U44E
Layout note: C366 needs be placed within 100mils of pinAD17 of ICH7 on the bottom side or 140 mils on the top
Layout note: C293 needs be placed within 100mils of pin F6 of ICH7 on the bottom side or 140 mils on the top
Layout note: Place above Caps within 100 mils of ICH on the bottom side or 140 mils on the top near D28,T28,AD28
Place within 100 mils of ICH on the bottom side or 140 mils on the top .
Place within 100 mils of ICH on the bottom side or 140 mils on the top near pin AG5
Place within 100 mils of ICH on the bottom side or 140 mils on the top
Place within 100 mils of ICH on the bottom side or 140 mils on the top near pin AG9
Place within 100 mils of ICH7 on the bottom side or 140 mils on the top near pin
Place within 100 mils of ICH on the bottom side or 140 mils on the top
Place within 100 mils of ICH on the bottom side or 140 mils on the top
Title
<Title>
Size C
Document Number <Doc>
Rev <RevCode>
Date: Wednesday, February 18, 2009
Sheet 18 of 40

Title	<Title>	
Size: C	Document Number: <Doc>	Rev: <RevCode>
Date: Wednesday, February 18, 2009	Sheet 19 of 40	



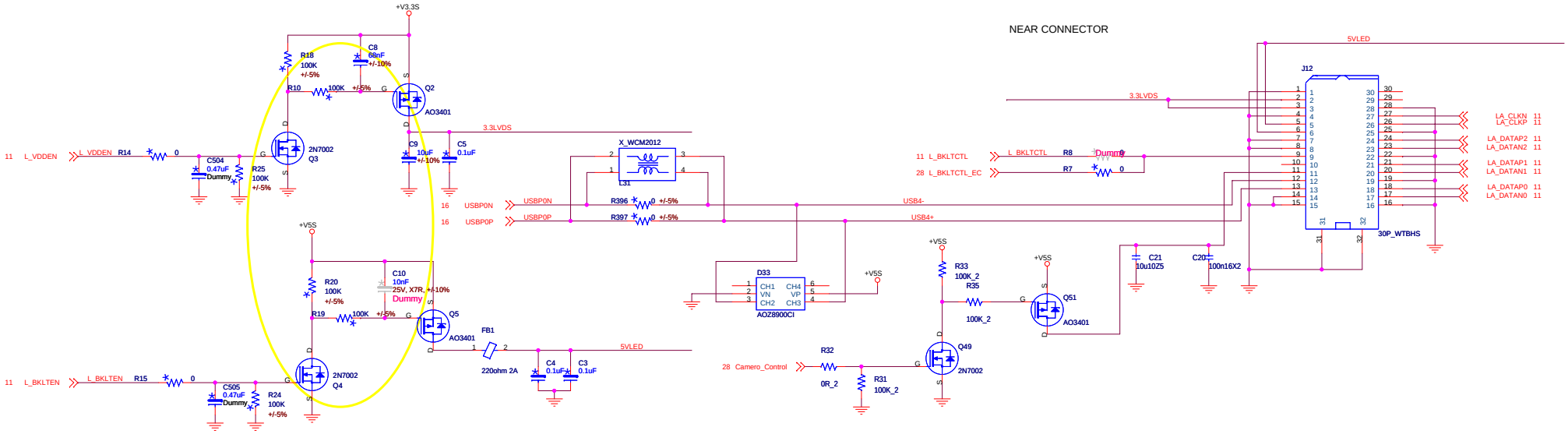
Title	<Title>	
Size C	Document Number <Doc>	Rev <RevCode>
Date: Saturday, March 28, 2009	Sheet 20 of 40	

RGB routing
1. from GMCH to the first 150 ohm resistor: 12 mils(min. 6 mils spacing)
2. from the first 150 ohm res. to the second 150 ohm resistor: 7 mils
3. from the second 150 ohm resistor to connector: 4 mils
4. spacing minimum 6 mils, 30 mils spacing is recommended
5. R,G,B should be length matched to 200 mils, max. length is 8400 mils
6. R,G,B signals should be ground referenced

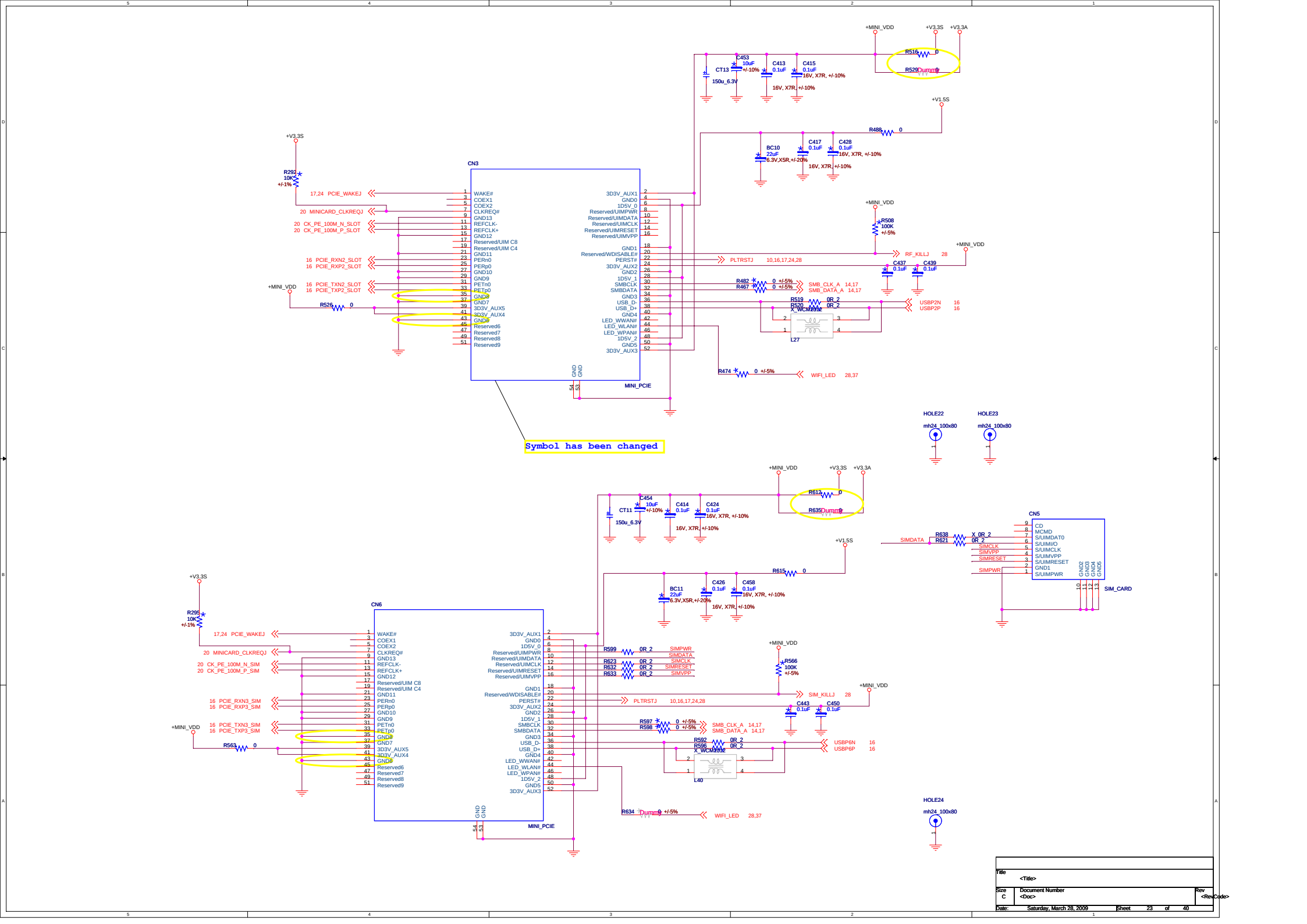


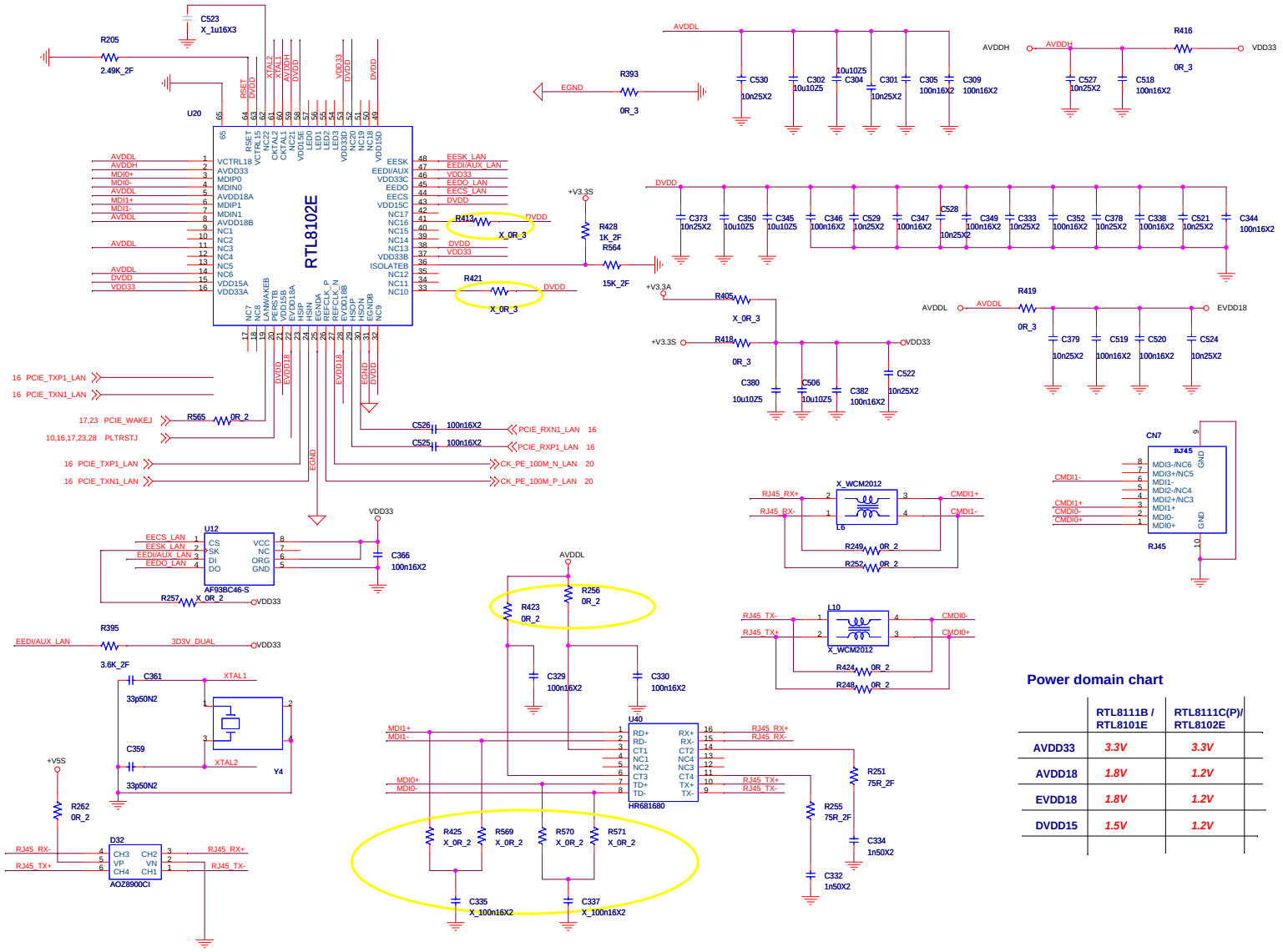
The 150 Ohm resistors near VGA connector and minimizing length to filter. The filters to VGA connector maximum distance 800 mils.

Title	<Title>	
Size C	Document Number <Doc>	Rev <RevCode>
Date: Saturday, March 28, 2009	Sheet 21 of 40	



Title	<Title>	
Size C	Document Number <Doc>	Rev <RevCode>
Date: Saturday, March 28, 2009	Sheet 22 of 40	

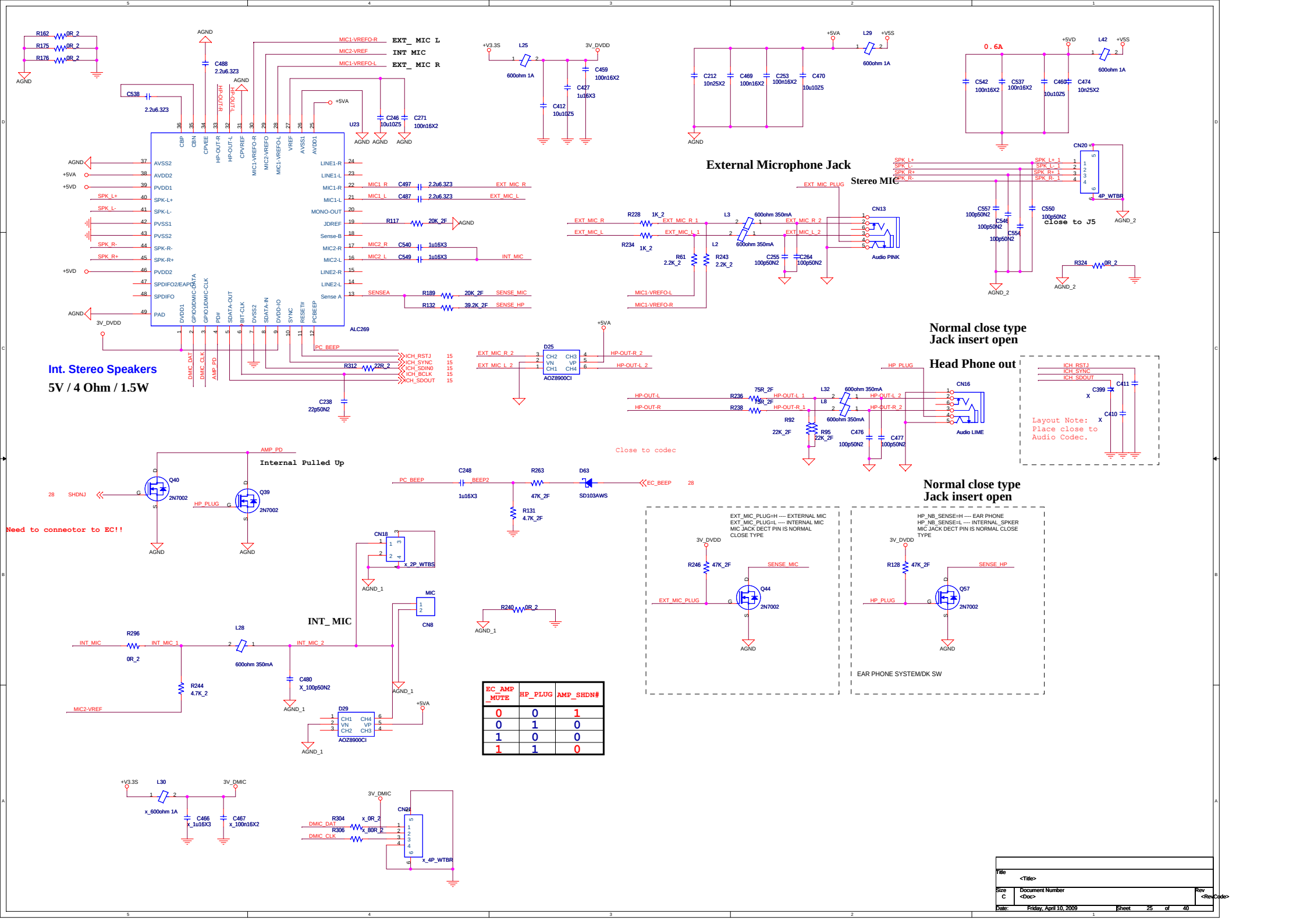

+MINI_VDD
+V3.3S
+V3.3A
+V1.5S
CN3
MINI_PCIE
WAKE#
COEX1
COEX2
CLKREQ#
GND13
REFCLK-
REFCLK+
GND12
Reserved/UIM C8
Reserved/UIM C4
GND11
PERn0
PERp0
GND10
GND9
PETn0
PETp0
GND8
GND7
3D3V_AUX5
3D3V_AUX4
GND6
Reserved6
Reserved7
Reserved8
Reserved9
3D3V_AUX1
GND0
1D5V_0
Reserved/UIMPWR
Reserved/UIMDATA
Reserved/UIMCLK
Reserved/UIMRESET
Reserved/UIMVPP
GND1
Reserved/WDISABLE#
PERST#
3D3V_AUX2
GND2
1D5V_1
SMBCLK
SMBDATA
GND3
USB_D-
USB_D+
GND4
LED_WWAN#
LED_WLAN#
LED_WPAN#
1D5V_2
GND5
3D3V_AUX3
17,24 PCIE_WAKEJ
20 MINICARD_CLKREQJ
20 CK_PE_100M_N_SLOT
20 CK_PE_100M_P_SLOT
16 PCIE_RXN2_SLOT
16 PCIE_RXP2_SLOT
16 PCIE_TXN2_SLOT
16 PCIE_TXP2_SLOT
PLTRSTJ 10,16,17,24,28
RF_KILLJ 28
SMB_CLK_A 14,17
SMB_DATA_A 14,17
USBP2N 16
USBP2P 16
WIFI_LED 28,37
Symbol has been changed
HOLE22
HOLE23
HOLE24
mh24_100x80
CN5
SIM_CARD
CD
MCMD
S/UIMDAT0
S/UIM/O
S/UIMCLK
S/UIMVPP
S/UIMRESET
GND1
S/UIMPWR
SIMDATA
SIMCLK
SIMVPP
SIMRESET
SIMPWR
CN6
SIM_KILLJ 28
USBP6N 16
USBP6P 16
Title
<Title>
Size C
Document Number <Doc>
Rev <RevCode>
Date: Saturday, March 28, 2009
Sheet 23 of 40

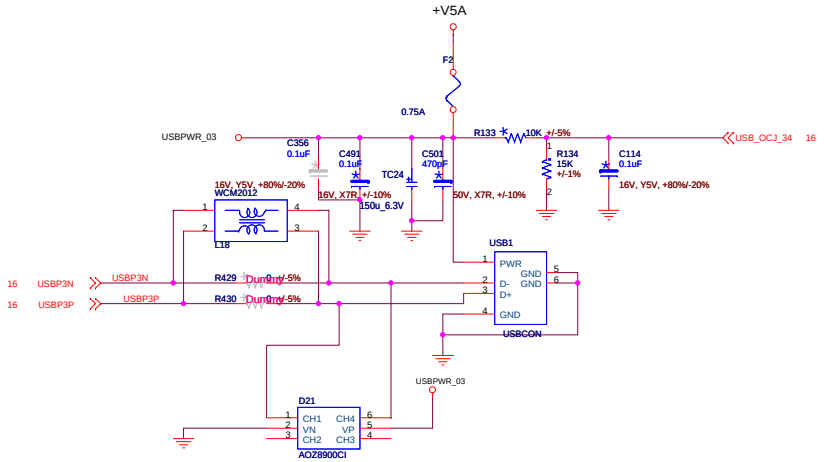


Power domain chart

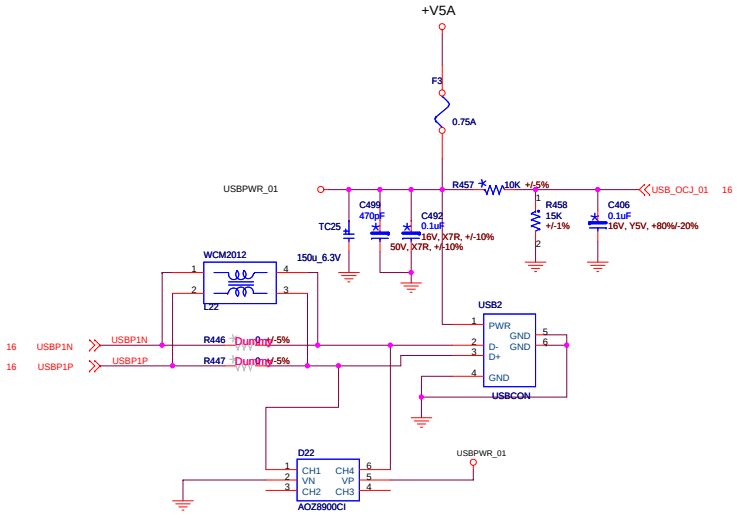
	RTL8111B / RTL8101E	RTL8111C(P)/ RTL8102E
AVDD33	3.3V	3.3V
AVDD18	1.8V	1.2V
EVDD18	1.8V	1.2V
DVDD15	1.5V	1.2V

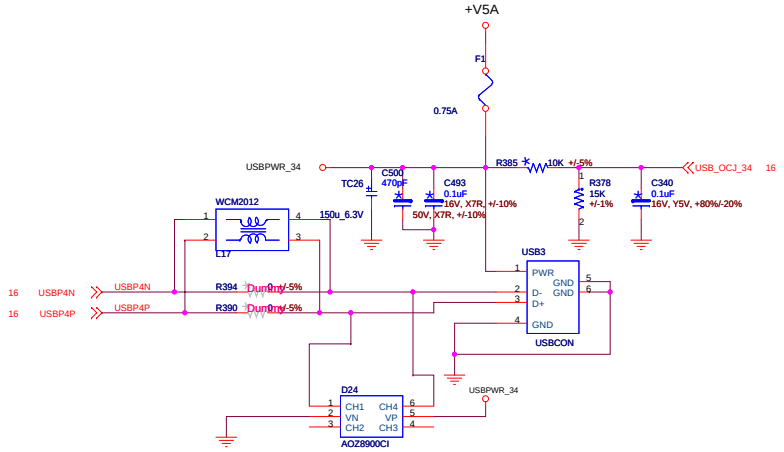
Title	<Title>	
Size C	Document Number <Doc>	Rev <RevCode>
Date: Monday, April 13, 2009	Sheet 24 of 40	


R162 0R_2
R175 0R_2
R176 0R_2
AGND
C488 2.2u6.3Z3
C538 2.2u6.3Z3
MIC1-VREFO-R
MIC2-VREF
MIC1-VREFO-L
EXT_ MIC L
INT MIC
EXT_ MIC R
HP-OUT-R
HP-OUT-L
+5VA
C246 10u10Z5
C271 100n16X2
U23
ALC269
AVSS2
AVDD2
PVDD1
SPK-L+
SPK-L-
PVSS1
PVSS2
SPK-R-
SPK-R+
PVDD2
SPDIFO2/EAPD
SPDIFO
PAD
LINE1-R
LINE1-L
MIC1-R
MIC1-L
MONO-OUT
JDREF
Sense-B
MIC2-R
MIC2-L
LINE2-R
LINE2-L
Sense A
MIC1_R C497 2.2u6.3Z3 EXT_MIC_R
MIC1_L C487 2.2u6.3Z3 EXT_MIC_L
R117 20K_2F
MIC2_R C540 1u16X3
MIC2_L C549 1u16X3 INT_MIC
SENSEA R189 20K_2F SENSE_MIC
R132 39.2K_2F SENSE_HP
3V_DVDD
PC_BEEP
R312 22R_2
C238 22p50N2
ICH_RSTJ
ICH_SYNC
ICH_SDIN0
ICH_BCLK
ICH_SDOUT
DMIC_DAT
DMIC_CLK
AMP_PD
Int. Stereo Speakers
5V / 4 Ohm / 1.5W
+V3.3S L25 600ohm 1A
3V_DVDD
C459 100n16X2
C427 1u16X3
C412 10u10Z5
+5VA L29 600ohm 1A +VSS
C212 10n25X2
C469 100n16X2
C253 100n16X2
C470 10u10Z5
0.6A
+5VD L42 600ohm 1A +VSS
C542 100n16X2
C537 100n16X2
C460 10u10Z5
C474 10n25X2
External Microphone Jack
Stereo MIC
EXT_MIC_PLUG
CN13
Audio PINK
R228 1K_2
R234 1K_2
L3 600ohm 350mA
L2 600ohm 350mA
R61 2.2K_2
R243 2.2K_2
C255 100p50N2
C264 100p50N2
MIC1-VREFO-L
MIC1-VREFO-R
CN20
SPK_L+ 1
SPK_L- 1
SPK_R+ 1
SPK_R- 1
4P_WTBR
C557 100p50N2
C546 100p50N2
C554 100p50N2
C550 100p50N2
close to J5
AGND_2
R324 0R_2
Normal close type
Jack insert open
Head Phone out
D25
AOZ8900CI
HP-OUT-R_2
HP-OUT-L_2
HP_PLUG
CN16
Audio LIME
R236 75R_2F
R238 75R_2F
L32 600ohm 350mA
L8 600ohm 350mA
R92 22K_2F
R95 22K_2F
C476 100p50N2
C477 100p50N2
ICH_RSTJ
ICH_SYNC
ICH_SDOUT
C399
C411
C410
Layout Note:
Place close to
Audio Codec.
Close to codec
Internal Pulled Up
AMP_PD
Q40 2N7002
Q39 2N7002
SHDNJ
HP_PLUG
Need to conneotor to EC!!
C248 1u16X3
R263 47K_2F
D63 SD103AWS
BEEP2
EC_BEEP
R131 4.7K_2F
Normal close type
Jack insert open
EXT_MIC_PLUG=H ---- EXTERNAL MIC
EXT_MIC_PLUG=L ---- INTERNAL MIC
MIC JACK DECT PIN IS NORMAL
CLOSE TYPE
R246 47K_2F
SENSE_MIC
Q44 2N7002
HP_NB_SENSE=H ---- EAR PHONE
HP_NB_SENSE=L ---- INTERNAL_SPKER
MIC JACK DECT PIN IS NORMAL CLOSE
TYPE
R128 47K_2F
SENSE_HP
Q57 2N7002
EAR PHONE SYSTEM/DK SW
CN18
x_2P_WTBS
MIC
CN8
INT_ MIC
R296 0R_2
L28 600ohm 350mA
R244 4.7K_2
C480 X_100p50N2
D29 AOZ8900CI
R240 0R_2
EC_AMP_MUTE | HP_PLUG | AMP_SHDN#
0 | 0 | 1
0 | 1 | 0
1 | 0 | 0
1 | 1 | 0
+V3.3S L30 x_600ohm 1A
3V_DMIC
C466 x_1u16X3
C467 x_100n16X2
R304 x_0R_2
R306 x_80R_2
CN21
x_4P_WTBR
Title
<Title>
Size C
Document Number
<Doc>
Rev
<RevCode>
Date: Friday, April 10, 2009
Sheet 25 of 40

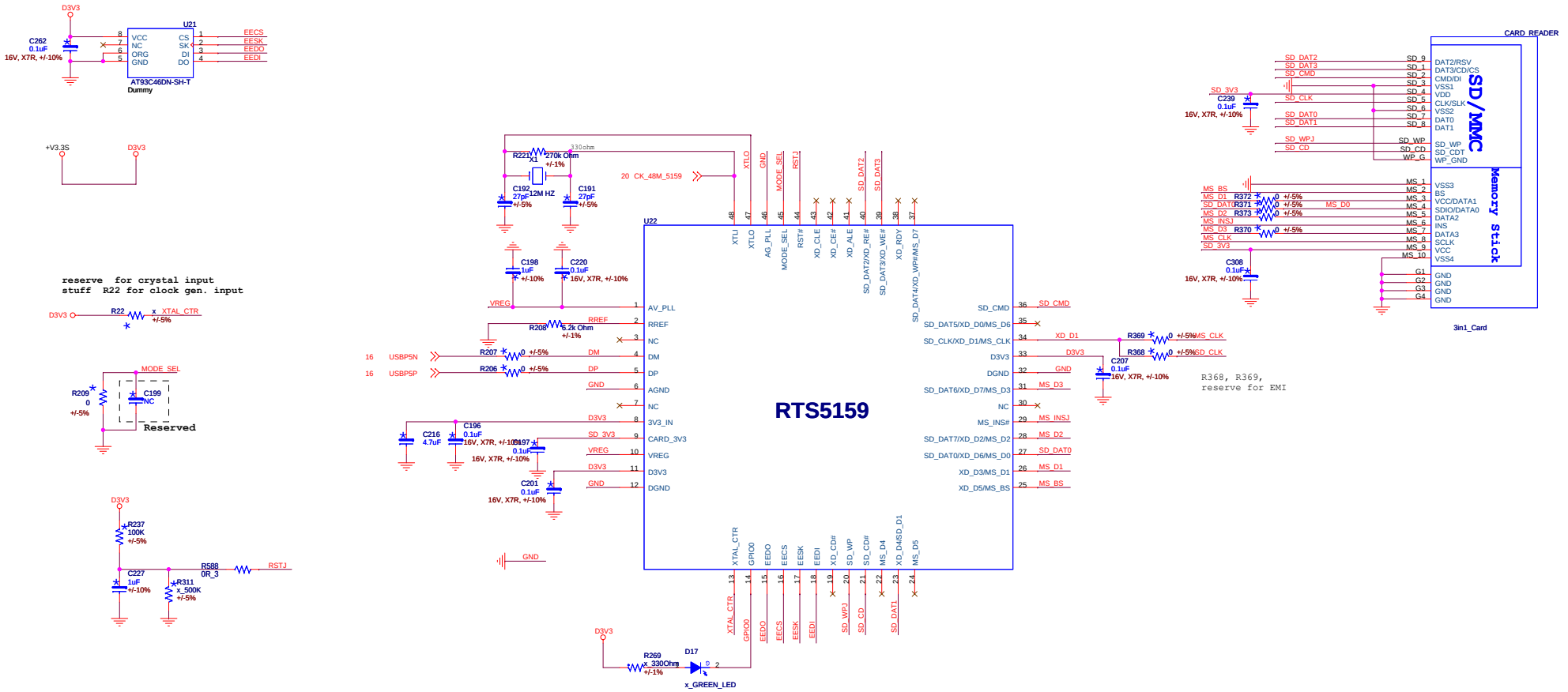


Blue tooth





Title	<Title>	
Size C	Document Number <Doc>	Rev <RevCode>
Date: Saturday, March 28, 2009	Sheet 26 of 40	



Title	<Title>	
Size C	Document Number <Doc>	Rev <RevCode>
Date: Thursday, April 16, 2009	Sheet 27 of 40	

Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.
Note 2 :
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.

ITE confirm why there is no LDRQ

IT8512E_J

Note:Please do not place any pull-up resistor on GPG0,G2 and GPG6(Reserved hardware strapping)

FLASH TYPE SELECT
Pull High: LPC/FWH FLASH
Pull Down: SPI FLASH

32.768kHz clock lines:
a. If possible, please avoid using any through-hole.
b. Please make the trace length short, and the trace width wide enough.
c. The spacing to the closest neighbor should be wide enough.

PS/2 Interface (3.3V CMOS I/F, 5V tolerant)

Debug port : For LPC debug only

SPI Interface

TM FUNCTION: Pull Up: ENABLE TMKBC Pull Down: DISABLE TMKBC

Reserved or not

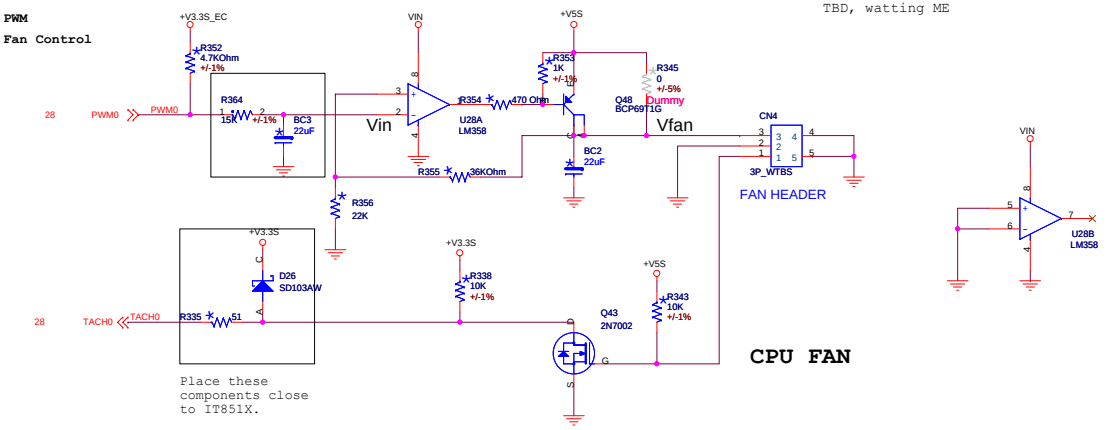
For Input Pin

Title	<Title>
Size C	Document Number <Doc>
Rev	<RevCode>
Date:	Friday, April 10, 2009
Sheet	28 of 40

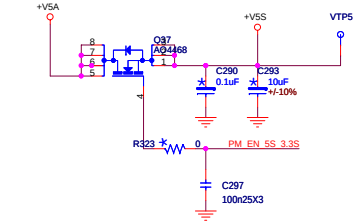
PWM

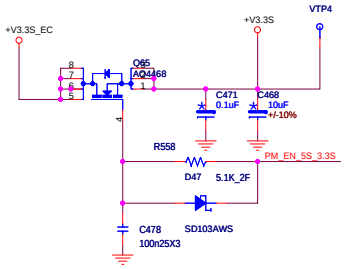
Fan Control

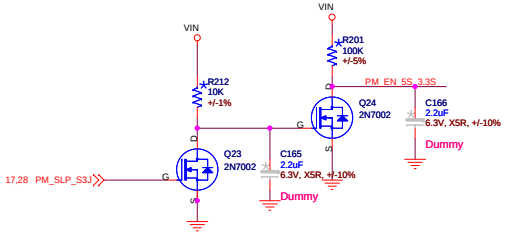
TBD, watting ME

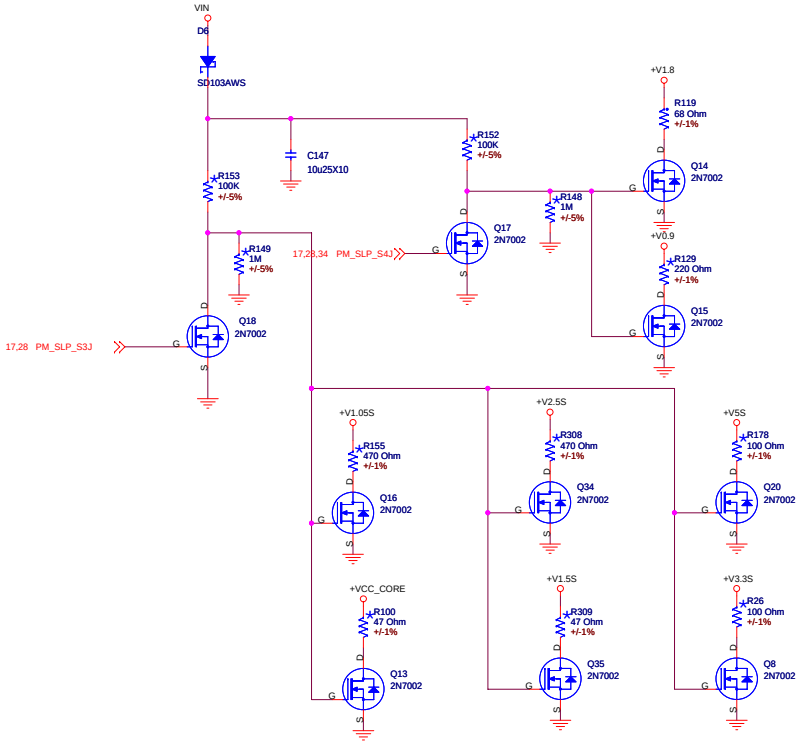


Title	<Title>	
Size C	Document Number <Doc>	Rev <RevCode>
Date: Saturday, March 28, 2009	Sheet 29 of 40	

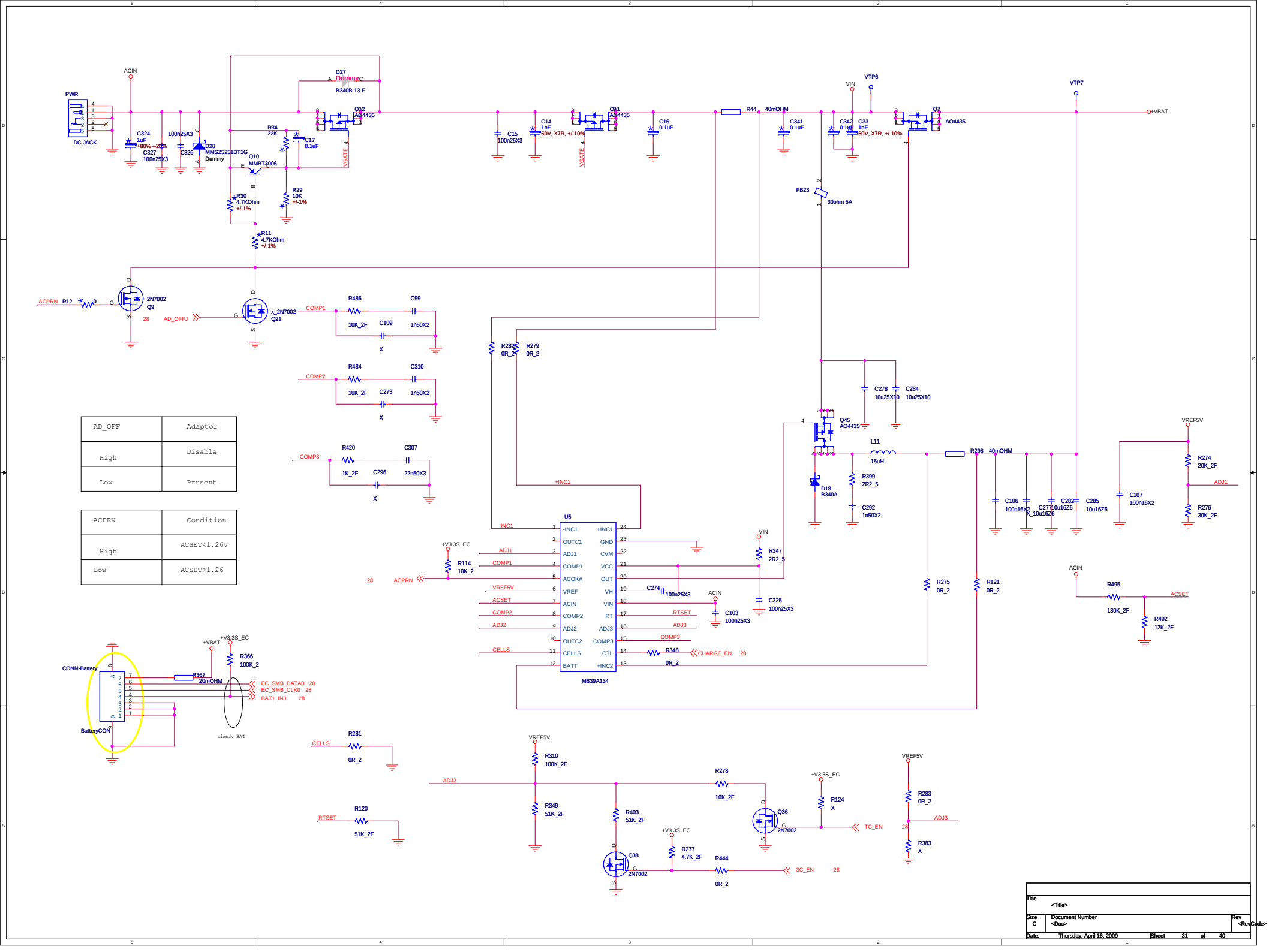








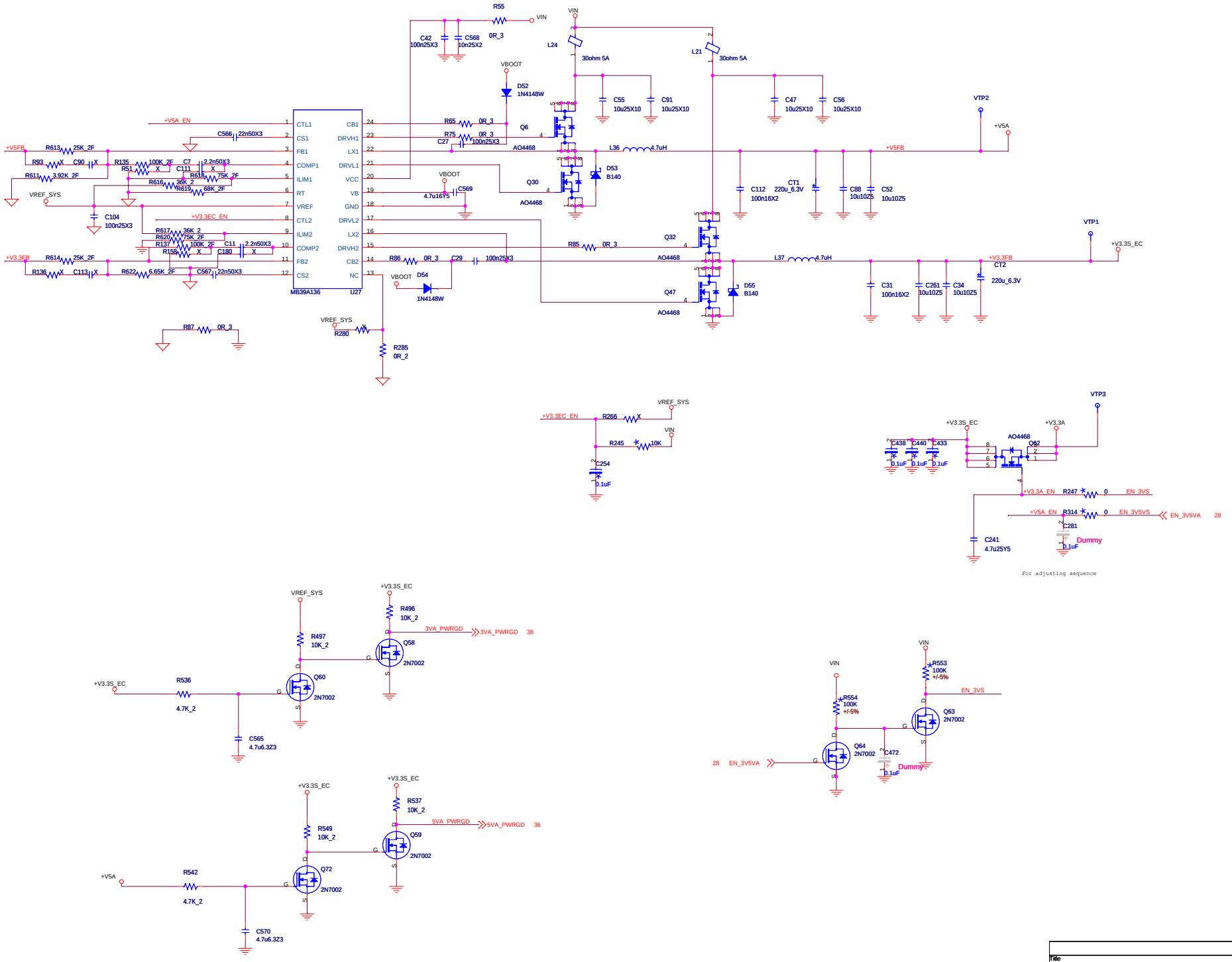
Title	<Title>	
Size C	Document Number <Doc>	Rev <RevCode>
Date: Saturday, March 28, 2009	Sheet 30 of 40	



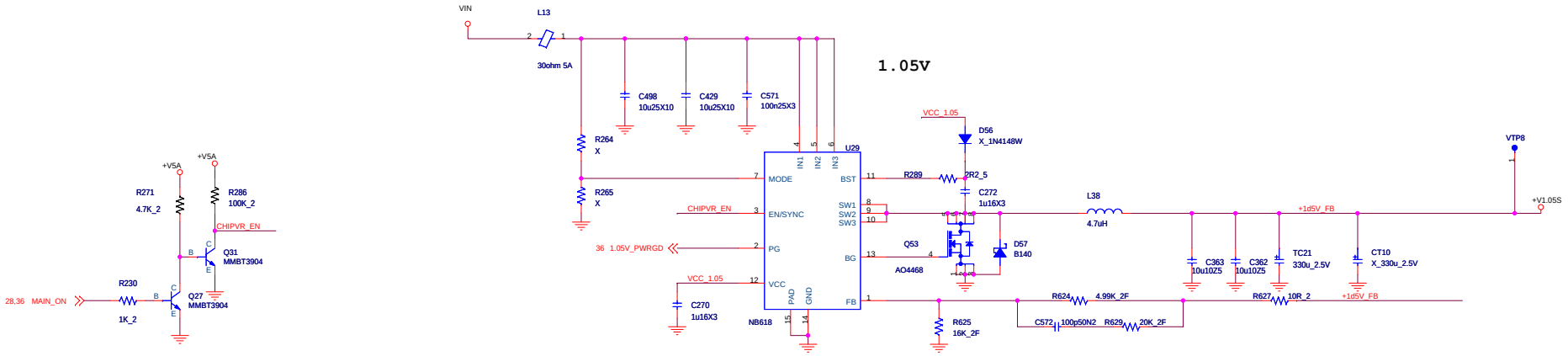
AD_OFF	Adaptor
High	Disable
Low	Present

ACPRN	Condition
High	ACSET<1.26v
Low	ACSET>1.26

Title	<Title>		
Size C	Document Number <Doc>		Rev <RevCode>
Date: Thursday, April 16, 2009		Sheet 31 of 40	

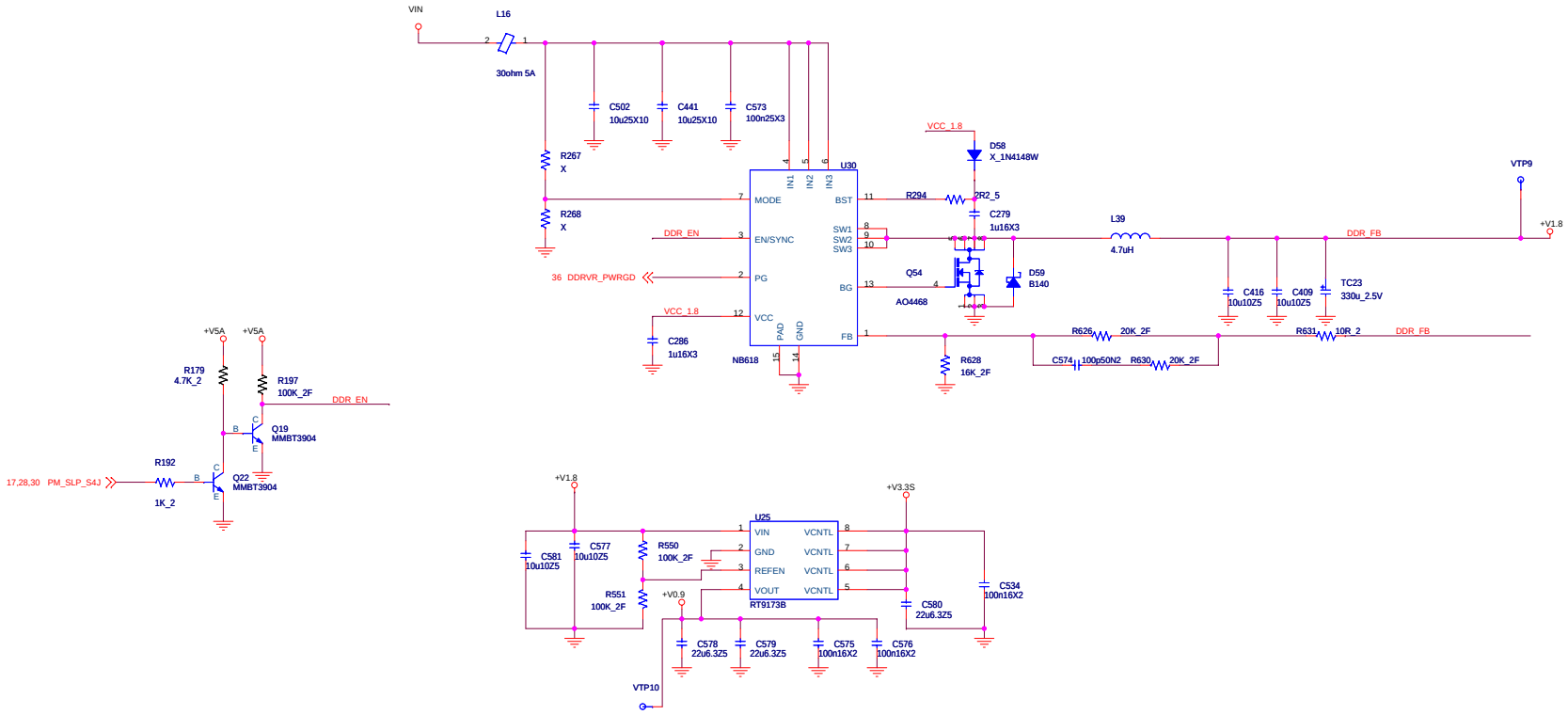


Title	<Title>	
Size C	Document Number <Doc>	Rev <RevCode>
Date: Wednesday, April 15, 2009	Sheet 32 of 40	

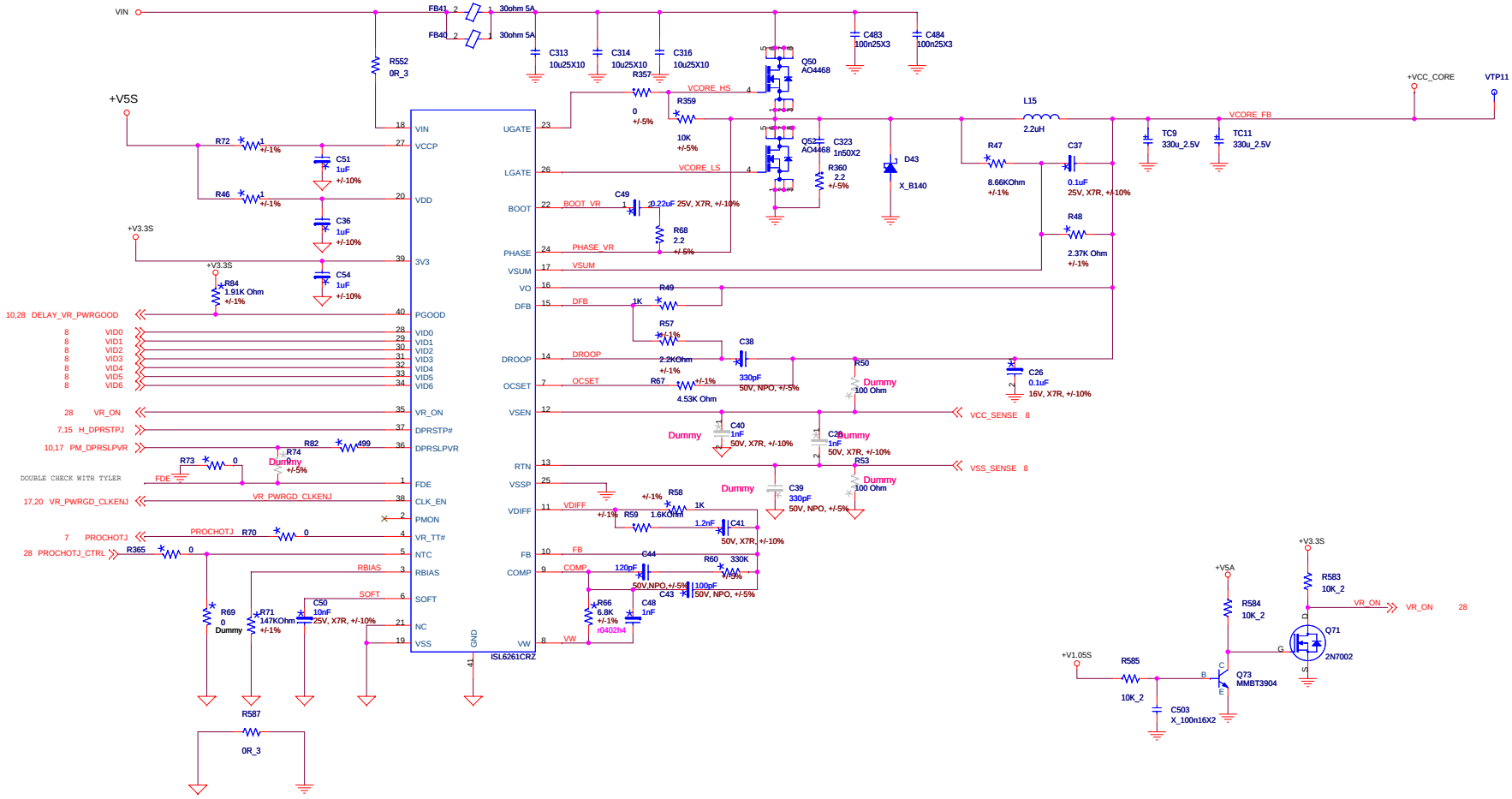


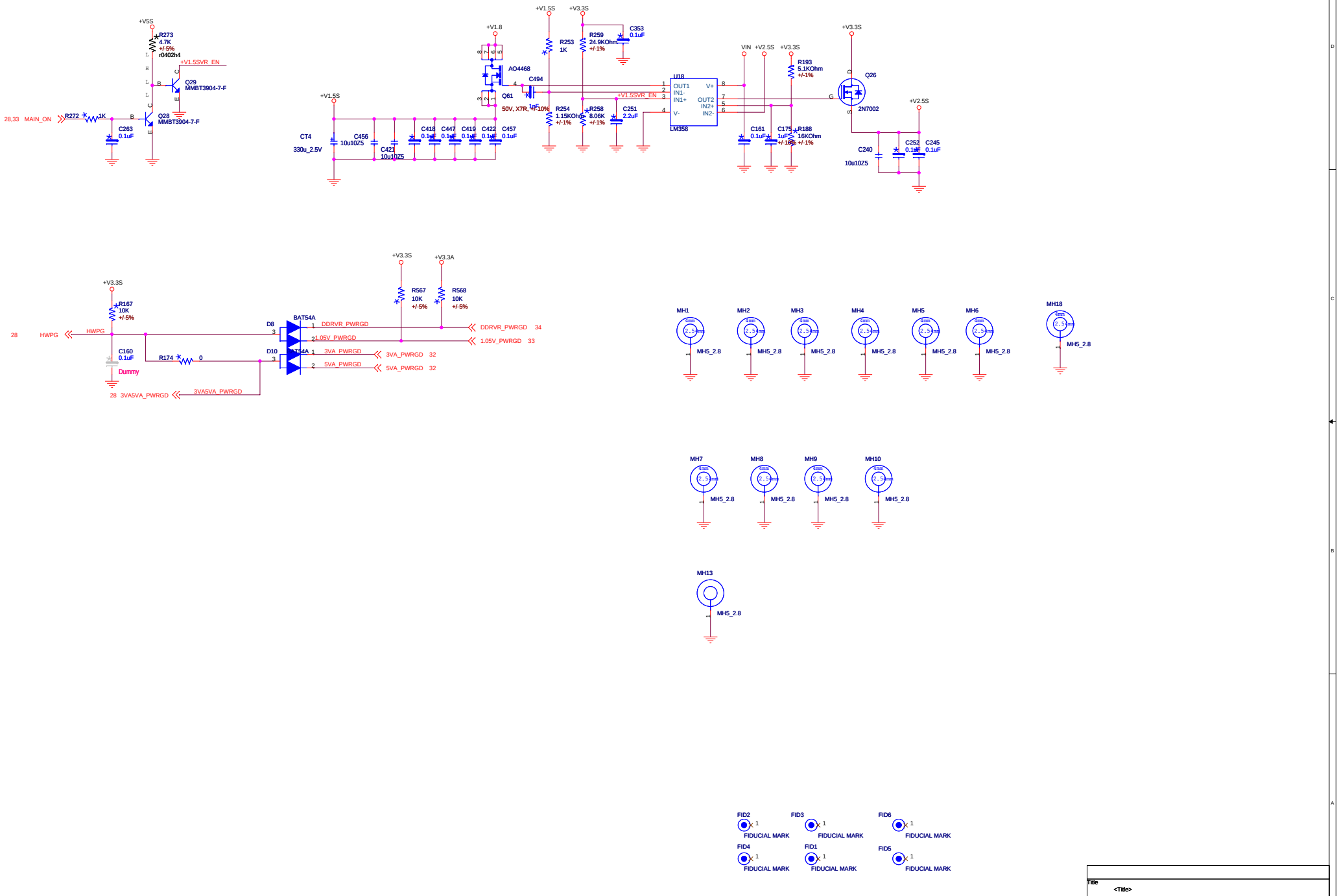
Title	<Title>	
Size C	Document Number <Doc>	Rev <RevCode>
Date: Saturday, March 28, 2009	Sheet 33 of 40	

1.8V

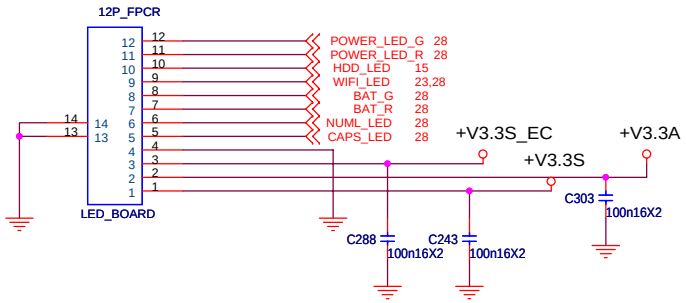


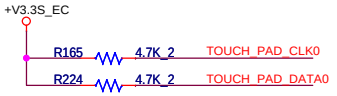
Title	<Title>	
Size C	Document Number <Doc>	Rev <RevCode>
Date: Saturday, March 28, 2009	Sheet 34 of 40	

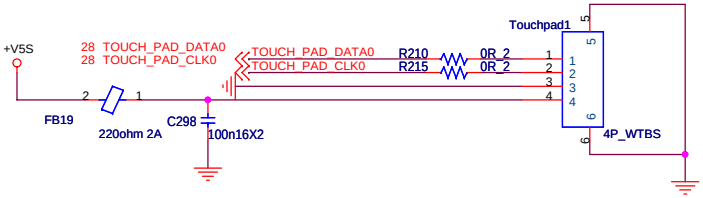

VIN
FB41 30ohm 5A
FB40 30ohm 5A
C313 10u25X10
C314 10u25X10
C316 10u25X10
C483 100n25X3
C484 100n25X3
R552 0R_3
+V5S
Q50 AO4468
Q52 AO4468
C323 1n50X2
R357
R359 0 +/-5%
VCORE_HS
VCORE_LS
R360 2.2 +/-5%
D43 X_B140
L15 2.2uH
VCORE_FB
+VCC_CORE
VTP11
TC9 330u_2.5V
TC11 330u_2.5V
R47 8.66KOhm +/-1%
C37 0.1uF 25V, X7R, +/-10%
R48 2.37K Ohm +/-1%
R72 1 +/-1%
R46 1 +/-1%
C51 1uF +/-10%
C36 1uF +/-10%
C54 1uF +/-10%
+V3.3S
R84 1.91K Ohm +/-1%
R68 2.2 +/-5%
C49 0.22uF 25V, X7R, +/-10%
R49 1K
R57 +/-1%
2.2KOhm +/-1%
C38 330pF 50V, NPO, +/-5%
R67 +/-1% 4.53K Ohm
R50 Dummy 100 Ohm
C26 0.1uF 16V, X7R, +/-10%
VCC_SENSE 8
C40 1nF 50V, X7R, +/-10%
C28 Dummy 1nF 50V, X7R, +/-10%
R53 Dummy 100 Ohm
VSS_SENSE 8
C39 330pF 50V, NPO, +/-5%
R58 1K
R59 1.6KOhm
C41 1.2nF 50V, X7R, +/-10%
C44 120pF 50V,NPO,+/-5%
R60 330K +/-5%
C43 100pF 50V, NPO, +/-5%
R66 6.8K +/-1%
C48 1nF
r0402h4
R69 0 Dummy
R71 147KOhm +/-1%
C50 10nF 25V, X7R, +/-10%
R587 0R_3
R74 Dummy +/-5%
R73 0
R82 499
R70 0
R365 0
DOUBLE CHECK WITH TYLER
10,28 DELAY_VR_PWRGOOD
8 VID0
8 VID1
8 VID2
8 VID3
8 VID4
8 VID5
8 VID6
28 VR_ON
7,15 H_DPRSTPJ
10,17 PM_DPRSLPVR
FDE
17,20 VR_PWRGD_CLKENJ
7 PROCHOTJ
28 PROCHOTJ_CTRL
RBIAS
SOFT
VIN
VCCP
VDD
3V3
PGOOD
VID0
VID1
VID2
VID3
VID4
VID5
VID6
VR_ON
DPRSTP#
DPRSLPVR
FDE
CLK_EN
PMON
VR_TT#
NTC
RBIAS
SOFT
NC
VSS
GND
UGATE
LGATE
BOOT
PHASE
VSUM
VO
DFB
DROOP
OCSET
VSEN
RTN
VSSP
VDIFF
FB
COMP
VW
ISL6261CRZ
+V1.05S
R585 10K_2
C503 X_100n16X2
+V5A
R584 10K_2
R583 10K_2
Q71 2N7002
Q73 MMBT3904
VR_ON
28
Title
<Title>
Size C
Document Number <Doc>
Rev <RevCode>
Date: Monday, April 13, 2009
Sheet 35 of 40

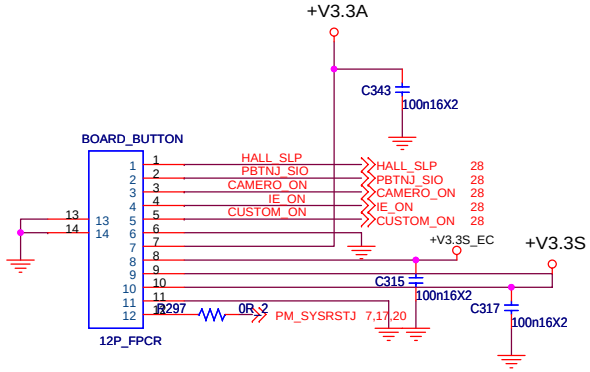


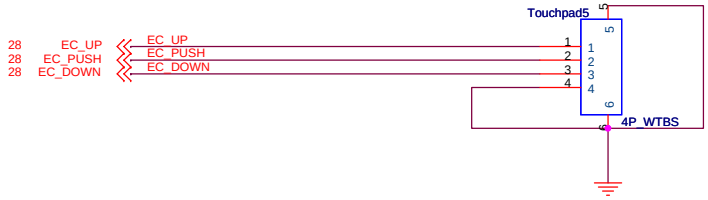
Title	<Title>	
Size C	Document Number <Doc>	Rev <RevCode>
Date: Saturday, March 28, 2009	Sheet 36 of 40	





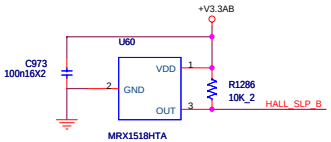


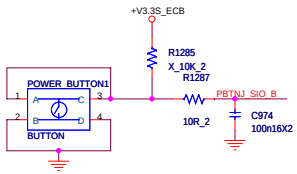


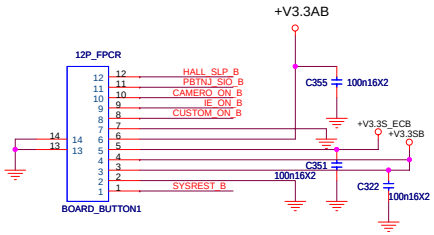


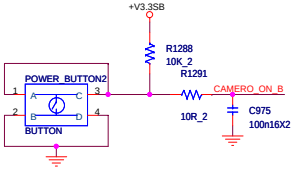
Title	<Title>	
Size: Custom	Document Number: <Doc>	Rev: <RevCode>
Date: Saturday, March 28, 2009	Sheet 37 of 40	

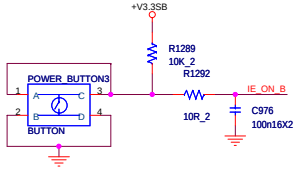
BOM 不上

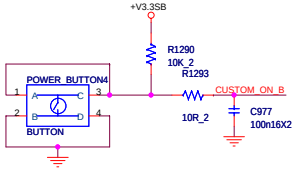


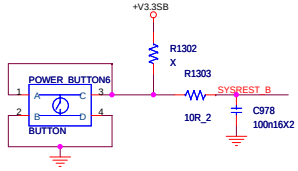


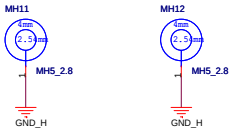


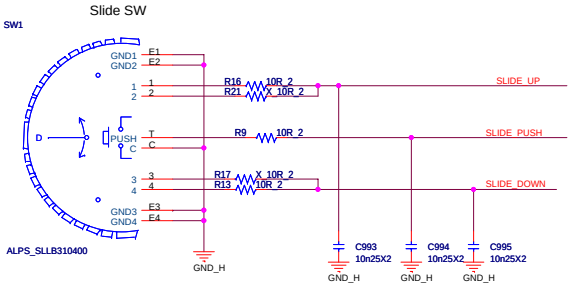


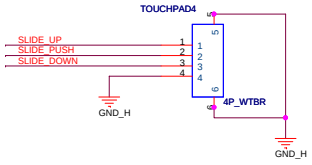




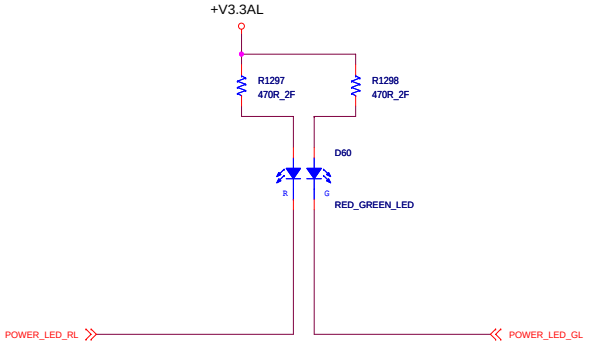


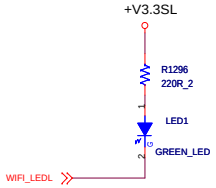


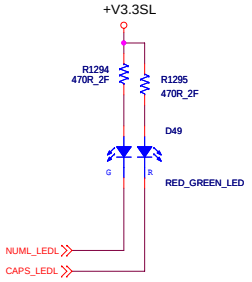


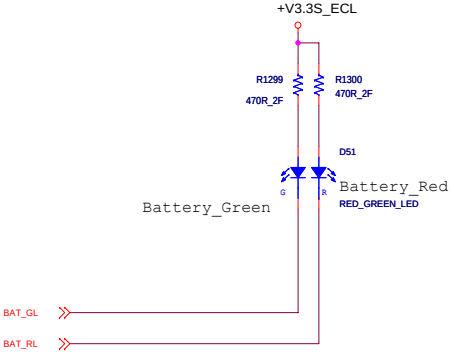


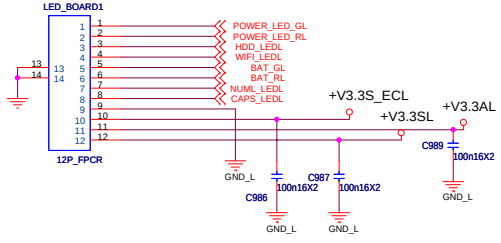
Title	<Title>	
Size C	Document Number <Doc>	Rev <RevCode>
Date: Thursday, April 16, 2009	Sheet 38 of 40	

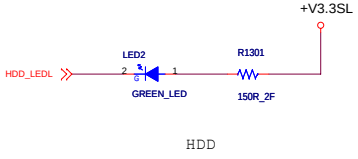


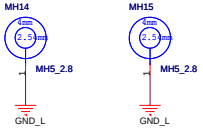






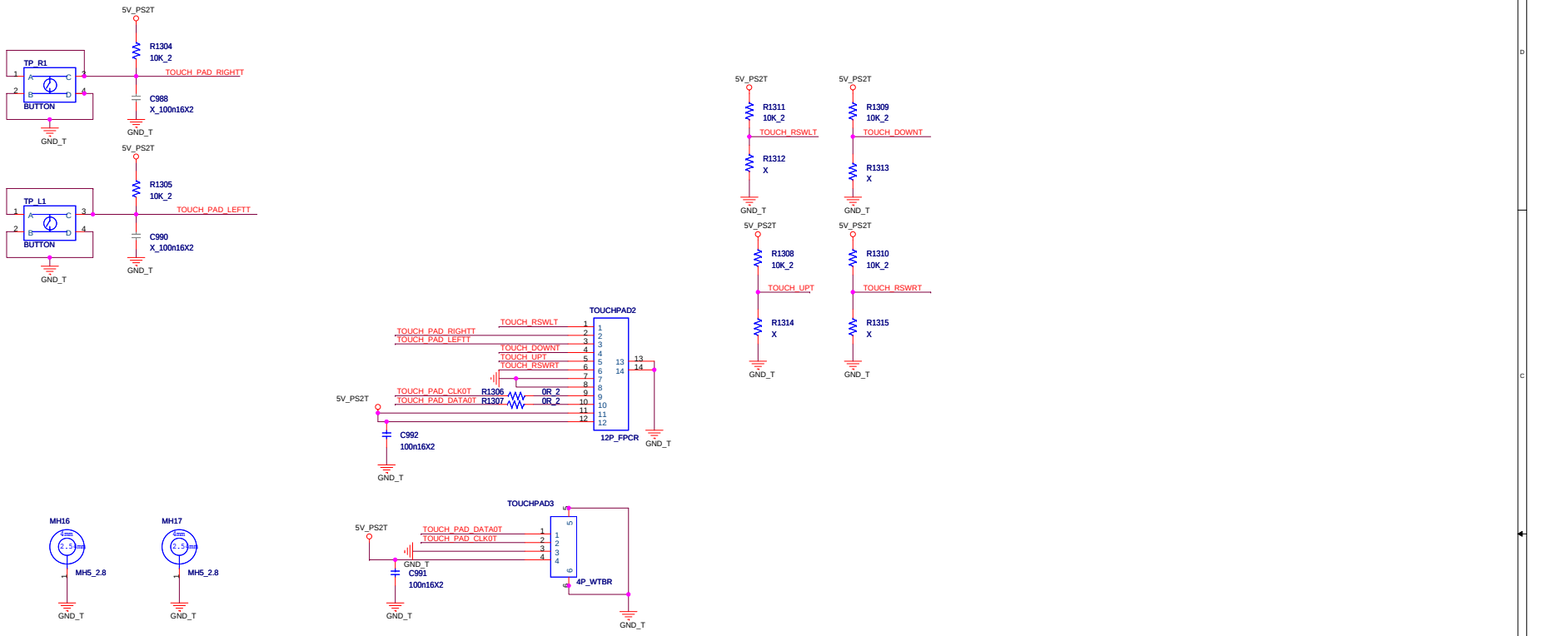






	ON	OFF	REMARK
POWER_LED_G	L	H	GREEN
POWER_LED_R	L	H	RED
WIFI_LED	L	H	GREEN
BAT_G	L	H	GREEN
BAT_R	L	H	RED
CAPS_LED	L	H	RED
NUM_LED	L	H	GREEN

Title	<Title>		
Size C	Document Number <Doc>		Rev <RevCode>
Date: Tuesday, April 14, 2009		Sheet 39 of 40	



Title	<Title>	
Size C	Document Number <Doc>	Rev <RevCode>
Date: Monday, April 13, 2009	Sheet 40 of 40	