

AR5312 Memory Interface

GPIO 0 and 1 used as I2C bus,
GPIO 2,3,4 used to read write NAND Flash
GPIO 5, reserved,
GPIO 6, recover system configuration
GPIO 7, system status LED

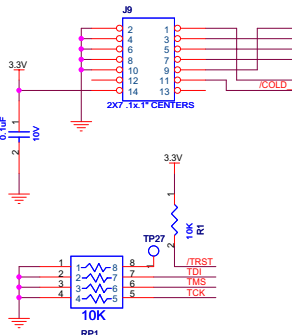
Place a 0.1uF cap by each flash power pin. and a 2.2uF cap close to each.

Flash

AFTER COLD RESET, GPIOs IS ALL 0
USE GPIO2 AS 2nd FLASH ADDR22. IN CASE WE NEED
MORE THAN 24MBYTE FLASH

Place a 0.01uF cap by each sdrum power pin. and a 2.2uF cap close to each chip.

SDRAM



EJTAG

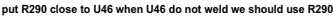
UART_TXDATA1 <-- U0_SOUT
UART_RTS_N1 <-- U0_RTS
UART_CTS_N1 <-- U0_CTS
UART_RXDATA1 <-- U0_SIN

AR5312 EJTAG, GPIOs, UART

DO NOT STUFF

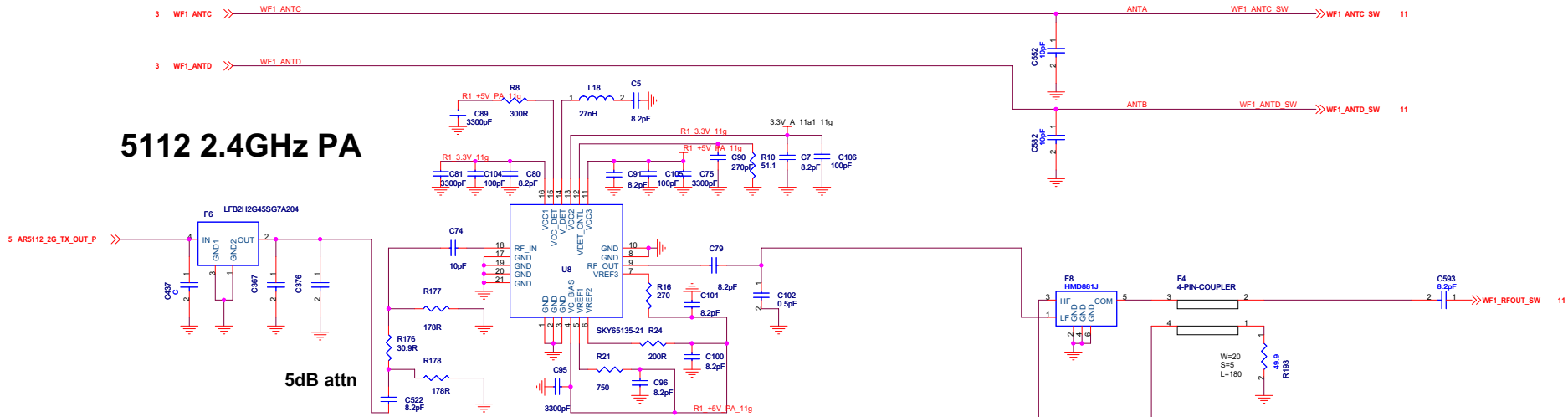
RESET MONITOR

AR5312 Reset, NMI, and Clocks

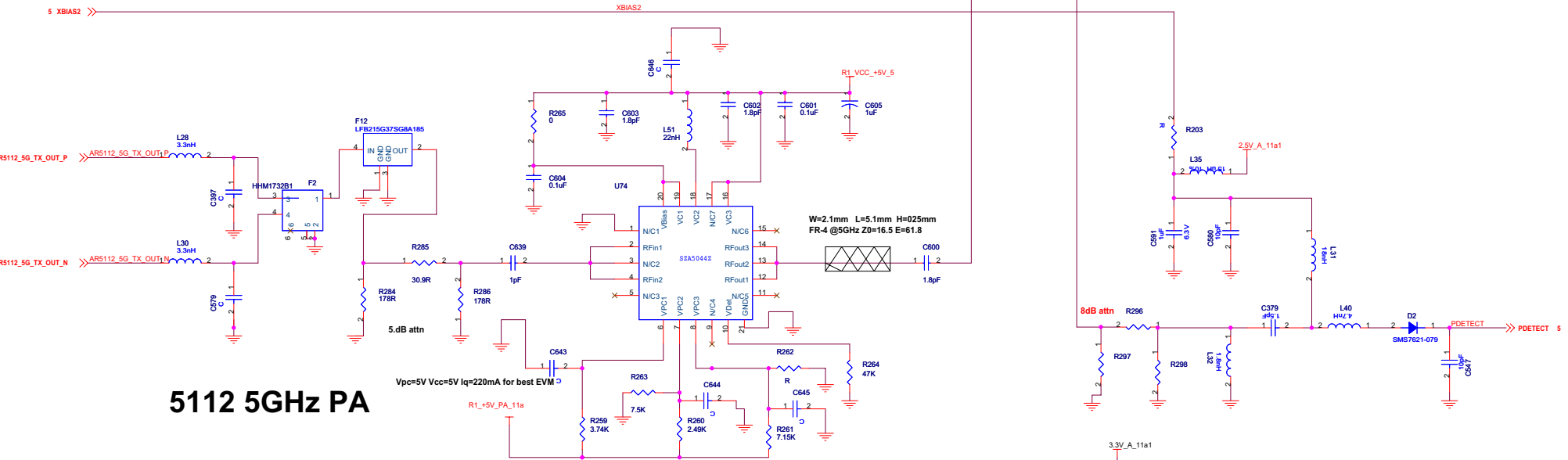


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5112 2.4GHz PA



5112 5GHz PA



V_{pc}=5V V_{cc}=5V I_q=220mA for best EVM

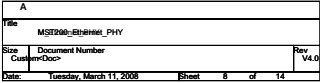
R1_+5V_PA_11a

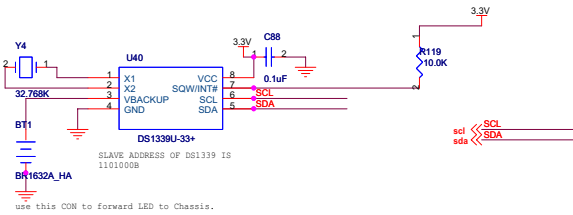
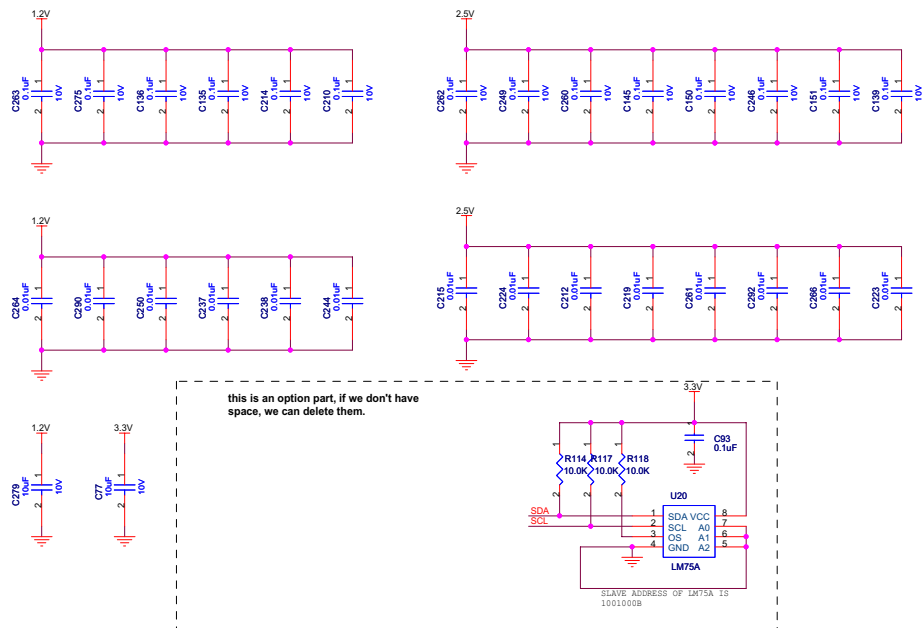
W=2.1mm L=5.1mm H=0.25mm
FR-4 @5GHz Z0=16.5 E=61.8

5112 5GHz PA enable

if WF1_TX5 can o/p from 0V - 2.9V above , then it can be direct connect to VPC of SZA5044

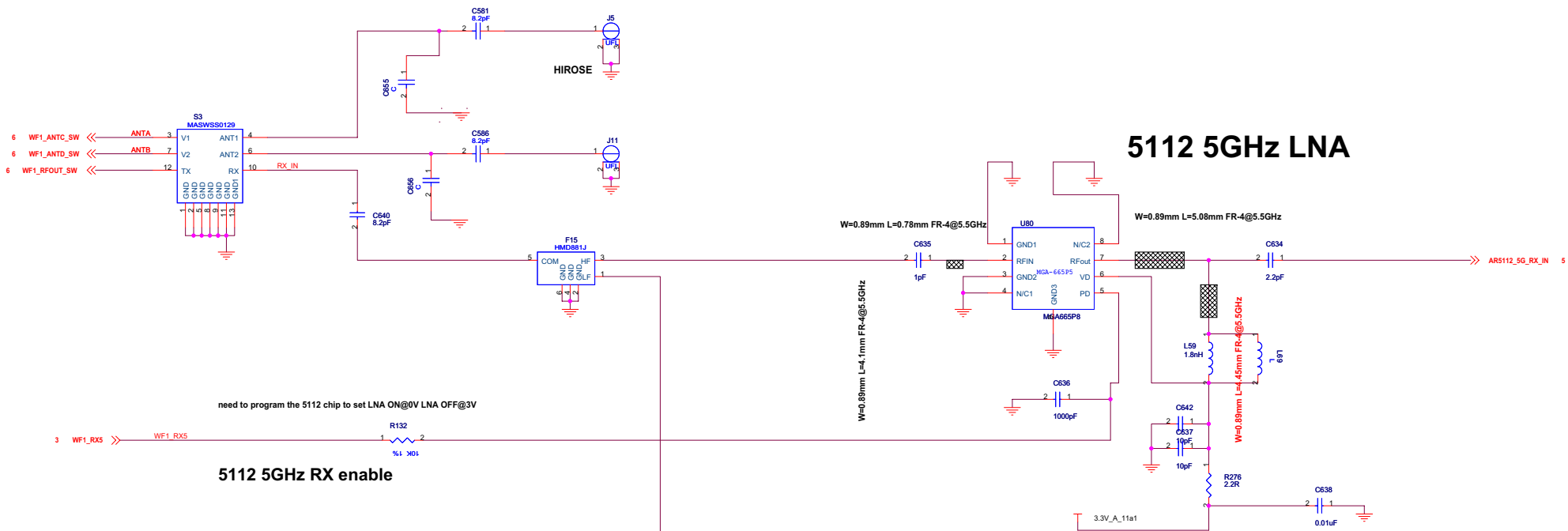
A			
Title MST200; ARS(t2)ne902; Ftabg1_Radio1			
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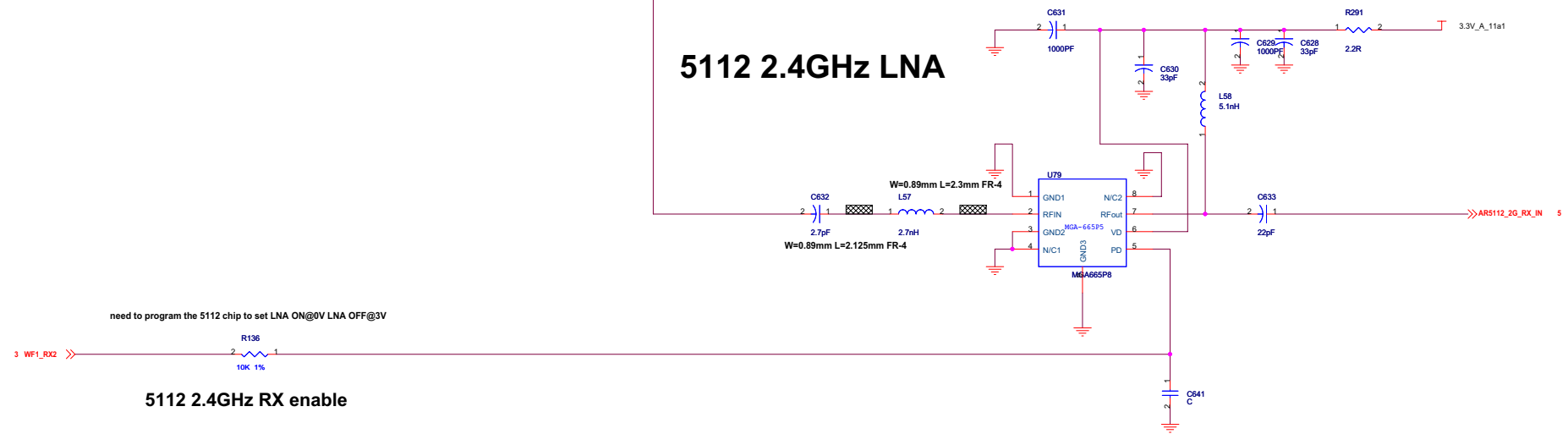


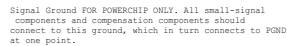
**ATHEROS CONFIDENTIAL
PRELIMINARY**

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5112 2.4GHz LNA





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