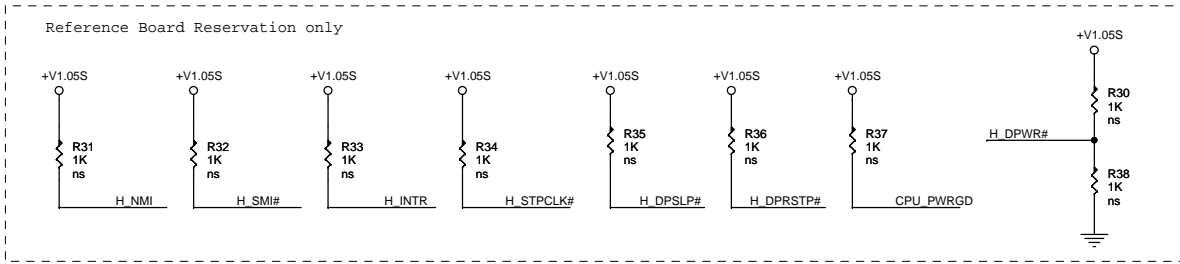


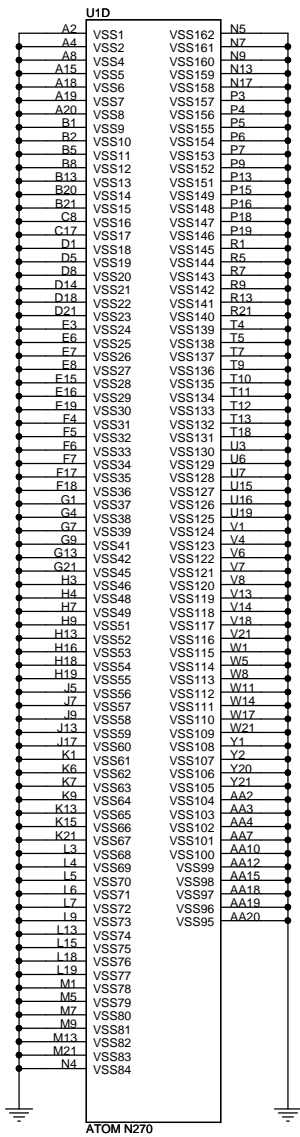
Layout note:
Comp0,2 connect with Zo=27.4 ohm,make
trace length shorter than 0.5''
Comp1,3 connect with Zo=55 ohm,make
trace length shorter than 0.5''

Layout note: Zo=55 ohm,
0.5" max for GTLREF

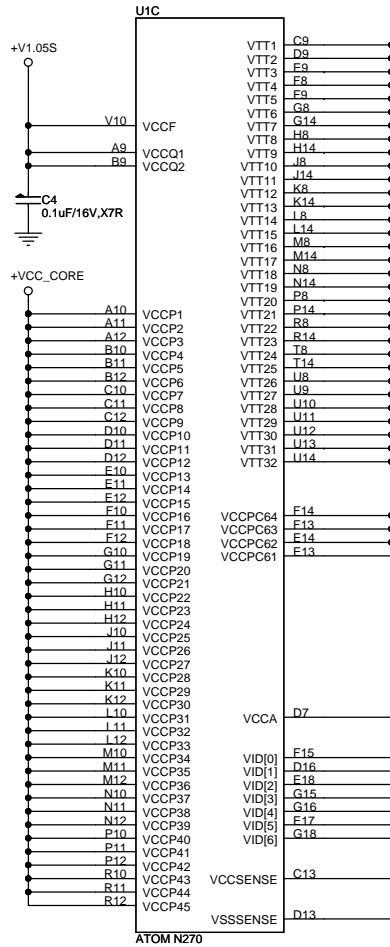
Layout note: Zo=55 ohm,
0.5" max for EXTGBREF

Layout note: Zo=55 ohm,
0.5" max for CMREF

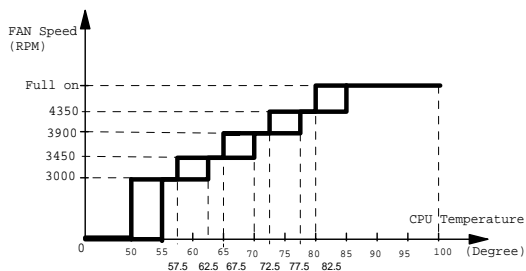
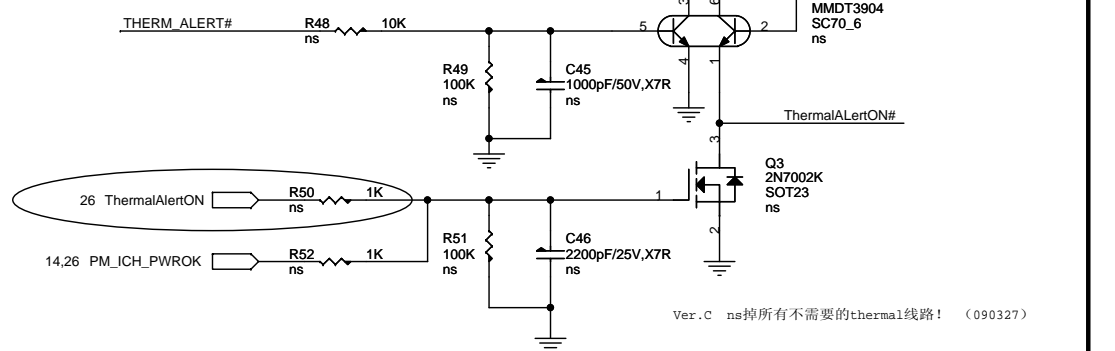
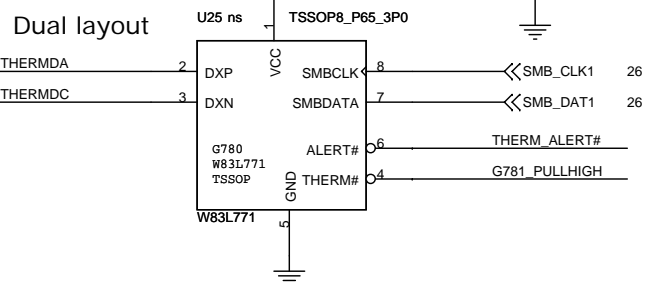
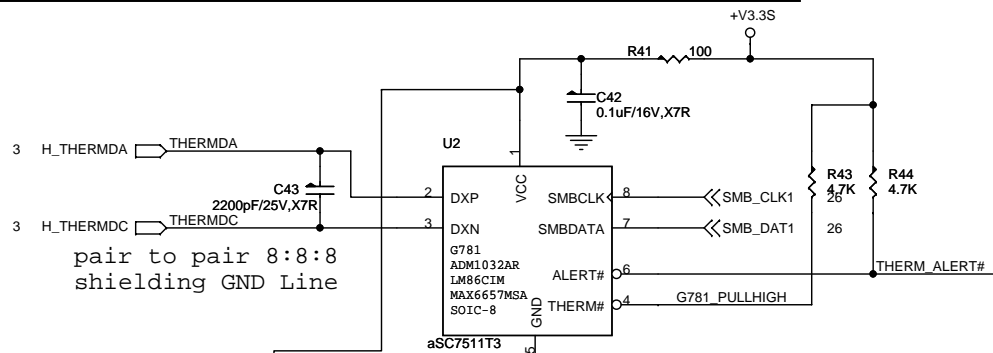




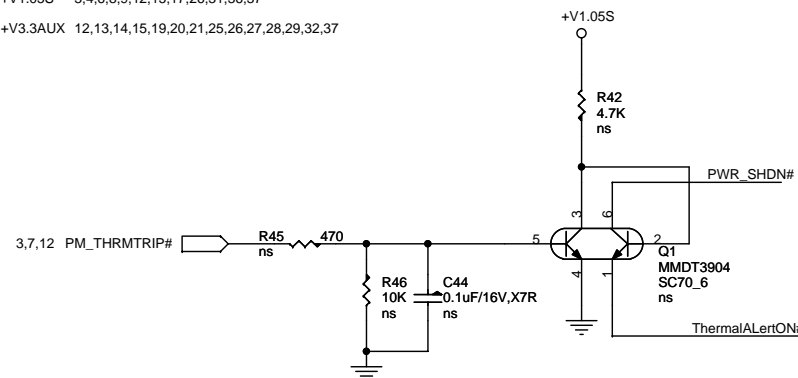
ATOM N270



CPU Thermal

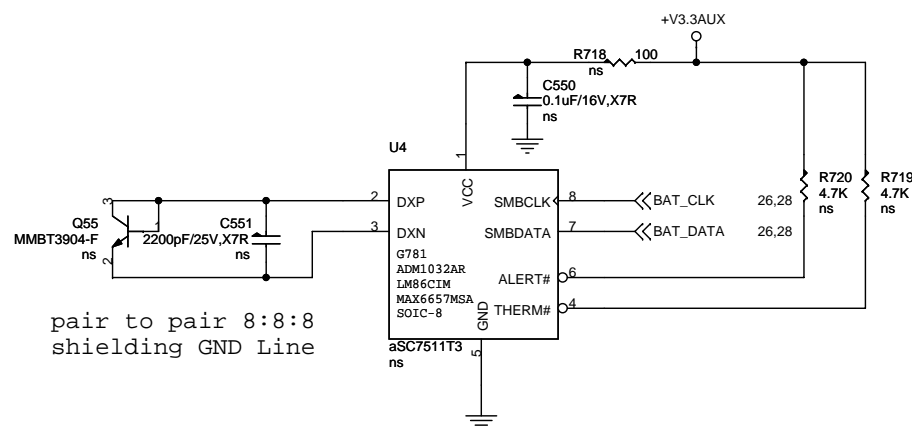


+V3.3S 7,8,9,11,12,13,14,15,17,18,19,20,21,22,23,24,25,26,32,33,34,36,37
+V1.05S 3,4,6,8,9,12,15,17,26,31,36,37
+V3.3AUX 12,13,14,15,19,20,21,25,26,27,28,29,32,37



System Thermal

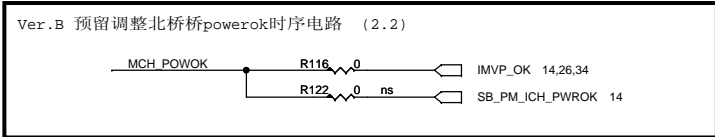
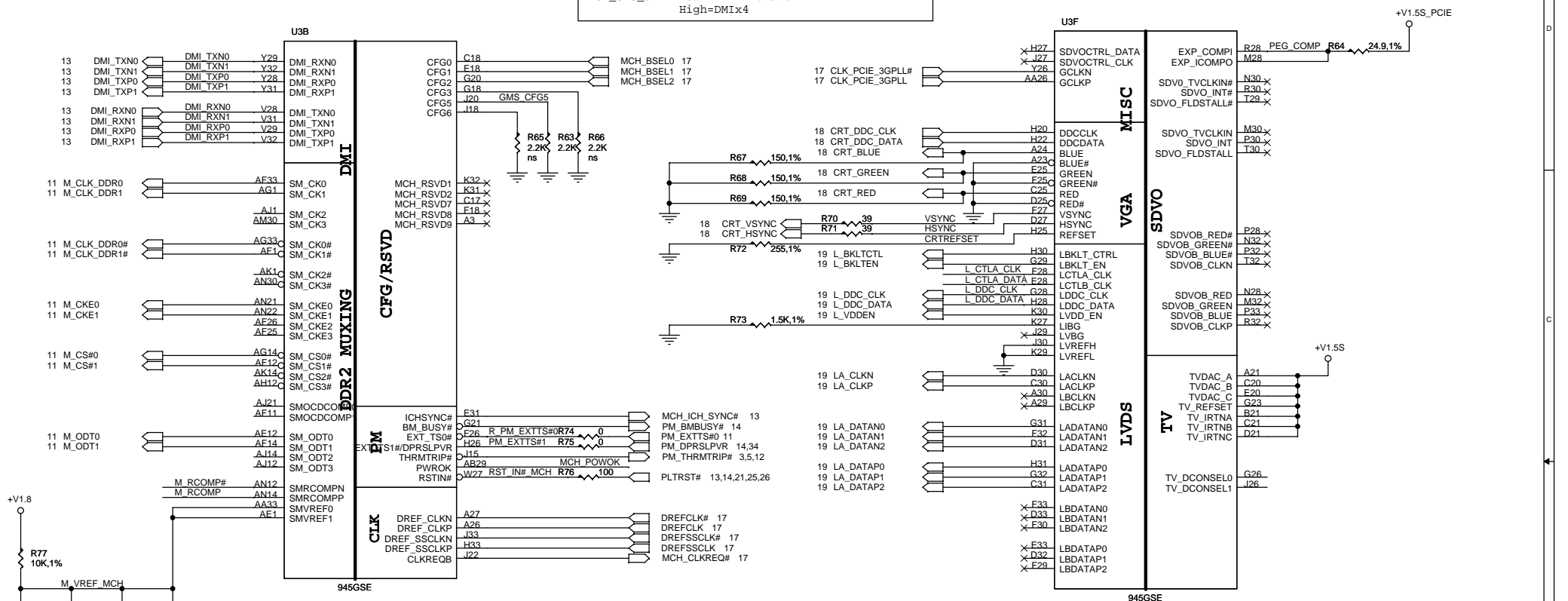
Note: Need be placed near the area of the highest temp



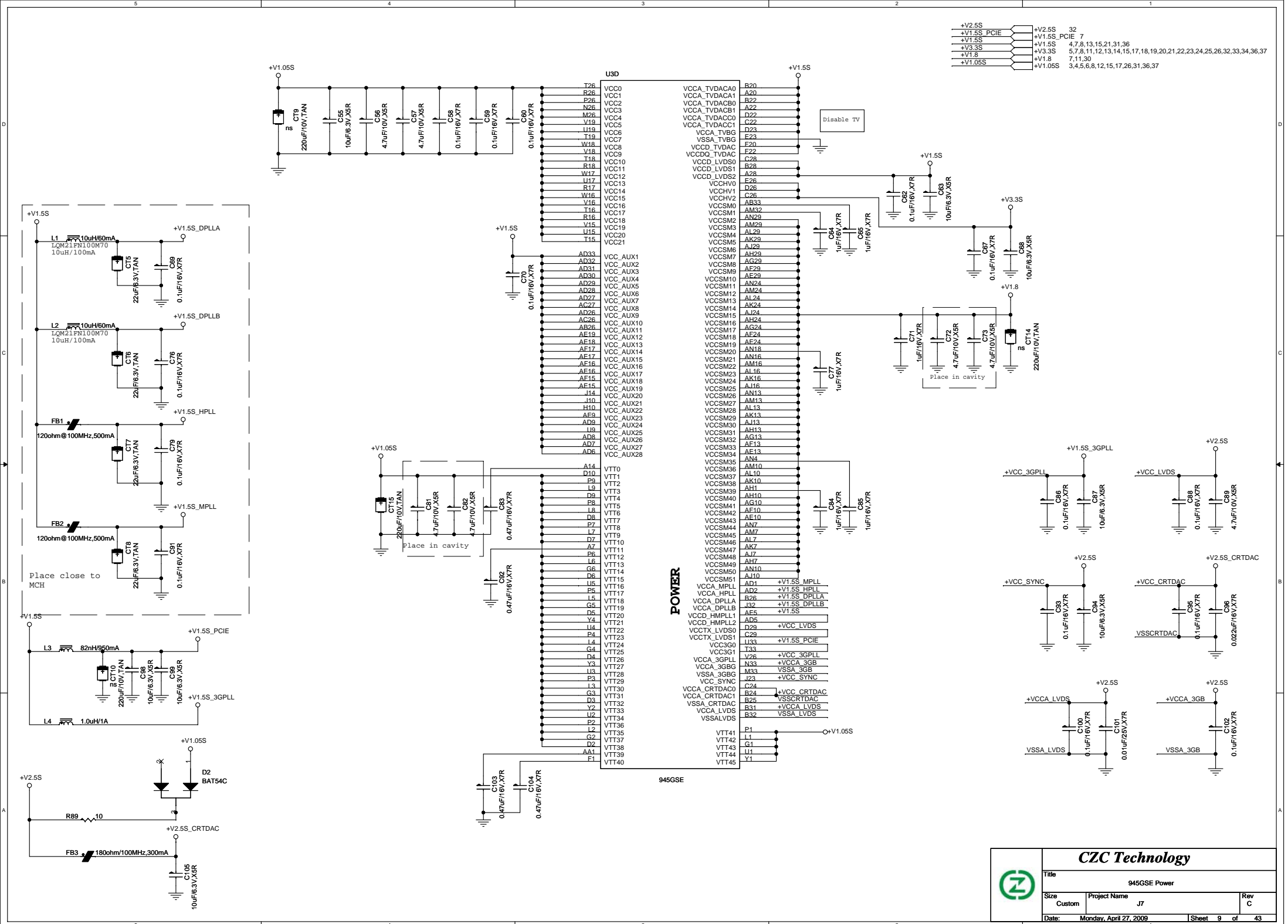
CZC Technology		
Title		
CPU THERMAL SENSOR		
Size	Project Name	Rev
Custom	J7	C
Date:	Monday, April 27, 2009	Sheet 5 of 43

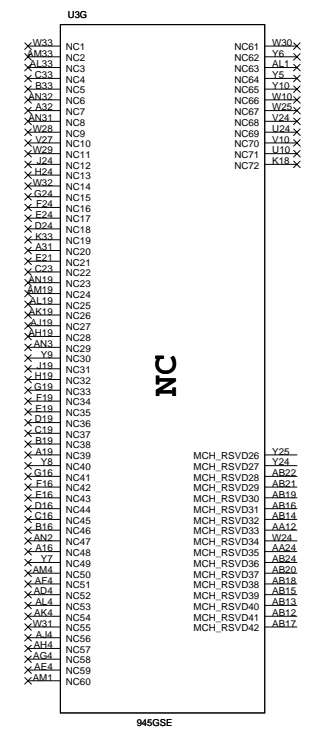
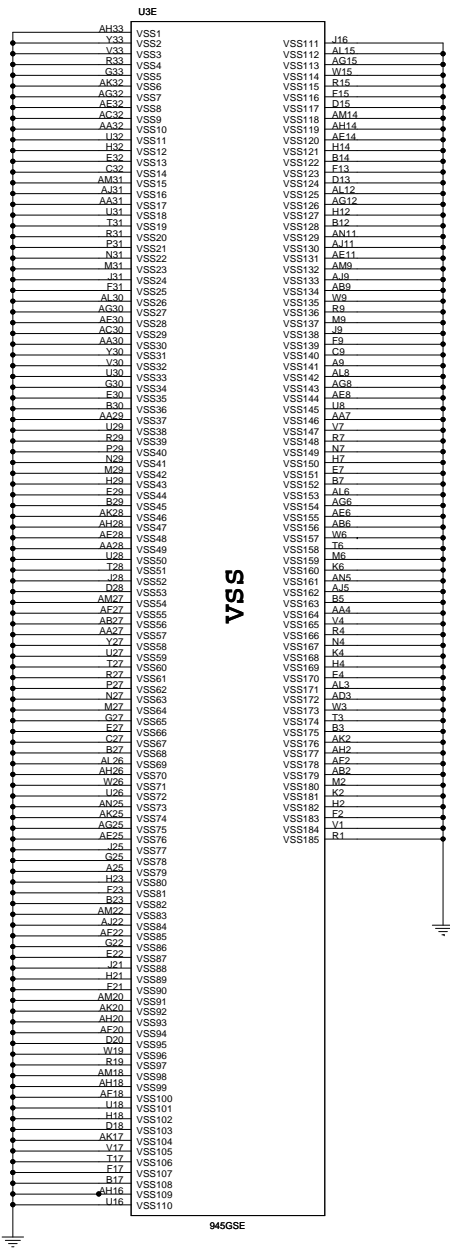
+V1.5S_PCIE	+V1.5S_PCIE 9
+V1.5S	4,8,9,13,15,21,31,36
+V3.3S	5,8,9,11,12,13,14,15,17,18,19,20,21,22,23,24,25,26,32,33,34,36,37
+V1.8	9,11,30

MCH_CFG_3	Reserve
MCH_CFG_6	Reserve
MCH_CFG_5	Low=DMix2 Default High=DMix4

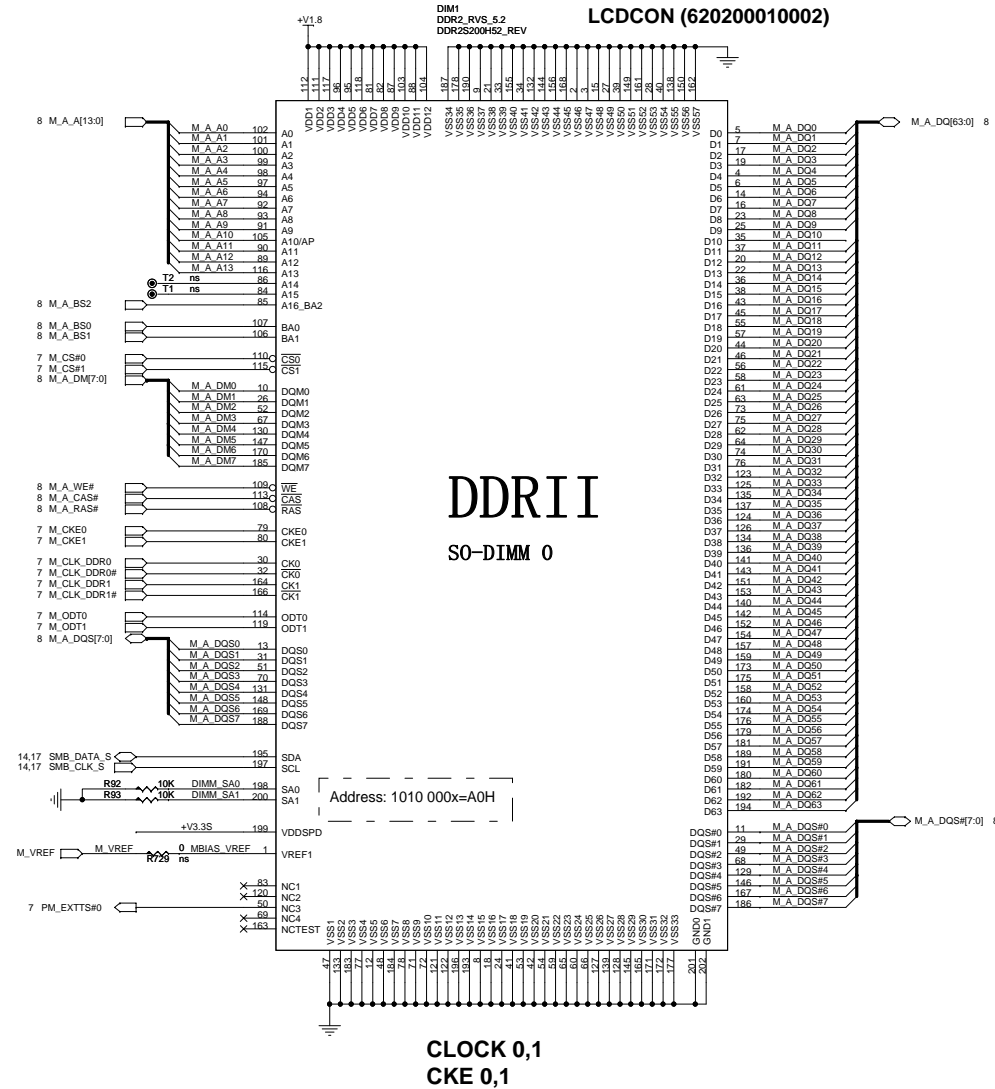


	CZC Technology		
	Title 945GSE DMI/MISC/VGA/LVDS		
	Size A3	Project Name J7	Rev C
	Date: Monday, April 27, 2009	Sheet 7 of 43	



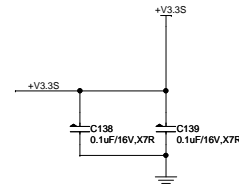
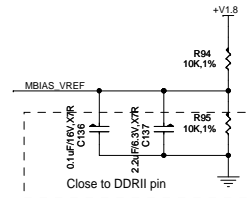
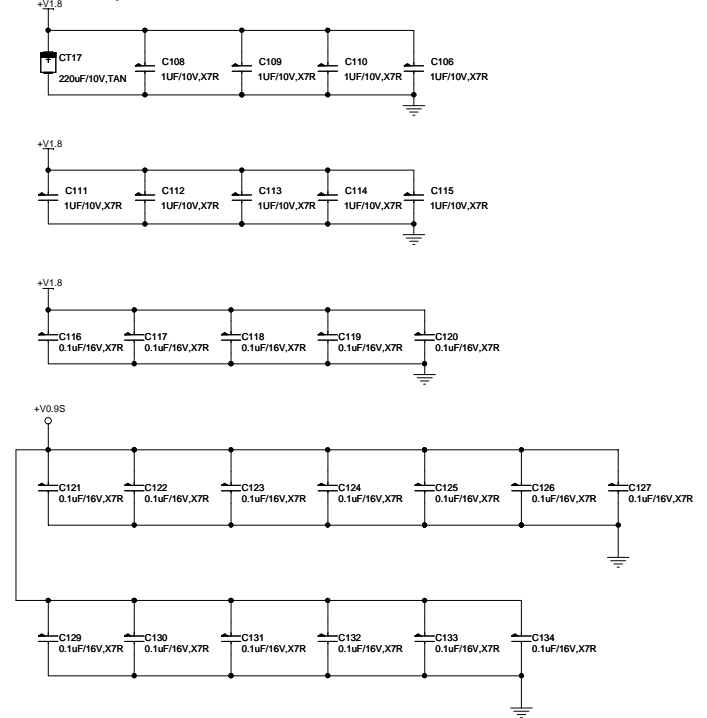
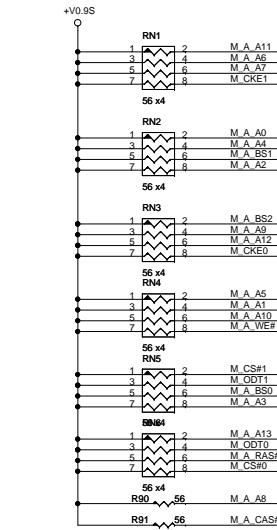



Foxconn: ASOA426-N2RN-7F
LCDCON (620200010002)



+V1.8 7,9,30
+V0.9S 30
+V3.3S 5,7,8,9,12,13,14,15,17,18,19,20,21,22,23,24,25,26,32,33,34,36,37

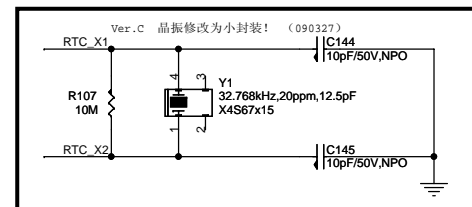
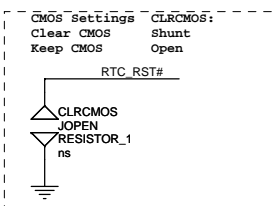
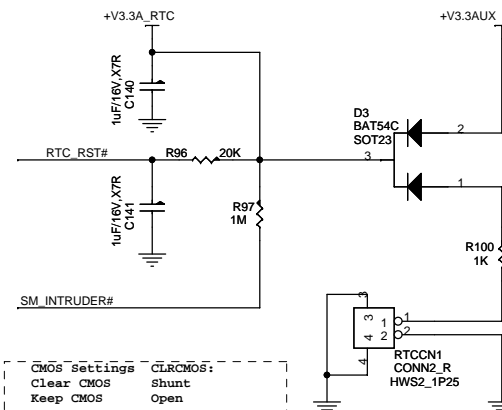
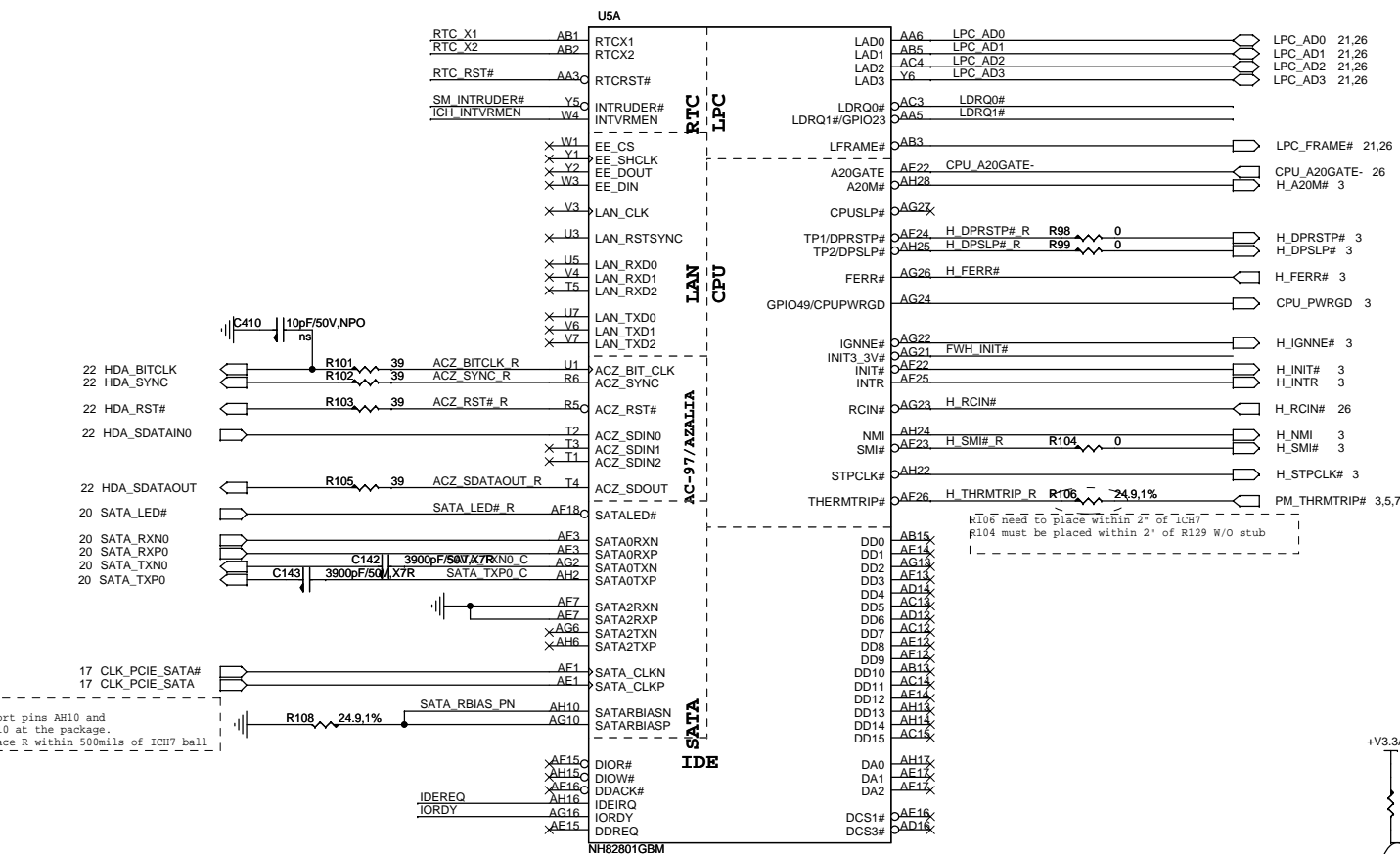
Layout note: 电容靠近DDR slot VDD PIN



CZC Technology			
	Title		
	DDR2 SODIMM		
	Size	Project Name	Rev
	Custom	J7	C
Date: Monday, April 27, 2009		Sheet	11 of 43

+V1.05S
+V3.3S
+V3.3A_RTC
+V3.3AUX

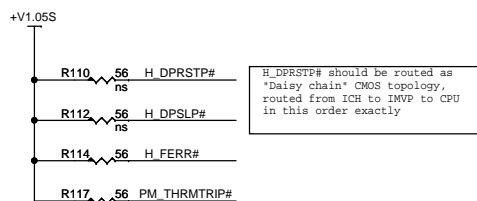
+V1.05S 3,4,5,6,8,9,15,17,26,31,36,37
+V3.3S 5,7,8,9,11,13,14,15,17,18,19,20,21,22,23,24,25,26,32,33,34,36,37
+V3.3A_RTC 15
+V3.3AUX 5,13,14,15,19,20,21,25,26,27,28,29,32,37



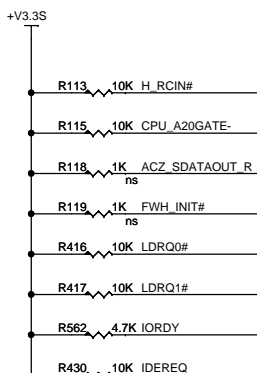
ICH7 intel VccSus1.05 enable strap

	INTRVLMEN	HWS2_1P25	
Enable(default)	1	STUFF	UNSTUFF
Disable	0	UNSTUFF	STUFF

+V3.3A_RTC
R111 332K,1%
DEL R116



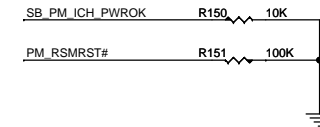
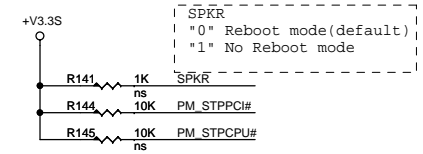
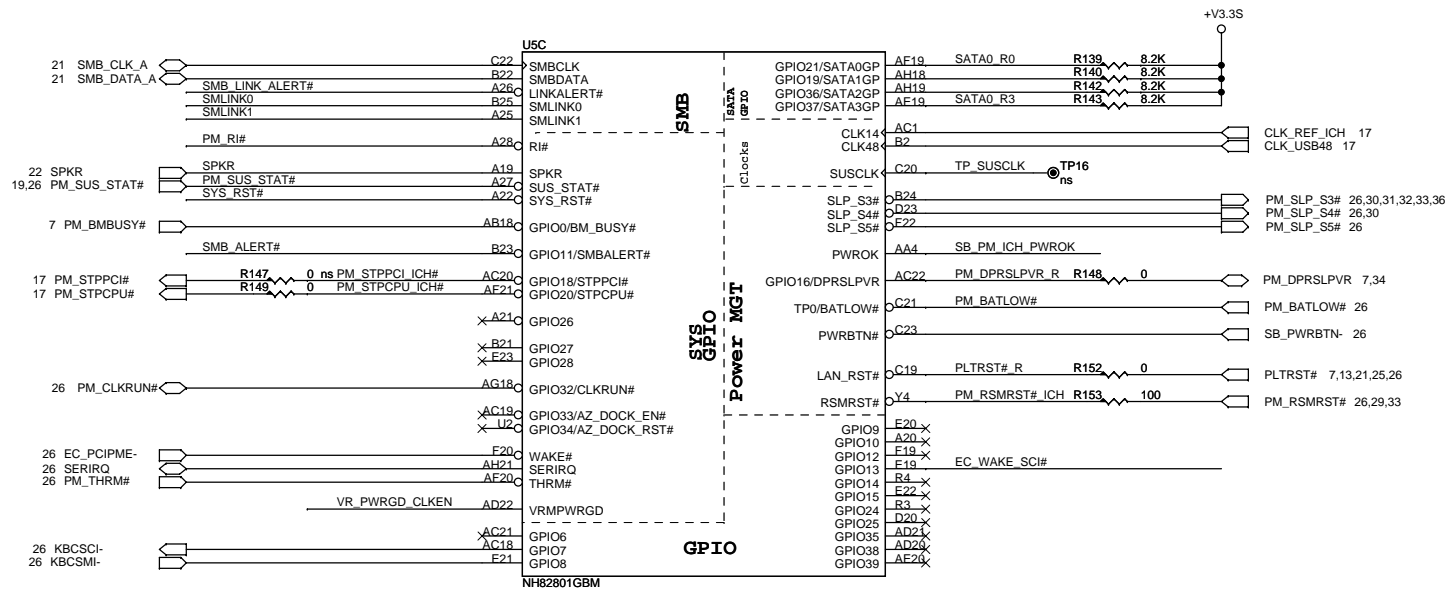
H_DPRSTP# should be routed as "Daisy chain" CMOS topology, routed from ICH to IMVP to CPU in this order exactly



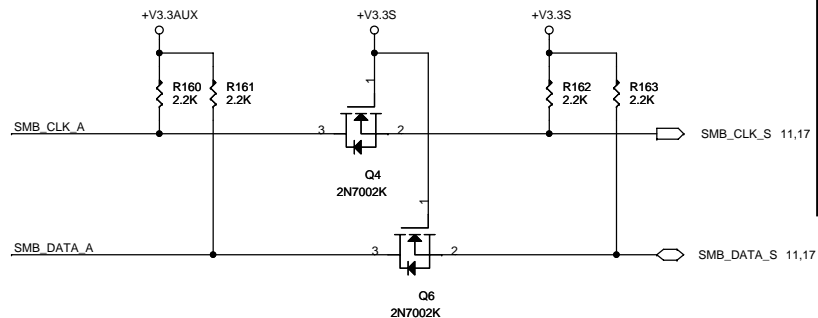
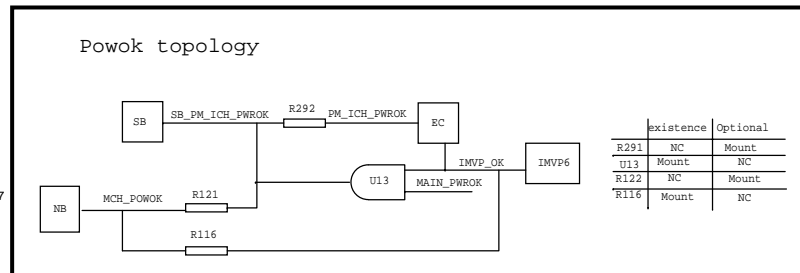
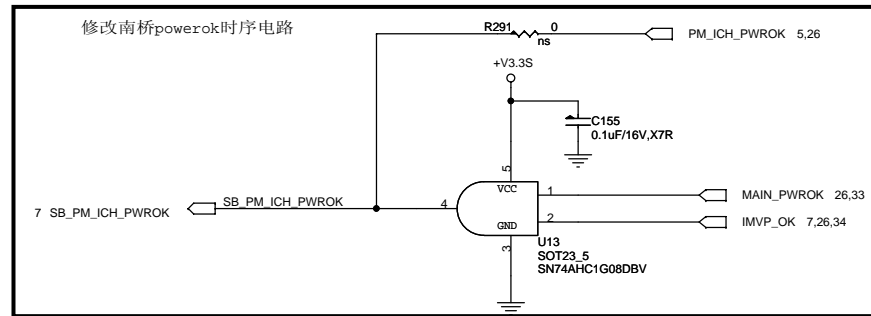
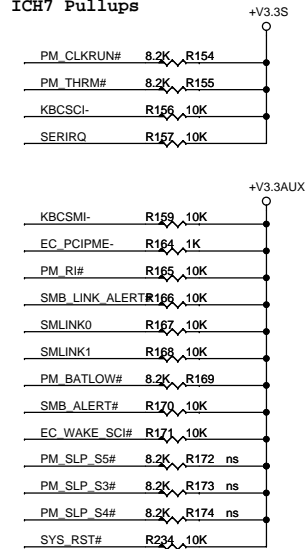
R118 strap functionality based on ICH_TP3 strap:
XOR chain entrance(ICH_TP3 pulled low)
PCIS port config bit 1(ICH_TP3 not pulled low)

+V3.3S
+V3.3AUX

+V3.3S 5,7,8,9,11,12,13,15,17,18,19,20,21,22,23,24,25,26,32,33,34,36,37
+V3.3AUX 5,12,13,15,19,20,21,25,26,27,28,29,32,37

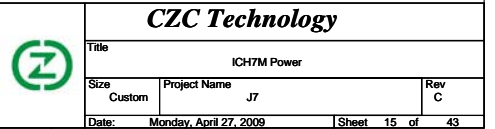


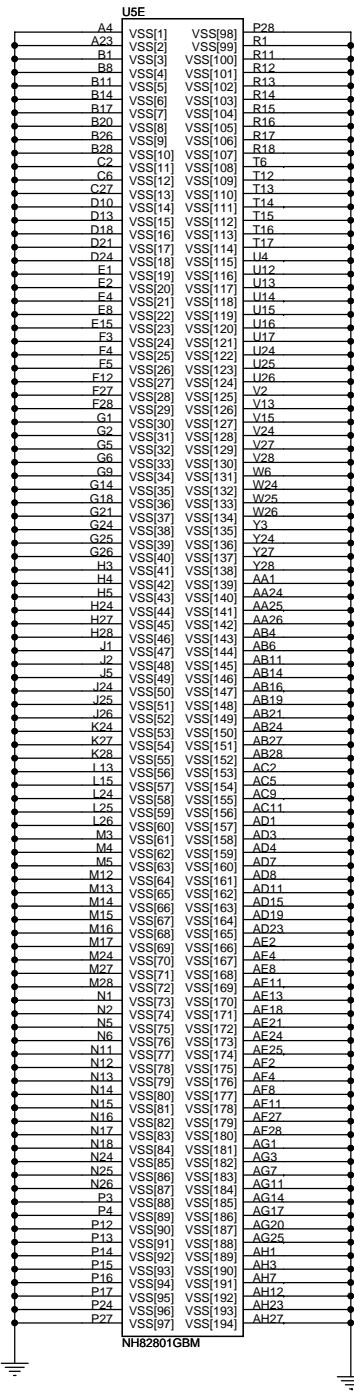
ICH7 Pullups




CZC Technology

Title ICH7M GPIO/SMBUS/Power MGT		
Size A3	Project Name J7	Rev C
Date: Monday, April 27, 2009	Sheet 14	of 43







CZC Technology

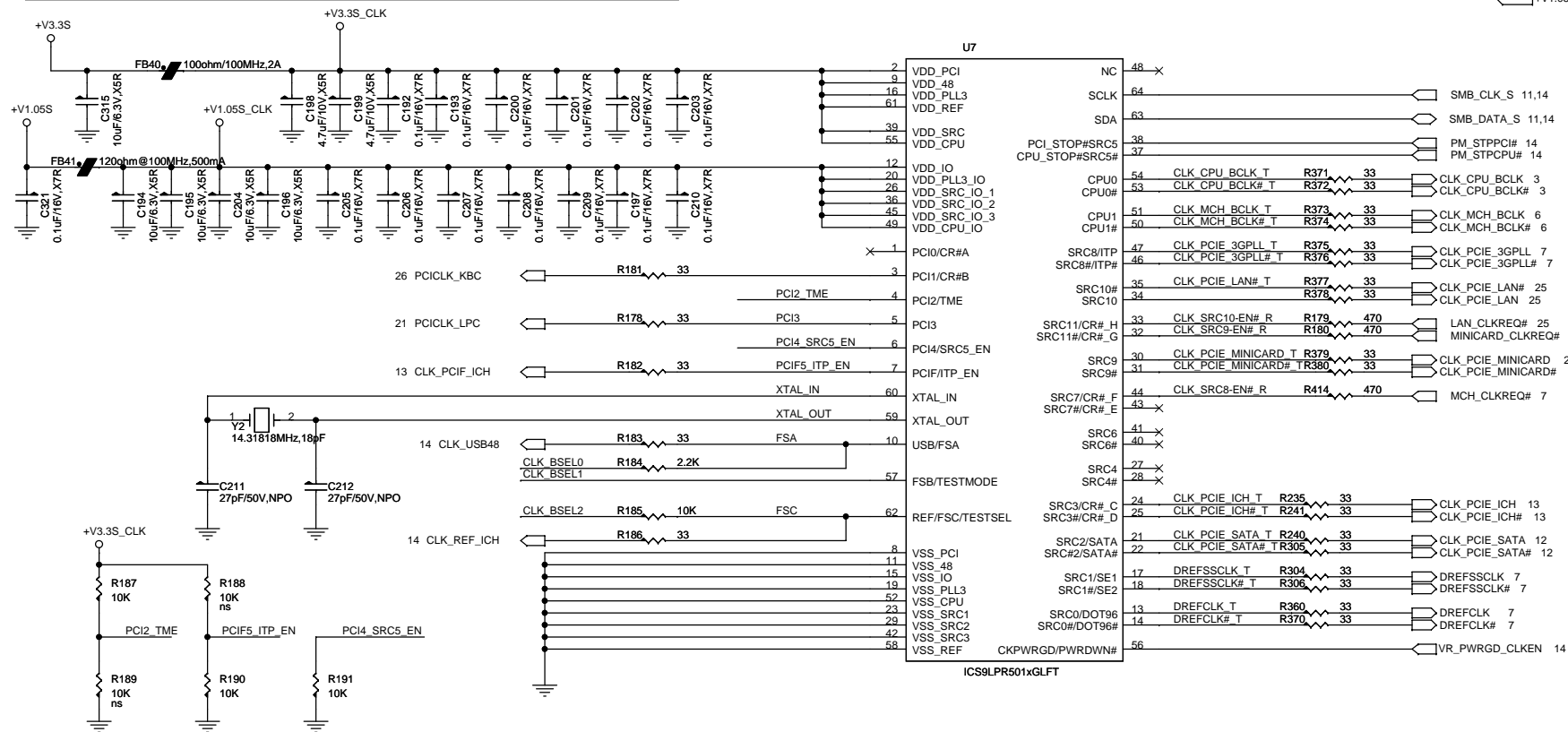
Title

ICH7M GND

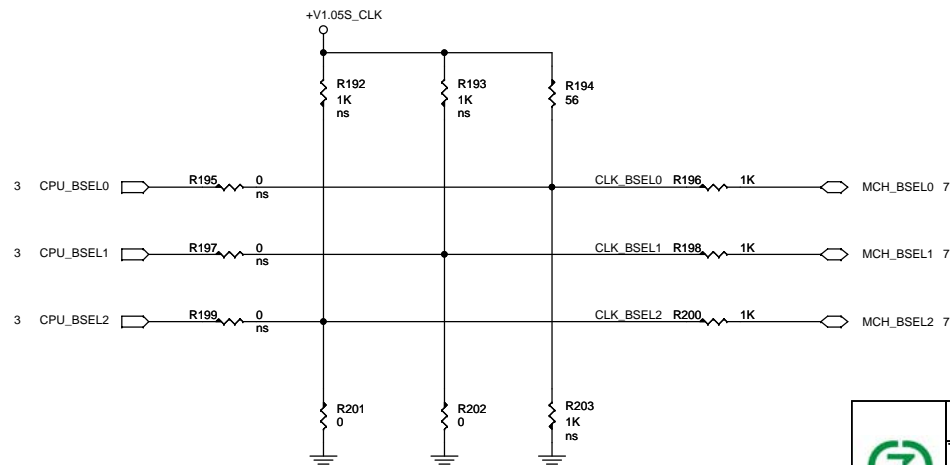
SizeA3Project NameJ7RevC

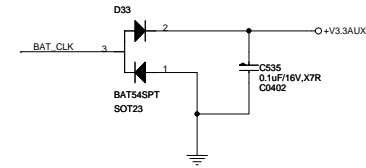
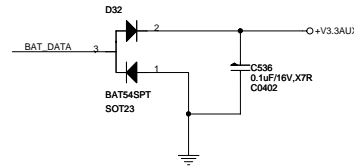
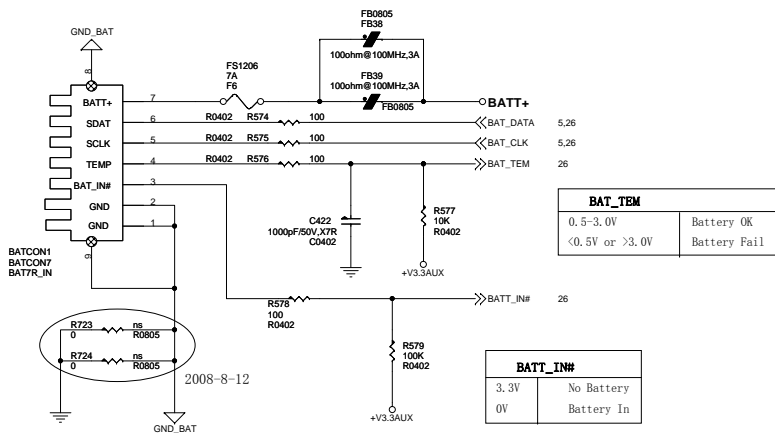
Date:Monday, April 27, 2009Sheet 16 of 43

CK505 ICS9LPR501



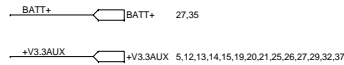
FSC BSEL2	FSA BSEL1	FSA BSEL0	Host Clock frequency MHz
1	0	1	100
0	0	1	133
0	1	1	166
0	1	0	200
0	0	0	266
1	0	0	333
1	1	0	400
1	1	1	Reserved





修改Batcon1的footprint为BAT7R_IN

Use bridge connect
GND_AD and GND



RTC MF52 D 103 F 3950		
Temperature	Voltage	RT
-15	3.0	74.18K
70	0.5	1.740K

Del CPU Power Debug Circuit
2008-9-28

CPU Core Debug

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Vout
0	0	1	1	0	0	0	1.2000V
0	1	1	0	0	0	0	0.9000V

CZC 创智成

Anfeng

File

Battery In

Size C

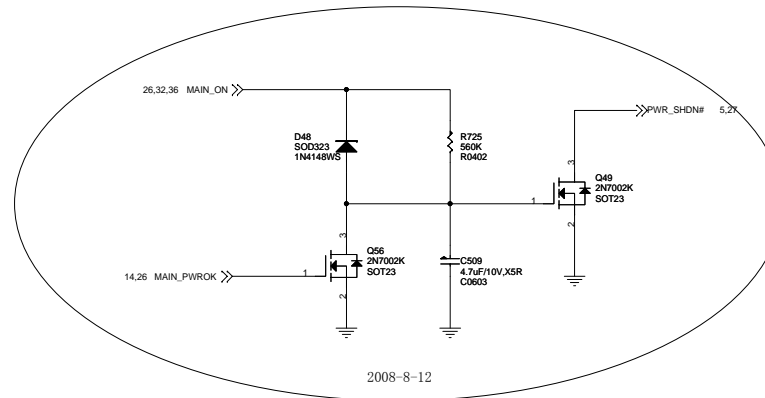
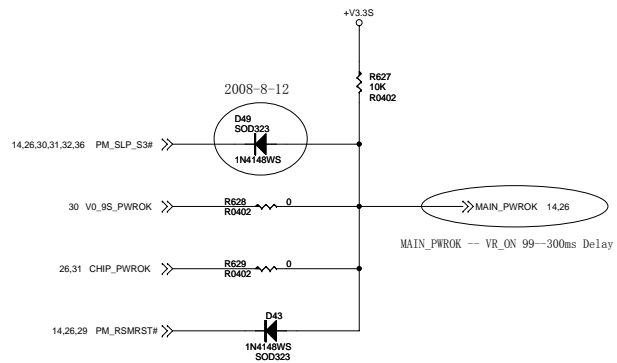
Document Number J7

Rev C

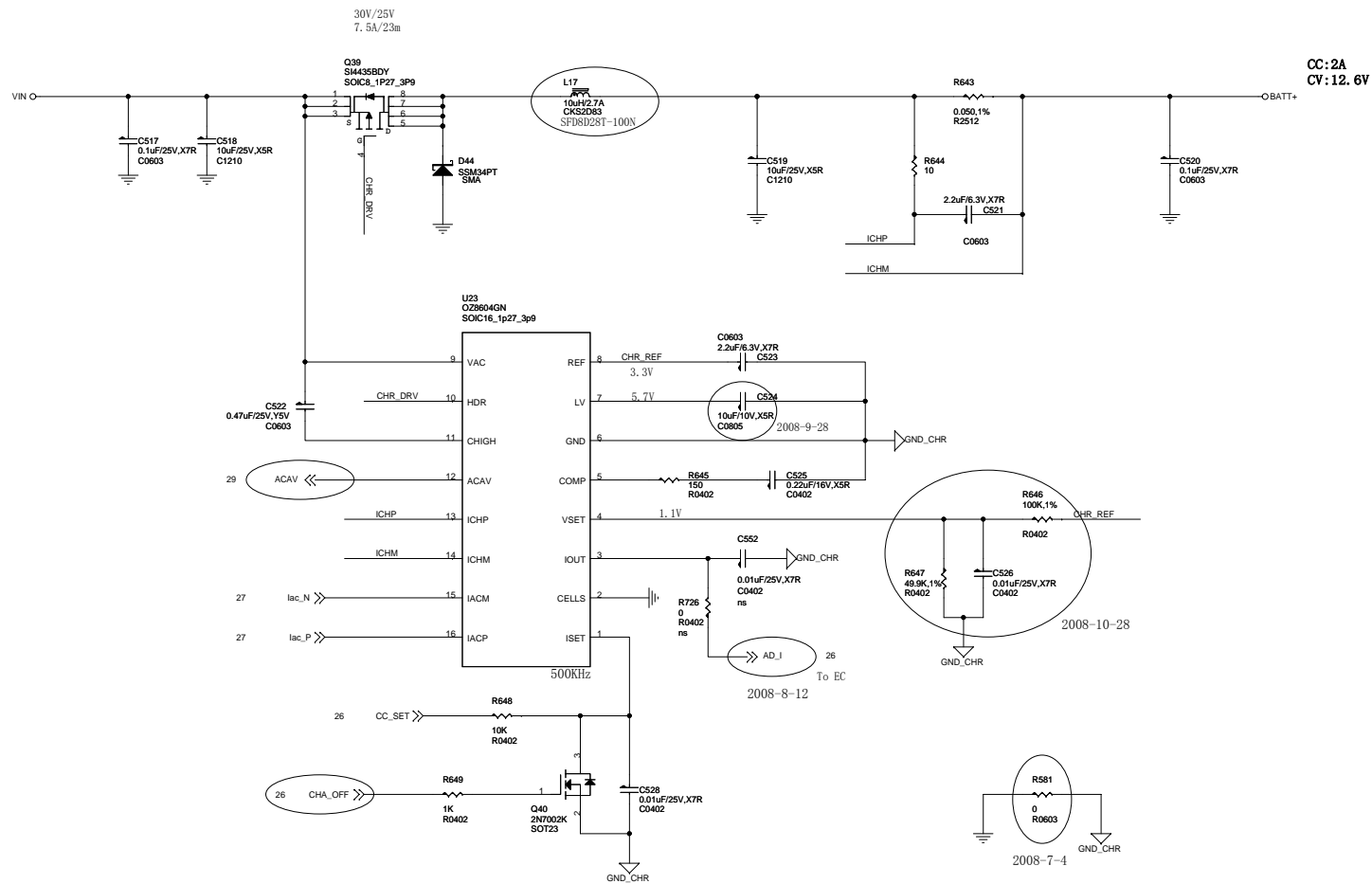
Date: Monday, April 27, 2009

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+V3.3S +V3.3S 5,7,8,9,11,12,13,14,15,17,18,19,20,21,22,23,24,25,26,32,34,36,37



CC_SET	Charge Current
3.0V	2.0A
1.5V	1.0A
0.45V	300mA
<0.15V	=CHA_OFF

BATT+ 27,28

VIN 20,27

CZC 创智成

Anfeng

File

Charger

Size C

Document Number J7

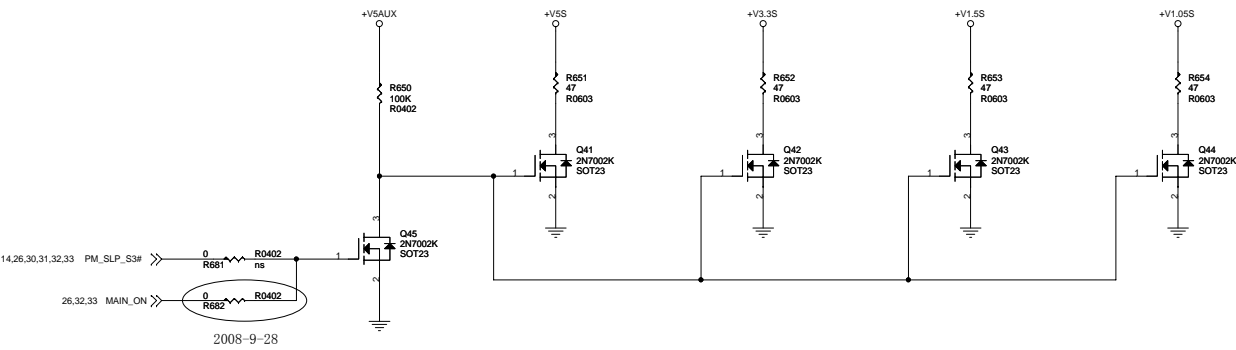
Rev C

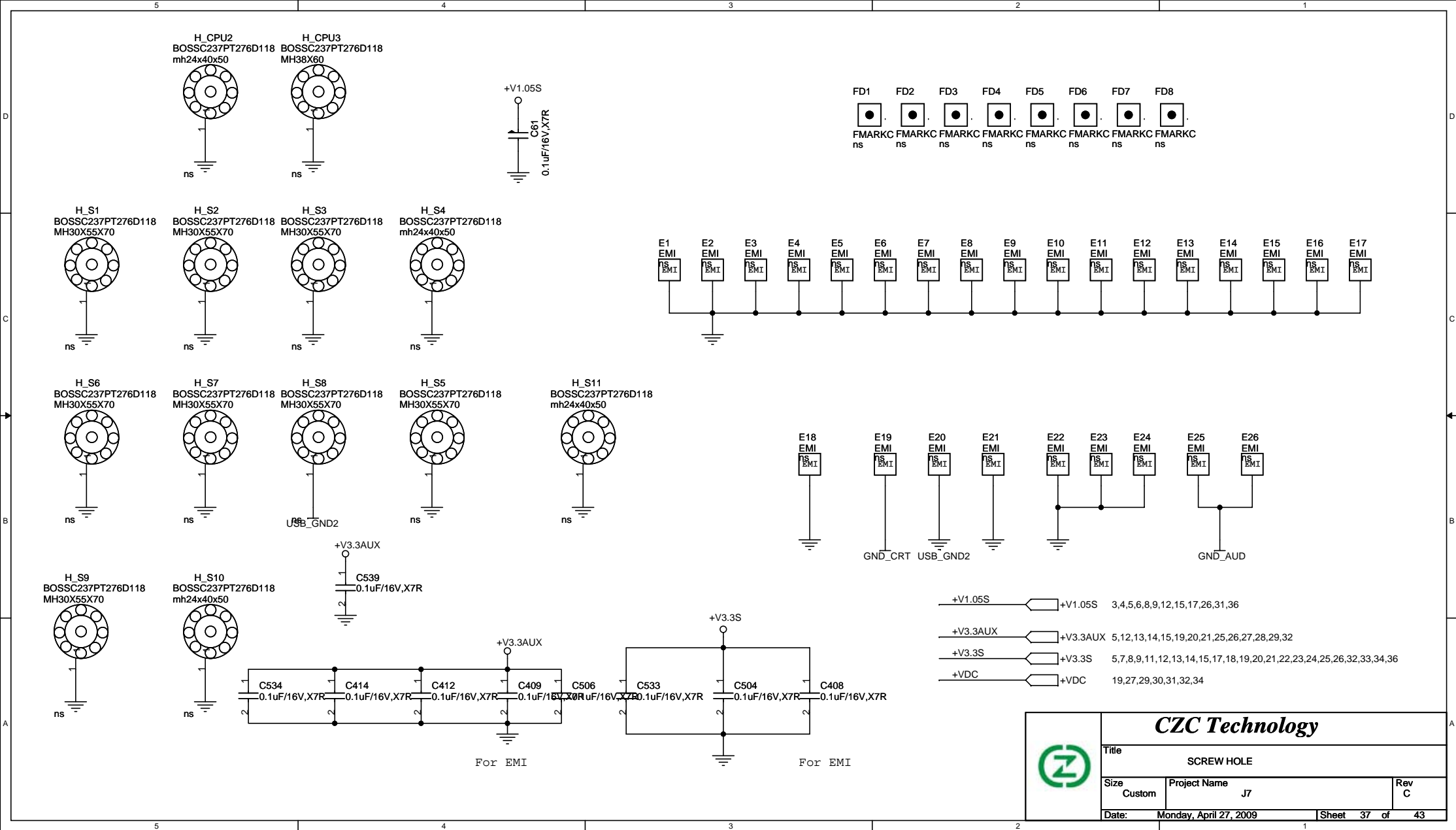
Date: Monday, April 27, 2009

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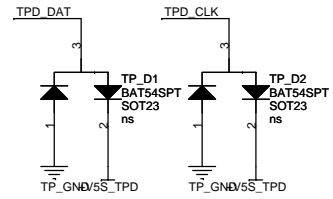
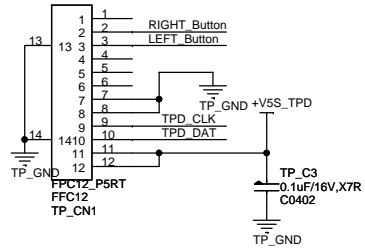
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+V3.3S +V3.3S 5,7,8,9,11,12,13,14,15,17,18,19,20,21,22,23,24,25,26,32,33,34,37
+VSS +VSS 15,18,19,20,22,23,25,26,31,32,34
+V5AUX +V5AUX 15,19,23,26,29,30,31,32
+V1.05S +V1.05S 3,4,5,6,8,9,12,15,17,26,31,37
+V1.5S +V1.5S 4,7,8,9,13,15,21,31

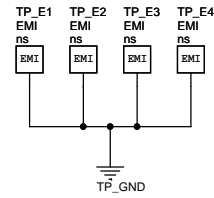
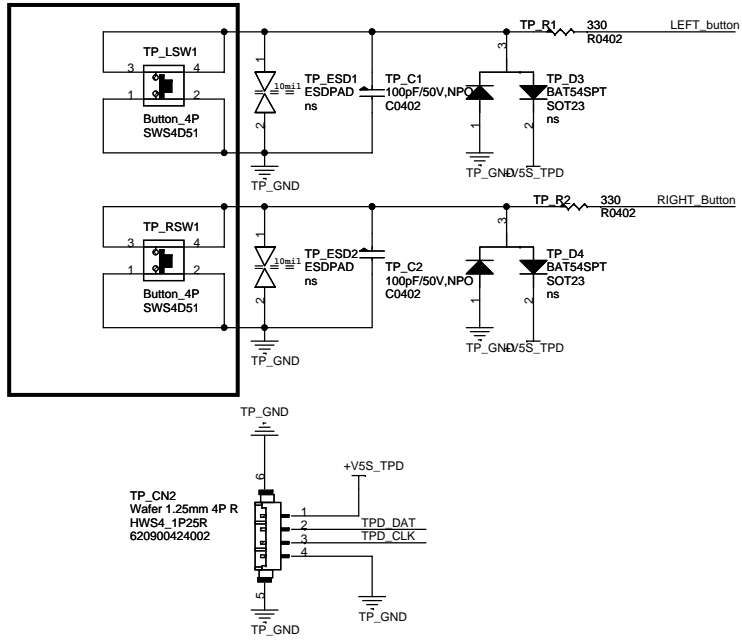




Synaptics : TM-00450-001



Ver.C 修改按键封装! (090327)



CZC Technology

Jack Ouyang

Title	HDD_BAT IOBOARD
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Size	Project Name	Rev
A3	J7	C

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