

MR8000 : Power Block

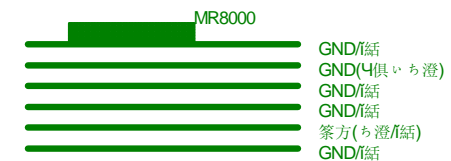
Layout Rule

Designer 4 Layer layout



VDD 欄總D3V3, 九 策方i結
D1V8/A1V8 策臻 , 叫i結30mil

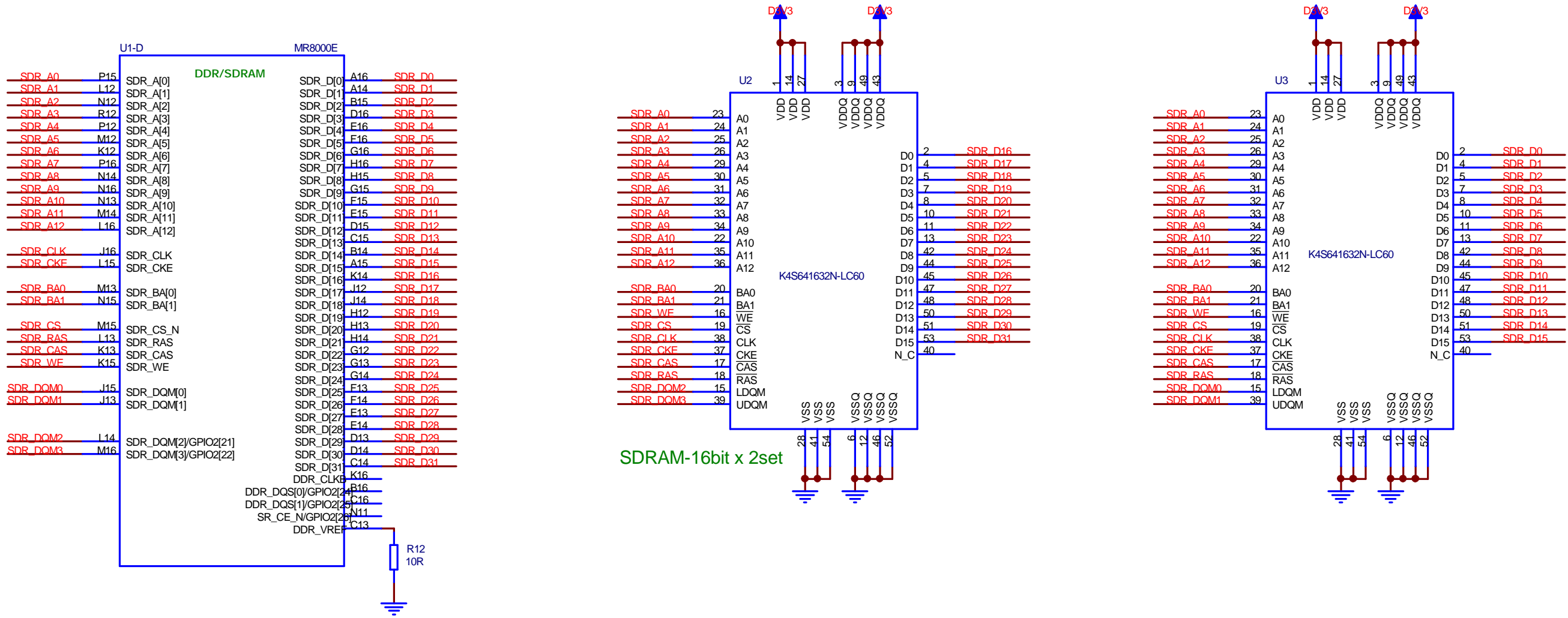
Designer 6 Layer layout

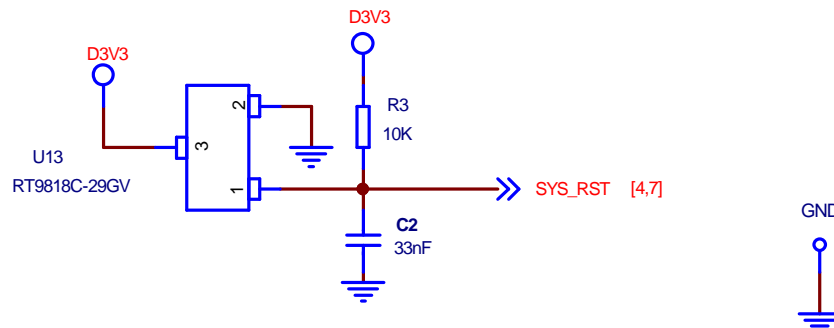
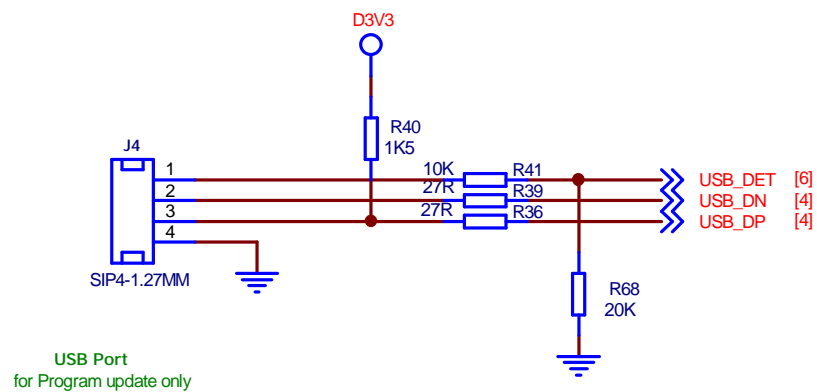
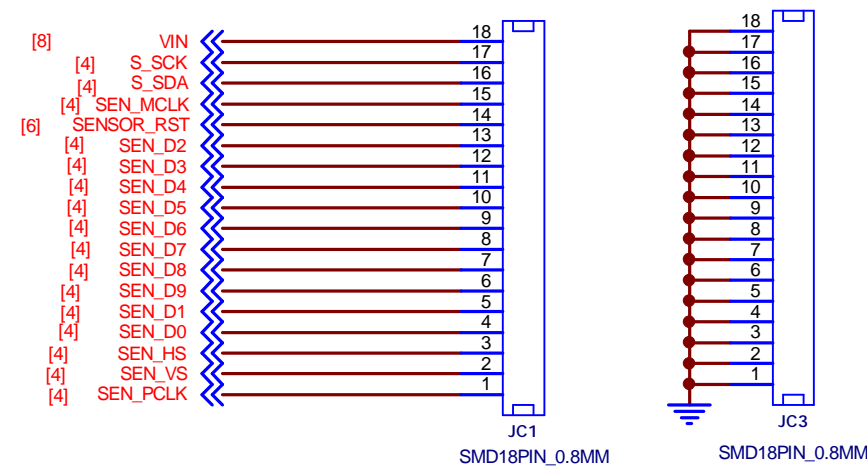
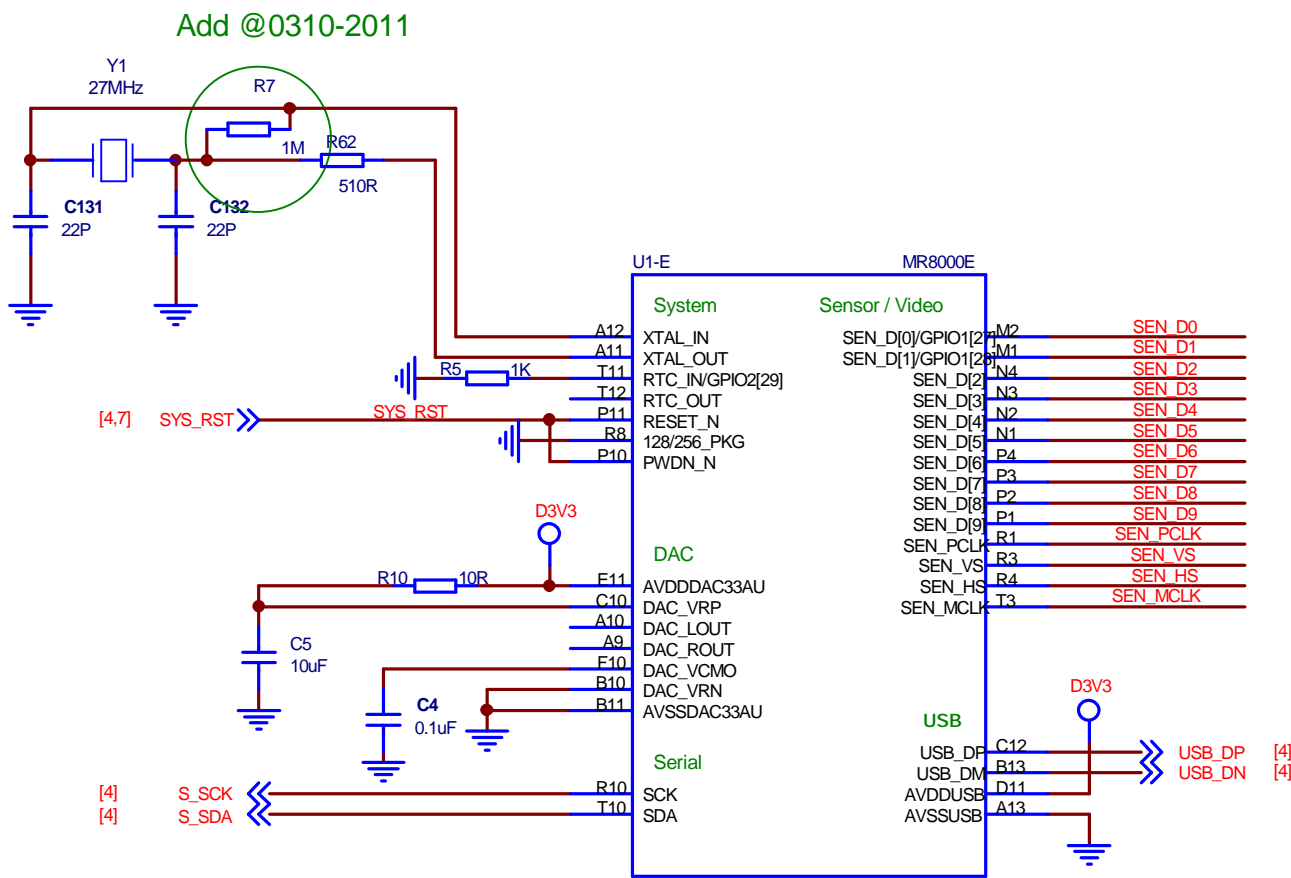


Operating Current

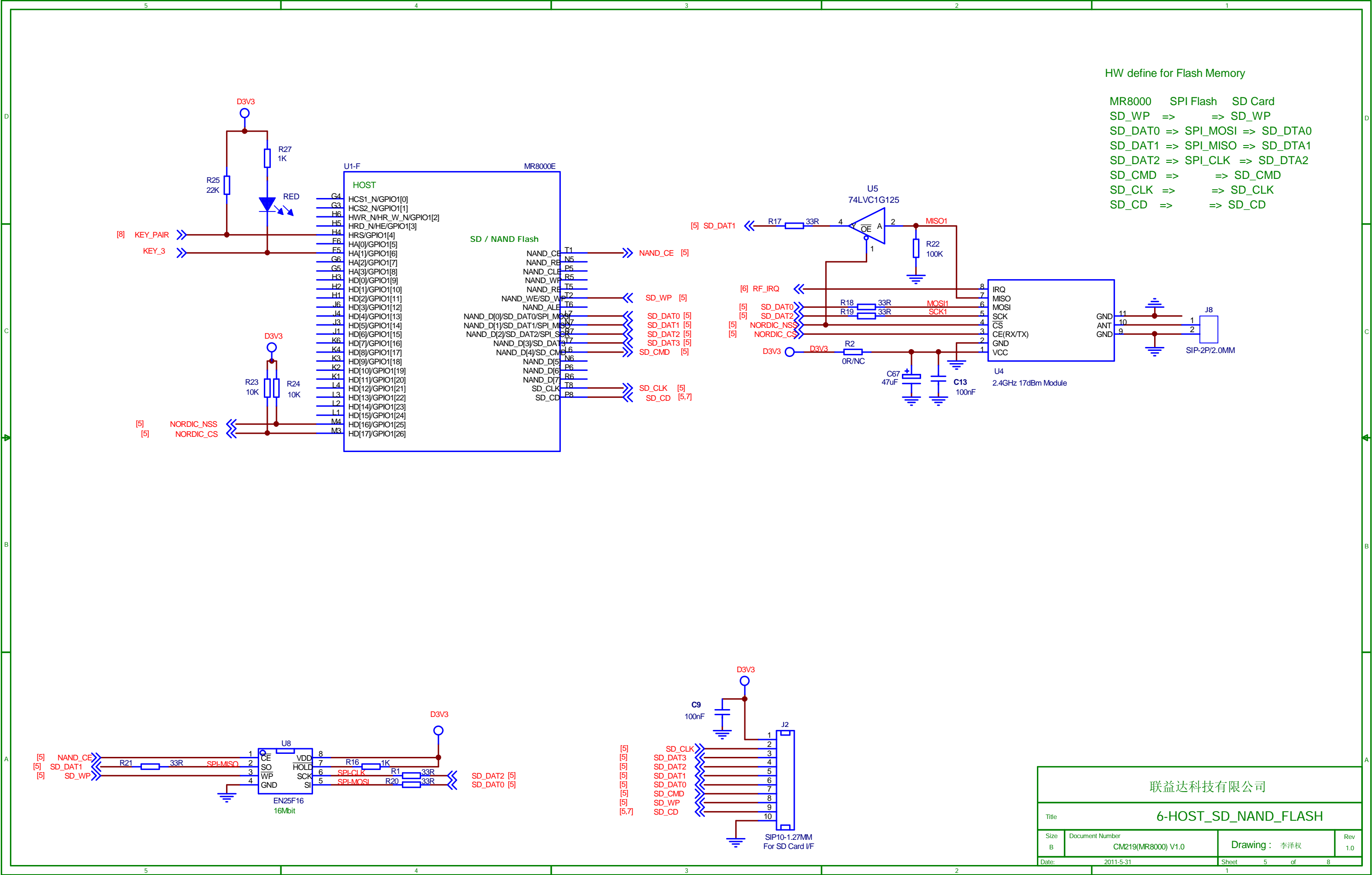
Power : SDRAM -5 280mA -6 210mA -7 180mA

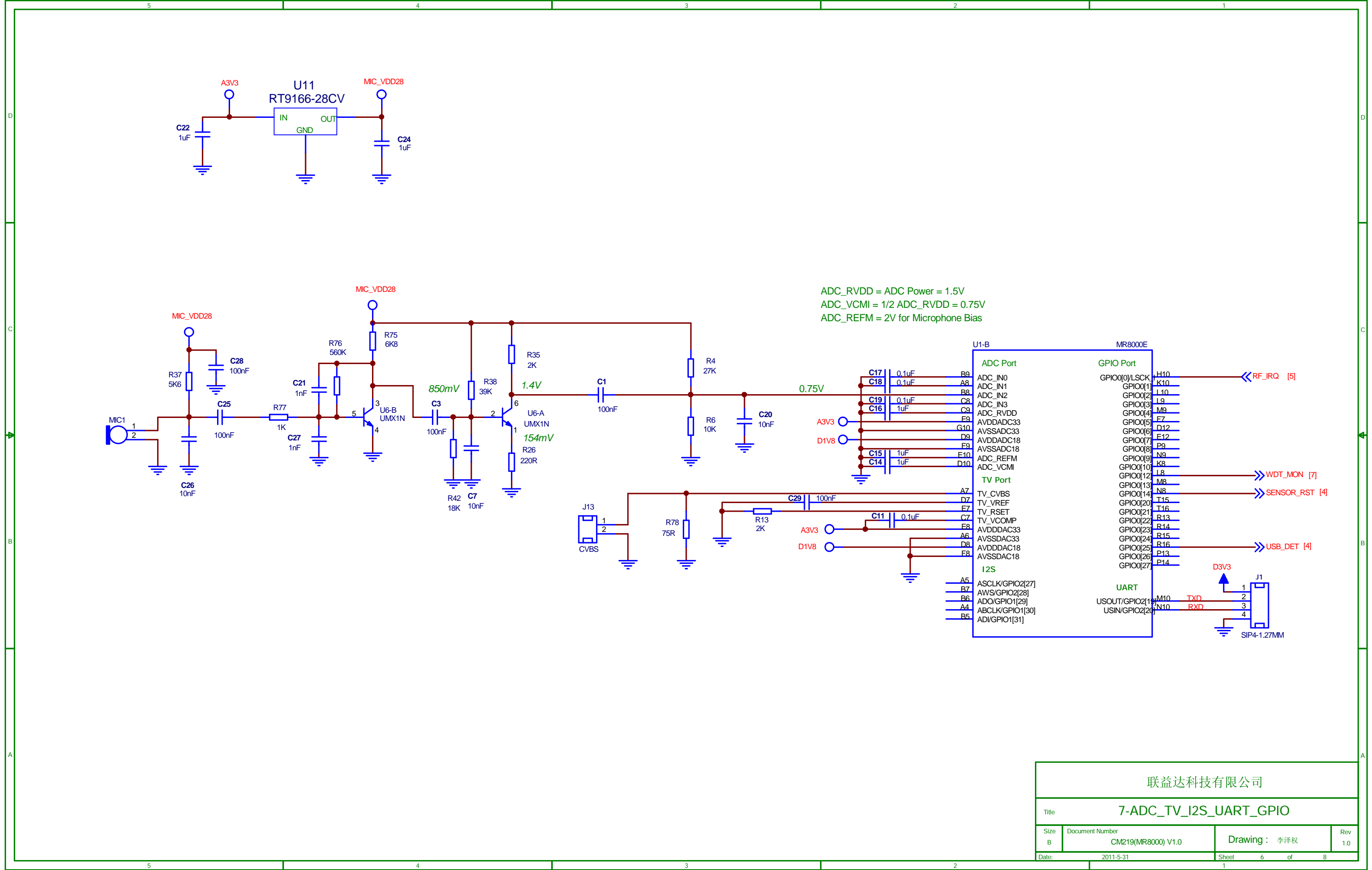
Power : MARS MR8000





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Title 4-DAC_I2C_SENSOR_USB			
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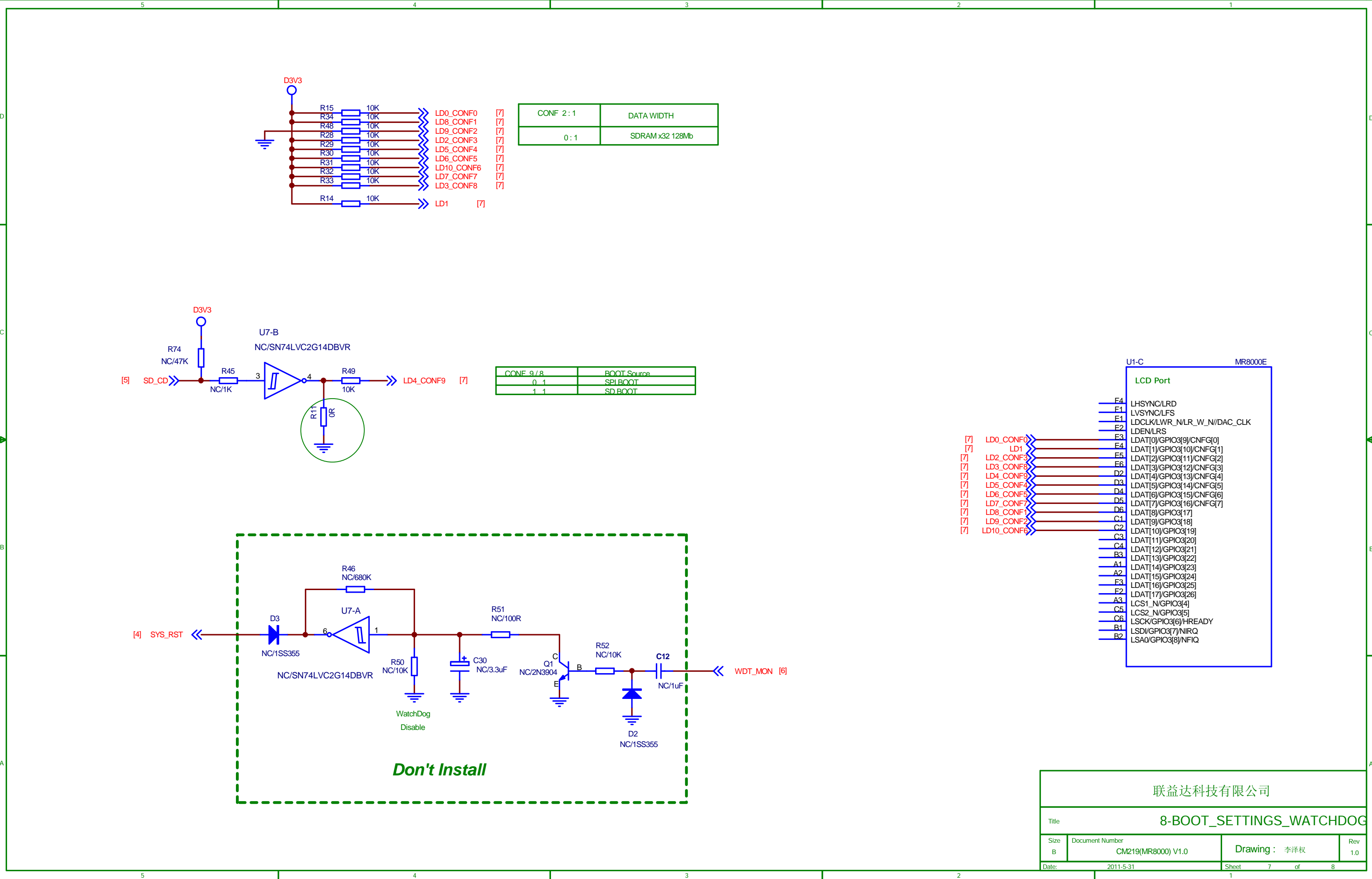


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7-ADC_TV_I2S_UART_GPIO

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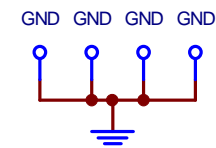
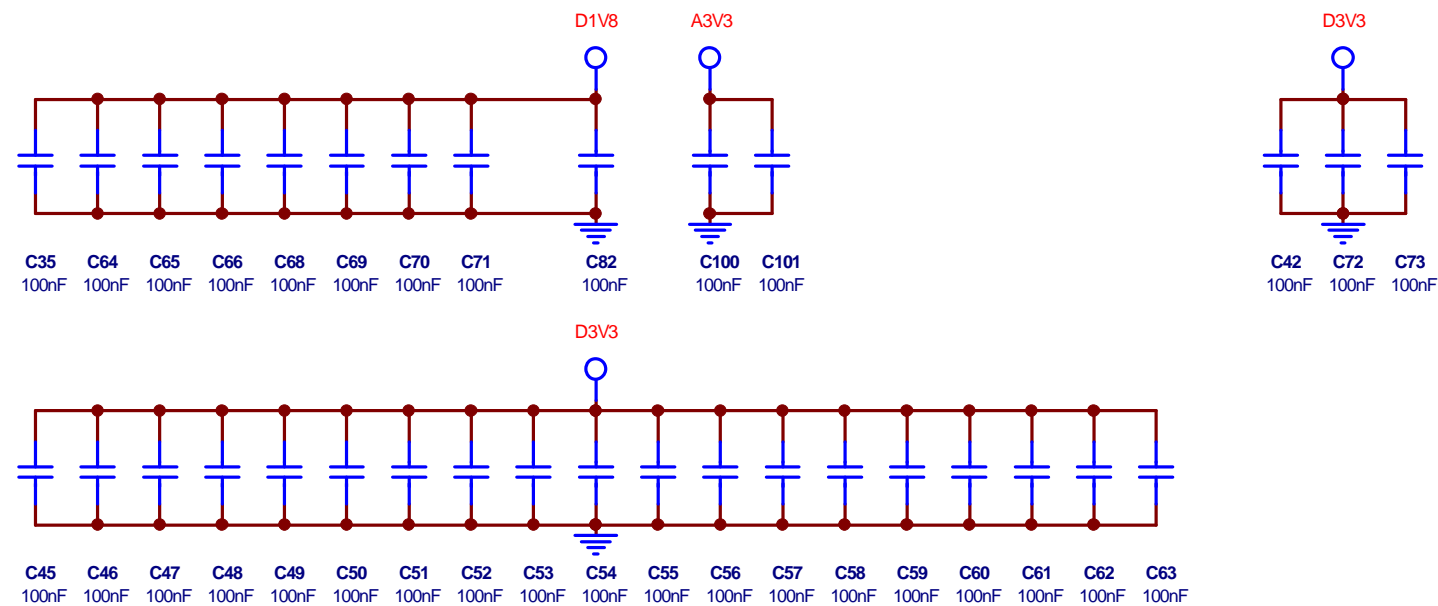
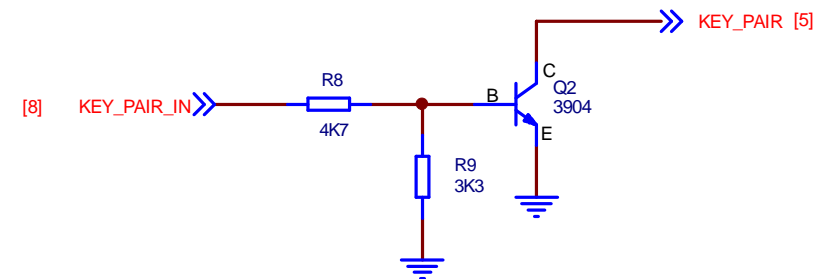
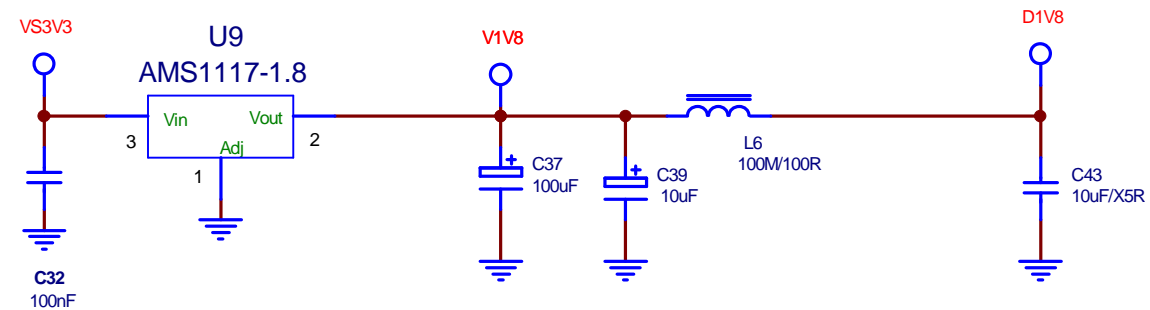
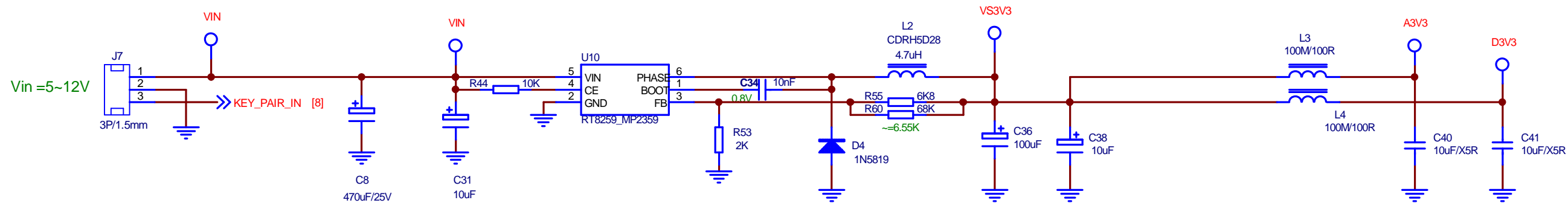


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Title 8-BOOT_SETTINGS_WATCHDOG

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9-POWER

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