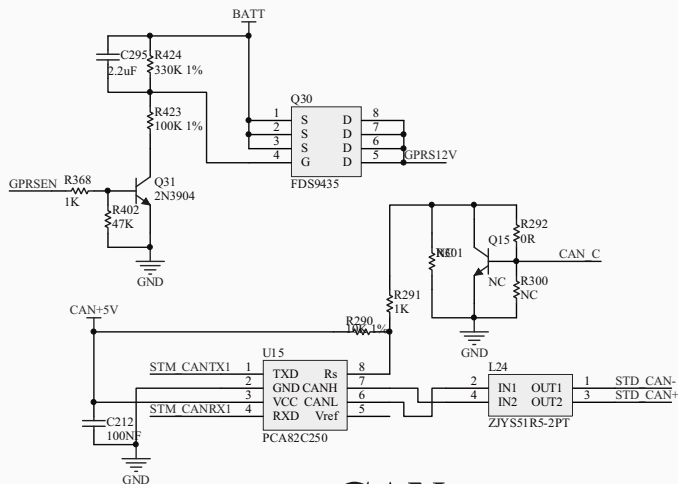
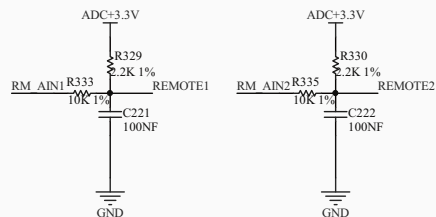
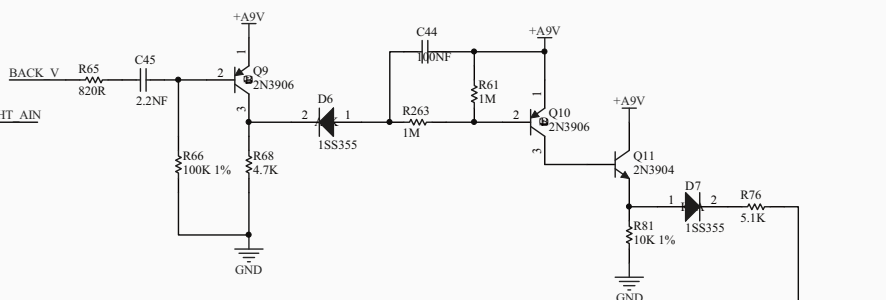
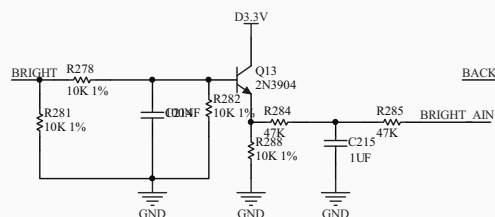


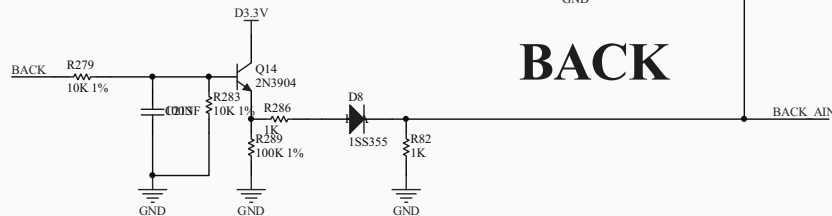
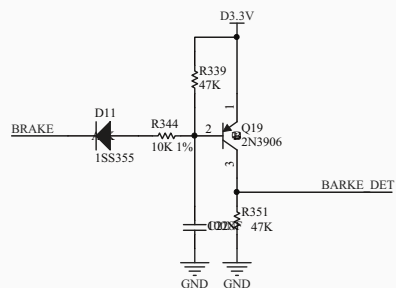
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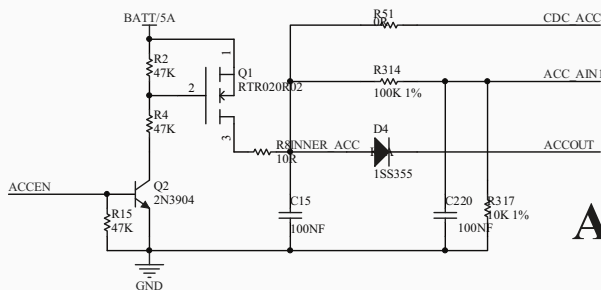
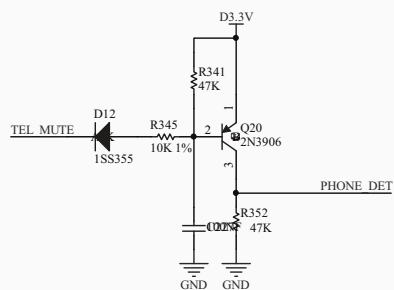
CAN



BACK

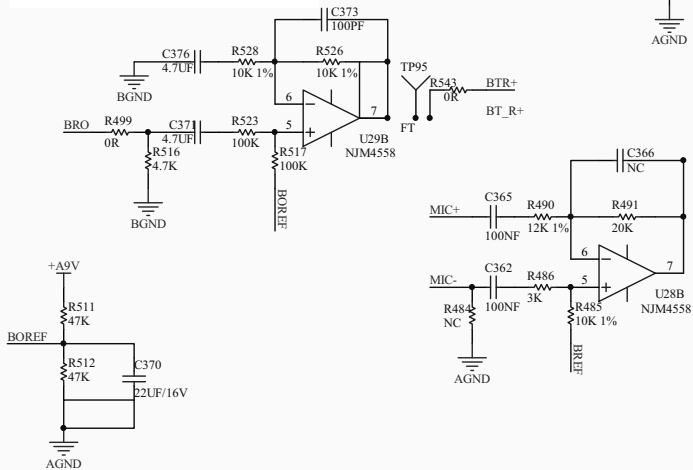


ACC

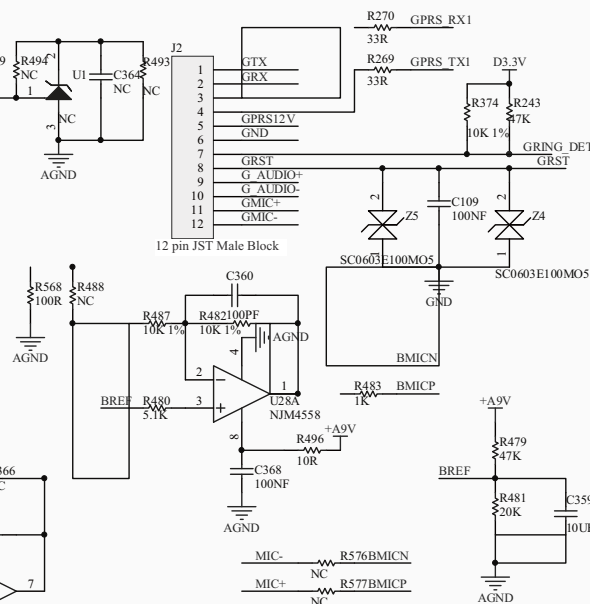


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Size	Number	Revision
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Date:	2010-11-18	Sheet of
File:	E:\Project\BUS.SchDoc	Drawn By:

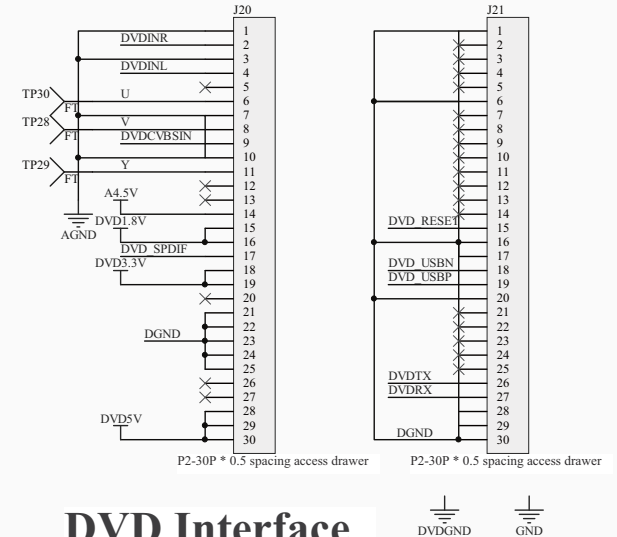
## Bluetooth-MIC



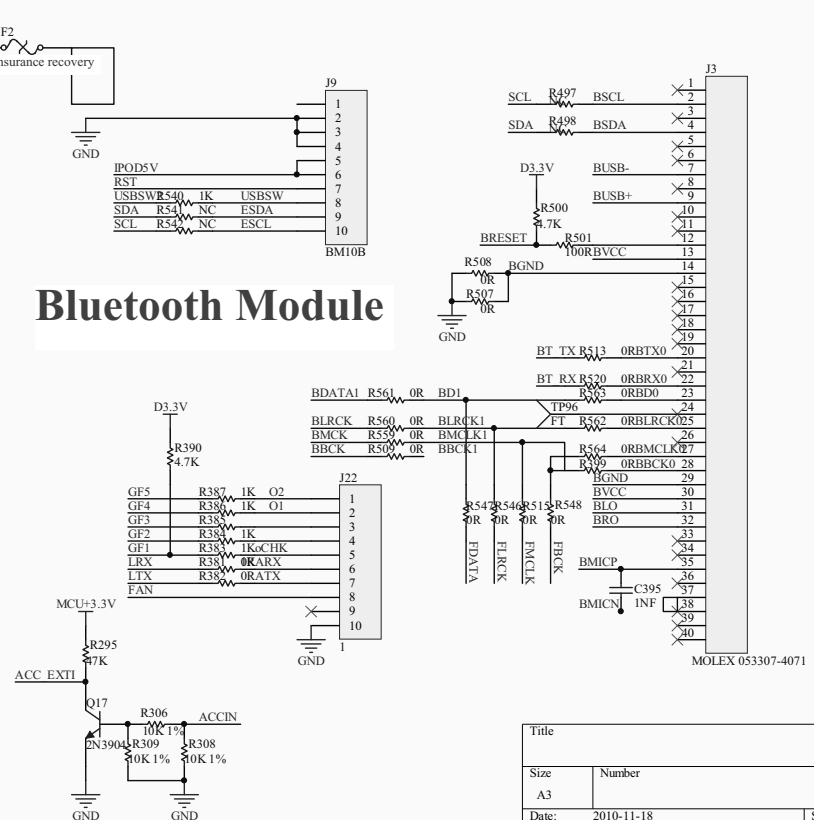
## GPRS



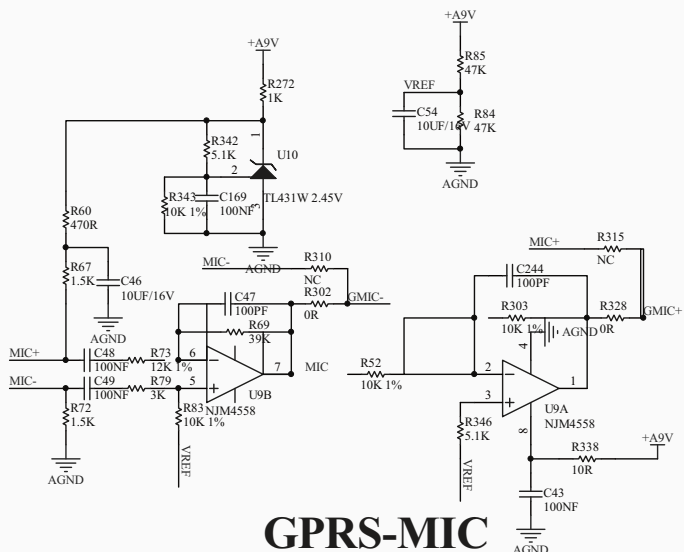
## DVD Interface



## Bluetooth Module

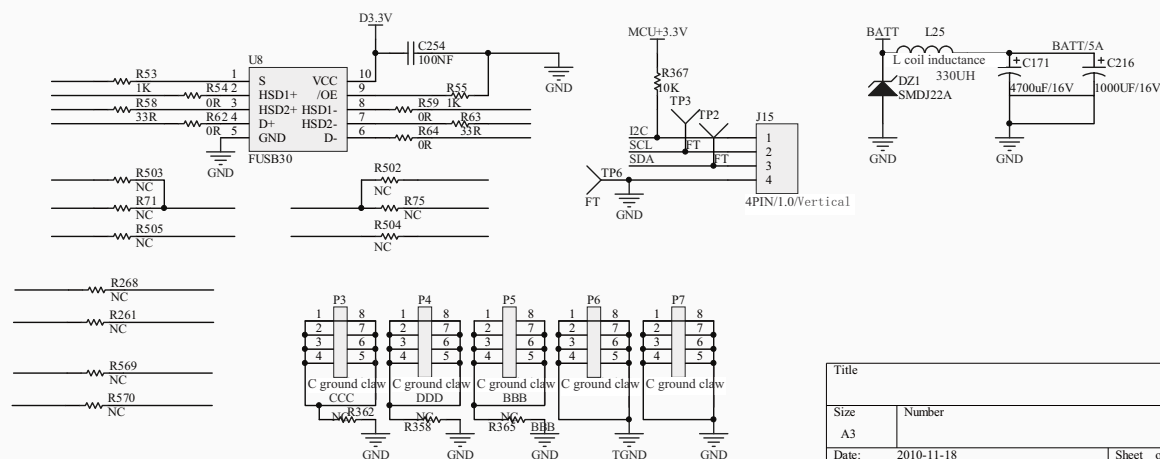
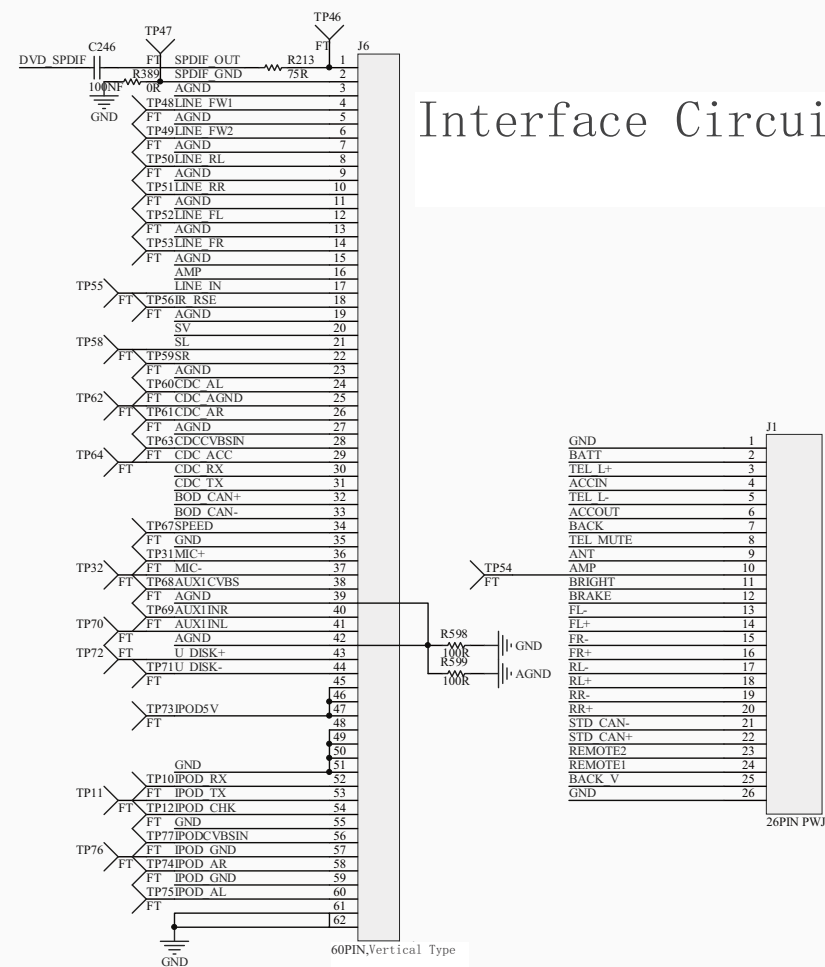
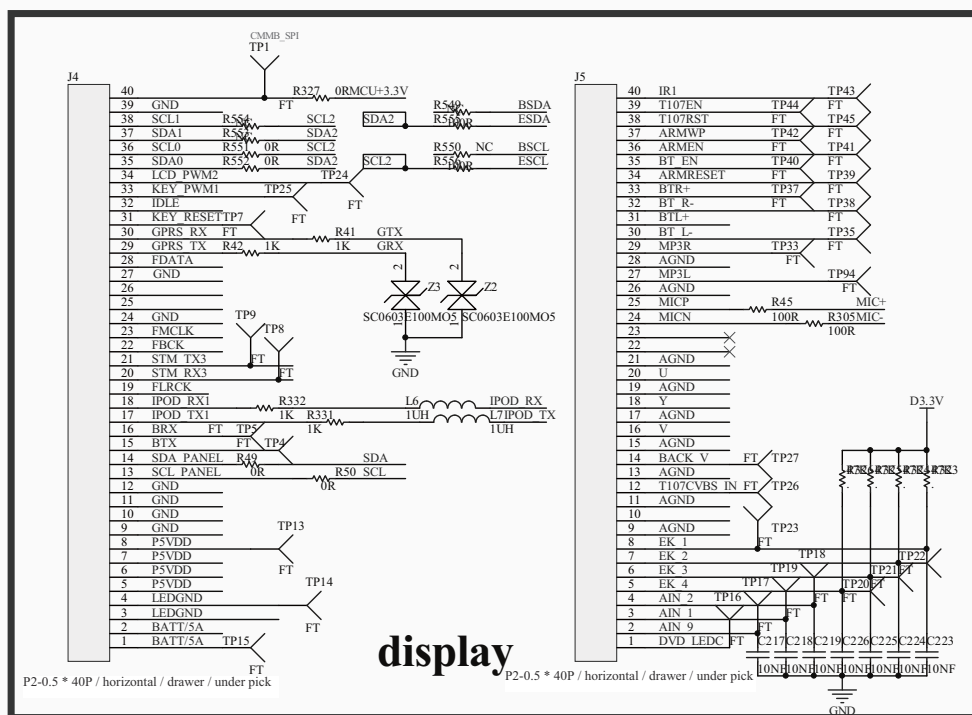


## GPRS-MIC



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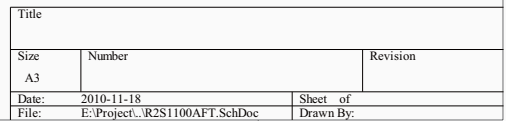
## Interface Circuit



Title			
Size A3	Number		Revision
Date:	2010-11-18	Sheet	of
File:	E:\Project\_接口市路_SchDoc	Drawn By:	

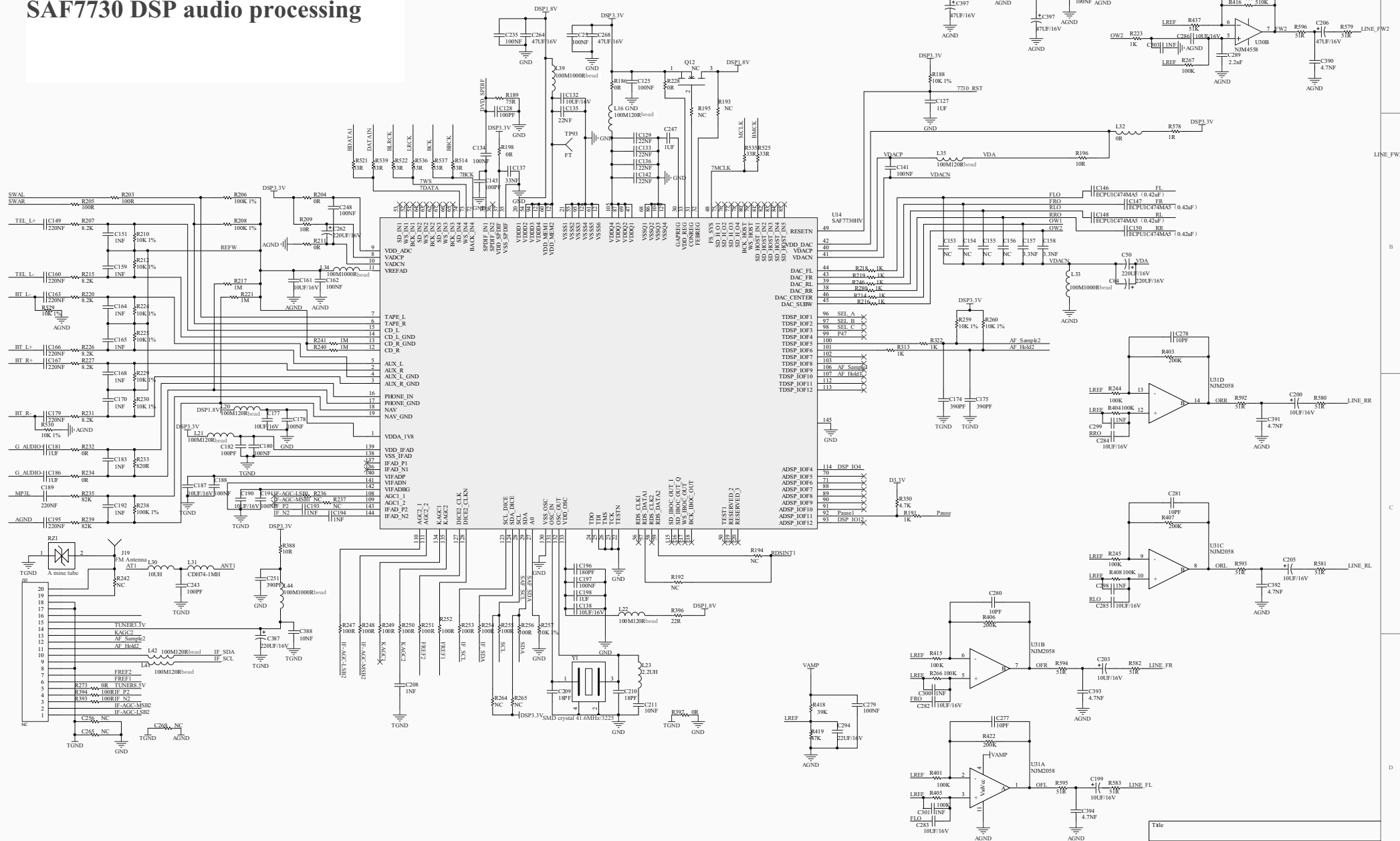


## A



7	8
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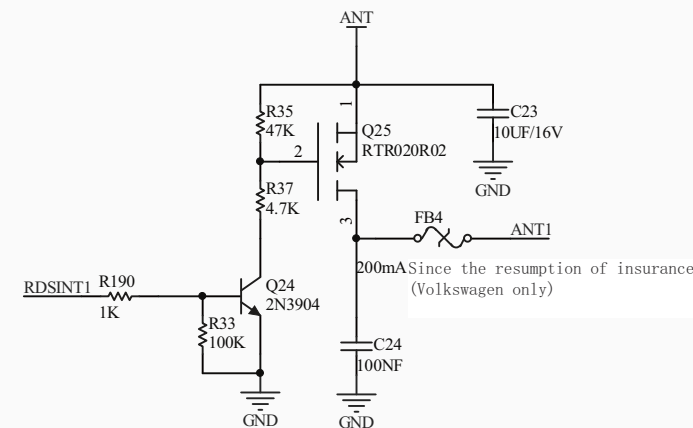
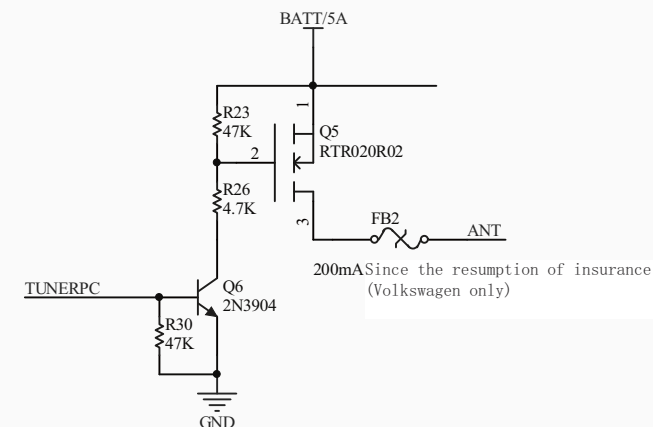
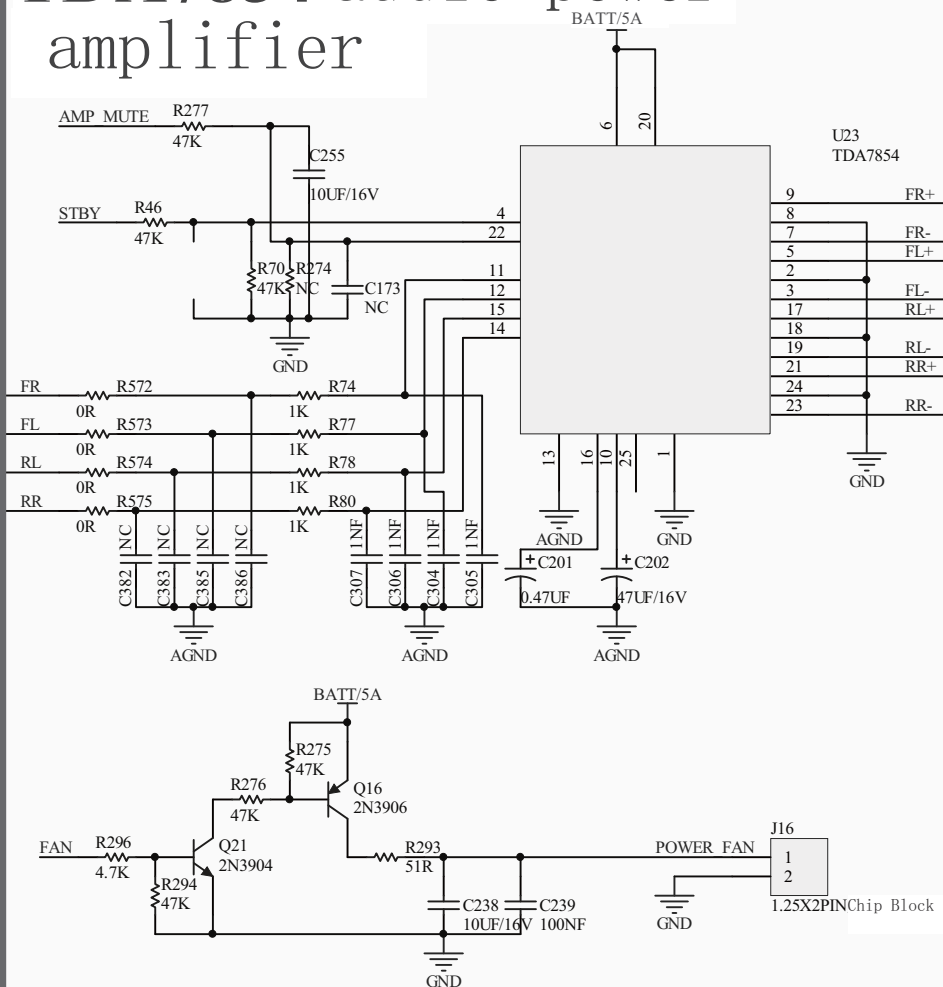
# SAF7730 DSP audio processing



Title		
Size	Number	Revision
A2		
Date	2010-11-18	Sheet of
File	E:\Project\7730\SchDoc	Down By



# TDA7854 audio power amplifier

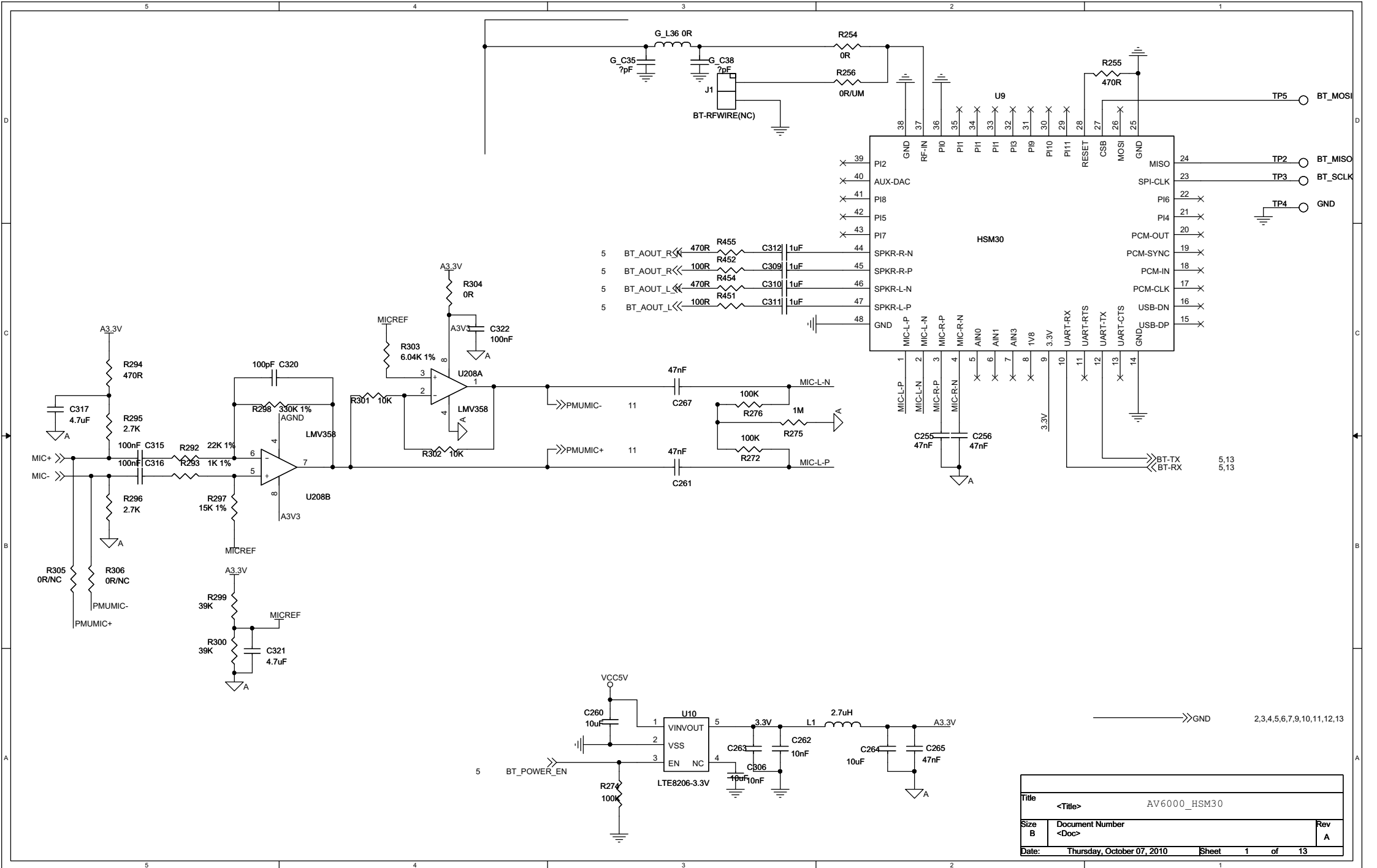


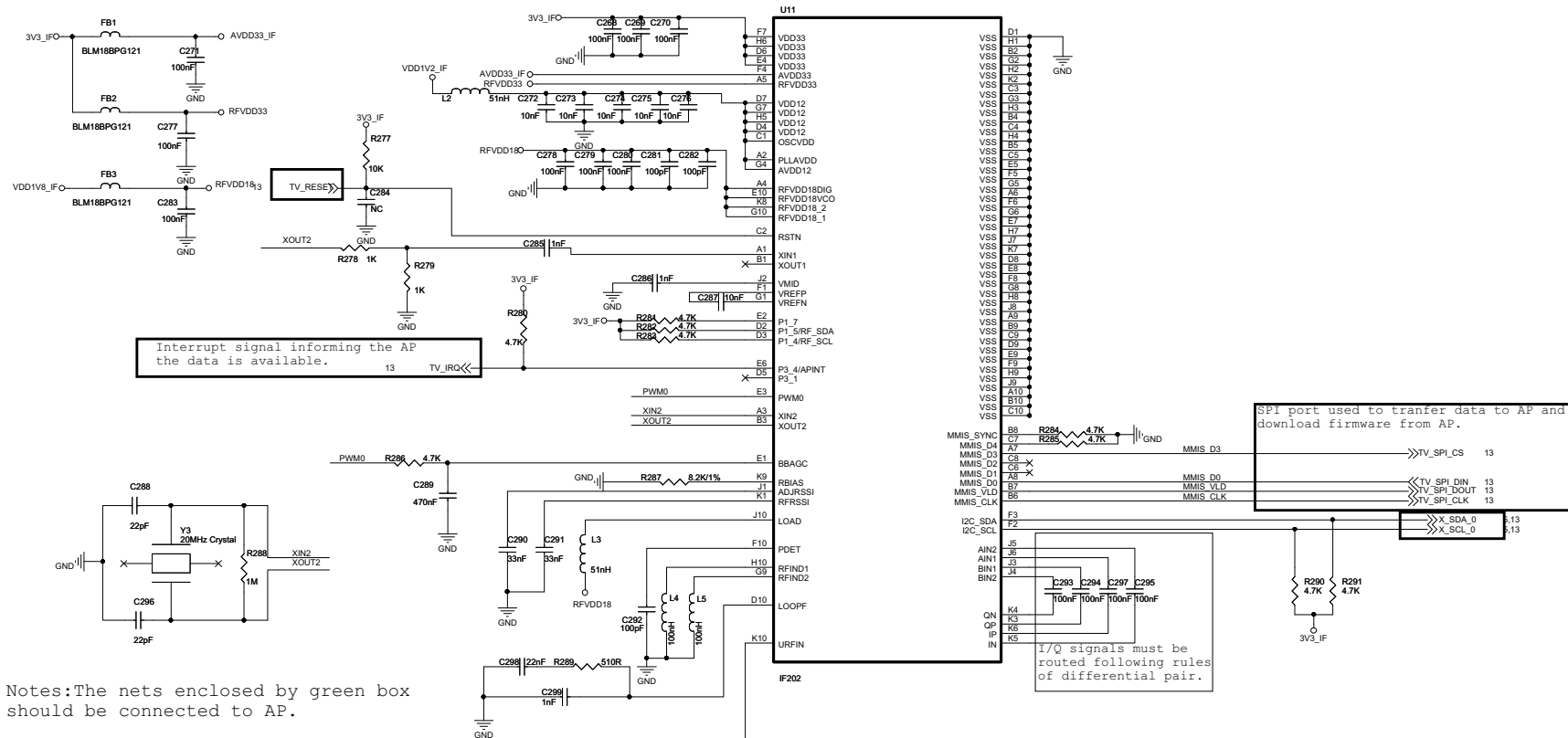
## Antenna power control

Title		
Size A4	Number	Revision
Date:	2010-11-18	Sheet of
File:	E:\Project\..功放-ANT.SchDoc	Drawn By:

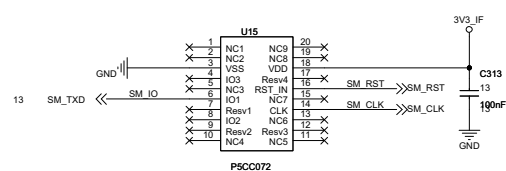
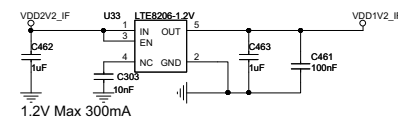
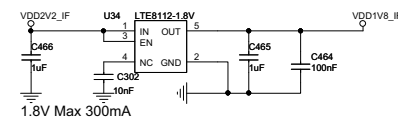
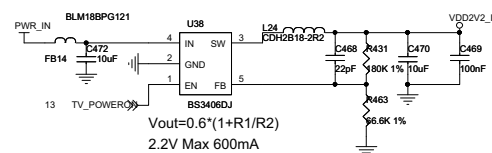
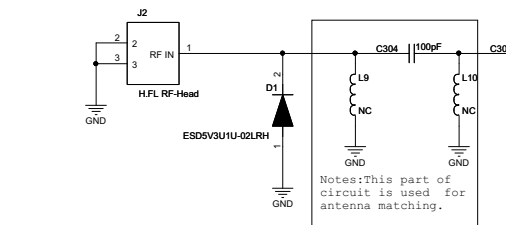








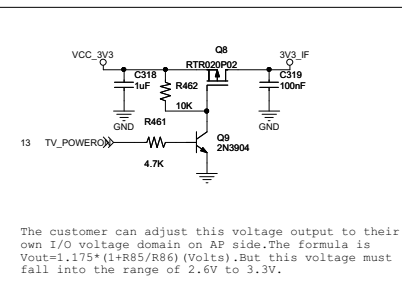
Notes: The nets enclosed by green box should be connected to AP.

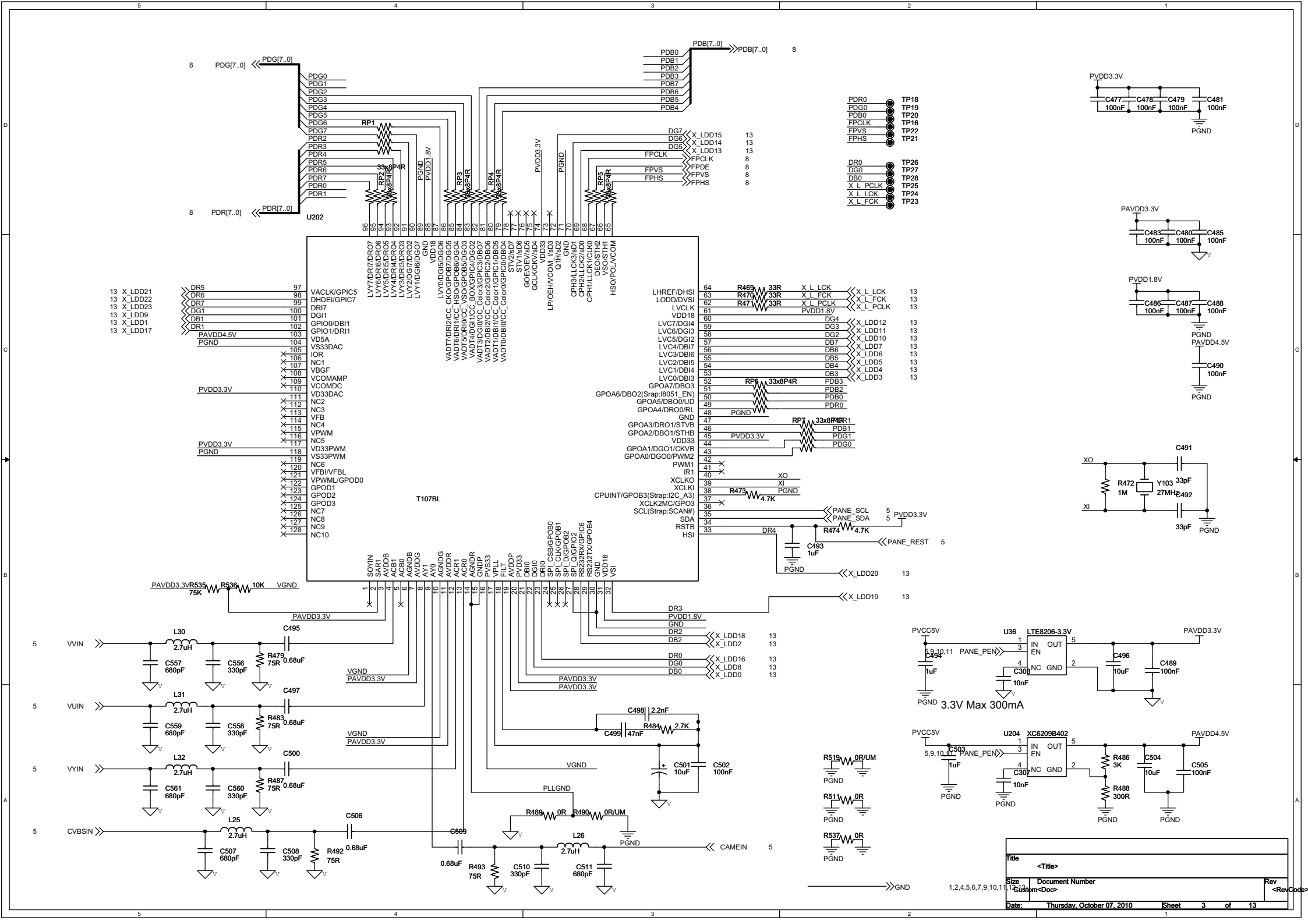


VCC\_3V3 5,7,11,12,13  
GND 1,3,4,5,6,7,9,10,11,12,13

0 < V<sub>EN</sub> < 0.4  
2.0 < V<sub>EN\_H</sub> < V<sub>IN</sub>

A signal powering on the whole TV subsystem should be connected to a GPIO on the AP side. IF202 has no shutdown control pin, so this signal can be used to power down the TV subsystem when it is not needed.



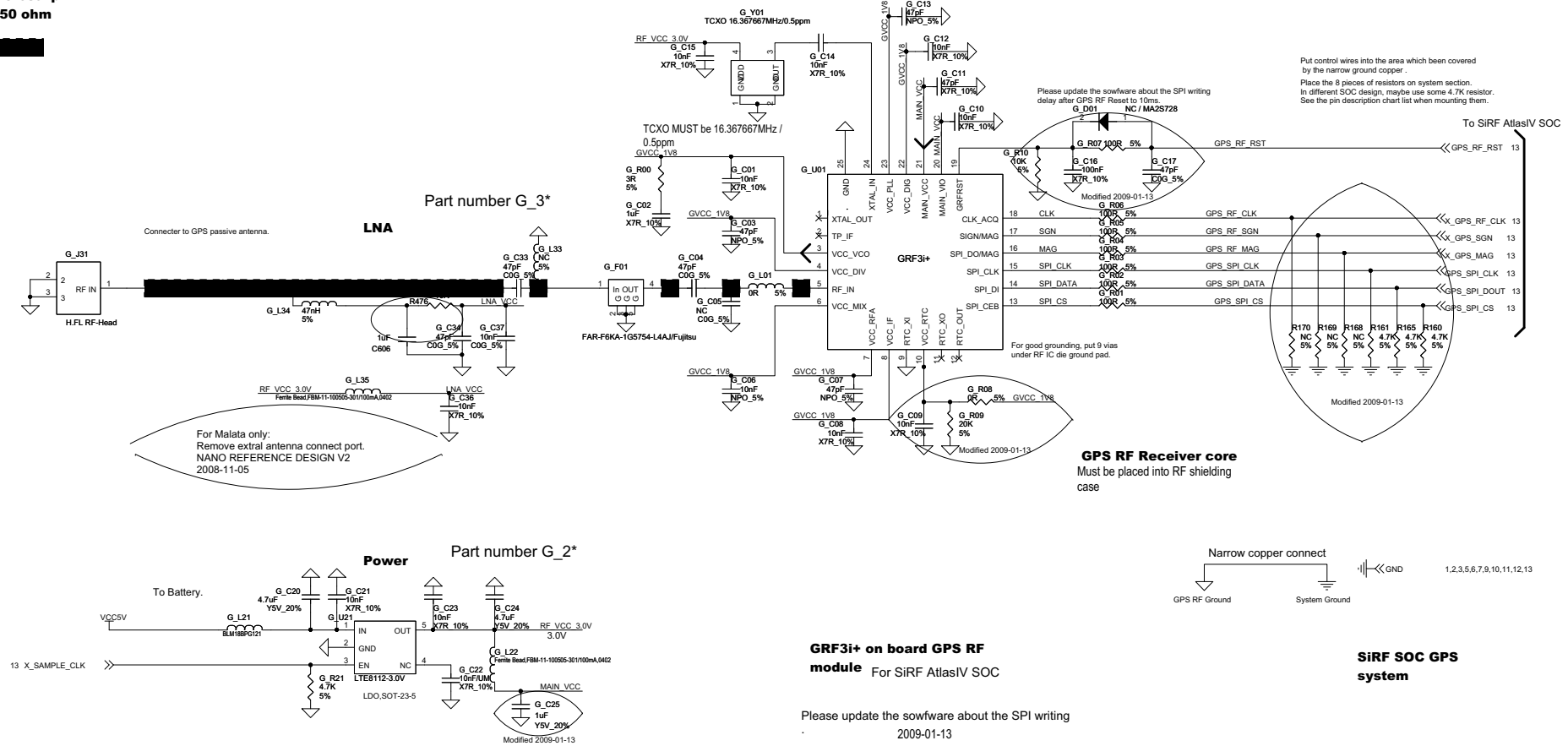


**Caution:**

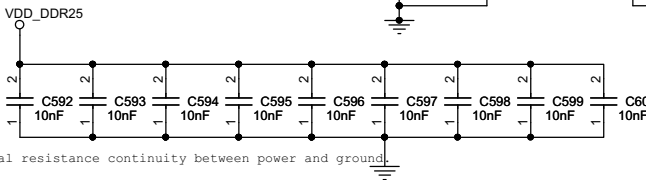
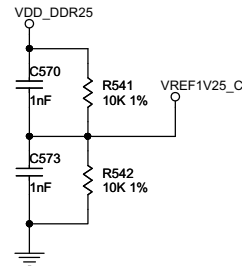
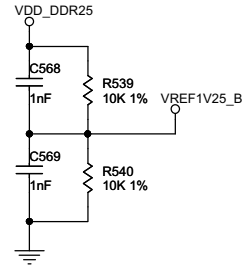
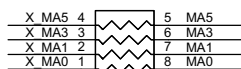
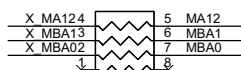
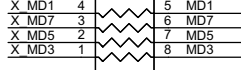
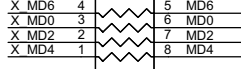
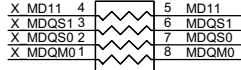
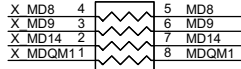
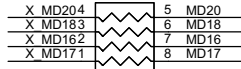
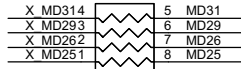
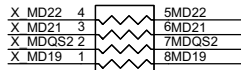
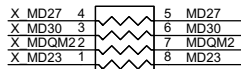
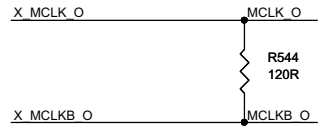
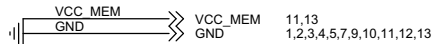
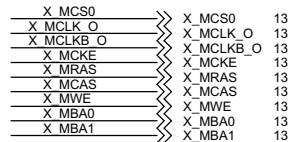
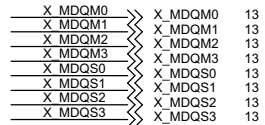
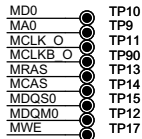
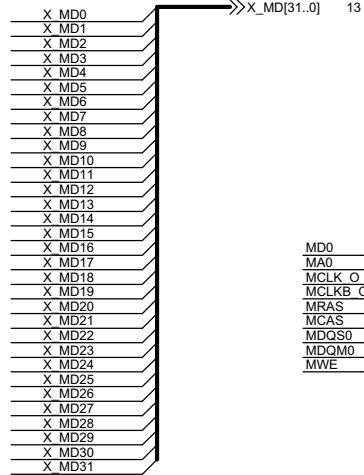
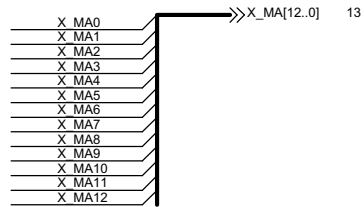
1. This page is RF module, so should pay more attention to PCB layout. The RF Z0 is 50ohm, the drawing should fit RF rules and RF portion must be put into one shielding case.
2. The value of components which marked asterisk "\*" may be tuned in different product. These components are in RF matching nets, their values are effected by the PCB material parameter, tolerance of component, and so on.
3. The idiosyncrasy and tolerance of passive components such as capacitors, inductances, has been appointed. These components just can be substituted by which are more high precision.
4. There are many DC filtering capacitors in the schematic, please put them close to the source pins. Putting some ground vias near to the ground pin and in ground panel is well for DC filtering and EMI rejection also.

**RF Microstrip**  
**Z0= 50 ohm**

Part number G\_0/1\*

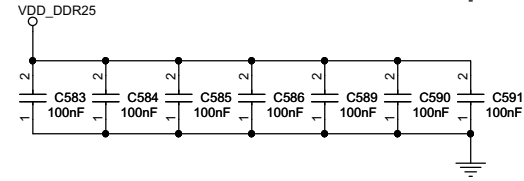
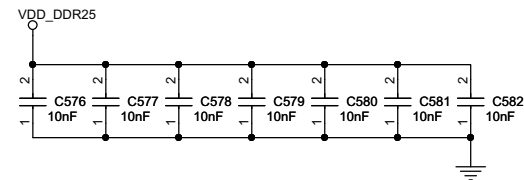
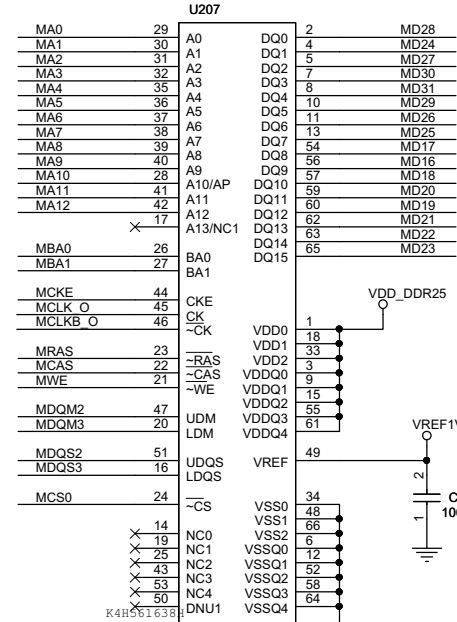
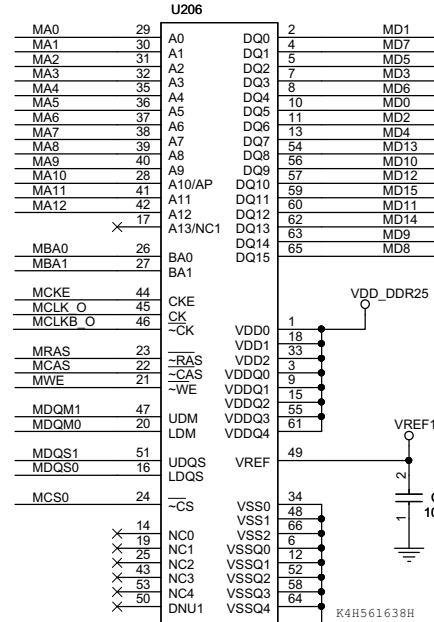






For DDR signal resistance continuity between power and ground.

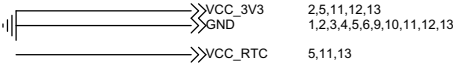
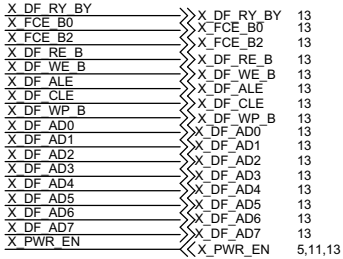
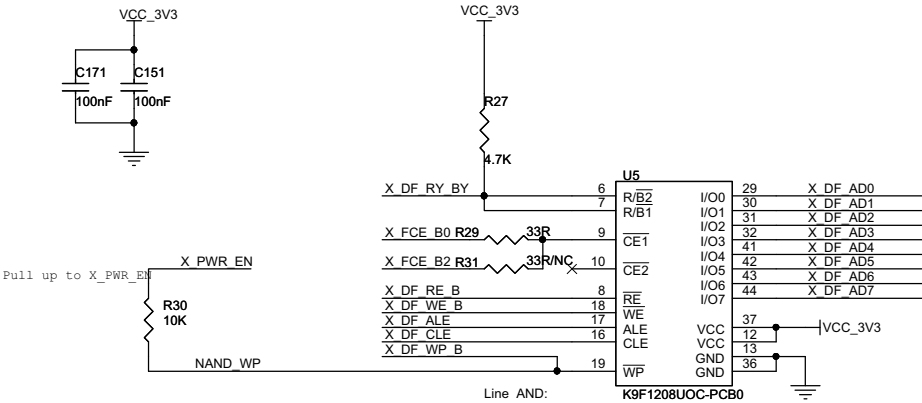
16M\*16, DDR1 SDRAM



SiRF Inc.  
Suite 3401, KingTower, PuDong,  
ShangHai, China, (201206)  
Tel: 86-021-28981400

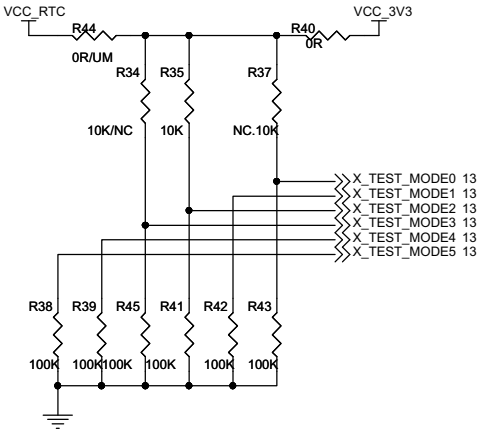
Title Nano  
Size B Document Name DDR1 RAM Rev 2.0  
Date: Thursday, October 07, 2010 Sheet 6 of 13

K9G8G08-----2K/page:  
K9GAG08-----4K/page:



Now

Boot configuration	X_TEST_MODE[5:0]
Boundary Scan	6b110000
SLC Nand Boot 2KB Page 8 Bit	6b000101
MLC Nand Boot 2KB Page 8 Bit	6b001000
INAND Boot	6b001100
EFuse	6b110010
MLC Nand Boot 4KB Page 8 Bit	6b001001

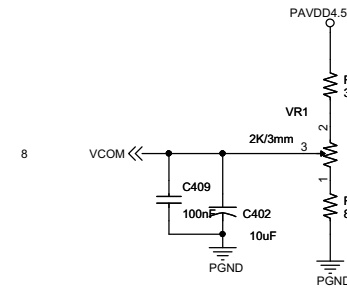
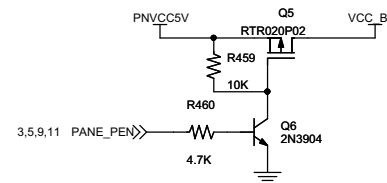
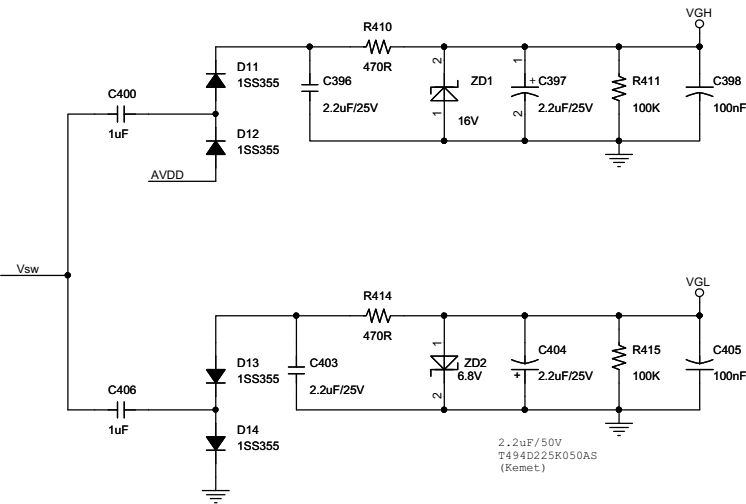
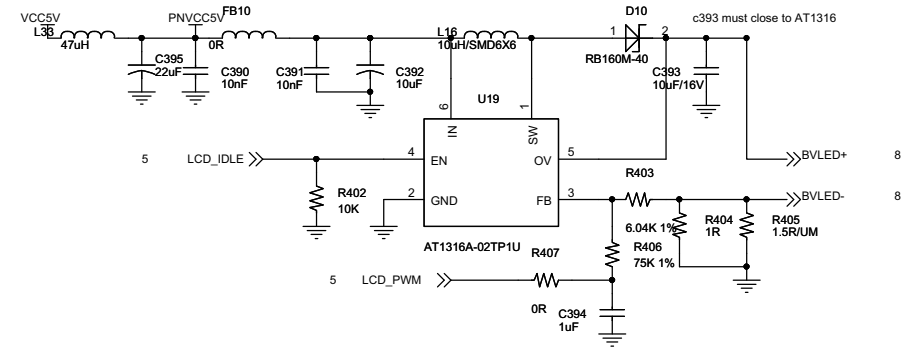
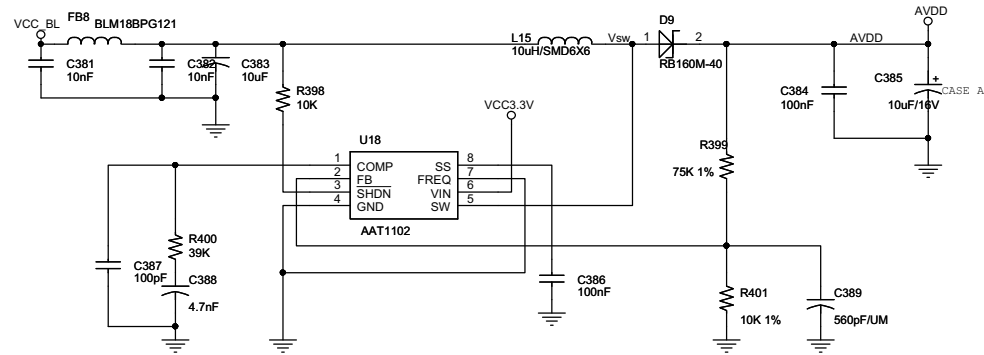


SiRF Inc.		
Suite 3401, KingTower, PuDong, Shanghai, China, (201206)		
Tel: 86-021-28981400		
Title	Nano	
Size	Document Name	Rev
B	MLC Flash	2.0
Date:	Thursday, October 07, 2010	Sheet 7 of 13



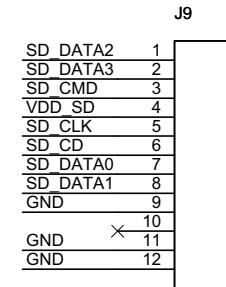
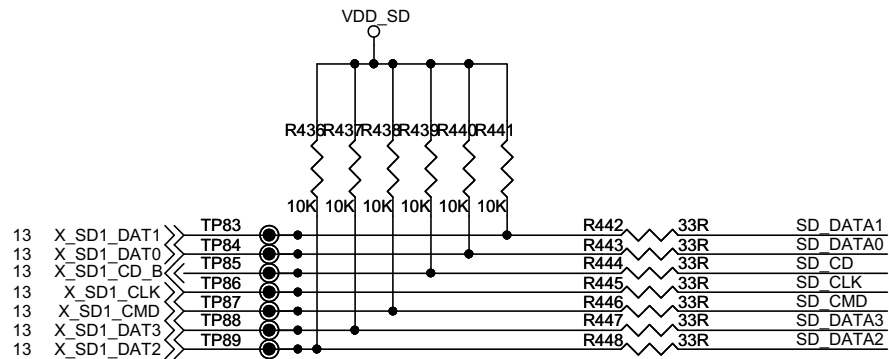






>>GND 1,2,3,4,5,6,7,9,11,12,13  
 >>BGND 5,9





SD CARD silkscreen  
10P/0.5mm interface under push-pull, horizontal

