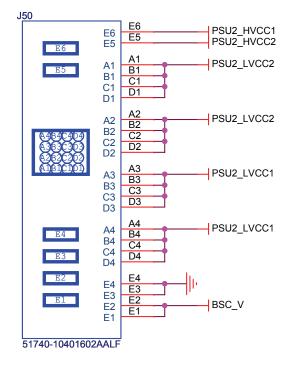
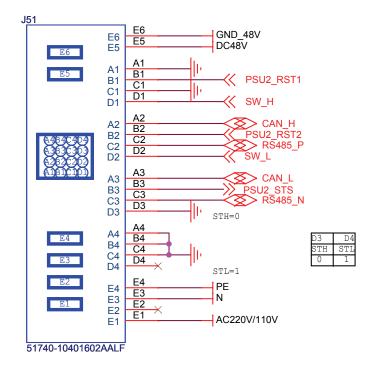
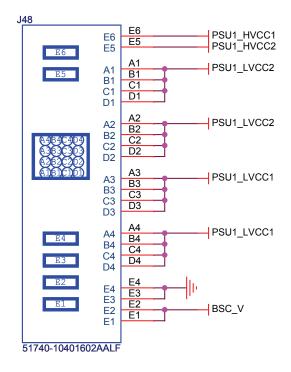


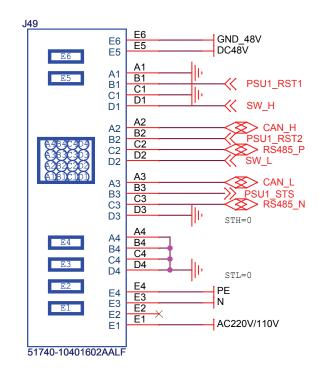
DS-6210 ICB Schematic Diagram (CHU\_2)



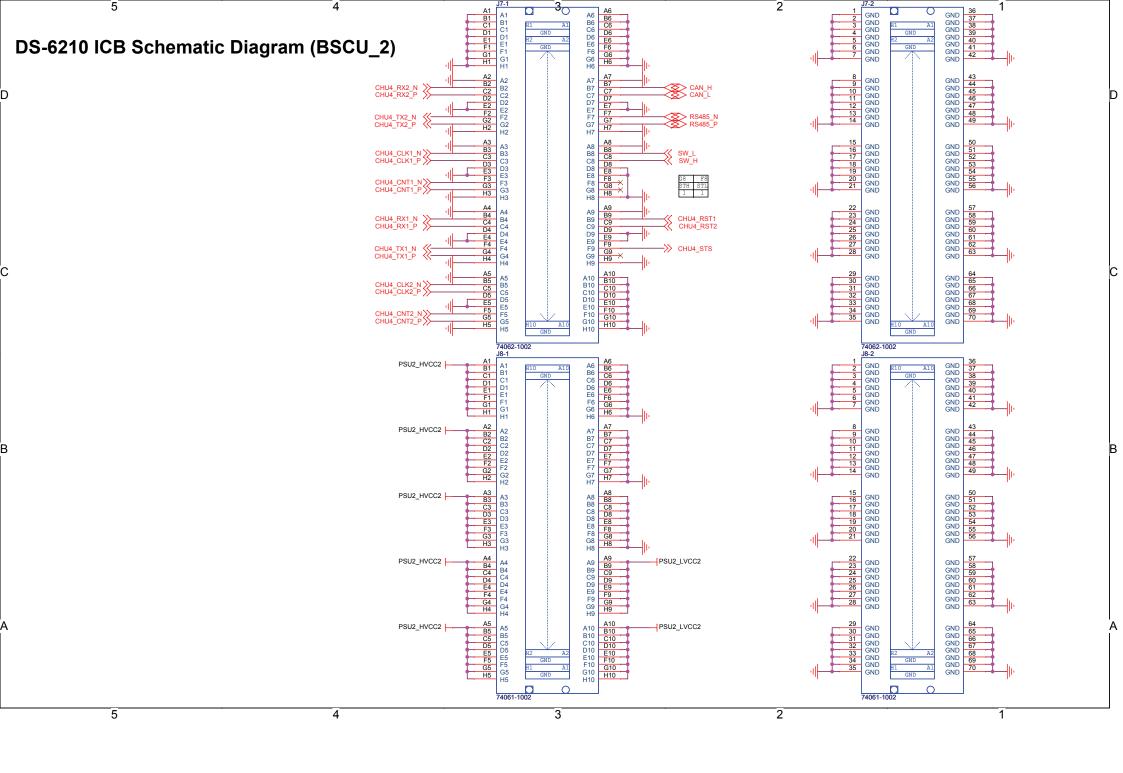


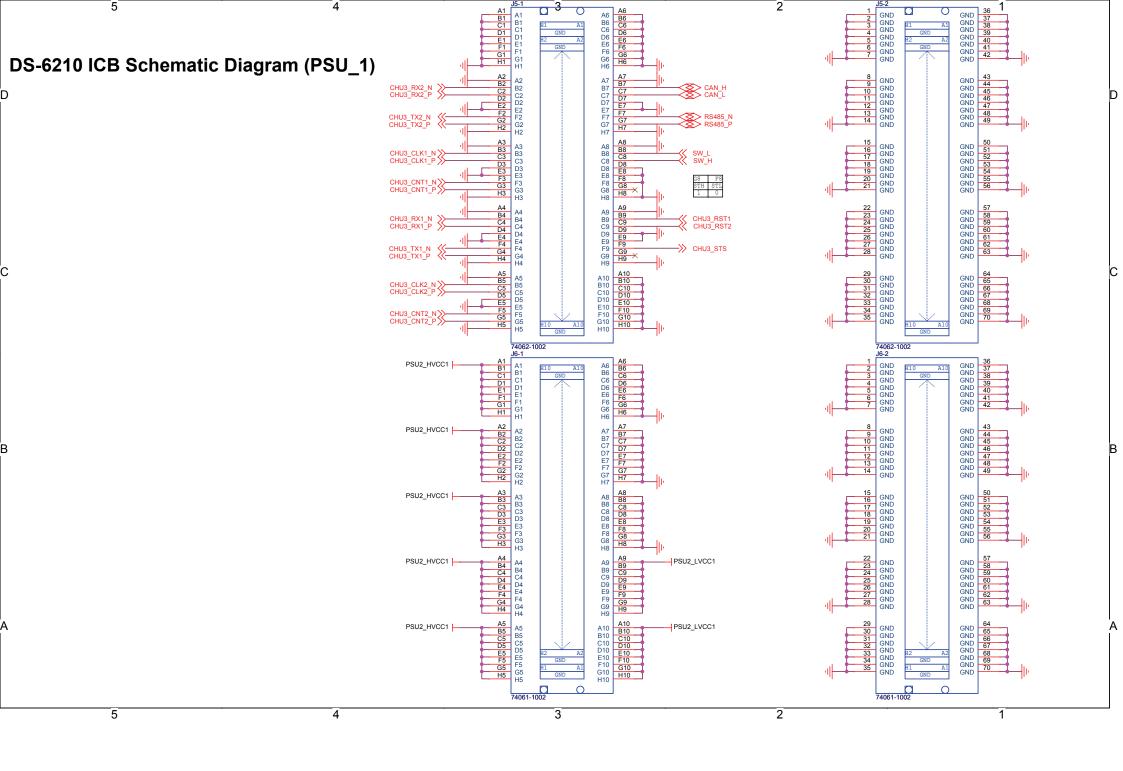
### DS-6210 ICB Schematic Diagram (CHU\_3)

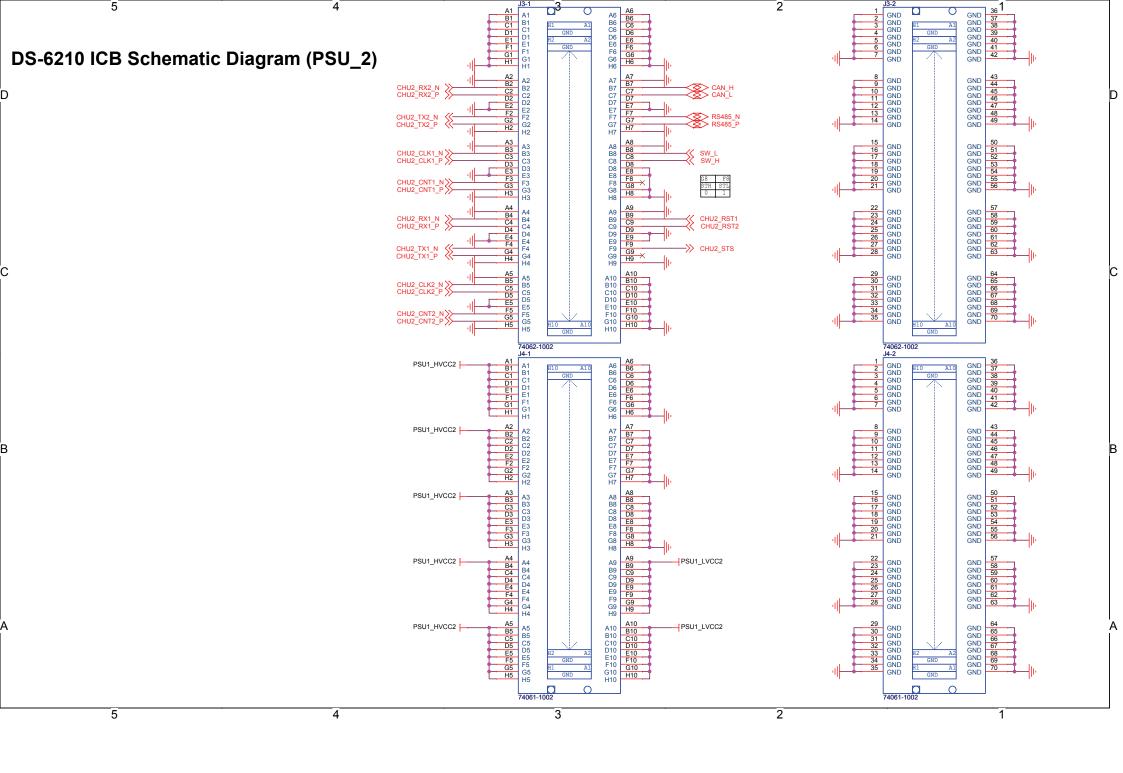


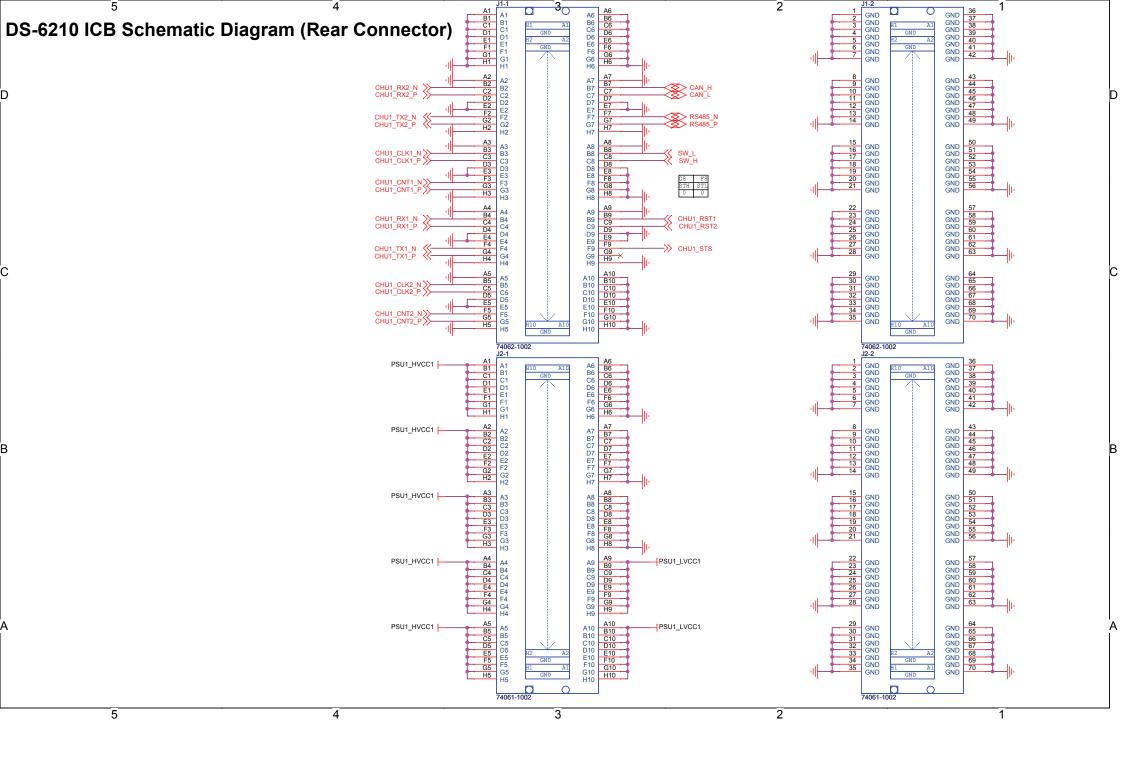


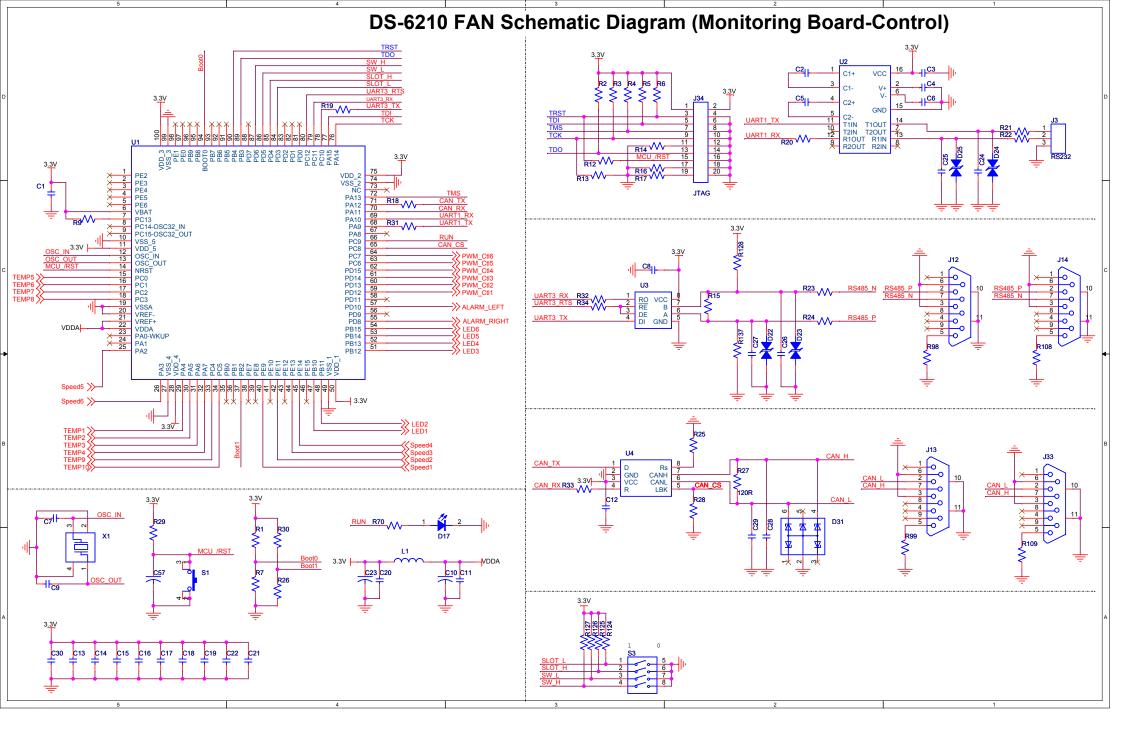
13	D4	
TH	STL	
0	0	



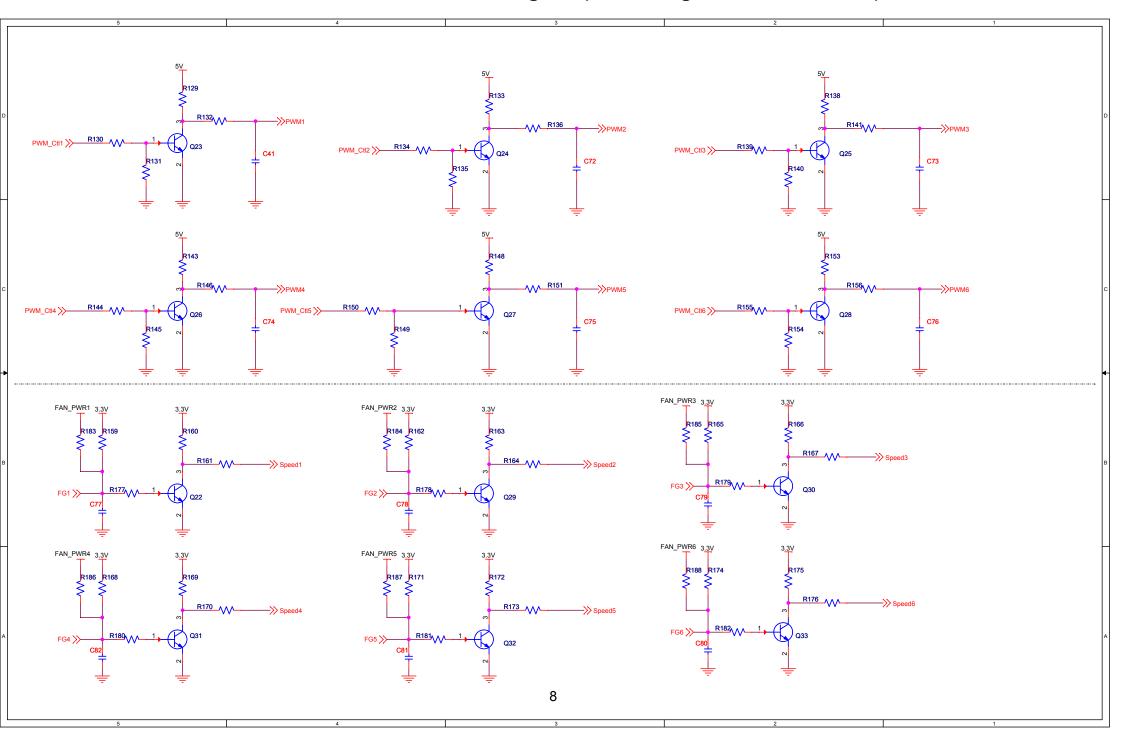




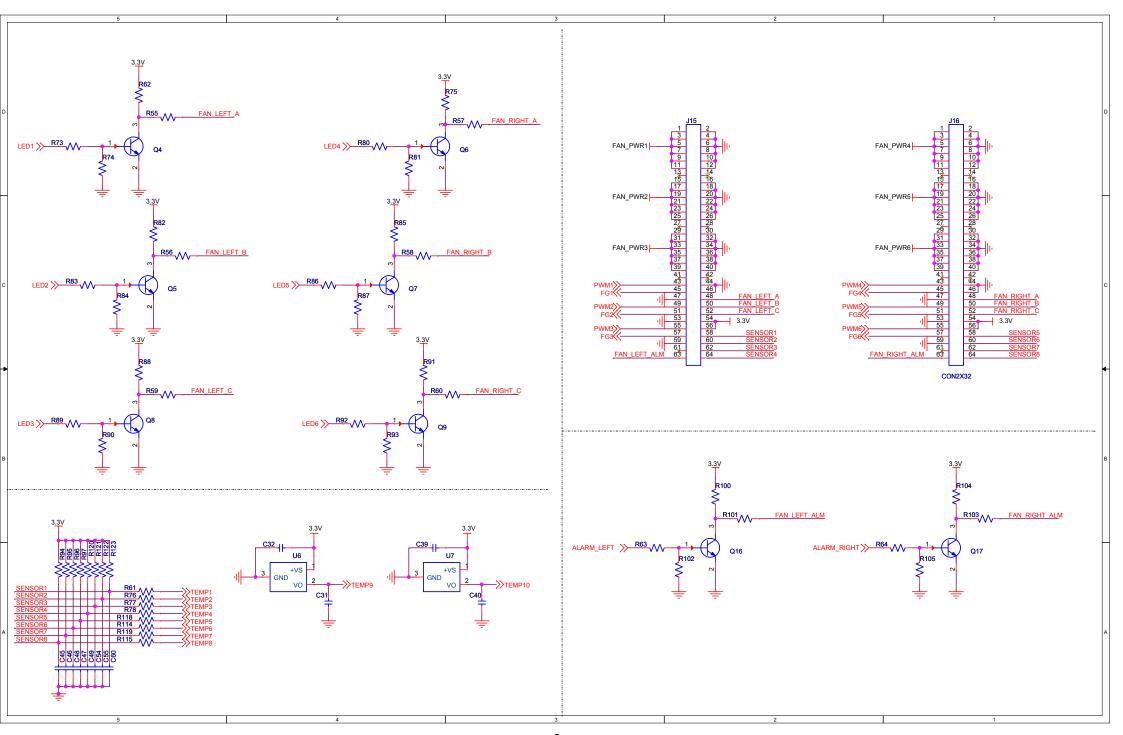


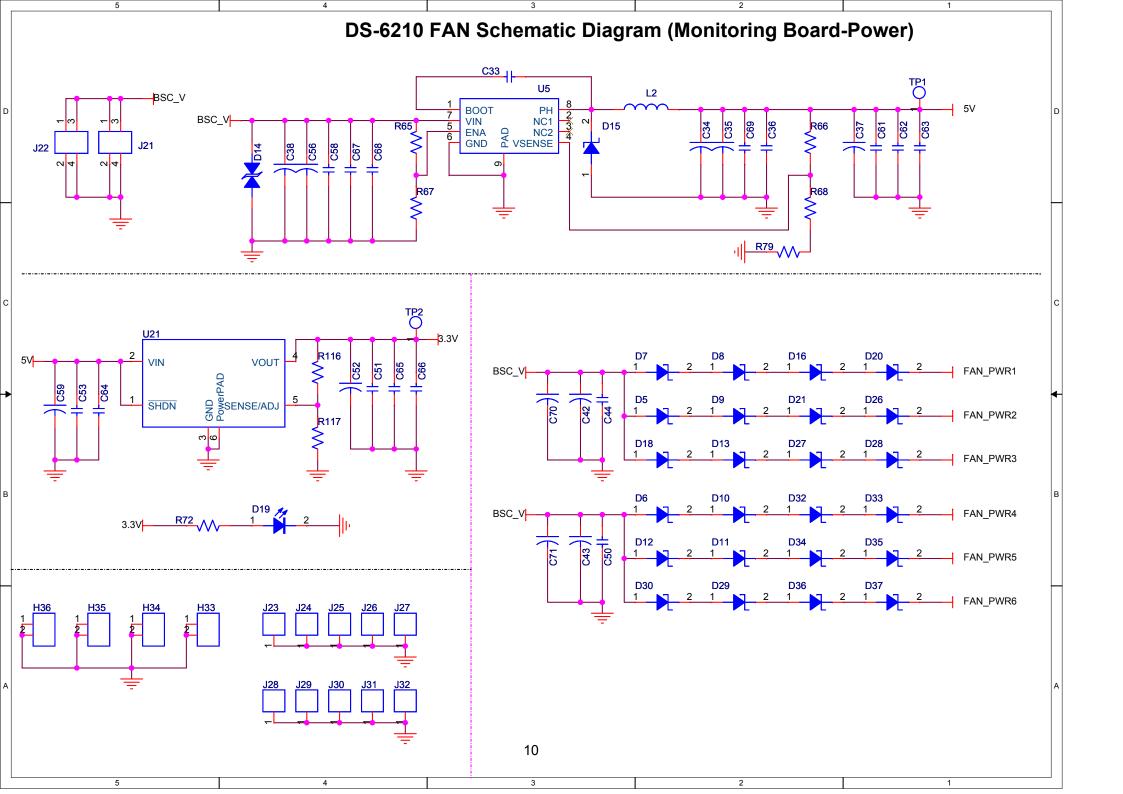


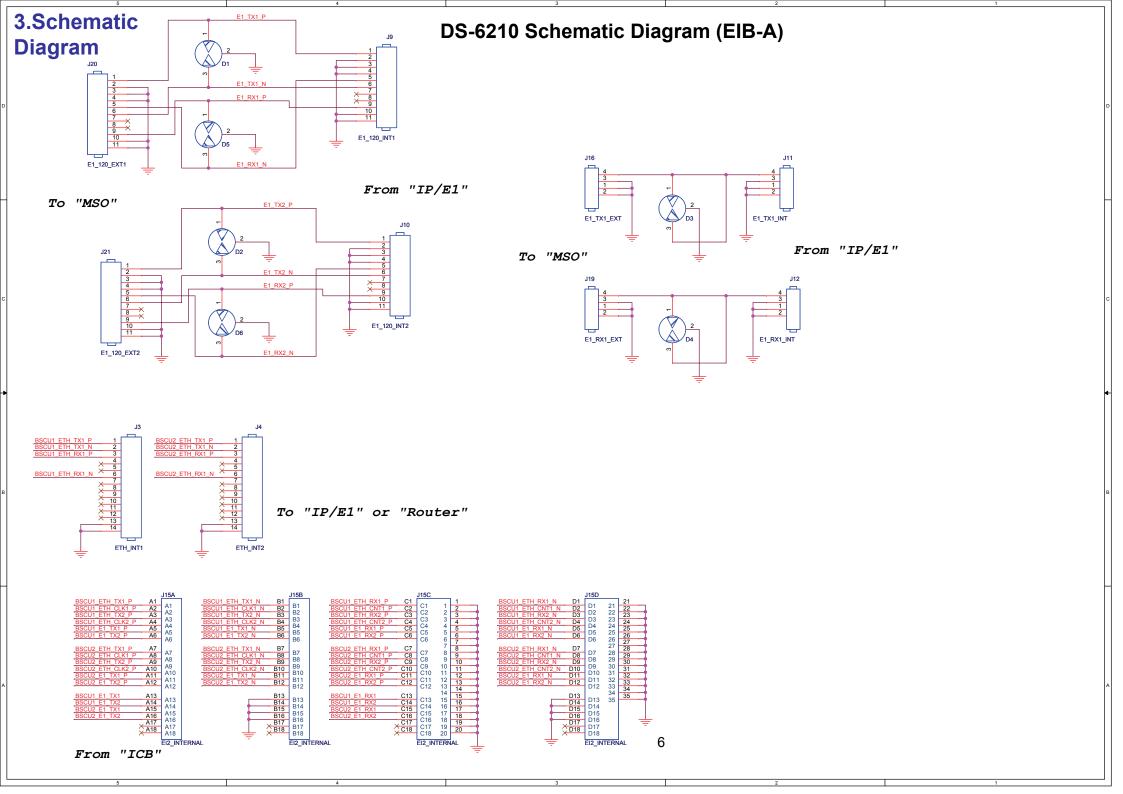
### **DS-6210 FAN Schematic Diagram (Monitoring Board-Fan Control)**

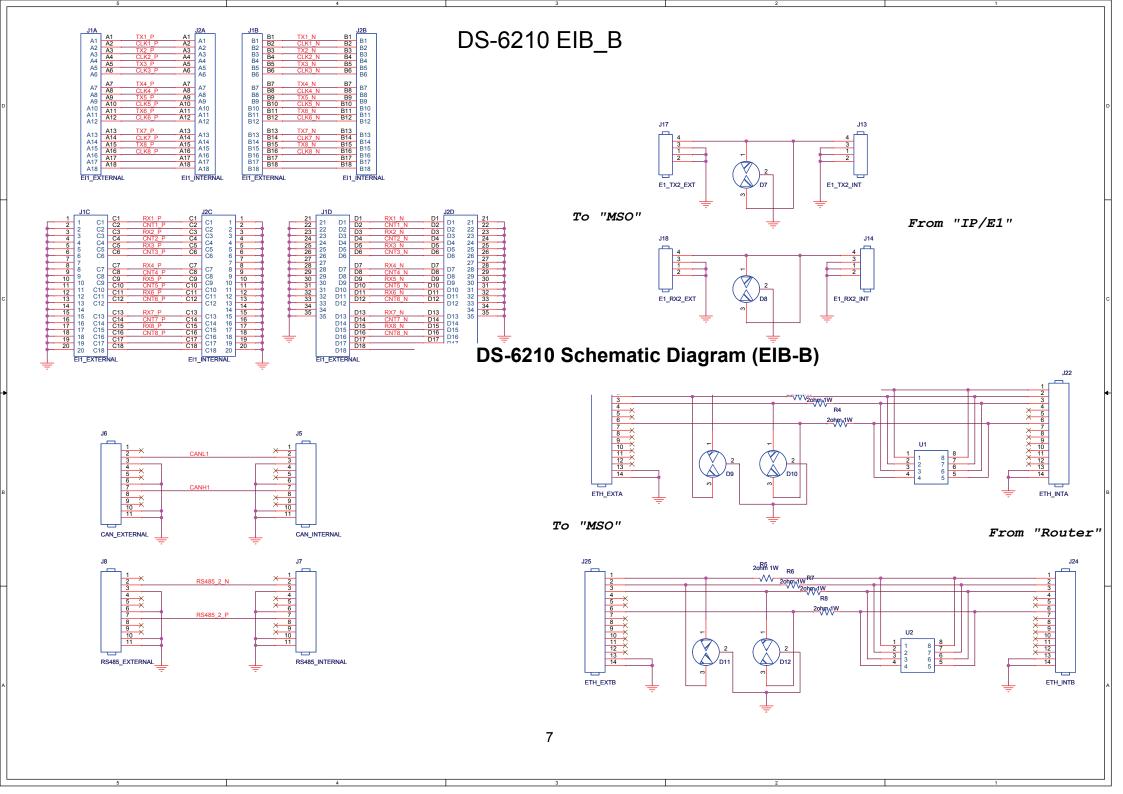


### **DS-6210 FAN Schematic Diagram (Monitoring Board-LED)**



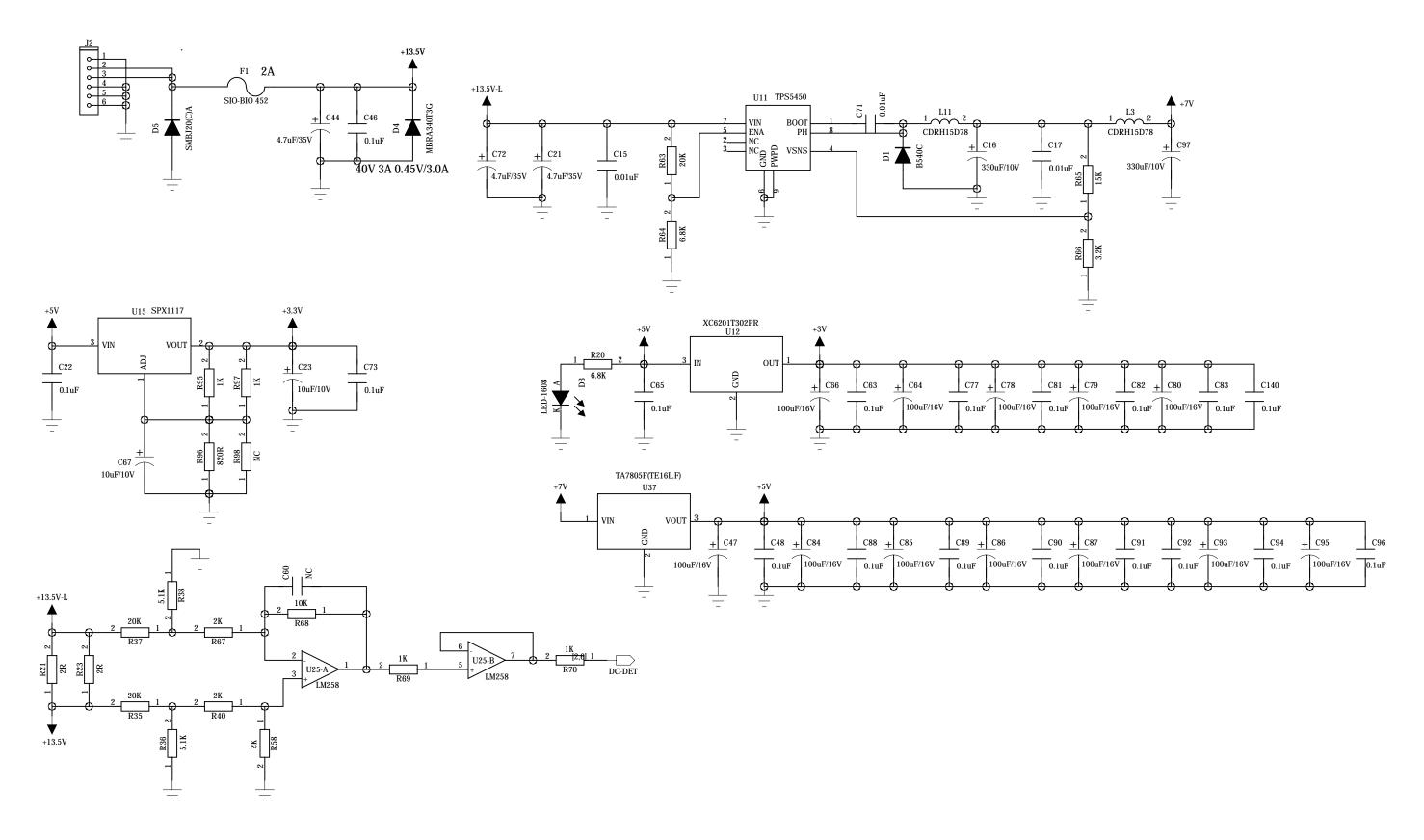




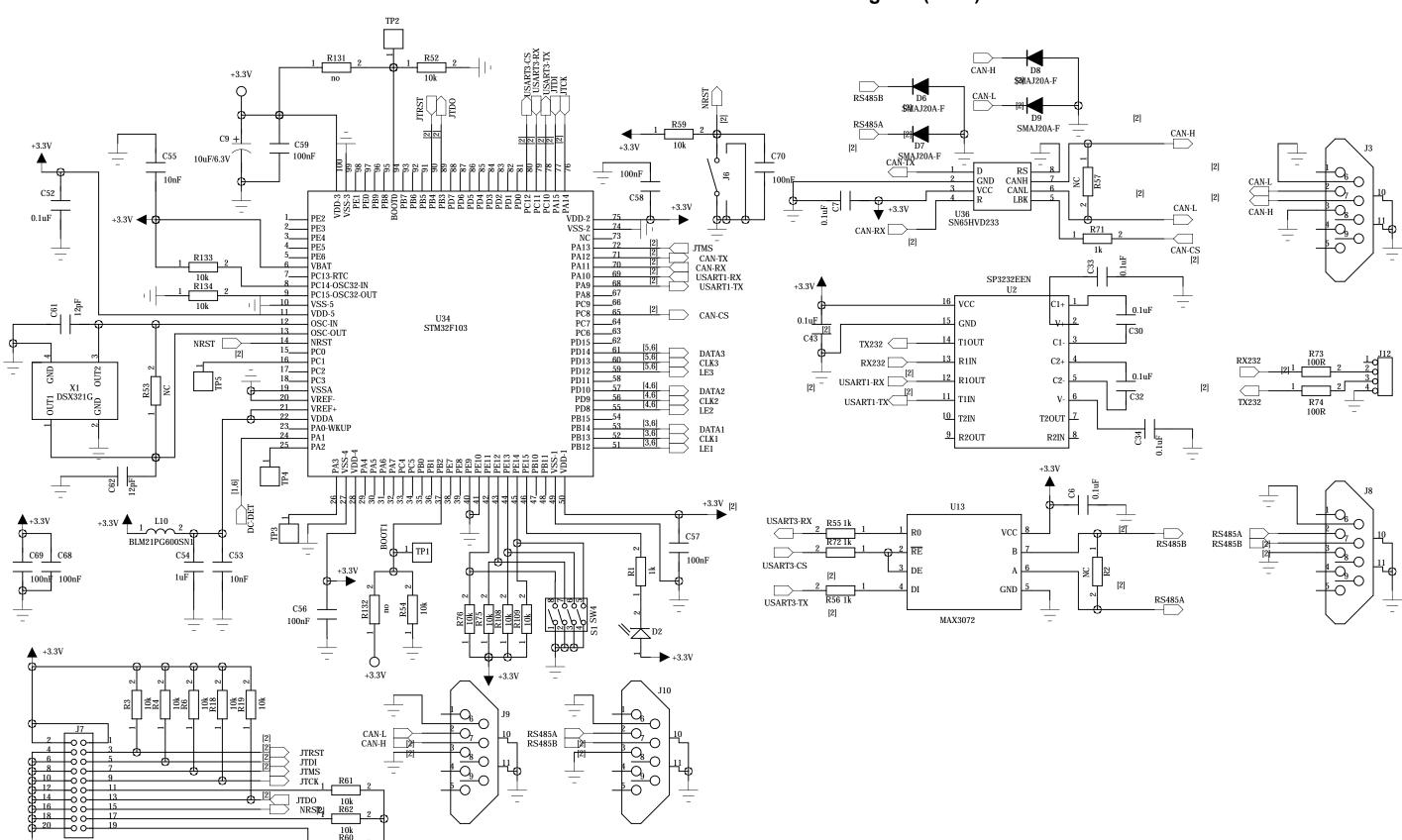


### 3. Schematic Diagram

### **DS-6210 DIU Schematic Diagram (Power)**

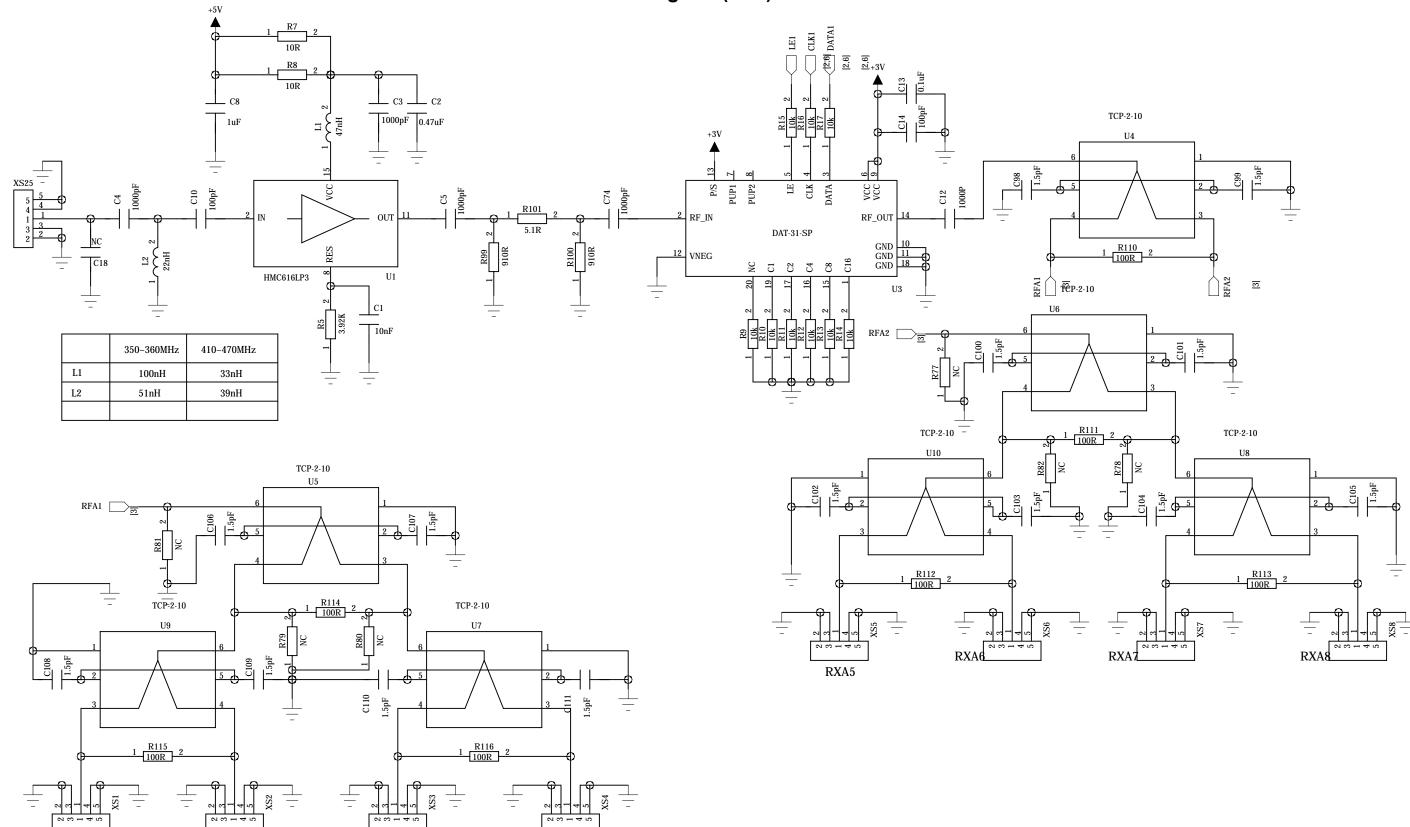


### **DS-6210 DIU Schematic Diagram (MCU)**



NRS[2]

### **DS-6210 DIU Schematic Diagram (RF1)**



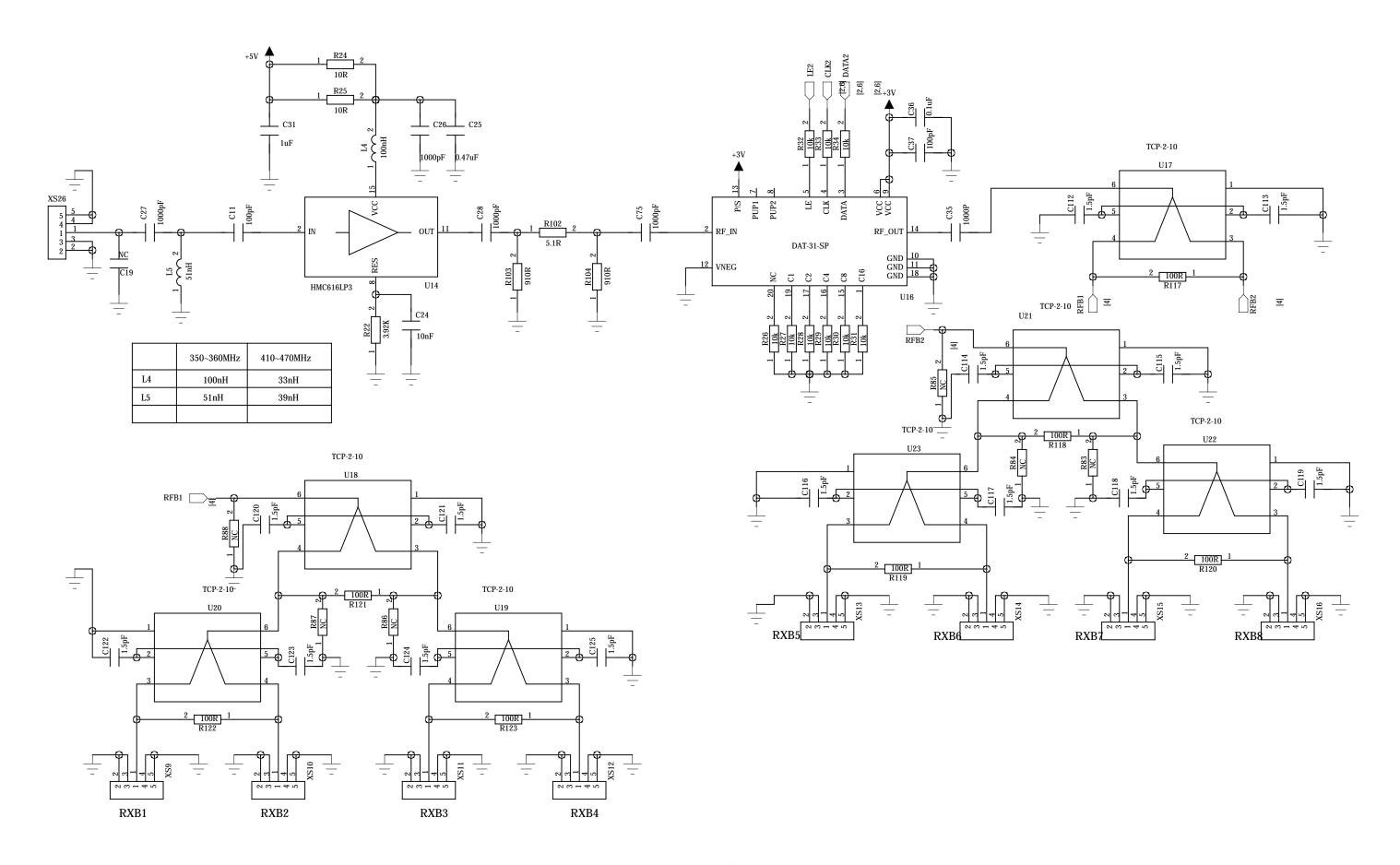
RXA4

RXA1

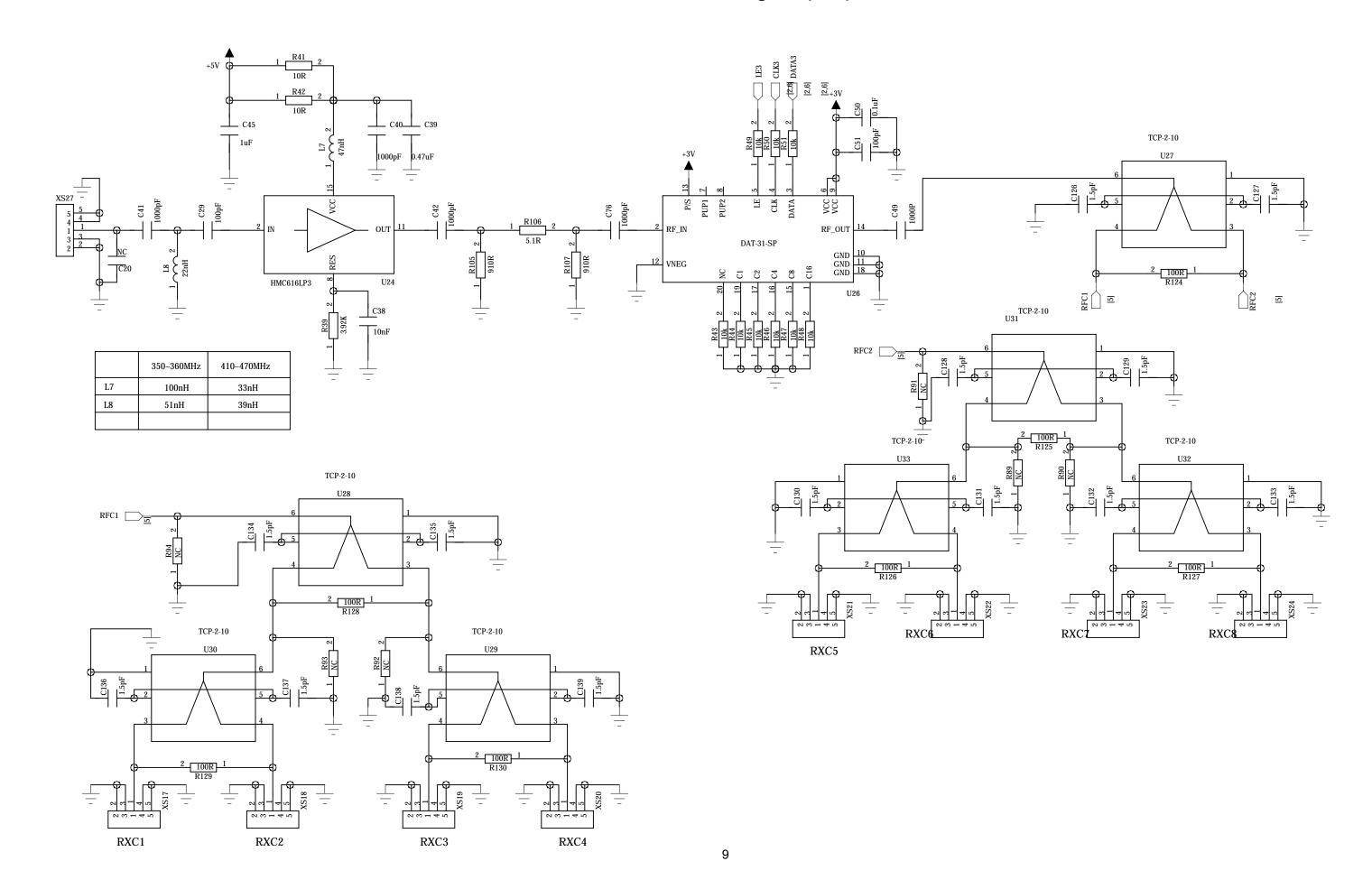
RXA2

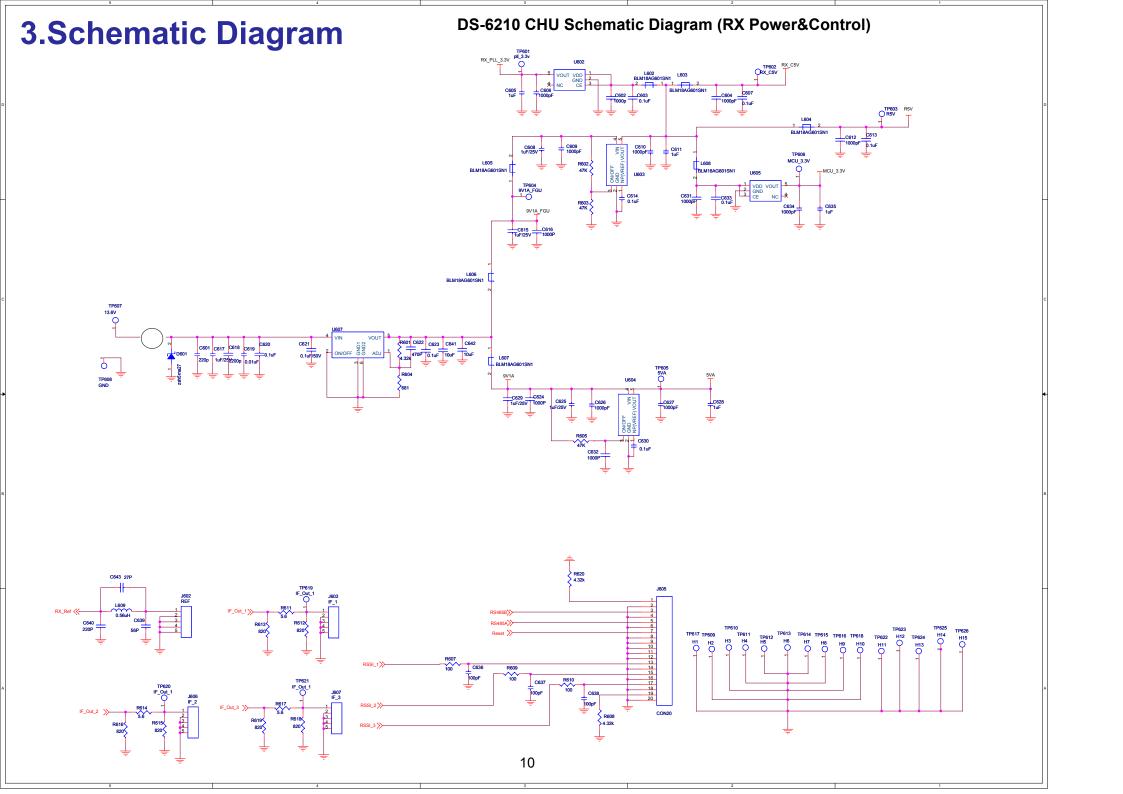
RXA3

### **DS-6210 DIU Schematic Diagram (RF2)**

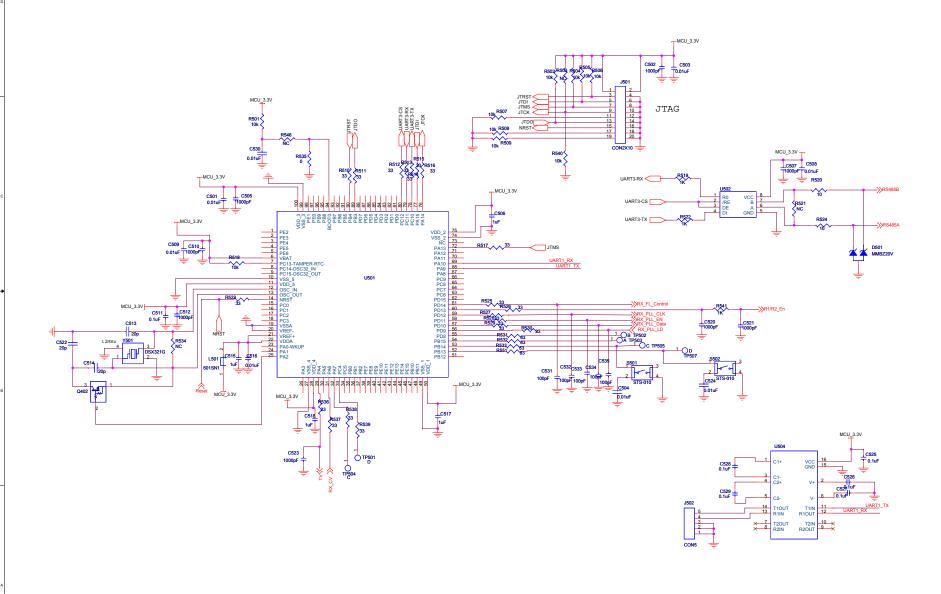


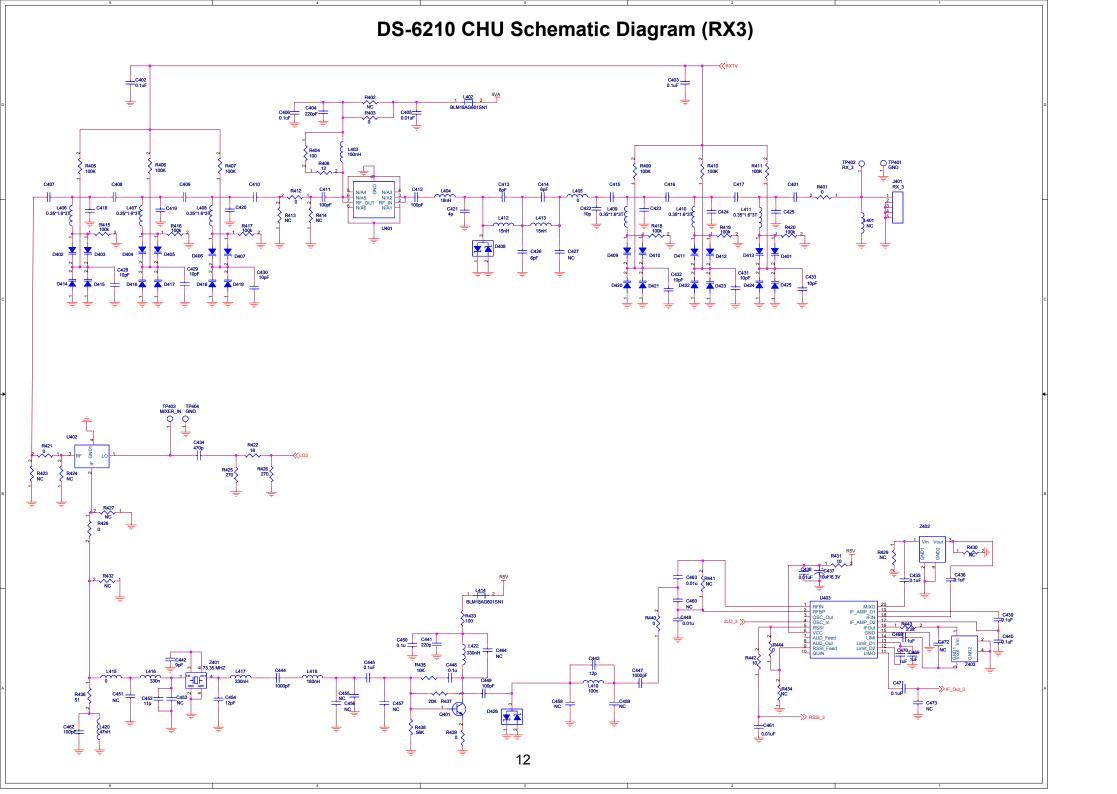
### **DS-6210 DIU Schematic Diagram (RF3)**





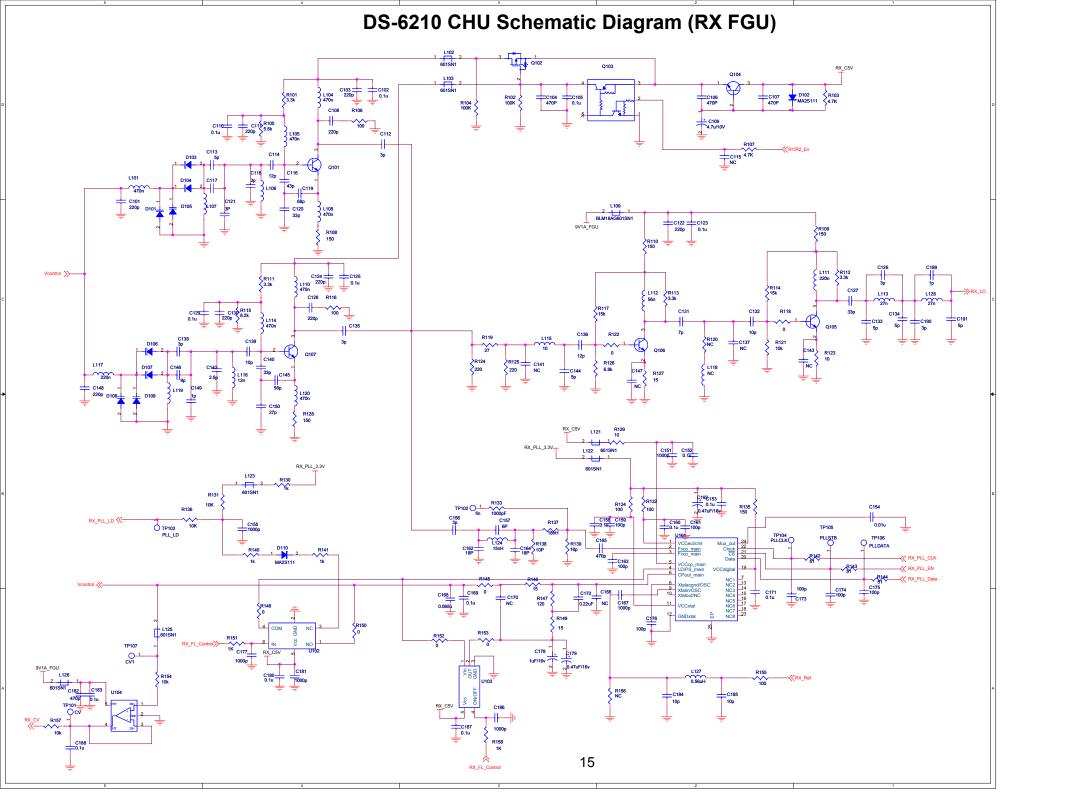
### **DS-6210 CHU Schematic Diagram (RX MCU)**

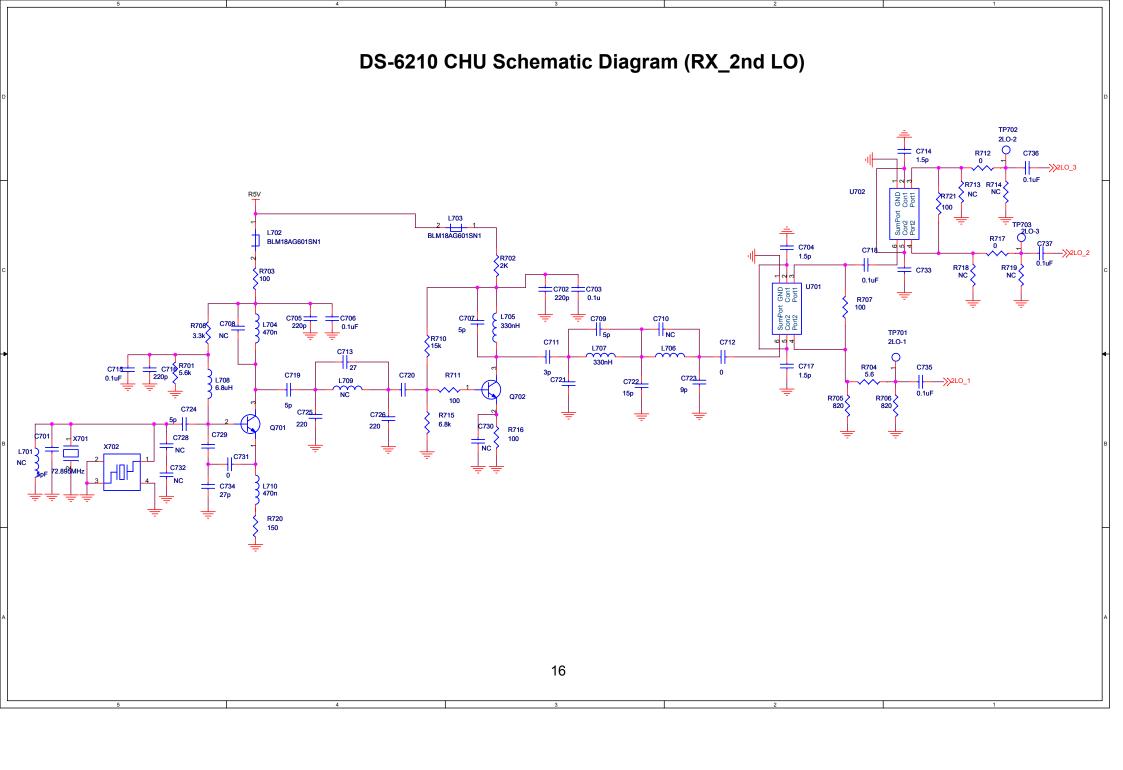




# **DS-6210 CHU Schematic Diagram (RX2)** 13

# **DS-6210 CHU Schematic Diagram (RX1)** 14

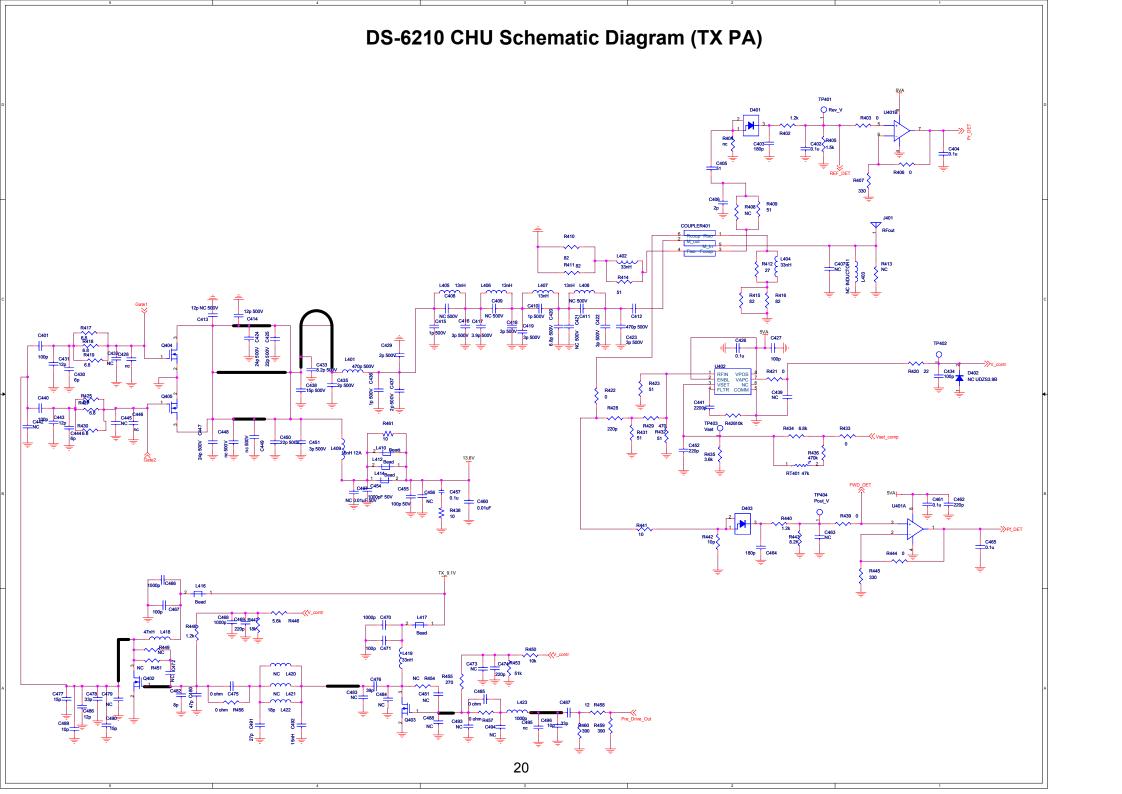


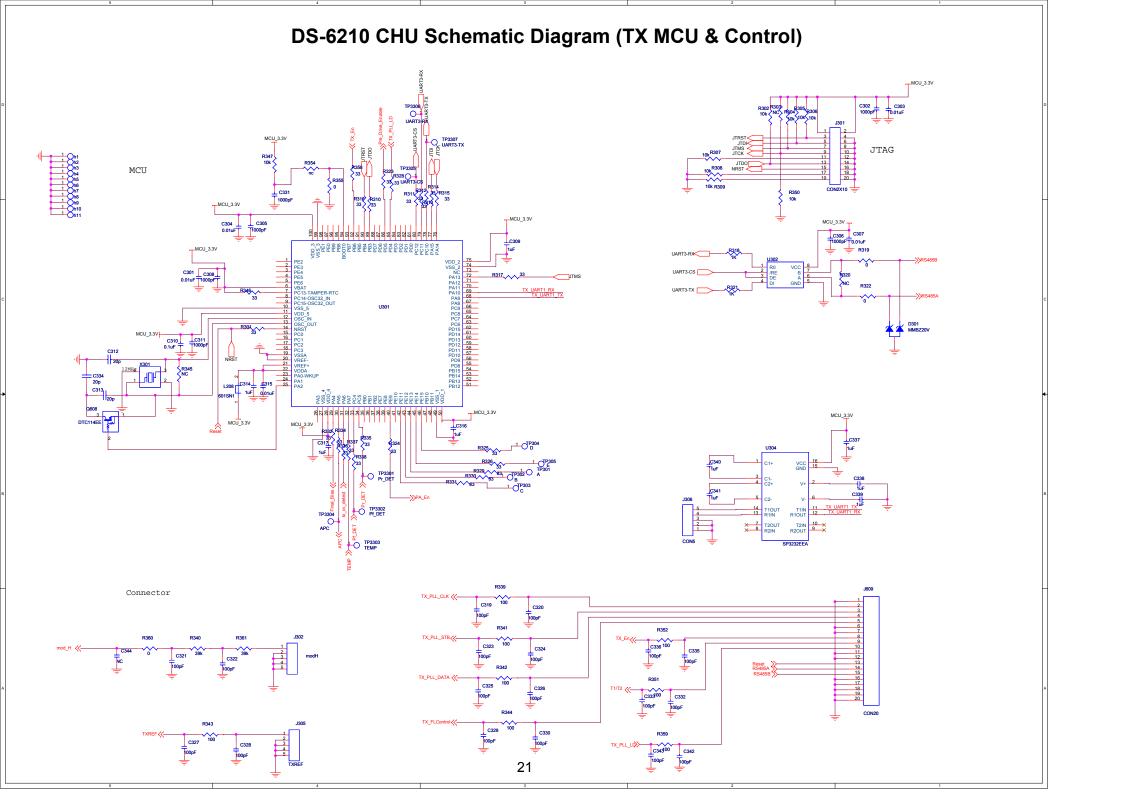


## **DS-6210 CHU Schematic Diagram (RX Power Divider)** 17

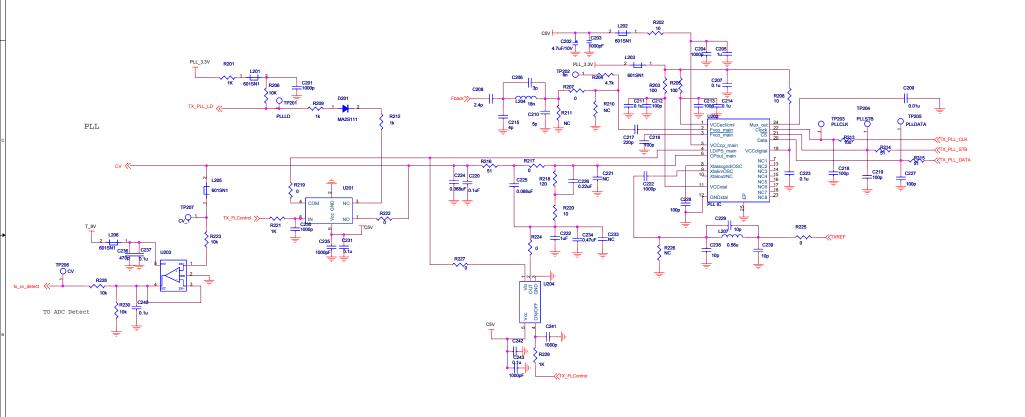
### **DS-6210 CHU Schematic Diagram (TX PA Power)** L602 Bead L606 Bead R627 4.7K L614 18

# **DS-6210 CHU Schematic Diagram (TX PA Protect)** 19

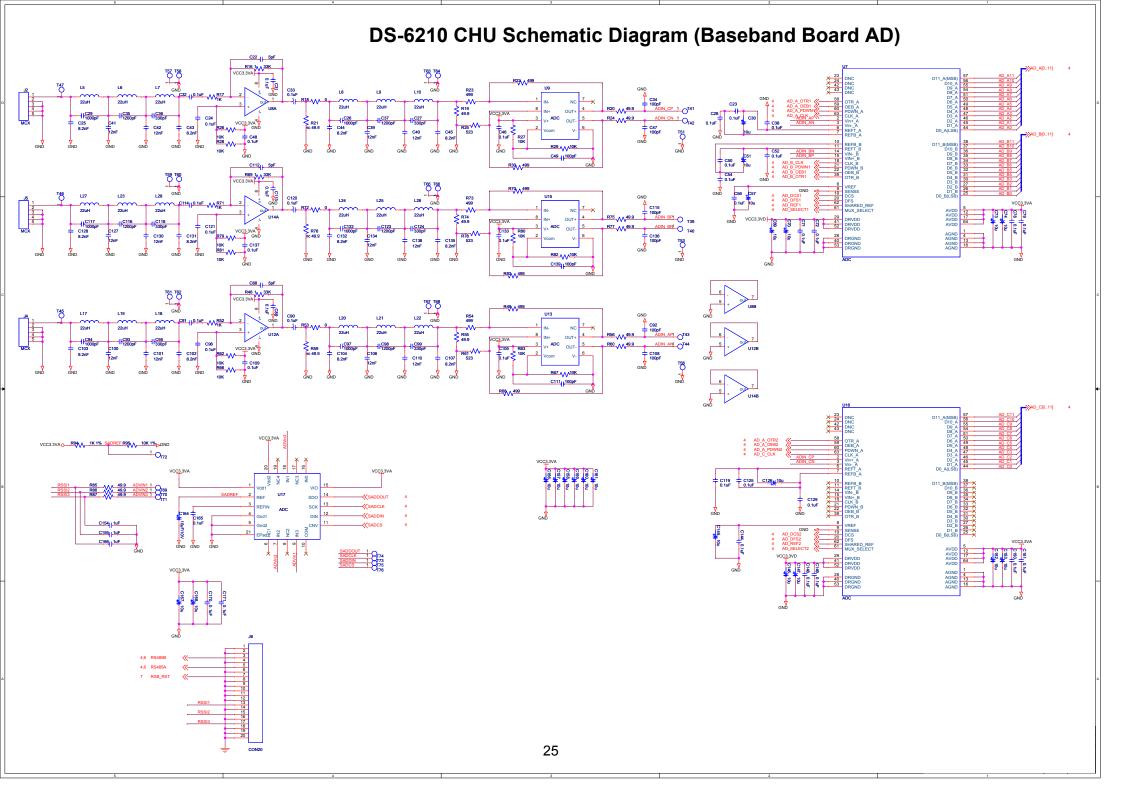




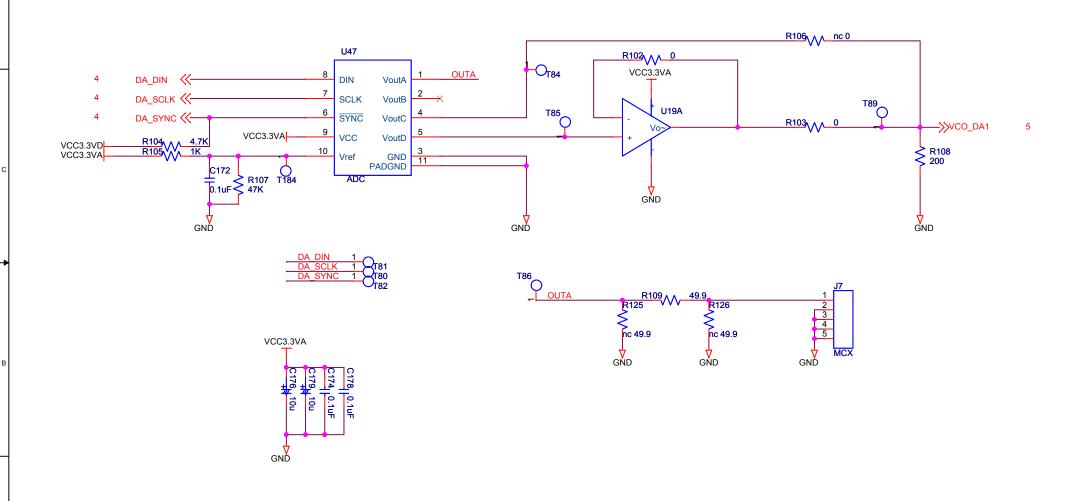
### **DS-6210 CHU Schematic Diagram (TX FGU PLL)**

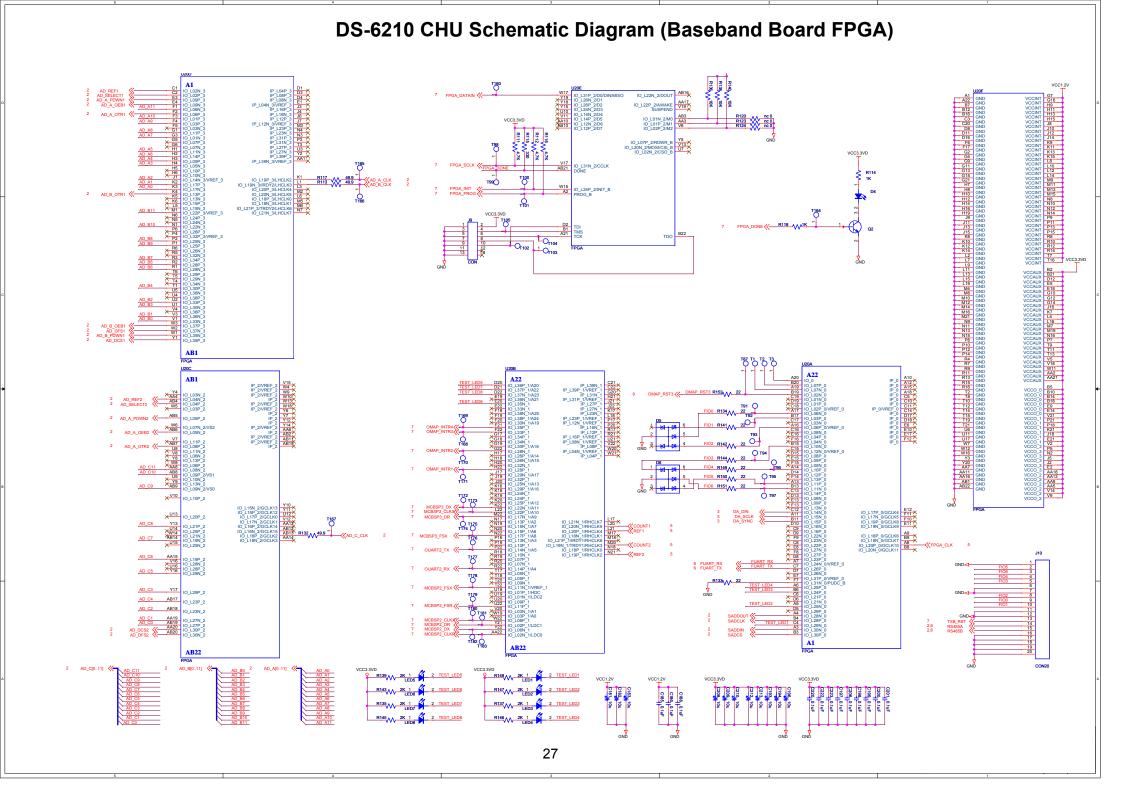


### **DS-6210 CHU Schematic Diagram (TX FGU VCO)** VCO VCO Power VCO Buffer PA Pre\_Drive 23

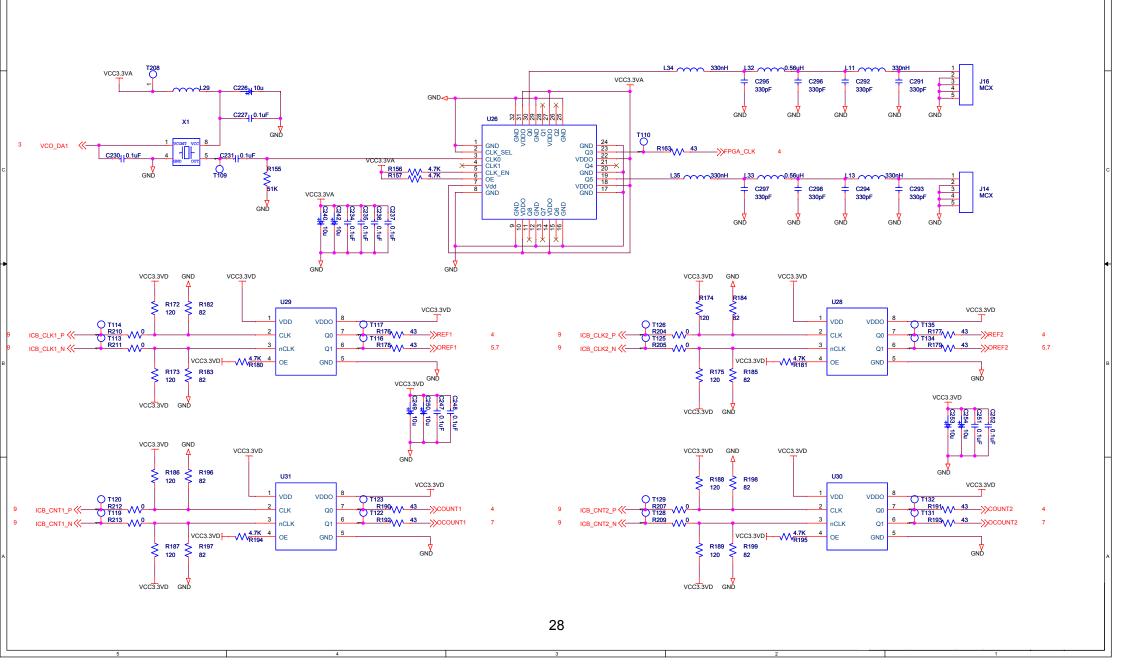


## **DS-6210 CHU Schematic Diagram (Baseband Board DA)**

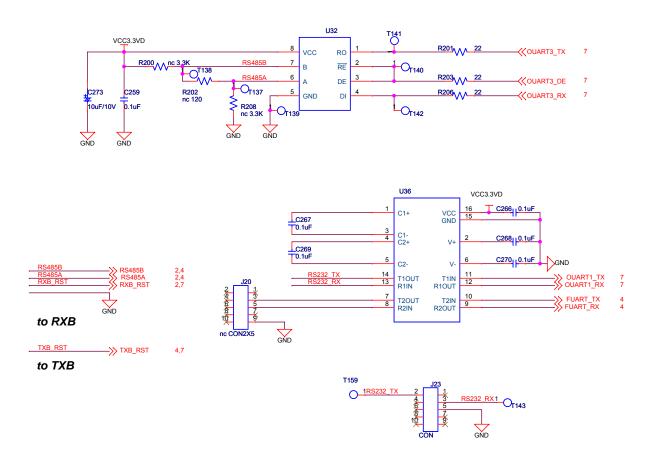




#### **DS-6210 CHU Schematic Diagram (Baseband Board Sync)**

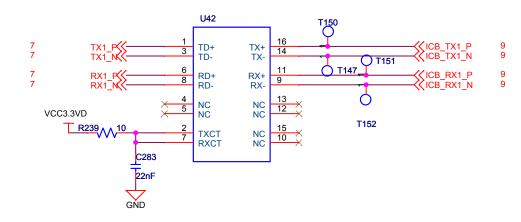


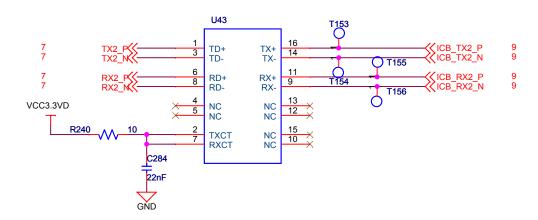
### **DS-6210 CHU Schematic Diagram (Baseband Board STM32)**



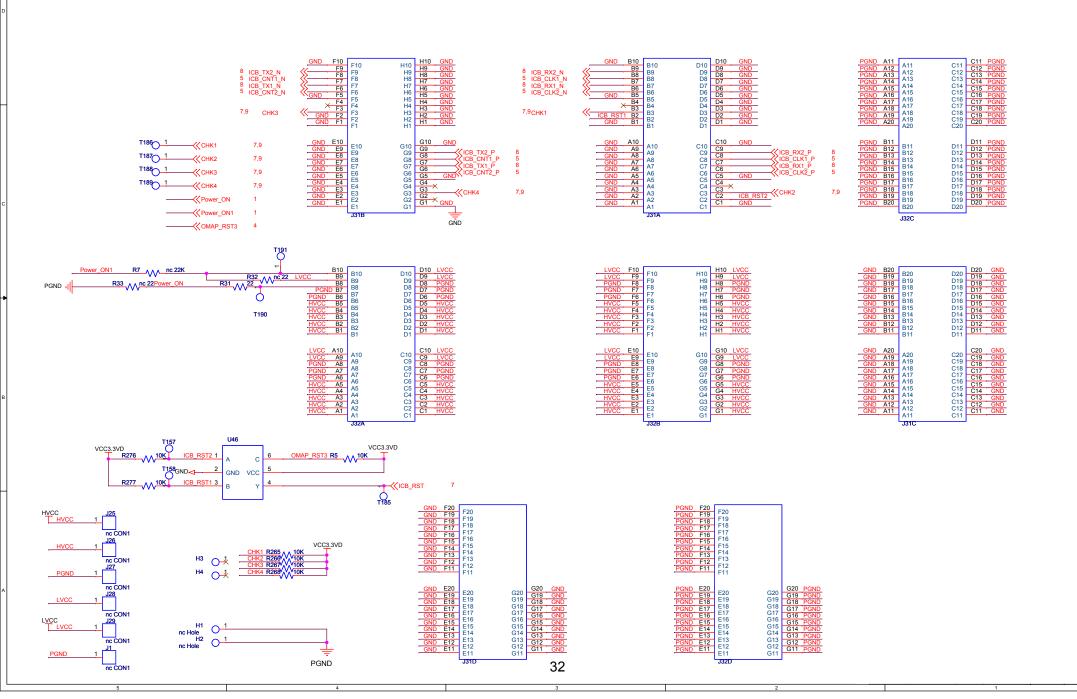
#### **DS-6210 CHU Schematic Diagram (Baseband Board OMAP GPIO)** C1 C2 C1 C2 C3 C2 C3 C2 C5 C5 C5 C6 C5 C7 C6 C7 C8 C8 C8 C7 C10 C11 C11 C11 C11 C12 C13 C14 C13 C14 C15 C15 C15 F16 OUART2\_TX F17 GND F18 MCBSP3\_FS3 F19 MCBSP3\_DR K1 K2 K3 K4 K5 K6 K7 K8 K9 K10 K11 >>> OUART2\_TX C16 C17 C18 C19 C20 C21 C22 C23 C24 C25 C26 C27 C28 C29 C30 K2 K3 K4 K5 K6 K7 K8 K9 K10 K11 K12 K13 K14 K15 FPGA\_DONE FPGA\_PROG FPGA\_INIT FPGA\_SCLK K19 K19 K20 K20 K21 K21 K22 K23 K23 K24 K24 K25 K26 K26 K26 K27 K28 K28 K29 K30 K30 MCBSP3\_DR MCBSP3\_CLKX MCBSP3\_DX F19 P20 MCBSP3 CLK. F21 F21 MCBSP3 DX F21 F22 F22 GND F22 F22 F22 GND F23 OMAP JINTR1 F23 P24 F24 OMAP JINTR2 F26 F26 OMAP JINTR3 F26 F27 GND F27 F28 F29 F30 F30 E21 E22 E23 E24 E25 E26 E27 E28 E29 E30 5,7OREF1 5,7OCOUNT1 OMAP\_INTR2 OMAP\_INTR3 OMAP\_INTR3 OMAP\_INTR4 7 OREF2 5,7OCOUNT2 MCBSP2\_DR MCBSP2\_DX MCBSP2\_CLKX MCBSP2\_FSR MCBSP2\_FSX OUART2\_RX H16 OUART1\_TX H17 OUART1\_RX H18 GND H19 H20 H21 H16 H17 H18 D1 D2 D1 D3 D4 D5 D6 D6 D7 D8 D7 D8 D9 D9 D10 D11 D10 D12 D13 D14 D13 D14 D15 D15 D15 D15 J1 J2 J3 J4 J5 J6 J7 J8 J9 J10 J11 J12 J13 J14 J16 J17 J18 J19 J20 J21 J22 J23 J24 J25 J26 J27 J28 J29 G1 G2 G3 G4 G5 G6 G7 G8 G9 G10 G11 G12 G13 G14 G15 OUART3\_RX OUART3\_TX OUART3\_DE J2 J3 J4 J5 J6 J7 J8 J9 J10 J11 J12 J13 G1 G2 G3 G4 G5 G6 G7 G8 G10 G11 G12 G13 G14 G15 D16 D17 D18 D19 D20 D21 D22 D23 D24 D25 D26 D27 D28 D29 D30 H18 H19 H20 H20 H21 H21 H21 H22 H23 X H24 H25 X H25 H26 H27 X H27 H28 X H29 H30 X H30 X G18 G19 G20 G21 G22 G23 G24 G25 G26 G27 G28 G29 G30 G21 G22 G23 G24 D21 D22 D23 D24 J22 J23 J24 J25 J26 J27 J28 J29 J30 TX1\_P TX1\_N RX1\_P RX1\_N RX2\_P RX2\_N TX2\_P TX2\_N G24 G25 G26 G27 G28 G29 G30 D25 D26 D27 D28 D29 × J14 × J15 A16 A17 A18 A19 A19 A19 A20 A21 A21 A22 A23 A24 A25 A26 A27 A28 A29 A30 Vi A1 A1 A1 A1 A14 A15 A15 GND B1 B2 B3 B4 B5 GND B6 B7 B8 B9 B10 GND B11 B12 B13 B14 B15 B16 B17 B18 B19 B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12 B13 B14 B15 CHK1 CHK2 CHK3 CHK4 B19 B20 B20 B21 B21 B22 B22 B23 B23 B24 B24 B25 B26 B26 B26 B27 B27 B28 B29 B30 B30 5,7 OREF1 5,7 OCOUNT1 7 OREF2 5,7 OCOUNT2 VCC3.8V U41 H11 1 nc Hole 1 nc Hole 1 1A1 1A2 1A3 1A4 1Y1 1Y2 1Y3 1Y4 180\\R230 H7 1 H13 1 H9 1 11 13 2A1 2A2 15 2A3 2A4 2Y1 7 2Y2 5 2Y3 3 2Y4 V( D24 1 H10 1 H14 1 3 VCC3.3VD 20 10 VCC GND OE1 OE2 R237 22 -√√<del>R238</del> GND 30

### **DS-6210 CHU Schematic Diagram (Baseband Board Ethernet)**

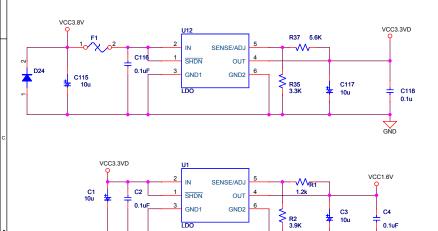


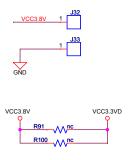


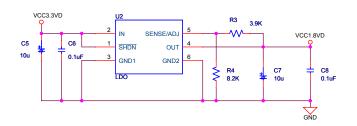
#### **DS-6210 CHU Schematic Diagram (Baseband Board ICB Interface)**

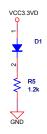


## **DS-6210 CHU Schematic Diagram (Baseband Sub-board Power)**

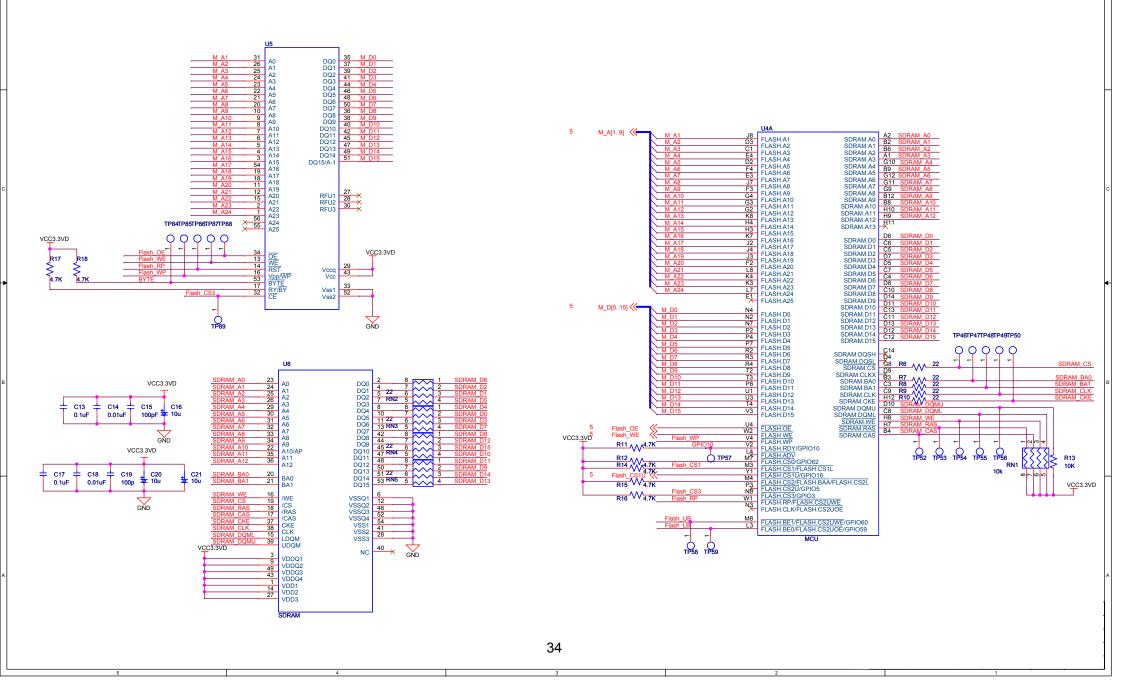




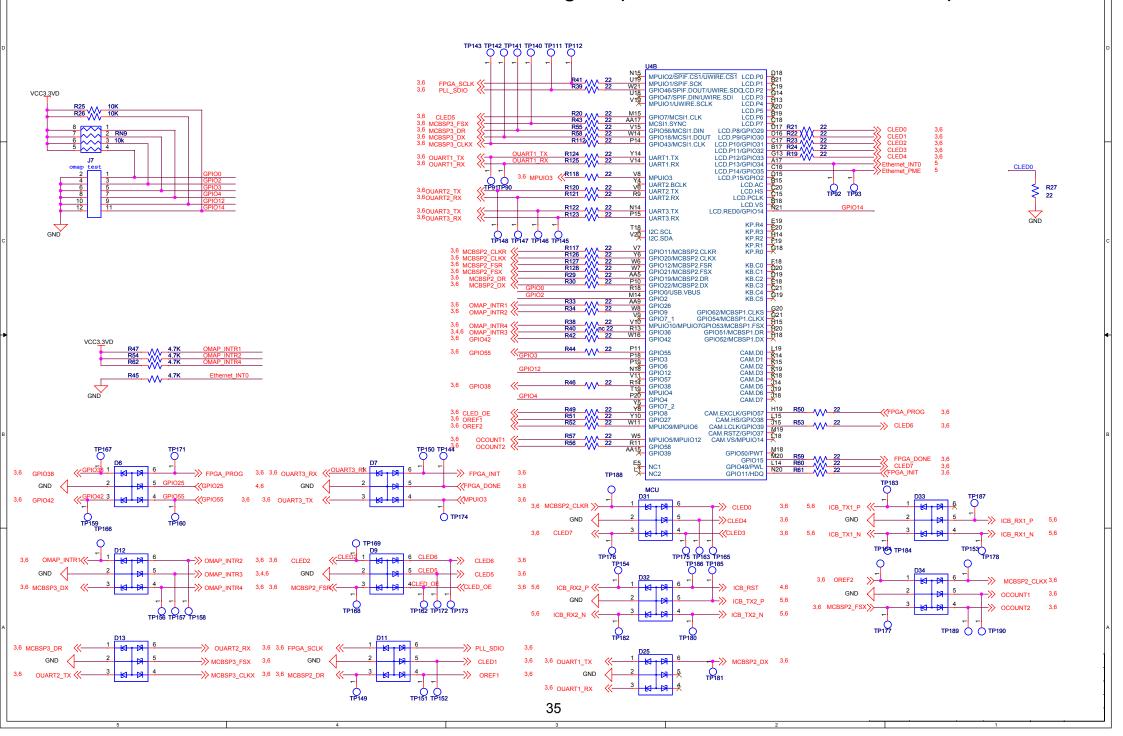


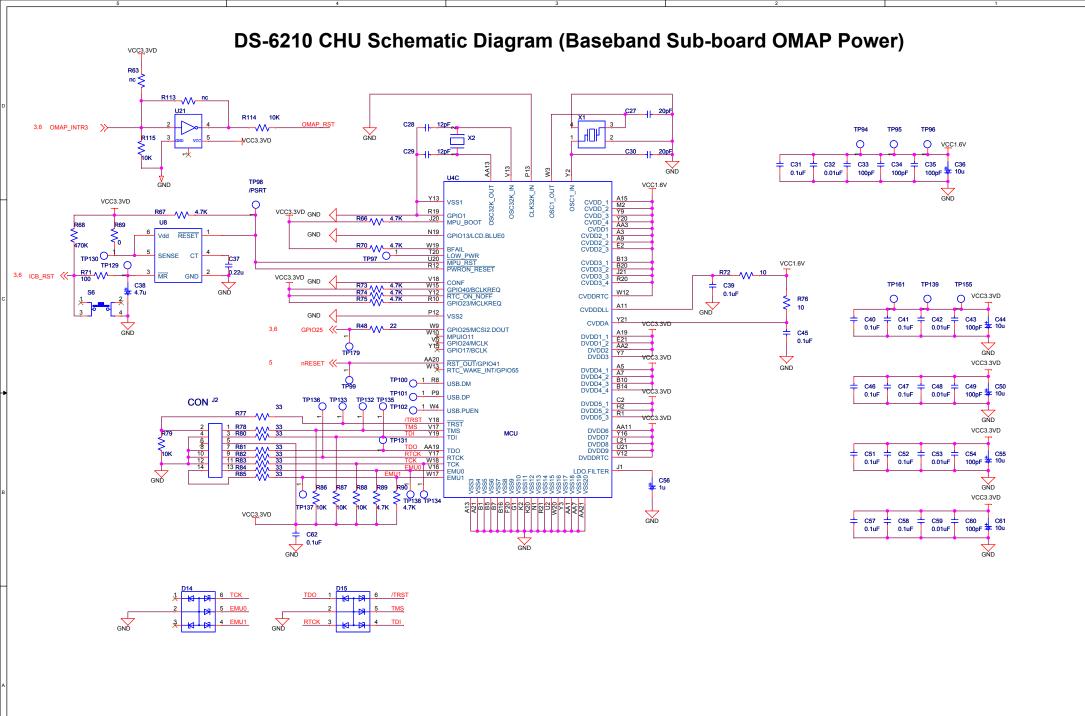


#### **DS-6210 CHU Schematic Diagram (Baseband Sub-board OMAP Mem)**

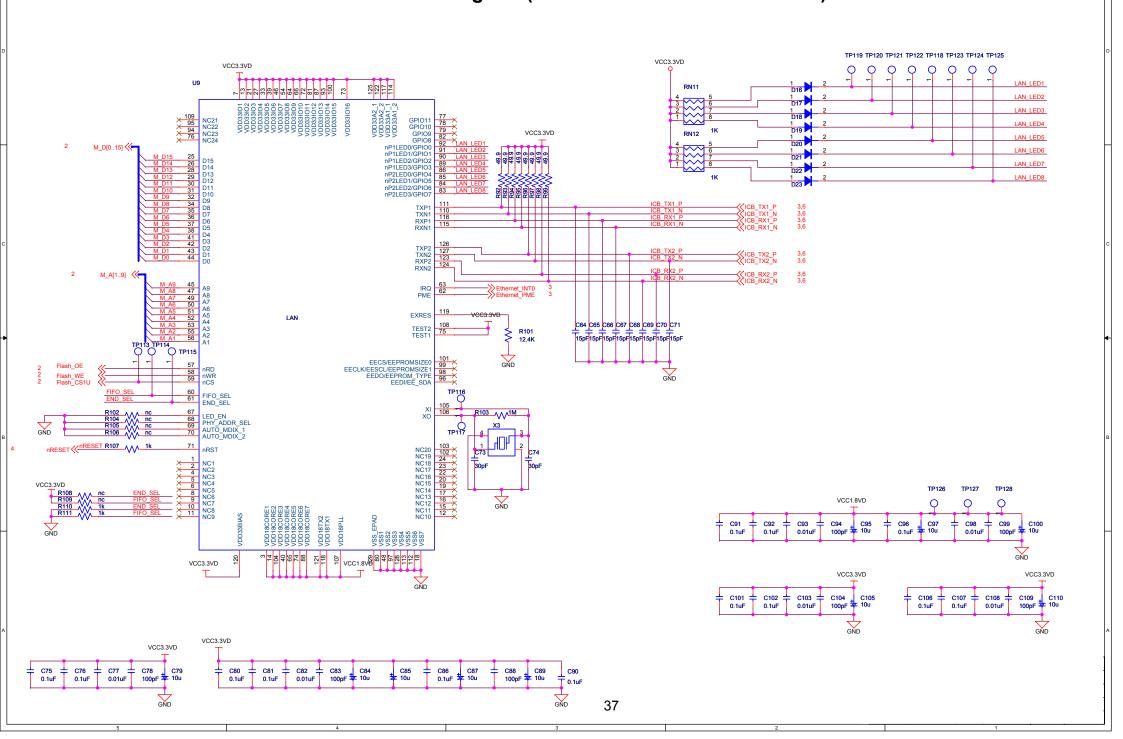


#### **DS-6210 CHU Schematic Diagram (Baseband Sub-board OMAP GPIO)**

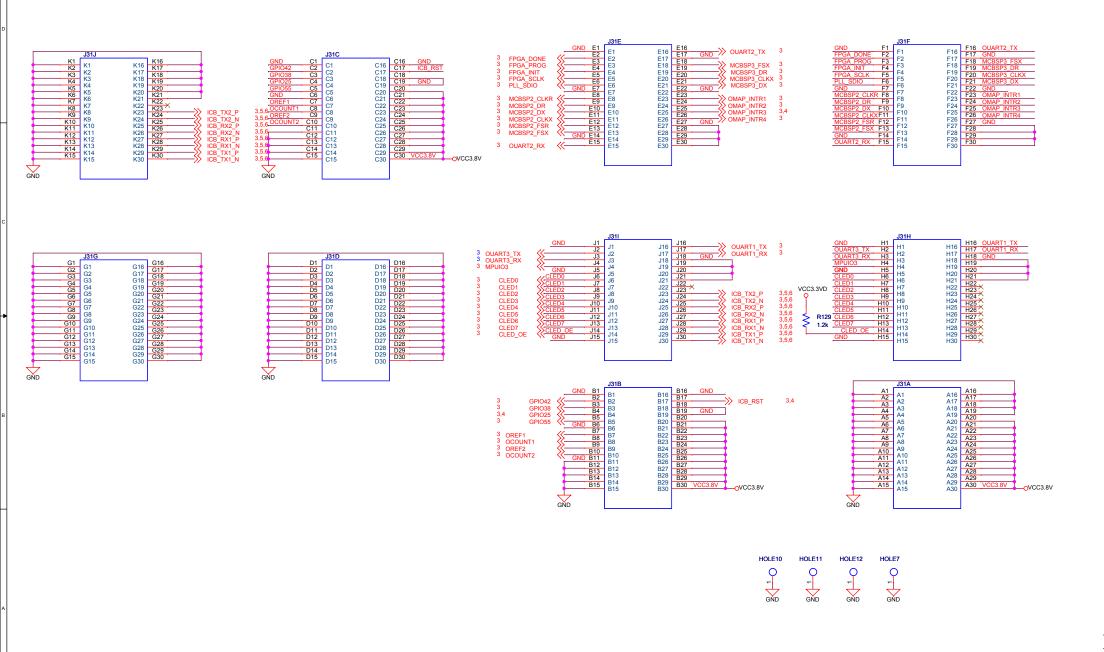




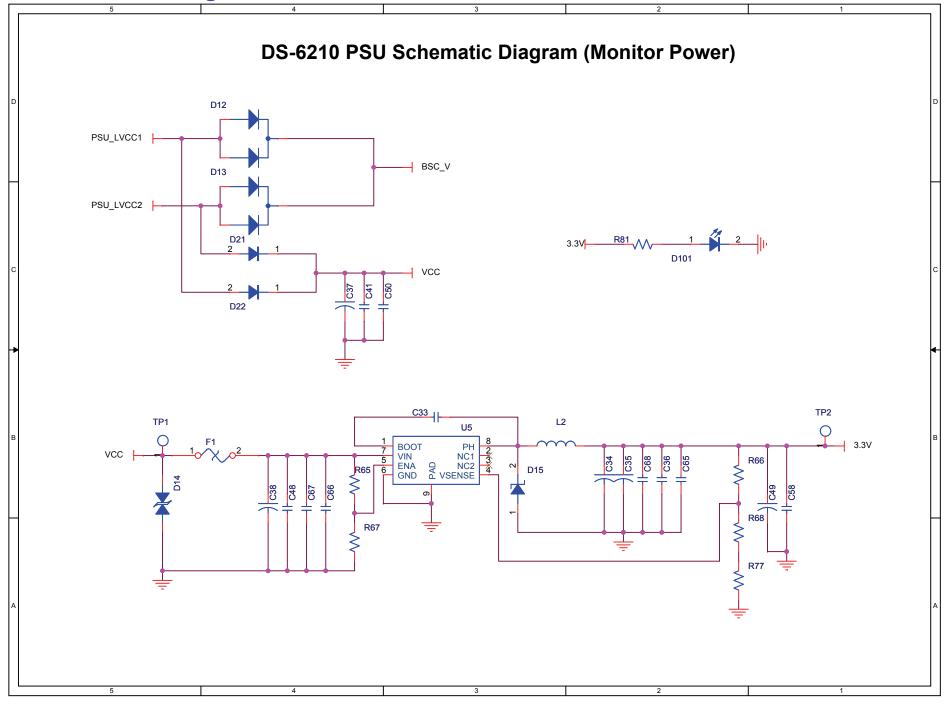
#### **DS-6210 CHU Schematic Diagram (Baseband Sub-board Ethernet)**

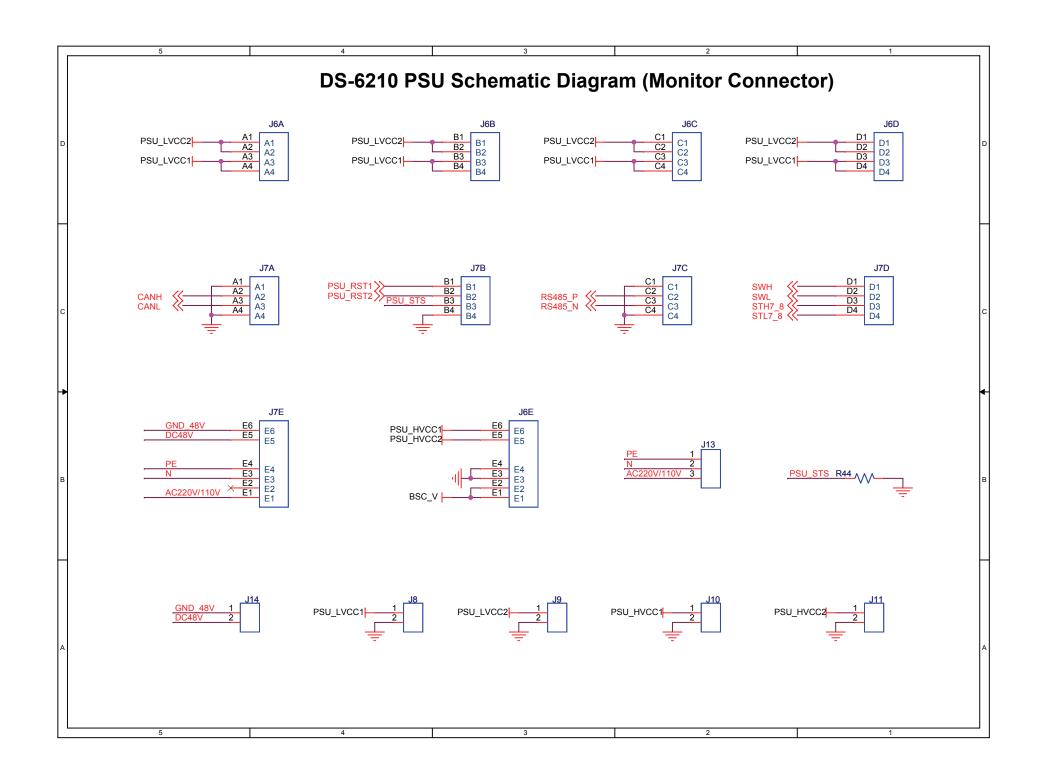


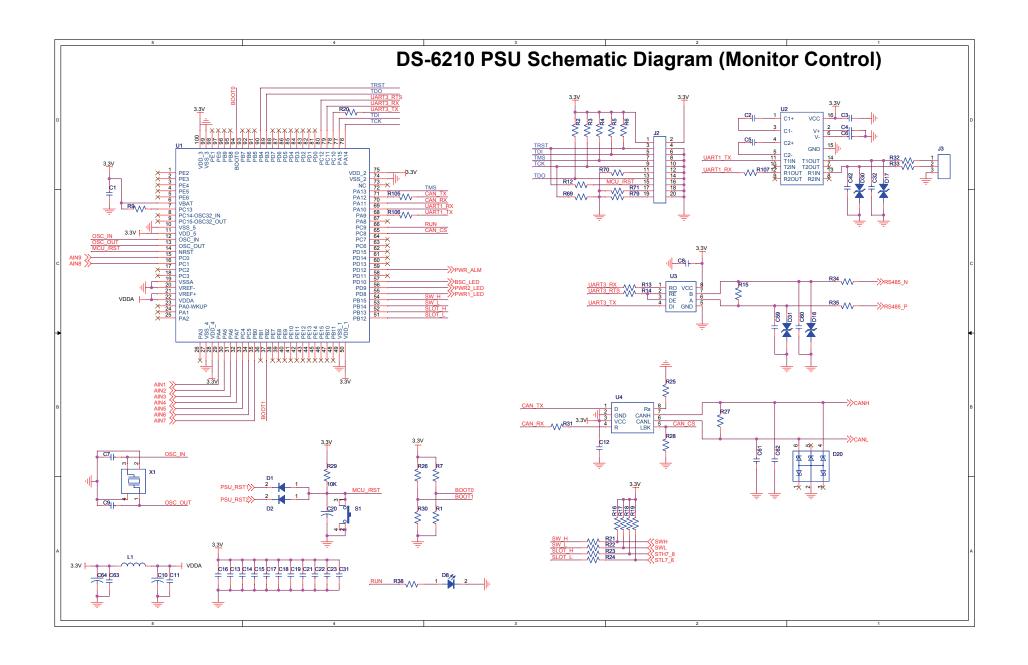
#### **DS-6210 CHU Schematic Diagram (Baseband Sub-board Ethernet)**

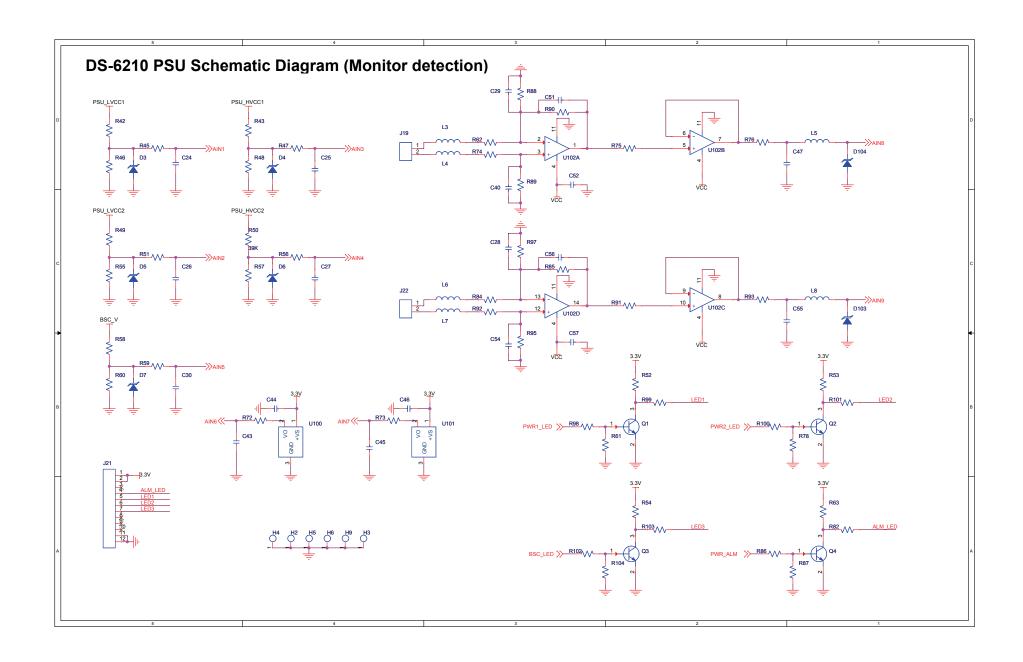


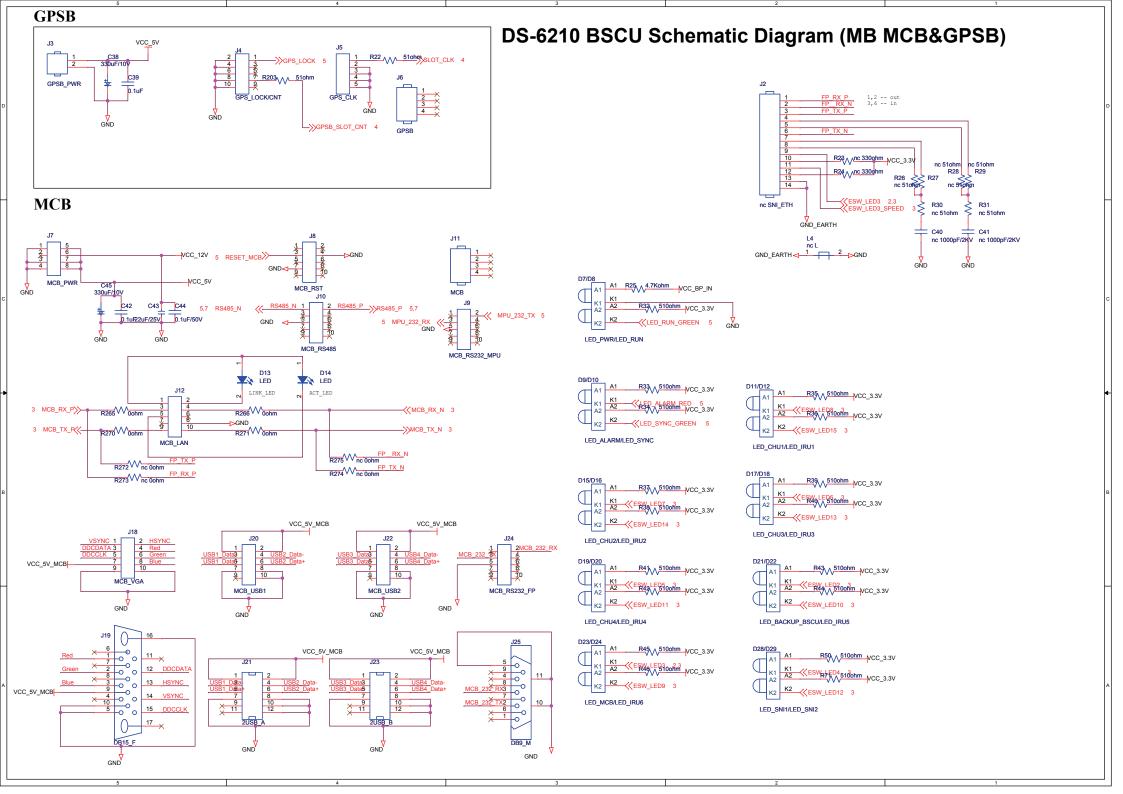
# 3. Schematic Diagram

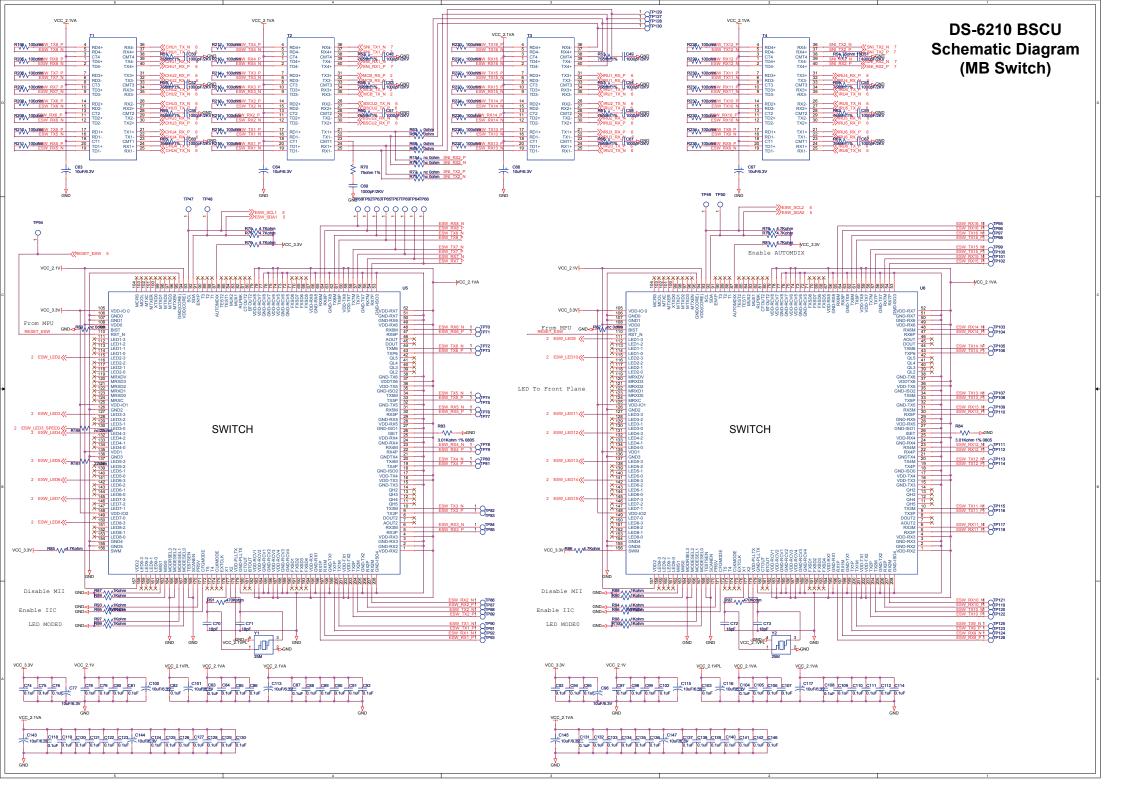


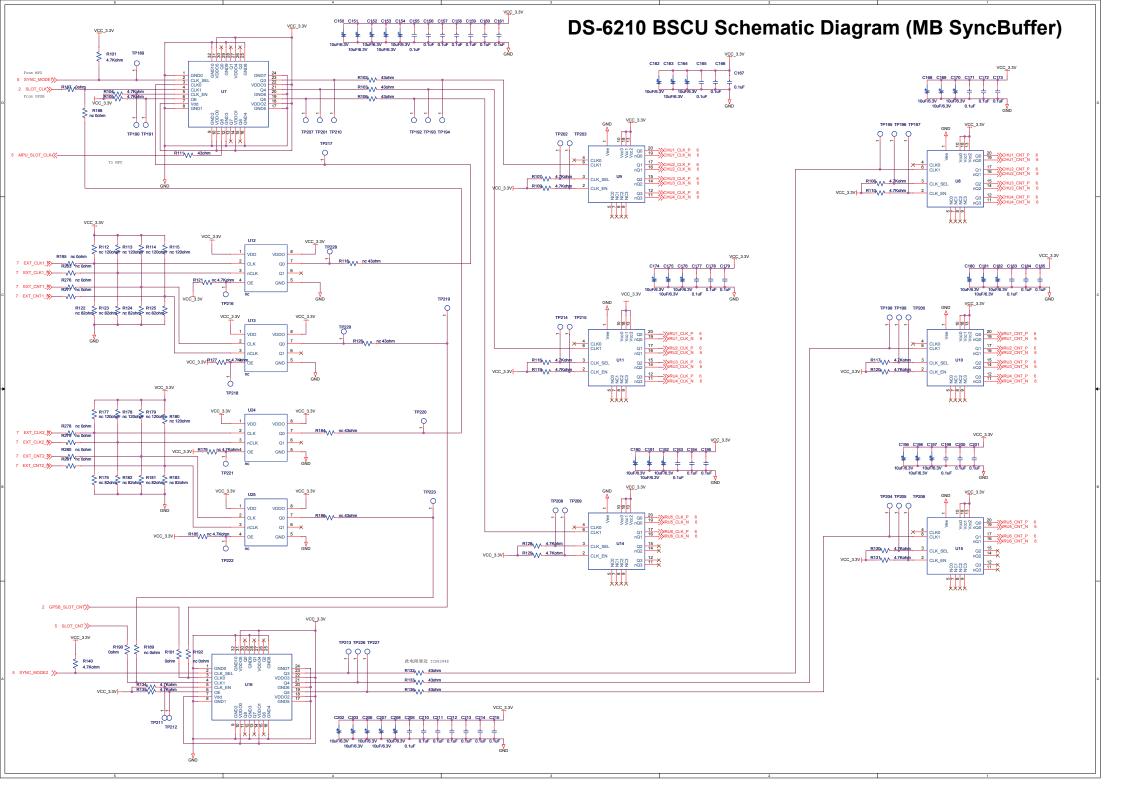


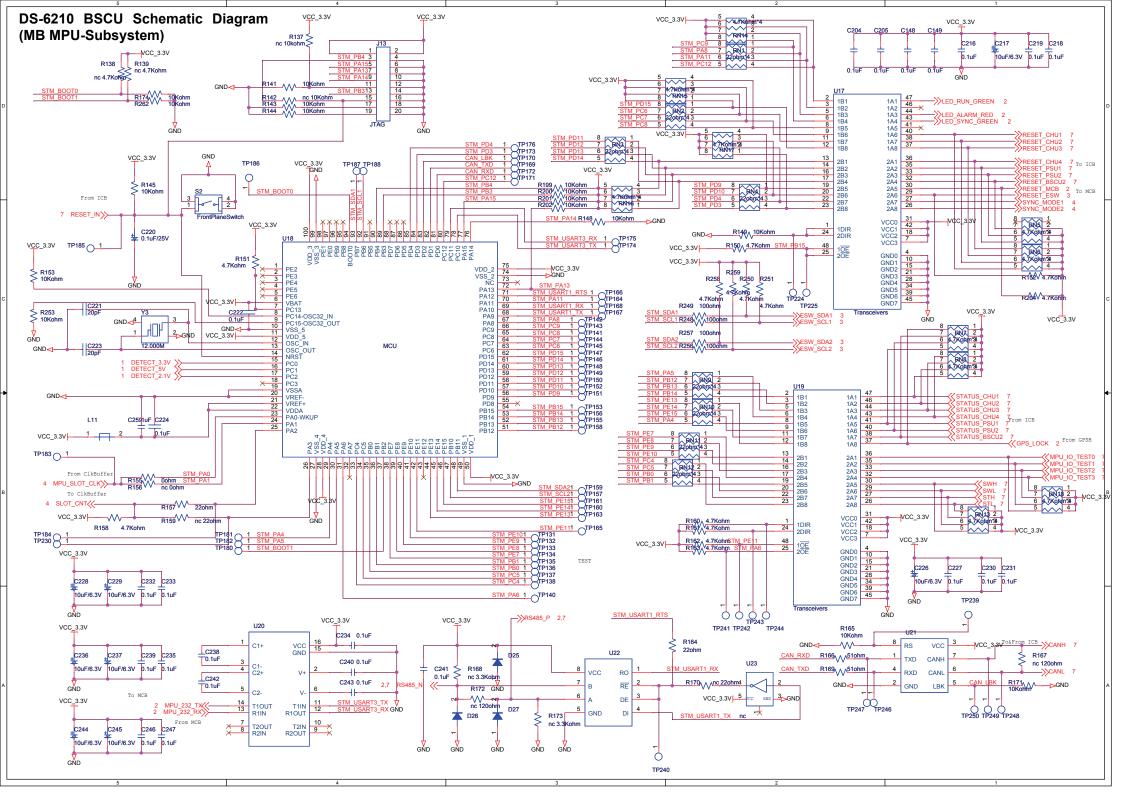


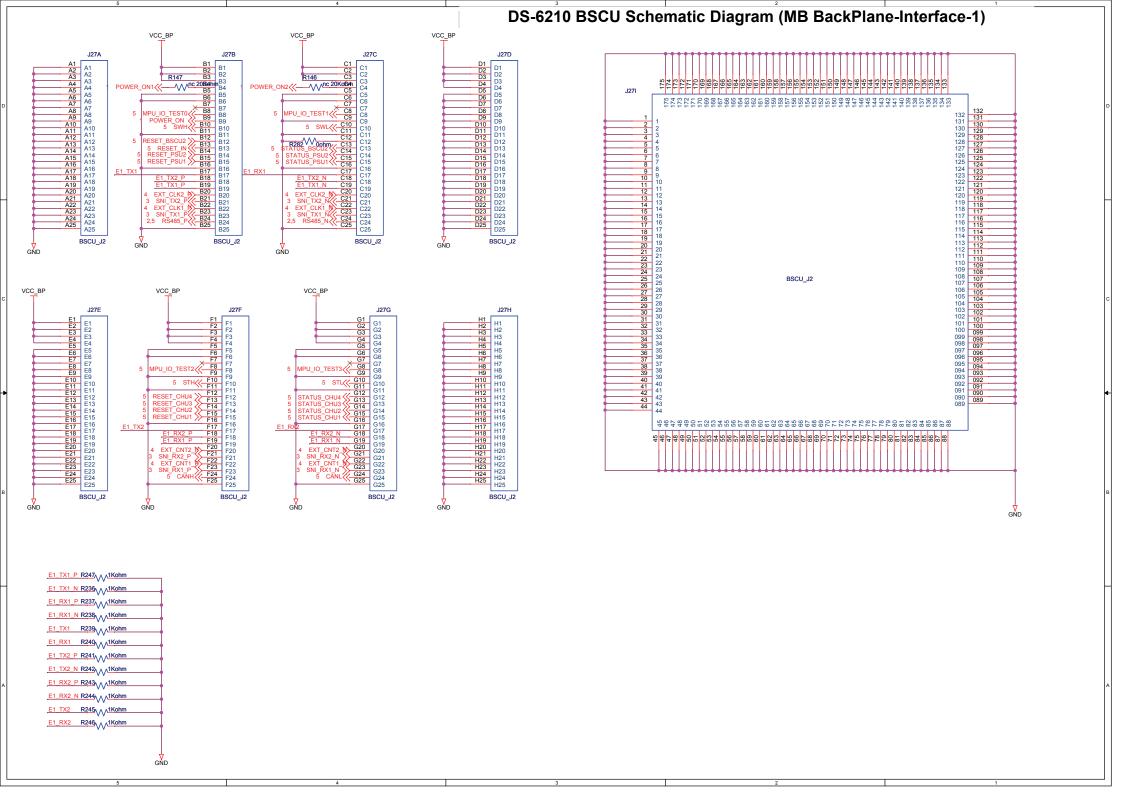












#### **DS-6210 BSCU Schematic Diagram (MB BackPlane-Interface-2)**

