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88MW300/302

WLAN Microcontroller
IEEE 802.11n/g/b
Datasheet

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88MW300/302 **Datasheet**

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88MW300/302 WLAN Microcontroller

Datasheet

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PRODUCT OVERVIEW

The Marvell® 88MW300/302 is a highly ntegrated, low-power WLAN Microcontroller System-one Chip (SoC) solution designed for a broad array of smart designed for Internet of Things (IoT), wearables, accessories, Machine-to-Machine (M2M), home automation, and Smart Energy applications

A high degree of integration enables very low system costs requiring only a single 3.3V power input, a 38.4 MHz crystal, and SPI Flash. The RF path needs only a lowpass filter for antenna connection.

The SoC includes a full-featured W LAN subsystem powered by proven and mature IEEE 802.11n/g/b Marvell technology. The WLAN subsystem integrates a WLAN MAC, baseband, and direct-conversion RF radio with integrated PA, LNA, and transmit/receive switch. It also integrates a CPU subsystem with integrated memory to run Marvell WLAN firmware to handle real time WLAN protocol processing to off-load many WLAN functions from the main application CPU.

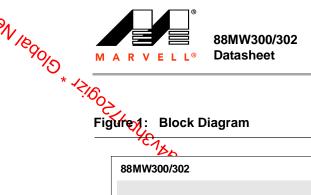
The 88MW300/302 application subsystem is powered by an ARM Cortex-M4F CPU that operates up to 200 MHz. The device supports an integrated 512 KB SRAM, 128 KB mask ROM, and a QSPI interface to external Flash. An integrated Flash Controller with a 32 KB SRAM cache enables eXecute In Place (XIP) support for firmware from Flash.

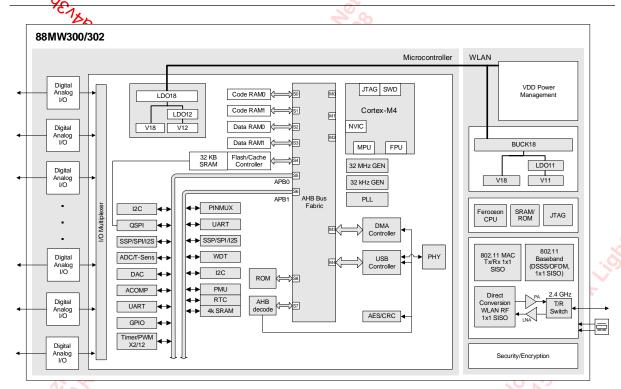
The SoC is designed for low-power operation and includes several low-power states and fast wake-up times. Multiple power domains and clocks can be individually shut down to save power. The SoC also has a high-efficiency internal PA that can be operated in low-power mode to save power. The microcontroller and WLAN subsystems can be placed into low-power states, independently, supporting a variety of application use cases. An internal DC-DC regulator provides the 1.8V rail for the WLAN subsystem.

The SoC provides a full array of peripheral interfaces including SSP/SPI/I²S (3x), UART (3x), I²C (2x), General Purpose Timers and PWM, ADC, DAC, Analog Comparator, and GPIOs. It also includes a hardware cryptographic engine, RTC, and Watchdog Timer. The 88MW302 includes a high speed USB On-The-Go (OTG) interface to enable USB audio, video, and other applications.

A complete set of digital and analog interfaces enable direct interfacing for I/O avoiding the need for external chips. The application CPU can be used to support custom application development avoiding the need for another microcontroller or processor.

Figure 1 shows an overall block diagram of the device.





Applications

- White goods/appliances—refrigerator, washer, dryer, oven range, microwave, dishwasher, water heater, air conditioner
- Consumer devices and accessories—toys, speakers, headset, alarm clock, gaming accessory, remote control
- Home automation—smart outlet, light switch, security camera, thermostat, sprinkler controller, sensor, door lock, door bell, garage door, security system
- Personal health devices—weighing scale, glucometer, blood pressure monitor, fitness equipment
- loT/wearables—coffee pot, rice cooker, vacuum cleaner, air purifier, smart watch, fitness bracelet, pet monitor
- Commercial/industrial—lighting, building automation, asset management, Point of Sale (POS) sales
- Gateways—Connecting IR, sub-Gig or Legacy RF, Bluetooth Smart, ZigBee, ZWave and other radios to Wi-Fi/IP network

Key Features

- Highly integrated SoC requiring very few external components for a full system operation
- Multiple low-power modes and fast wake-up times
- Full-featured, single stream 802.11n/g/b WLAN
- High-efficiency PA with a low-power (10 dB) mode
- Cortex-M4F application CPU for applications with integrated 512 KB SRAM and 128 KB mask ROM
- Flash Controller with embedded 32 KB SRAM cache to support XIP from external SPI Flash
- Secure boot
- Full set of digital and analog I/O interfaces

Power Management

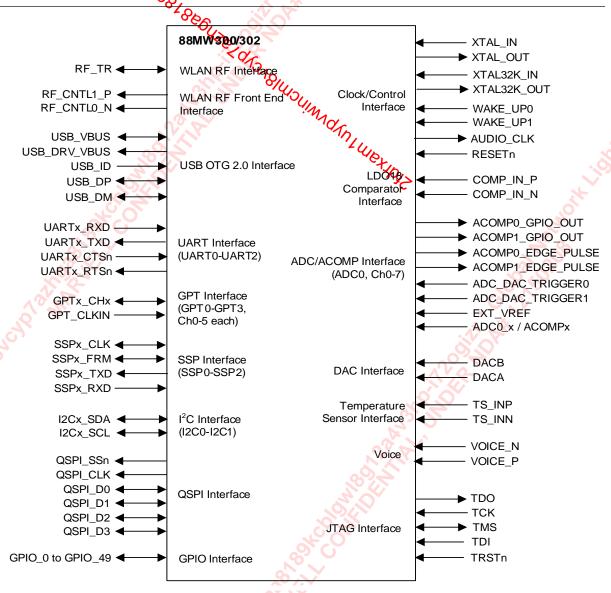
- Power modes—active, idle, standby, sleep, shutoff, power-down
- Integrated high efficiency buck DC-DC converter
- Independent power domains
- Brownout detection
- Integrated POR
- Wake-up through dedicated GPIO, IRQ, and RTC



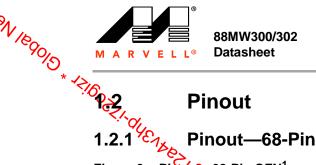
1 Package

1.1 Signal Diagram

Figure 2: Signal Diagram 12 3 4



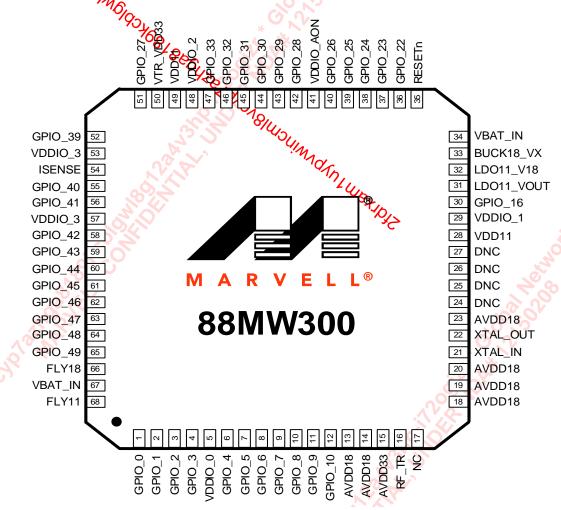
- 1. Signals are muxed on dedicated pins. See Section 1.4. Pin Description. on page 46 for dedicated pin / muxed signal descriptions.
- 2. Some pins/signals are available on the 88-pin QFN only. See Section 1.4. Pin Description, on page 46.
- 3. RF TR. USB OTG. XTAL IN/OUT, and RESETn pins are dedicated. Others are muxed on GPIOs.
- 4. See Table 16, Power and Ground, on page 66 for power signals.



Pinout

Pinout—68-Pin QFN

Figure 3: Pinous 68-Pin QFN¹

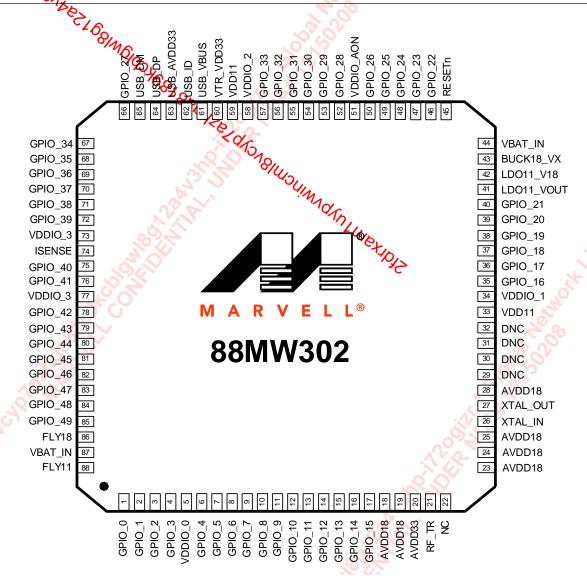


1. Connect pin 17 to ground.

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Pinout—88-Pin QFN

Figure Pinout—88-Pin QFN¹



1. Connect pin 22 to ground.

Mechanical Drawing

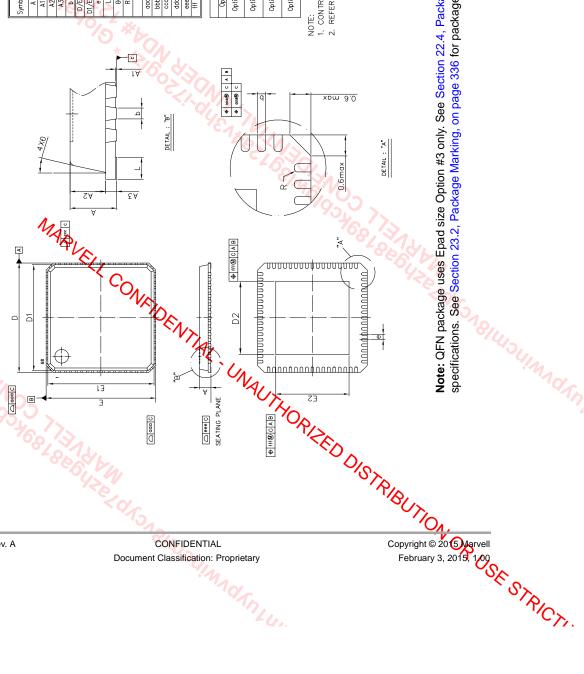
Mechanical Drawing—68-Pin QFN

Mechanical Drawing—68-Pin QFN Figure 5:

Sul lotanos & Enitalis																				
10/3/		inch	MAX	0.039	0.002		0.010				0.020	14*	-	2000	0.000	0.004	0.004	0.002	0.003	0.004
30		Dimension in i	MON	0.033	0.026	0.008 REF	0.008	0,315 BSC	0,305 BSC	0.016 BSC	0.016	1	:		:	1		:		1
6 6 _{U1}		Dime	N	0.031	0.004		900'0				0.012	.0	0.003		:	1		1		:
**46		mm	MAX	1,00	0.00		0.25				0.50	14*	:	0.45	0.10	0.10	0.10	0.05	0.08	0.10
	14	Dimension in	MOM	0.85	0.02	0.20 REF	0.20	8.00 BSC	7.75 BSC	0.40 BSC	0.40	1	1		:	1	1	1		:
		Dime	MIN	0.80	0.00		0.15				0,30	٥.	0.075			1	1	1	:	:
			symbol	¥ ;	A2	A3	q	D/E	D1/E1	е	7	Ф	~	000	3	ggg	၁၁၁	ppp	eee	≝
								7												

		EPad Size Options	
Option	Symbol	Dimension in mn	Dimension in mm Dimension in inch
Ontion #4	D ₂	91.0 ± 55.3	.211 ± 0.006
i# liondo	E ₂	5.35 ± 0.15	.211 ± 0.006
Ontion #2	D ₂	4.47 ± 0.15	.176 ± 0.006
7# IIIII	E ₂	4.47 ± 0.15	.176 ± 0.006
Option #3	D2	5,49 ± 0,15	.216 ±0.006
option #2	E2	5.49 ± 0.15	.216 ±0.006
Ontion #4	D2	3.50 ± 0.15	.138 ±0.006
t# lioudo	Ľ	350 + 015	138 +0.006

- 1. CONTROLLING DIMENSION: MILLIMETER 2. REFERENCE DOCUMENT: JEDEC MO-220.



Note: QFN package uses Epad size Option #3 only. See Section 22.4, Package Thermal Conditions, on page 315 for electrical specifications. See Section 23.2, Package Marking, on page 336 for package marking.

Mechanical Drawing—88-Pin QFN Ē

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		EPad Size Options	Options	
Option	Symbol	Symbol Dimension in mm	in mm	Dim
001:00	D ₂	6.64 ±	0.15	.261 ± 0.006
upindo	E ₂	6,64 ±	0.15	.261 ± 0.006
Ontion #2	D2	€.00 ±	0.15	.236 ± 0.006
z# iiondo	E2	€,00 ±		.236 ± 0.006
2/1 00:100	D ₂	4,30 ±		.169 ± 0.006
CH IIOIIdo	E,	4.30 ±	0.15	.169 ± 0.006

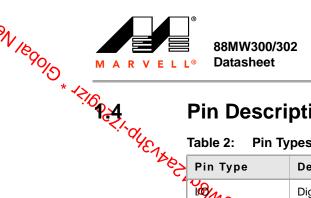
NOTE:

1. CONTROLLING DIMENSION: MILLIMETER

2. REFERENCE DOCUMENT : JEDEC MO-220.

The property of the property o

Note: QFN package uses Epad size Option #3 only. See Section 22.4, Package Thermal Conditions, on page 315 for electrical specifications. See Section 23.2, Package Marking, on page 336 for package marking.



Pin Description

Table 2: Pin Types

Pin Type	Description
1	Digital input/output
1 1904	Digital input *
0 000	Digital output
A, I	Apalog input
A, O	Analog Output
NC	No connect 8/4/2
DNC	Do not connect
PWR	No connect S/Us/Union Power
Ground	Ground

Table 3: WLAN RF Interface

88-Pin	68-Pin	Pin Name	Type	Supply	Description
21	16	RF_TR	A, I/O	AVDD18	WLAN RF Interface (2.4 GHz Transmit/Receive) Baseband input/output data

Table 4: WLAN RF Front End Interface

					A. C.
88-Pin	68-Pin	Pin Name	Type	Supply	Description
GPIO_44		RF_CNTL1_P	A, O	VDDIO_3	WLAN Radio Control 1 Power-down output high signal
GPIO_45		RF_CNTL0_N	A, O	VDDIO_3	WLAN Radio Control 0 Power-down output low signal

* 100 Table 5: NOTE: 05

Table 5: USB 2.0 OTG Interface1

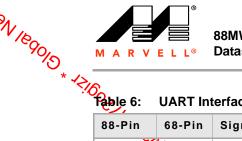
NOTE: (%) ailable on 88-pin package only (88MW302)

88-Pin	68-Pin	Pin Name	Type	Supply	Description
61	C169/	USB_VBUS	A, I/O	USB_AVDD33	USB VBUS Selection Input In Device Mode Unused in host mode; I/O for OTG mode to supply +5V@10mA during session negotiation.
GPIO_27		USB_DRV_MBUS	A, O	VDDIO_3	Drive 5V on VBUS 0 = do not drive VBUS 1 = drive 5V on VBUS The USB_DRV_VBUS port is connected to the SoC pad to drive an external power management chip to provide power for USB VBUS.
62		USB_ID	A, I	USB_AVDD33	USB 2.0 OTG IDPIN
63		USB_AVDD33	A, I	- "74	USB 3.3V Analog Power Supply See Table 16, Power and Ground, on page 66.
64		USB_DP	A, I/O	USB_AVDD33	USB 2.0 Bus Data+
65	- 04	USB_DM	A, I/O	USB_AVDD33	USB 2.0 Bus Data-

^{1.} After POR, if USB is in host mode, USB_DPUSB_DM will be SE0. If USB is in device mode, USB_DP/USB_DM will be High-z.

Table 6: UART Interface¹

88-Pin	68-Pin	Signal Name	Type	Supply	Description
GPIO_0		UART0_CTSn	I	VDDIO_0	UART 0 CTSn (active low)
GPIO_1		UART0_RTSn	0	VDDIO_0	UART 0 RTSn (active low)
GPIO_2		UART0_TXD	0	VDDIO_0	UART 0 TXD
GPIO_3		UART0_RXD	I	VDDIO_0	UART 0 RXD
					00,5%
GPIO_23		UART0_CTSn	I	VDDIO_AON	UART 0 CTSn (active low)
GPIO_24		UART0_RXD	I	VDDIO_AON	UART 0 RXD
				6020	y
GPIO_30		UART0_CTSn	I	VDDIO_2	UART 0 CTSn (active low)
GPIO_31		UART0_RTSn	0	VDDIO_2	UART 0 RTSn (active low)
GPIO_32		UART0_TXD	0	VDDIO_2	UART 0 TXD
GPIO_33		UART0_RXD	1018	VDDIO_2	UART 0 RXD
			6 4		



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UART Interface¹

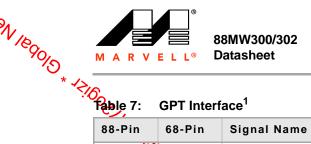
٠ (ري					
88-Pin	68-Pin	Signal Name	Type	Supply	Description
GPIO_37	AS.	UART0_RTSn	0	VDDIO_3	UART 0 RTSn (active low)
GPIO_27	100/s	UARTO_TXD	0	VDDIO_3	UART 0 TXD
	•				
GPIO_11		UART POTSn	1	VDDIO_0	UART 1 CTSn (active low)
GPIO_12		UART1_RTSn	00	VDDIO_0	UART 1 RTSn (active low)
GPIO_13		UART1_TXD	1 3/8/	VDDIO_0	UART 1 TXD
GPIO_14		UART1_RXD	D. 20	VDDIO_0	UART 1 RXD
GPIO_35		UART1_CTSn	I	VDDIO_STA	UART 1 CTSn (active low)
GPIO_36		UART1_RTSn	0	Z 1	WART 1 RTSn (active low)
GPIO_38		UART1_TXD	0	VDDIO_3	UART TXD
GPIO_39	رک	UART1_RXD	I	VDDIO_3	UART 1 RXD
GPIO_42	897	UART1_CTSn	I	VDDIO_3	UART 1 CTSn (active low)
GPIO_43	204	UART1_RTSn	0	VDDIO_3	UART 1 RTSn (active low)
GPIO_44	200	UART1_TXD	0	VDDIO_3	UART 1 TXD
GPIO_45		UART1_RXD	I	VDDIO_3	UART 1 RXD
GPIO_7		UART2_CTSn	I	VDDIO_0	UART 2 CTSn (active low)
GPIO_8		UART2_RTSn	0	VDDIO_0	UART 2 RTSn (active low)
GPIO_9		UART2_TXD	0	VDDIO_0	UART 2 TXD
GPIO_10		UART2_RXD	I	VDDIO_0	UART 2 RXD
GPIO_46		UART2_CTSn	I	VDDIO_3	UART 2 CTSn (active low)
GPIO_47		UART2_RTSn	0	VDDIO_3	UART 2 RTSn (active low)
GPIO_48		UART2_TXD	0	VDDIO_3	UART 2 TXD
GPIO_49		UART2_RXD	I	VDDIO_3	UART 2 RXD

^{1.} All UART signals are muxed on GPIO pins. See Table 11, GPIO Interface, on page 53 for GPIO muxing.

* 42/16 Table 7:

Table 7: GPT Interface1

Table 7:	GP1 Intert	ac e			
88-Pin	68-Pin	Signal Name	Type	Supply	Description
GPIO_0	262	GPT0_CH0	I/O	VDDIO_0	General Purpose Timer 0, Channel 0
GPIO_1	PEZLES/M	GPT0_CH1	I/O	VDDIO_0	General Purpose Timer 0, Channel 1
GPIO_2	Ĩ	O O O O O O O O O O O O O O O O O O O	1/0	VDDIO_0	General Purpose Timer 0, Channel 2
GPIO_3		GPT0_CH3	1/0	VDDIO_0	General Purpose Timer 0, Channel 3
GPIO_4		GPT0_CH4	1/0	VDDIO_0	General Purpose Timer 0, Channel 4
GPIO_5		GPT0_CH5	9/9	VDDIO_0	General Purpose Timer 0, Channel 5
GPIO_35		GPT0_CLKIN	1/0 1/0 1/8/14	VDDIO_3	General Purpose Timer 0, Clock Input
GPIO_28		GPT1_CH0	I/O	VDDIO_1	General Purpose Timer 1, Channel 0
GPIO_29		GPT1_CH1	I/O	VDDIO_2	General Purpose Timer 1, Channel 1
GPIO_30		GPT1_CH2	I/O	VDDIO_2	General Purpose Timer 1, Channel 2
GPIO_31	400	GPT1_CH3	I/O	VDDIO_2	General Purpose Timer 1, Channel 3
GPIO_32	850	GPT1_CH4	I/O	VDDIO_2	General Purpose Timer 1, Channel 4
GPIO_33	04	GPT1_CH5	I/O	VDDIO_2	General Purpose Timer 1, Channel 5
GPIO_24	2	GPT1_CH5	I/O	VDDIO_AON	General Purpose Timer 1, Channel 5
GPIO_36		GPT1_CLKIN	I	VDDIO_3	General Purpose Timer 1, Clock Input
GPIO_11		GPT2_CH0	I/O	VDDIO_0	General Purpose Timer 2, Channel 0
GPIO_12		GPT2_CH1	I/O	VDDIO_0	General Purpose Timer 2, Channel 1
GPIO_13		GPT2_CH2	I/O	VDDIO_0	General Purpose Timer 2, Channel 2
GPIO_14		GPT2_CH3	I/O	VDDIO_0	General Purpose Timer 2, Channel 3
GPIO_15		GPT2_CH4	I/O	VDDIO_0	General Purpose Timer 2, Channel 4
GPIO_37		GPT2_CH5	I/O	VDDIO_3	General Purpose Timer 2, Channel 5
GPIO_38		GPT2_CLKIN	I	VDDIO_3	General Purpose Timer 2, Clock Input
GPIO_17		GPT3_CH0	I/O	VDDIO_1	General Purpose Timer 3, Channel 0
GPIO_18		GPT3_CH1	1/0	VDDIO_1	General Purpose Timer 3, Channel 1
GPIO_19		GPT3_CH2	I/O	VDDIO_1	General Purpose Timer 3, Channel 2
GPIO_20		GPT3_CH3	1/0	VDDIO_1	General Purpose Timer 3, Channel 3



GPT Interface¹

88-Pin	68-Pin	Signal Name	Type	Supply	Description
GPIO_21	867.	GPT3_CH4	I/O	VDDIO_1	General Purpose Timer 3, Channel 4
GPIO_34	- 26	GPT3_CH5	I/O	VDDIO_3	General Purpose Timer 3, Channel 5
GPIO_39	*1,	GPT3_CLKIN	1 (VDDIO_3	General Purpose Timer 2, Clock Input

All GPT signals are muxed on Propins. See Table 11, GPIO Interface, on page 53 for GPIO muxing.

 See Table 11, GPIO Interface, on page 53 for GPIO muxing.

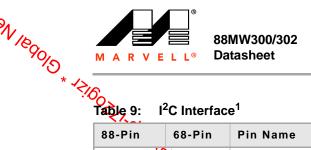
 See Table 11, GPIO Interface, on page 53 for GPIO muxing.

Table 8:

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88-Pin	68-Pin	Pin Name	Type	Supply	Description
GPIO_0		SSP0_CLK	1/0	O_OIQO	SSP 0 Serial Clock
GPIO_1		SSP0_FRM	I/O	VDDIO10	SSP 0 Frame Indicator
GPIO_2		SSP0_TXD	0	VDDIO_0 1/4	SSP 0 TXD
GPIO_3		SSP0_RXD	ı	VDDIO_0	SSEO RXD
GPIO_30	340	SSP0_CLK	I/O	VDDIO_2	SSP 0 Serial Clock
GPIO_31	8	SSP0_FRM	I/O	VDDIO_2	SSP 0 Frame Indicator
GPIO_32	2070	SSP0_TXD	0	VDDIO_2	SSP 0 TXD
GPIO_33	P	SSP0_RXD	I	VDDIO_2	SSP 0 RXD
GPIO_11		SSP1_CLK	I/O	VDDIO_0	SSP 1 Serial Clock
GPIO_12		SSP1_FRM	I/O	VDDIO_0	SSP 1 Frame Indicator
GPIO_13		SSP1_TXD	0	VDDIO_0	SSP 1 TXD
GPIO_14		SSP1_RXD	I	VDDIO_0	SSP 1 RXD
GPIO_18		SSP1_CLK	I/O	VDDIO_1	SSP 1 Serial Clock
GPIO_19		SSP1_FRM	I/O	VDDIO_1	SSP 1 Frame Indicator
GPIO_20		SSP1_TXD	0	VDDIO_1	SSP 1 TXD
GPIO_21		SSP1_RXD	I	VDDIO_1	SSP 1 RXD
GPIO_35		SSP1_CLK	1/0	VDDIO_3	SSP 1 Serial Clock
GPIO_36		SSP1_FRM	I/O	VDDIO_3	SSP 1 Frame Indicator
	-				

Fable 8:					Package Pin Description
Table 8:	SSP Inter	face ¹ (Continued))		*
88-Pin		Pin Name	Туре	Supply	Description
GPIO_38	1862	SSP1_TXD	0	VDDIO_3	SSP 1 TXD
GPIO_39	1865 108/1	SSP1_RXD	I	VDDIO_3	SSP 1 RXD
		"			
GPIO_42		SSP1_GPK	1/0	VDDIO_3	SSP 1 Serial Clock
GPIO_43		SSP1_FRM COL	1/0	VDDIO_3	SSP 1 Frame Indicator
GPIO_44		SSP1_TXD	<0/2	VDDIO_3	SSP 1 TXD
GPIO_45		SSP1_RXD	D 10/0	VDDIO_3	SSP 1 RXD
				0,	
GPIO_7		SSP2_CLK	I/O	VDDIO_6/7	SSP 2 Serial Clock
GPIO_8		SSP2_FRM	I/O	VDDIO_0	SSP 2 Frame Indicator
GPIO_9		SSP2_TXD	0	VDDIO_0	SSPZIXD
GPIO_10	100	SSP2_RXD	I	VDDIO_0	SSP 2 RXD
GPIO_46	2011	SSP2_CLK	I/O	VDDIO_3	SSP 2 Serial Clock
GPIO_47	07	SSP2_FRM	I/O	VDDIO_3	SSP 2 Frame Indicator
GPIO_48		SSP2_TXD	0	VDDIO_3	SSP 2 TXD
GPIO_49		SSP2_RXD	I	VDDIO_3	SSP 2 RXD

^{1.} All SSP signals are muxed on GPIO pins. See Table 11, GPIO Interface, on page 53 for GPIO muxing.



I²C Interface¹

88-Pin	68-Pin	Pin Name	Type	Supply	Description
GPIO_4 GPIO_7	265/60/	I2C0_SDA I2C1_SDA I2C1_SCL	I/O	VDDIO_0	I ² C 0 SDA
GPIO_5 GPIO_8	-inc	J2C0_SCL	1/0	VDDIO_0	I ² C 0 SCL
GPIO_6 GPIO_9		12C1_3DA	I/O	VDDIO_0	I ² C 1 SDA
GPIO_10		12C1_SCL	1/0	VDDIO_0	I ² C 1 SCL
			ar sa		'
GPIO_20		I2C0_SDA	1/0	CVDDIO_1	I ² C 0 SDA
GPIO_21		I2C0_SCL	I/O	VDDØ 1	I ² C 0 SCL
GPIO_18		I2C1_SDA	I/O	VDDIO_74/6	I ² C 1 SDA
GPIO_17 GPIO_19	- 10	I2C1_SCL	I/O	VDDIO_1	VOPC 1 SCL
GPIO_25	200	I2C1_SDA	I/O	VDDIO_AON	I ² C 1 SDA
GPIO_26	041	I2C1_SCL	I/O	VDDIO_AON	I ² C 1 SCL
GPIO_28		I2C0_SDA	I/O	VDDIO_2	I ² C 1 SDA *
GPIO_29		I2C0_SCL	I/O	VDDIO_2	I ² C 1 SCL

^{1.} All I²C signals are muxed on GPIO pins. See Table 11, GPIO Interface, on page 53 for GPIO muxing.

Table 10: QSPI Interface¹

					<u> </u>
88-Pin	68-Pin	Pin Name	Type	Supply	Description
GPIO_28		QSPI_SSn	0	VDDIO_2	QSPI Chip Select (active low)
GPIO_29		QSPI_CLK	0	VDDIO_2	QSPI Clock
GPIO_30		QSPI_D0	I/O	VDDIO_2	QSPI Data 0
GPIO_31		QSPI_D1	I/O	VDDIO_2	QSPI Data 1
GPIO_32		QSPI_D2	I/O	VDDIO_2	QSPI Data 2
GPIO_33		QSPI_D3	I/O	VDDIO_2	QSPI Data 3

^{1.} QSPI signals are used for external Flash only. All QSPI signals are muxed on GPIO pins. See Table 11, GPIO Interface, on page 53 for GPIO muxing.

						Packaç Pin Description
* <	Fable 11:	GPIO Int	terface ^{1 2}		.0	
	88-Pin	68-Pin	Pin/Signal Name	Туре	Supply	Description
	1	TAREZ LOGO	GPIO_0	I/O	VDDIO_0	General Purpose I/O 0
		200	GPT0_CH0	I/O	100 to	General Purpose Timer 0, Channel 0
			UARTO_CTSn	1		UART 0 CTSn (active low)
			SSP0_0	I/O	×	SSP 0 Serial Clock
	2	2	GPIO_1	2/1/0	VDDIO_0	General Purpose I/O 1
			GPT0_CH1	100/1		General Purpose Timer 0, Channel 1
			UART0_RTSn	0	U/M	UART 0 RTSn (active low)
			SSP0_FRM	I/O	Pulmaro,	SSP 0 Frame Indicator
	3	3	GPIO_2	I/O	VDDIO_0	General Purpose I/O 2
			GPT0_CH2	I/O		General Purpose Timer 0, Channel 2
		837	UART0_TXD	0		UART 0 TXD
		847	SSP0_TXD	0		SSP 0 TXD
	- A D	1 7	ania a	110	\/DDIQ 0	a 12 10 (A 0)
	4	4	GPIO_3	I/O	VDDIO_0	General Purpose I/O 3
			GPT0_CH3	I/O		General Purpose Timer 0, Channel 3
			UART0_RXD	I		UART 0 RXD
48 winere			SSP0_RXD	I		SSP 0 RXD
.012	6	6	GPIO_4	I/O	VDDIO_0	General Purpose I/O 4
24,			GPT0_CH4	I/O		General Purpose Timer 0, Channel 4
			I2C0_SDA	I/O	80	1 ² C 0 SDA
			AUDIO_CLK	0	Tropy of	Audio Clock AUPLL Audio clock output provided by Aud PLL for external codec.
	7	7	GPIO_5	I/O	VDDIO_0	General Purpose I/O 5
			GPT0_CH5	1/0		General Purpose Timer 0, Channel 5
			I2C0_SCL	1/0		I ² C 0 SCL



Table 11:	GPIO Int	terface ¹ (Continued) ²	2	3	<u> </u>
M A R V	68-Pin	Pin/Signal Name	Туре	Supply	Description
8	8 260	GPIO_6	I/O	VDDIO_0	General Purpose I/O 6
		TEQ2	0		JTAG Test Data
		12C1_\$B\$/	I/O	ķ.	I ² C 1 SDA
9	9	GPIO_7	1/0	VDDIO_0	General Purpose I/O 7
		TCK	1/0,	_	JTAG Test Clock
		UART2_CTSn	1	2410	UART 2 CTSn (active low)
		SSP2_CLK	I/O	My	SSP 2 Serial Clock
		I2C0_SDA	I/O	"124	∕⊳ J ² C 0 SDA
				Palmozuzuzuzuzuzuzuzuzuzuzuzuzuzuzuzuzuzuzu	Y.+.
10	10	GPIO_8	I/O	VDDIO_0	General Purpose I/O 8
	801	TMS	I/O	-	JTAG Controller Select
	200	UART2_RTSn	0	-	UART 2 RTSn (active low)
35	077	SSP2_FRM	I/O	-	SSP_2 Frame Indicator
10/		I2C0_SCL	I/O	-	1 ² C 0 SCL
	h		'		
11	11	GPIO_9	I/O	VDDIO_0	General Purpose I/O 9
		TDI	1		JTAG Test Data
		UART2_TXD	0		UART 2 TXD
		SSP2_TXD	0		SSP 2 TXD
		I2C1_SDA	I/O		I ² C 1 SDA
12	12	GPIO_10	I/O	VDDIO_0	General Purpose I/O 10
		TRSTn	1	400	JTAG Test Reset (active low)
		UART2_RXD	1	8. C	UART 2 RXD
		SSP2_TXD	0		SSP 2 RXD
		I2C1_SCL	1/0		I ² C 1 SCL

* [*] / _O Fabl e 11 88-Pin					Packaç Pin Description
* /6 Fable 11	: GPIO Int	terface ¹ (Continued)	2	.01	
88-Pin	68-Pin	Pin/Signal Name	Туре	Supply	Description
13	NASA.	GPIO_11	I/O	VDDIO_0	General Purpose I/O 11
	TER LON	GPT2_CH0	I/O	2000 N	General Purpose Timer 2, Channel 0
	·	UART1_CTSn	1 0		UART 1 CTSn (active low)
		SSP1_00	I/O	×	SSP 1 Serial Clock
		`&I	//	I	
14		GPIO_12	2/1/0	VDDIO_0	General Purpose I/O 12
		GPT2_CH1	100/4		General Purpose Timer 2, Channel 1
		UART1_RTSn	0	UM	UART 1 RTSn (active low)
		SSP1_FRM	I/O	Pulman,	SSP 1 Frame Indicator
15		GPIO_13	I/O	VDDIO_0	Gereral Purpose I/O 13
		General Purpose Timer 2, Channel 2			
	801	UART1_TXD	0		UART 1 TXD
	200	SSP1_TXD	0		SSP 1 TXD
		'			
16 🔨	Y	GPIO_14	I/O	VDDIO_0	General Purpose I/O 14
138		GPT2_CH3	I/O		General Purpose Timer 2, Channel 3
8		UART1_RXD	ı		UART 1 RXD
		SSP1_RXD	1		SSP 1 RXD
		<u>I</u>			
17		GPIO_15	I/O	VDDIO_0	General Purpose I/O 15
		GPT2_CH4	I/O		General Purpose Timer 2, Channel 4
				<u> </u>	
35	30	GPIO_16	I/O	VDDIO_1	General Purpose I/O 16
		CON[5]	I/O	9409	Configuration Bit See Table 17, Configuration Pins, on page 67.
		AUDIO_CLK	0.00		Audio Clock AUPLL Audio clock output provided by Audi PLL for external codec.



M A R V	/ E L L®	Datasheet			.8
M A R V	GPIO In	nterface ¹ (Continued)	2	.6	
88-Pin	68-Pin	Pin/Signal Name	Type	Supply	Description
36	1265 160	GPIO_17	I/O	VDDIO_1	General Purpose I/O 17
	200		I/O	0000V	General Purpose Timer 3, Channe
		1200 SCL	1/0	N. Committee	I ² C 1 SCL
37		GPIO_18	I/O	VDDIO_1	General Purpose I/O 18
		GPT3_CH1	2/1/0		General Purpose Timer 3, Channe
		I2C1_SDA	1/00/1		I ² C 1 SDA
		SSP1_CLK	1/0	Um.	SSP 1 Serial Clock
38		GPIO_19	I/O	VDDIO_124	General Purpose I/O 19
		GPT3_CH2	I/O		General Purpose Timer 3, Channe
		I2C1_SCL	I/O		I ² C 1 SDA
	83,	SSP1_FRM	I/O		SSP 1 Frame Indicator
39	52-2	GPIO_20	I/O	VDDIO_1	General Purpose I/O 20
70,		GPT3_CH3	I/O		General Purpose Timer 3, Chann
1018		I2C0_SDA	I/O		I ² C 0 SDA
		SSP1_TXD	0		SSP 1 TXD
40		GPIO_21	I/O	VDDIO_1	General Purpose I/O 21
		GPT3_CH4	I/O		General Purpose Timer 3, Channe
		I2C0_SCL	I/O		I ² C 0 SCL
		SSP1_RXD	I	180	SSP 1 RXD
			1,15		
46	36	GPIO_22	I/O	VDDIO_	General Purpose I/O 22

^		4			
Fabl e 11: 88-Pin	GPIO In	terface ¹ (Continued) ² Pin/Signal Name	Туре	Supply	Description
47	Tigge 2/08	GPIO_23	I/O	VDDIO_	General Purpose I/O 23
		UART0_CTSn	1	AON	UART 0 CTSn (active low)
		WARKE UP1	1 0		Wake-Up 1
		COMP GOD	A STOP	×	LDO18 Comparator Input, Positive Positive input to LDO18 comparato
48	38	GPIO_24	Tyo	VDDIO	General Purpose I/O 24
		UARTO_RXD	18/4	AON	UART 0 RXD
		GPT1_CH5	I/O	UM,	General Purpose Timer 1, Channel
		COMP_IN_N	I	VDDIO_ AON VIMOSTALLU	LDO18 Comparator Input, Negative
	'			'	1-17.
49	39	GPIO_25	I/O	VDDIO_	General Purpose I/O 25
	897	XTAL32K_IN	1	AON	32.768 kHz Crystal Input
	200	I2C1_SDA	I/O	-	I ² C 1 SDA
50	40	GPIO_26	I/O	VDDIO_ AON	General Purpose I/O 26
.38		XTAL32K_OUT	0		32.768 kHz Crystal Output
		I2C1_SCL	I/O	-	I ² C 1 SCL
66	51	GPIO_27	I/O	VDDIO_3	General Purpose I/O 27
		USB_DRV_VBUS	0	_	Drive 5V on VBUS
	51	UART0_TXD	0	- 0	UART 0 TXD
	51	CON[4]	I/O	01/0	Configuration Bit See Table 17, Configuration Pins, o page 67.
52	42	GPIO_28	I/O	VDDIO_2	General Purpose I/O 28
		QSPI_SSn	0.0		QSPI Chip Select (active low)
		I2C0_SDA	1/0		I ² C 0 SDA
		GPT1_CH0	1/0	-	General Purpose Timer 1, Channel



M A R V	E L L®	88MW300/302 Datasheet			dillo
Table 11:	GPIO In	terface ¹ (Continued) ²		Š	
88-Pin	68-Pin	Pin/Signal Name	Туре	Supply	Description
53	43 400	, GPIO_29	I/O	VDDIO_2	General Purpose I/O 29
	70 07	OKOL CLK	0	0 2	QSPI Clock
		12C0 S&P	I/O	X X	I ² C 0 SCL
		12C0_SC2_	1/0	,	General Purpose Timer 1, Channel
		92.0			
54	44	GPIO_30	1/00//	VDDIO_2	General Purpose I/O 30 QSPI Data 0 UART 0 CTSn (active low) SSP 0 Serial Clock General Purpose Timer 1, Channel
		QSPI_D0	1/0	4/10	QSPI Data 0
		UART0_CTSn	1	"MAY	UART 0 CTSn (active low)
		SSP0_CLK	I/O	14	SSP 0 Serial Clock
		GPT1_CH2	I/O		General Purpose Timer 1, Channel
55	45	GPIO_31	I/O	VDDIO_2	General Purpose I/O 31
	20/11	QSPI_D1	I/O	-	QSPI Data 1
X	07	UART0_RTSn	0		UART 0 RTSn (active low)
10	NA.	SSP0_FRM	I/O		SSP 0 Frame Indicator
		GPT1_CH3	I/O		General Purpose Timer 1, Channel
56	46	GPIO_32	I/O	VDDIO_2	General Purpose I/O 32
		QSPI_D2	I/O		QSPI Data 2
		UART0_TXD	0		UART 0 TXD
		SSP0_TXD	0		SSP 0 TXD
		GPT1_CH4	I/O	180	General Purpose Timer 1, Channel
57	47	GPIO_33	I/O	VDDIO_2	General Purpose I/O 33
		QSPI_D3	1/0	8,0	QSPI Data 3
		UART0_RXD	1 8		UART 0 RXD
		SSP0_RXD			SSP 0 RXD
		GPT1_CH5	1/0		General Purpose Timer 1, Channel

* [*]					Pa Pin Desc
* <>/o	: GPIO In	terface ¹ (Continued)	2	Š	
88-Pin	68-Pin	Pin/Signal Name	Туре	Supply	Description
67	- 20'5	GPIO_34	I/O	VDDIO_3	General Purpose I/O 34
		GP03_CH5	1/0		General Purpose Timer 3, Channel 5
		VA.		I	I
68		GPIO_35	1/0	VDDIO_3	General Purpose I/O 35
		GPT0_CLKIN	Q'1	VDDIO_3	General Purpose Timer 0, Clock Input
		UART1_CTSn	118/11		UART 1 CTSn (active low)
		SSP1_CLK	1/0	UM.	SSP 1 Serial Clock
69		GPIO_36	I/O	VDDIO_3	General Purpose I/O 36
		GPT1_CLKIN	I		General Purpose Timer 1, Clock Input
	4	UART1_RTSn	0		UART 1 RTSn (active low)
	80,	SSP1_FRM	I/O		SSP 1 Frame Indicator
				I	
70		GPIO_37	I/O	VDDIO_3	General Purpose I/O 37
.010		GPT2_CH5	I/O		General Purpose Timer 2, Channel 5
(3)		UART0_RTSn	0		UART 0 RTSn (active low)
2					Λ V Q~
71		GPIO_38	I/O	VDDIO_3	General Purpose I/O 38
		GPT2_CLKIN	I -		General Purpose Timer 2, Clock Input
		UART1_TXD	0		UART 1 TXD
		SSP1_TXD	0		SSP 1 TXD
72	52	GPIO_39	I/O	VDDIO_3	General Purpose I/O 39
		GPT3_CLKIN	l	199	General Purpose Timer 2, Clock Input
		UART1_RXD	1	3,0	UART 1 RXD
		SSP1_RXD	1 26		SSP 1 RXD



<u> </u>	GPIO In	terface ¹ (Continued) ²			
A R V	68-Pin	Pin/Signal Name	Type	Supply	Description
75	\$65 J	GPIO_40	I/O	VDDIO_3	General Purpose I/O 40
	TAREZ LOGI	ADC_DAC_TRIGGER0	ı	00,50	ADC/DAC External Trigger 0
		ACOMPO_GPIO_OUT	0 *	ķ.	ACOMP0 GPIO Output ACOMP0 output synchronous or asynchronous level signals.
		ACOMP1_GPIO_OUP	0		ACOMP1 GPIO Output ACOMP1 output synchronous or asynchronous level signals.
					<u>'</u>
76	56	GPIO_41	I/O	VDD16-3	General Purpose I/O 41
		ADC_DAC_TRIGGER1	I	VDDIO 3	ADC/DAC External Trigger 1
	عرف	ACOMP0_EDGE_ PULSE	0		ACOMP Edge Pulse 0 Output pulse aligned with synchronize comparison result.
	2011	ACOMP1_EDGE_ PULSE	0		ACOMP Edge Pulse 1 Output pulse aligned with synchronize comparison result.
78	58	GPIO_42	I/O	VDDIO_3	General Purpose I/O 42
		ADC0_0 / ACOMP0 / TS_INP / VOICE_P	Α, Ι		ADC0 Channel 0 ACOMP0 Channel 0 ACOMP1 Channel 0 Temperature sensor remote sensing poinput Voice sensing positive input
		UART1_CTSn	I	1	UART 1 CTSn (active low)
		SSP1_CLK	I/O	1	SSP 1 Serial Clock

* 4/	Table 11: 88-Pin	GPIO Inc	terface ¹ (Continued) ²		2	
	88-Pin	68-Pin	Pin/Signal Name	Type	Supply	Description
	79	1500	GPIO_43	I/O	VDDIO_3	General Purpose I/O 43
		1880 Z 1689	ADC0_1/ACOMP1/ Mo_INN/DACB/ VOICE_N UART1_RTSn SSP1_FRM	A, I	* 100,000	ADC0 Channel 1 ACOMP0 Channel 1 ACOMP1 Channel 1 Temperature sensor remote sensing negative input Voice sensing negative input
			UART1_RTSn	0		UART 1 RTSn (active low)
			SSP1_FRM	149 ₀ ,		SSP 1 Frame Indicator
			- V . A	I	:an	
	80	60	GPIO_44	I/O	VDD10/3	General Purpose I/O 44
		Ĉ	ADC0_2 / ACOMP2 / DACA	A, I	24	ADC0 Channel 2 ACOMP0 Channel 2 ACOMP1 Channel 2 DAC Channel A output
		SOF	UART1_TXD	0		UART 1 TXD
		8	SSP1_TXD	0		SSP 1 TXD
	×	90-77	RF_CNTL1_P	0		WLAN Radio Control 1
	81	61	GPIO_45	I/O	VDDIO_3	General Purpose I/O 45
dincing	707		ADC0_3 / ACOMP3 / EXT_VREF	A, I	.55.6_6	ADC0 Channel 3 ACOMP0 Channel 3 ACOMP1 Channel 3 ADC or DAC external voltage reference in
2			UART1_RXD	1	•	UART 1 RXD
			SSP1_RXD	1		SSP 1 RXD
			RF_CNTL0_N	0	.0	WLAN Radio Control 0
					<u> </u>	1
	82	62	GPIO_46	I/O	VDDIO_3	General Purpose I/O 46
			ADC0_4 / ACOMP4	A, I	3,0	ADC0 Channel 4 ACOMP0 Channel 4 ACOMP1 Channel 4
			UART2_CTSn	100	V	UART 2 CTSn (active low)
			SSP2_CLK	I/O		SSP 2 Serial Clock



	GPIO In	terface ¹ (Continued)	2	3	+
M A R V	68-Pin	Pin/Signal Name	Type	Supply	Description
83	(AS)	GPIO_47	I/O	VDDIO_3	General Purpose I/O 47
	The SIOS	ADC0_5 / ACOMP5	A, I	02/20	ADC0 Channel 5 ACOMP0 Channel 5 ACOMP1 Channel 5
		UART2_	0	×	UART 2 RTSn (active low)
		SSP2_FRM	1/0	-	SSP 2 Frame Indicator
				'	
84	64	GPIO_48	1/8/4	VDDIO_3	General Purpose I/O 48
		ADC0_6 / ACOMP6	A, I	JUM ONNIL	ADC0 Channel 6 ACOMP0 Channel 6 ACOMP1 Channel 6
		UART2_TXD	0	- 4	PUART 2 TXD
		SSP2_TXD	0		SSE2 TXD
85	65	GPIO_49	I/O	VDDIO_3	General Purpose I/O 49
X	SO LLY	ADC0_7 / ACOMP7	A, I		ADC0 Channel 7 ACOMP0 Channel 7 ACOMP1 Channel 7
10		UART2_RXD	ı	_	UART 2 RXD *
ST		SSP2_RXD	ı	-	SSP 2 RXD

- 1. GPIO 11 to GPIO 15. GPIO 17 to GPIO 21. GPIO 34 to GPIO 38 I/O and associated muxing available on 88-pin QFN only.
- 2. All GPIO pins are pull-up high after POR.

Table 12:	Clock/C	Control Interfac	1		Package Pin Description
88-Pin	68-Pin	Pin/Signal Name	Туре	Supply	Description
26	21 2/6	XTAL_IN	A, I	AVDD18	Crystal Oscillator Input
27	22	XON OUT	A, O	AVDD18	Crystal Oscillator Output Connect to ground when an external oscillator used.
GPIO_25		XTAL32K_N	A, I	VDDIO_AON	32.768 kHz Crystal Input
GPIO_26		XTAL32K_OUT	OKA KAS	VDDIO_AON	32.768 kHz Crystal Output
GPIO_22		WAKE_UP0	1 <0	CYDDIO_AON	Wake-Up 0
GPIO_23		WAKE_UP1	9	VBIMO_AON	Wake-Up 1
GPIO_4 GPIO_16		AUDIO_CLK	\^`	VDDIO_0/M10	Audio Clock AUPLL audio clock output provided by audio PLL for axternal codec.
45	35	RESETN	I	VDDIO_AON	Chip Reset (active low)

^{1.} The XTAL32K_IN/OUT and WAKE_UP0/1 signals are muxed on GPIO pins. See Table 11, GPIO Interface, on page 53 for GPIO muxing.



'0/5 * _/_	M A R V	88MW300/302 Datasheet 8-Pin 68-Pin Pin Name PIO_40 ACOMPO_GPIO_OUT			<u> </u>			
***//	Table 13:	ADC/DA	AC/ACOMP Interface ¹		401			
	88-Pin	68-Pin	Pin Name	Type	Supply	Description		
	GPIO_40	10g	Mr.	0	VDDIO_3	ACOMP0 GPIO Output ACOMP0 output synchronous or asynchronous level signals		
			ACMAP1_GPIO_OUT	0,0	VDDIO_3	ACOMP1 GPIO Output ACOMP1 output synchronous or asynchronous level signals		
			ADC_DAC_TRIGOERO	T	VDDIO_3	ADC/DAC External Trigger 0		
	GPIO_41		ADC_DAC_TRIGGERO ACOMPO_EDGE_PULSE	018/45	VDDIO_3	ACOMP Edge Pulse 0 Output pulse aligned with synchronize comparison result.		
			ACOMP1_EDGE_PULSE	0	1/40pio_3	ACOMP Edge Pulse 1 Output pulse aligned with synchronize comparison result.		
			ADC_DAC_TRIGGER1	ı	VDDIO_3	ADC/DAC External Trigger 1		
	GPIO_49	801	ADC0_7 / ACOMP7	A, I	VDDIO_3	ADC0 Channel 7 ACOMP0 Channel 7 ACOMP1 Channel 7		
	GPIO_48	DE LA	ADC0_6 / ACOMP6	A, I	VDDIO_3	ADC0 Channel 6 ACOMP0 Channel 6 ACOMP1 Channel 6		
.9	GPIO_47		ADC0_5 / ACOMP5	A, I	VDDIO_3	ADC0 Channel 5 ACOMP0 Channel 5 ACOMP1 Channel 5		
Anincin's	GPIO_46		ADC0_4 / ACOMP4	A, I	VDDIO_3	ADC0 Channel 4 ACOMP0 Channel 4 ACOMP1 Channel 4		
5	GPIO_45		ADC0_3 / ACOMP3 / EXT_VREF	A, I	VDDIO_3	ADC0 Channel 3 ACOMP0 Channel 3 ACOMP1 Channel 3 ADC or DAC external voltage reference input		
	GPIO_44		ADC0_2 / ACOMP2 / DACA	A, I	VDDIO_3	ADC0 Channel 2 ACOMP0 Channel 2 ACOMP1 Channel 2 DAC Channel A output		

Table 13:	ADC/DA	AC/ACOMP Interface ¹ (0	Continue	ed)	Packag Pin Description
88-Pin	68-Pin	Pin Name	Type	Supply	Description
GPIO_43	The Store	ADC0_1 / ACOMP1 / TS_INN / DACB / VOICE_N	A, I	VDDIO_3	ADC0 Channel 1 ACOMP0 Channel 1 ACOMP1 Channel 1 Temperature sensor remote sensing negative input Voice sensing negative input
GPIO_42		ADC0_0 / ACCOMBO / TS_INP / VOICE_	A, I	VDDIO_3	ADC0 Channel 0 ACOMP0 Channel 0 ACOMP1 Channel 0 Temperature sensor remote sensing positive input Voice sensing positive input

All ADC/DAC/ACOMP signals are muxed on GPIO pins. See Table 11/1/19PIO Interface, on page 53 for GPIO muxing.

 Dele 14: LDO18 Comparator Interface

Table 14: LDO18 Comparator Interface¹

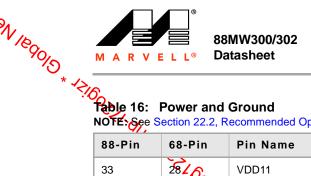
				<i></i>			
88-Pin	68-Pin	Pin Name	Type	Supply	Description		
GPIO_23	01	COMP_IN_P	A, I	VDDIO_AON	LDO18 Comparator Input, Positive Positive input to LDO18 comparator.		
GPIO_24	20/4/	COMP_IN_N	A, I	VDDIO_AON	LDO18 Comparator Input, Negative Positive input to LDO18 comparator.		

^{1.} All COMP signals are muxed on GPIO pins. See Table 11, GPIO Interface, on page 53 for GPIO muxing.

Table 15: JTAG Interface¹

88-Pin	68-Pin	Signal Name	Type	Supply	Description
GPIO_6		TDO	0	VDDIO_0	JTAG Test Data
GPIO_7		тск	ı	VDDIO_0	JTAG Test Clock
GPIO_8		TMS	I/O	VDDIO_0	JTAG Controller Select
GPIO_9		TDI	I	VDDIO_0	JTAG Test Data
GPIO_10		TRSTn	I	VDDIO_0	JTAG Test Reset I/O (active low)

^{1.} All JTAG signals are muxed on GPIO pins. See Table 11, GPIO Interface, on page 53 for GPIO muxing.



NOTE: See Section 22.2, Recommended Operating Conditions, on page 314 for ratings.

88-Pin	68-Pin	Pin Name	Type	Description
33 59	28/68/M	VDD11	PWR	1.1V Core Power Supply Input
5	5	% DIO _0	PWR _*	I/O Digital Power Supply
34	29	VDD10021	1	*
58	48	VDDIO_2	00/10	
77	57	VDDIO_3	<013	
73	53		18/L	
51	41	VDDIO_AON		Olin
60	50	VTR_VDD33	PWR	3.3V Off Analog Power Supply
63		USB_AVDD33	PWR	3.3V USB Analog Power Supply
74	54	ISENSE		3.3V Off Analog Power Supply 3.3V USB Analog Power Supply USB Current Source Connect pin to ground with resistance.
20	15	AVDD33	PWR	3.3V Analog Power Supply
18 19 23 24 25 28	13 14 18 19 20 23	AVDD18	PWR	1.8V Analog Power Supply
41	31	LDO11_VOUT	PWR	1.1V LV LDO Voltage Output
42	32	LDO11_V18		BUCK18 Inductor Connection
43	33	BUCK18_VX		BUCK18 Inductor Connection
44 87	34 67	VBAT_IN	PWR	LDO VBAT Input This pin must be connected to VBAT/V33 input even if BUCK18 is not used.
86	66	FLY18		1.8V LDO Fly Capacitor to Ground Connection
88	68	FLY11		1.1V LDO Fly Capacitor to Ground Connection
22	17	NC	NC	No Connect NOTE: CONNECT THESE PINS to GROUND.
29 30 31 32	24 25 26 27	DNC	DNC	Do Not Connect Do not connect these pins. Leave these pins floating.

⁽²⁾16**9.5**

Configuration Pins

Table 17 shows the pins used as configuration inputs to set parameters following a reset. The definition of these pins changes immediately after reset to their usual function. To set a configuration bit to 0, attach a 100 k Ω resistor from the pin to ground. No external circuitry is required to set a configuration bit to 1.

Table 17: Configuration Pins

0	D'in Name	One Grandler Francisco	
Configuration Bits	Pin Name	Configuration Function	
CON[5]	GPIO_16	Boot Options	
CON[4]	GPIO_27	90 = boot from UART 01 = period 10 = boot from USB 11 = boot from Flash (default)	
	NO NATIONAL PROPERTY OF THE PR	Will Wexible	, c
	15/10	%	

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- -- Reorient or relocate the receiving antenna.
- -- Increase the separation between the equipment and receiver.
- -- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- -- Consult the dealer or an experienced radio/TV technician for help.

FCC Radiation Exposure Statement

The modular can be installed or integrated in mobile or fix devices only. This modular cannot be installed in any portable device, for example, USB dongle like transmitters is forbidden.

This modular complies with FCC RF radiation exposure limits set forth for an uncontrolled environment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter. This modular must be installed and operated with a minimum distance of 20 cm between the radiator and user body.

If the FCC identification number is not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. This exterior label can use wording such as the following: "Contains Transmitter Module FCC ID: YCJGTIMW302" or "Contains FCC ID: YCJGTIMW302"

when the module is installed inside another device, the user manual of this device must contain below warning statements;

- 1. This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:
- (1) This device may not cause harmful interference.
- (2) This device must accept any interference received, including interference that may cause undesired operation.
- 2. Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

This device must be installed and operated with a minimum distance of 20 cm between the radiator and user body.