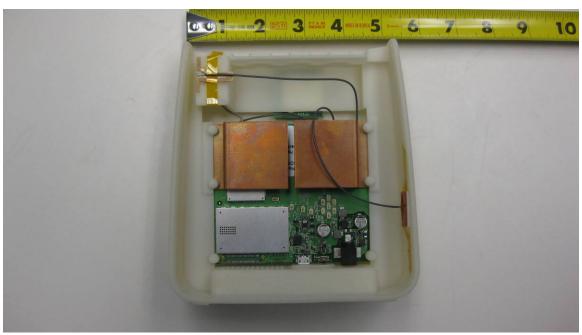


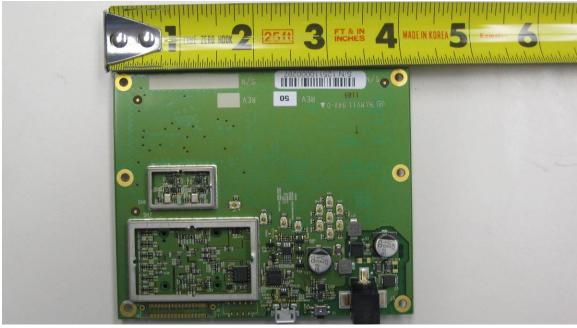
Back 1



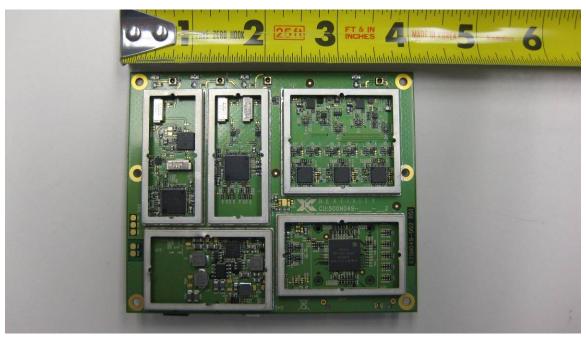
Back 2



Bareboard Back1



Bareboard Back2



Bareboard Front1



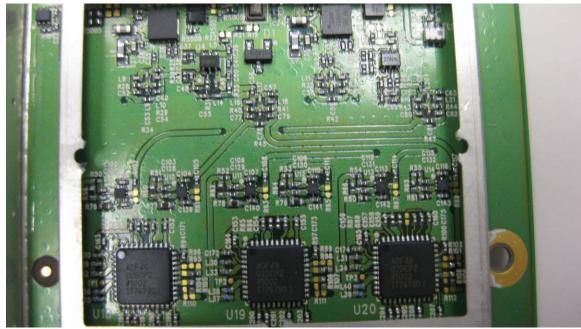
Bareboard Front2



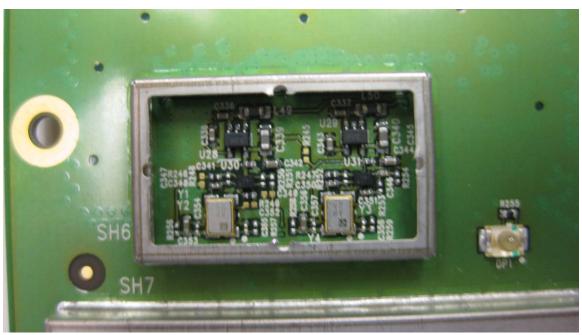
Baseband



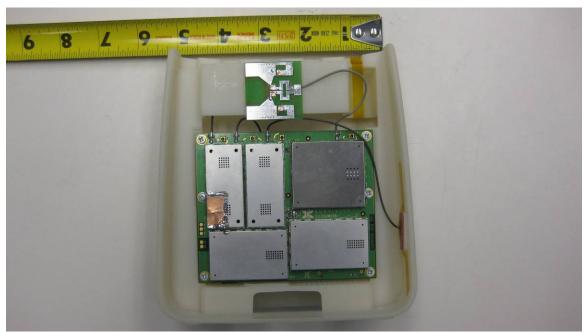
Cell Ant



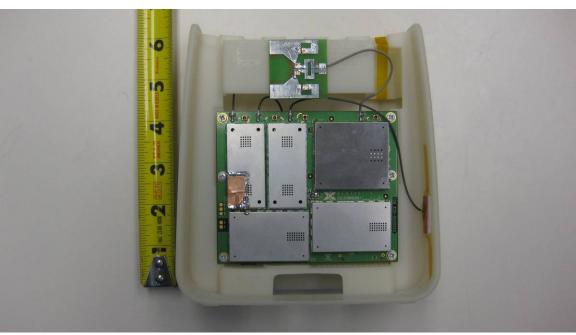
Cell



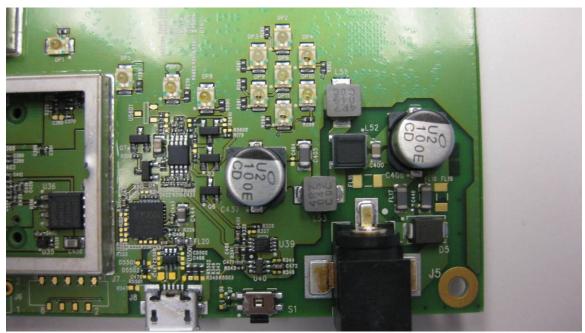
Clock



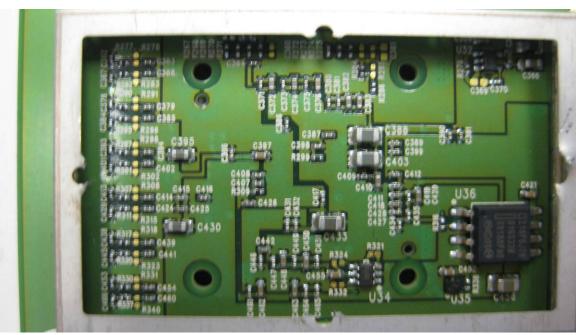
Front1



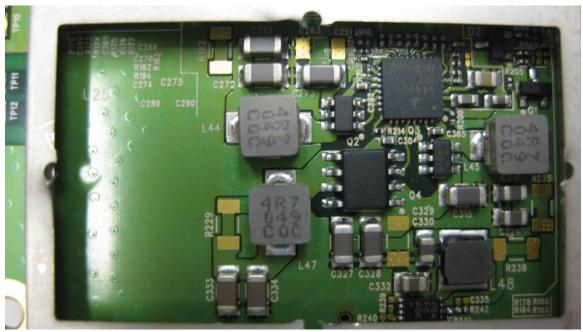
Front 2



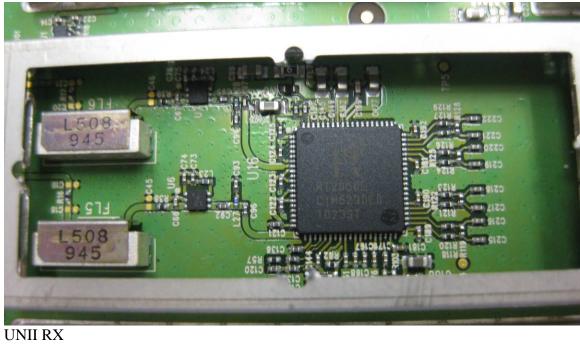
Interface

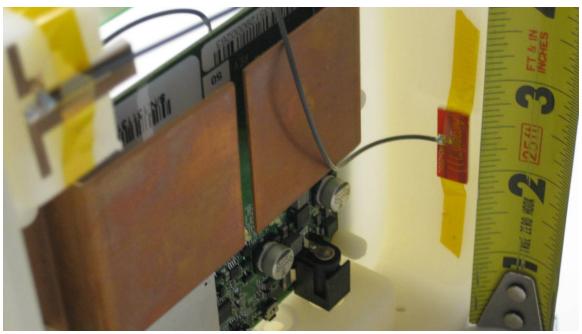


Memory

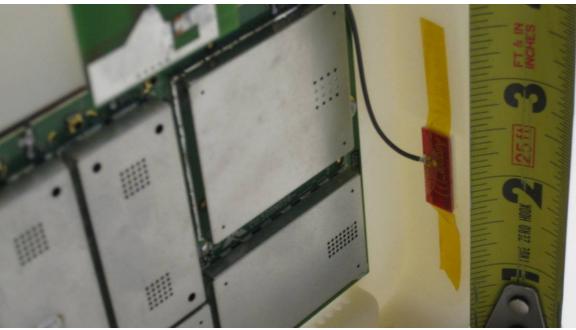


Power





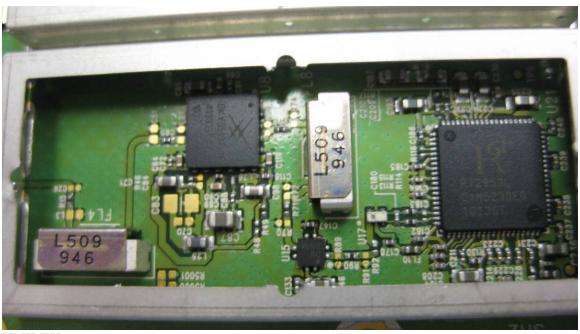
UNII RX1 ant



UNII RX2 ant



UNII TX Ant



UNII TX