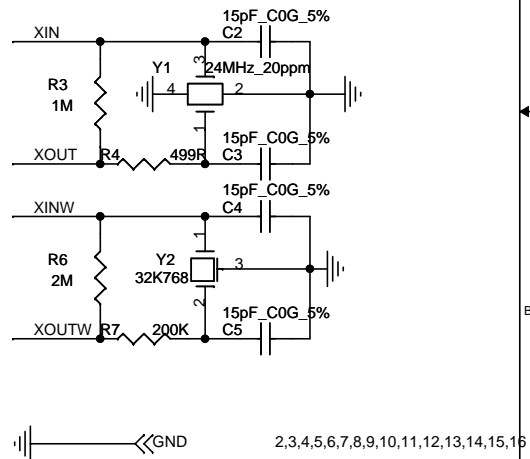
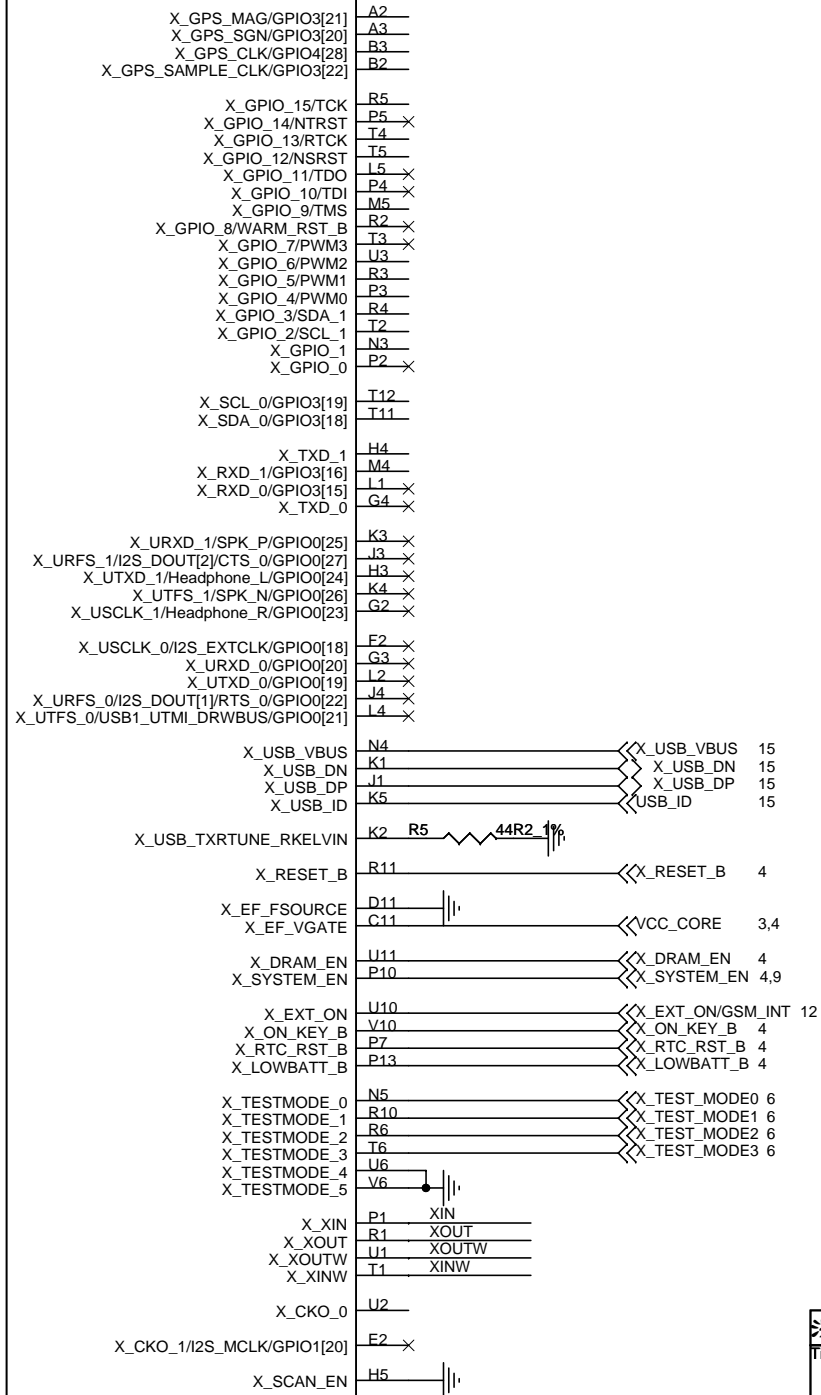


U1A



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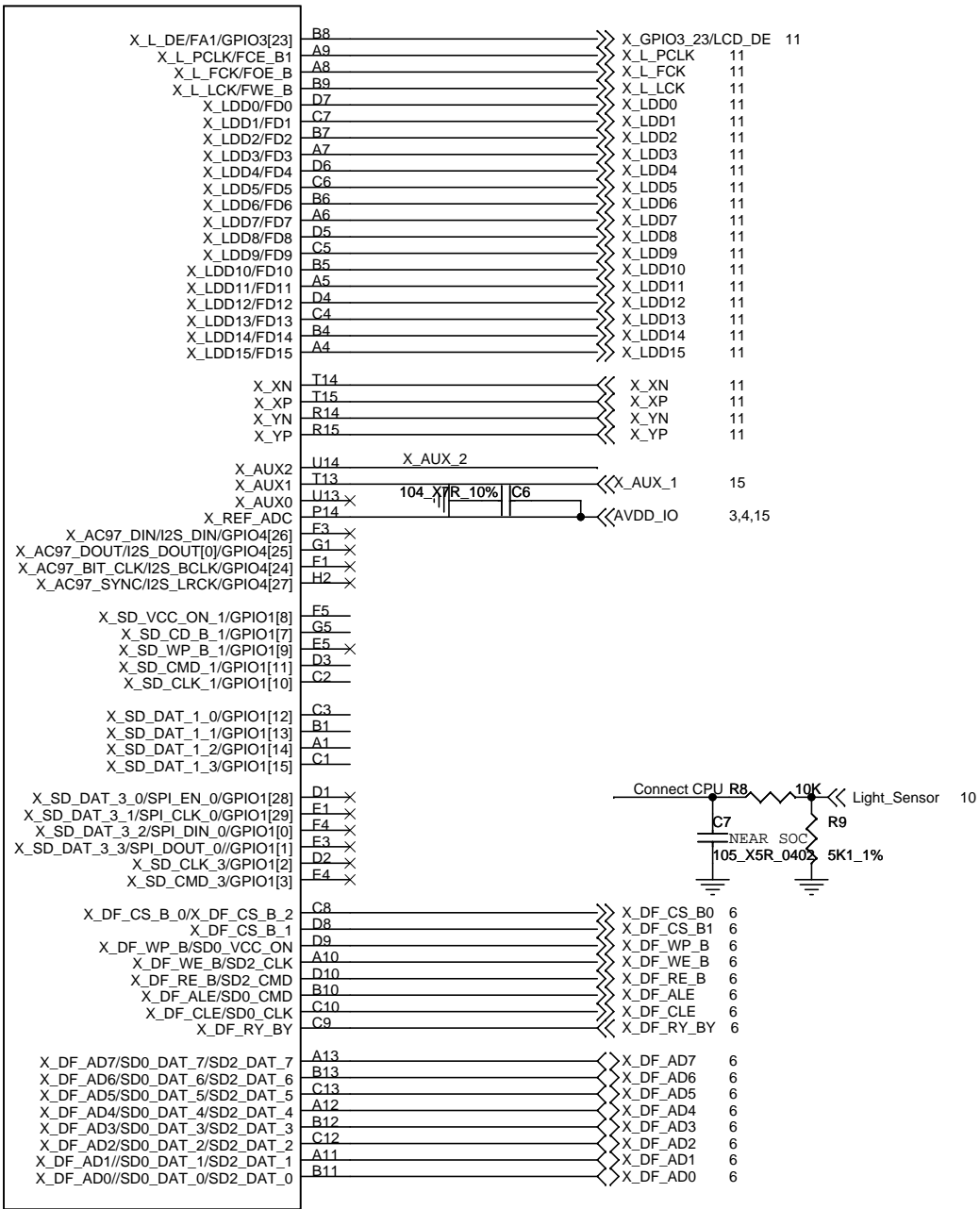
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U1B



1,3,4,5,6,7,8,9,10,11,12,13,14,15,16

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Size Document Number

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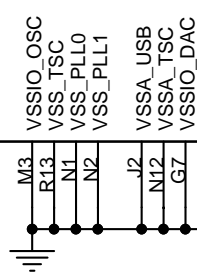
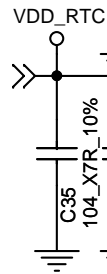
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U1C

X_MDQM0	C14	X_MDQM0	5
X_MDQS0	C15	X_MDQS0	5
X_MD0	A14	X_MD0	5
X_MD1	B14	X_MD1	5
X_MD2	A15	X_MD2	5
X_MD3	B15	X_MD3	5
X_MD4	D14	X_MD4	5
X_MD5	D15	X_MD5	5
X_MD6	E13	X_MD6	5
X_MD7	D13	X_MD7	5
X_MD8	F14	X_MD8	5
X_MD9	F15	X_MD9	5
X_MD10	E15	X_MD10	5
X_MD11	F13	X_MD11	5
X_MD12	G14	X_MD12	5
X_MD13	G13	X_MD13	5
X_MD14	H15	X_MD14	5
X_MD15	H14	X_MD15	5
X_MDQM1	G15	X_MDQM1	5
X_MDQS1	F14	X_MDQS1	5
X_GATE_I	P15	X_GATE_I	
X_GATE_O	N14	X_GATE_O	
X_MCLK_O	N15	X_MCLK_O	5
X_MCLKB_O	M15	X_MCLKB_O	5
X_MCS_B	K12	X_MCS_B	5
X_MCKE	L13	X_MCKE	5
X_MRAS_B	J15	X_MRAS_B	5
X_MCAS_B	K15	X_MCAS_B	5
X_MWE_B	J13	X_MWE_B	5
X_MBA0	J12	X_MBA0	5
X_MBA1	H13	X_MBA1	5
X_MA0	G12	X_MA0	5
X_MA1	F12	X_MA1	5
X_MA2	E12	X_MA2	5
X_MA3	D12	X_MA3	5
X_MA4	M13	X_MA4	5
X_MA5	M14	X_MA5	4,6,12,15
X_MA6	J14	X_MA6	5
X_MA7	M12	X_MA7	5
X_MA8	K14	X_MA8	5
X_MA9	L14	X_MA9	5
X_MA10	H12	X_MA10	5
X_MA11	L15	X_MA11	5
X_MA12	K13	X_MA12	5
X_MA13	L12	X_MA13	5

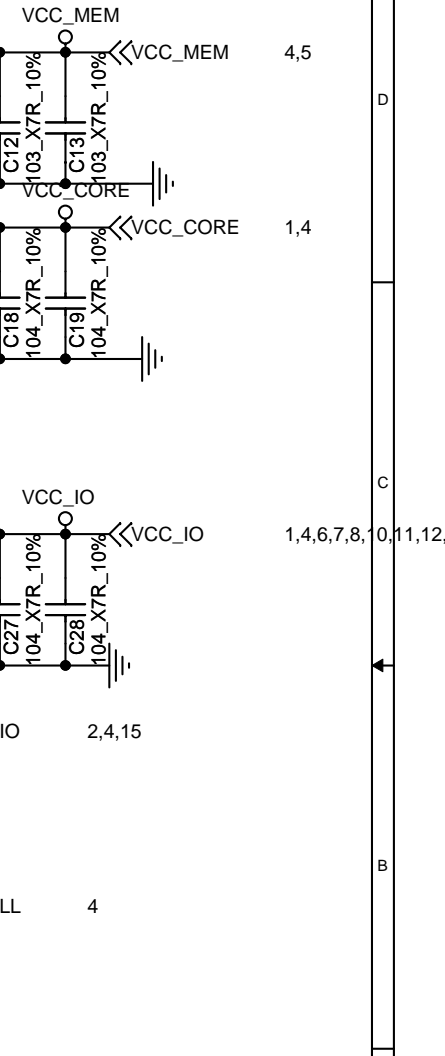
U1D

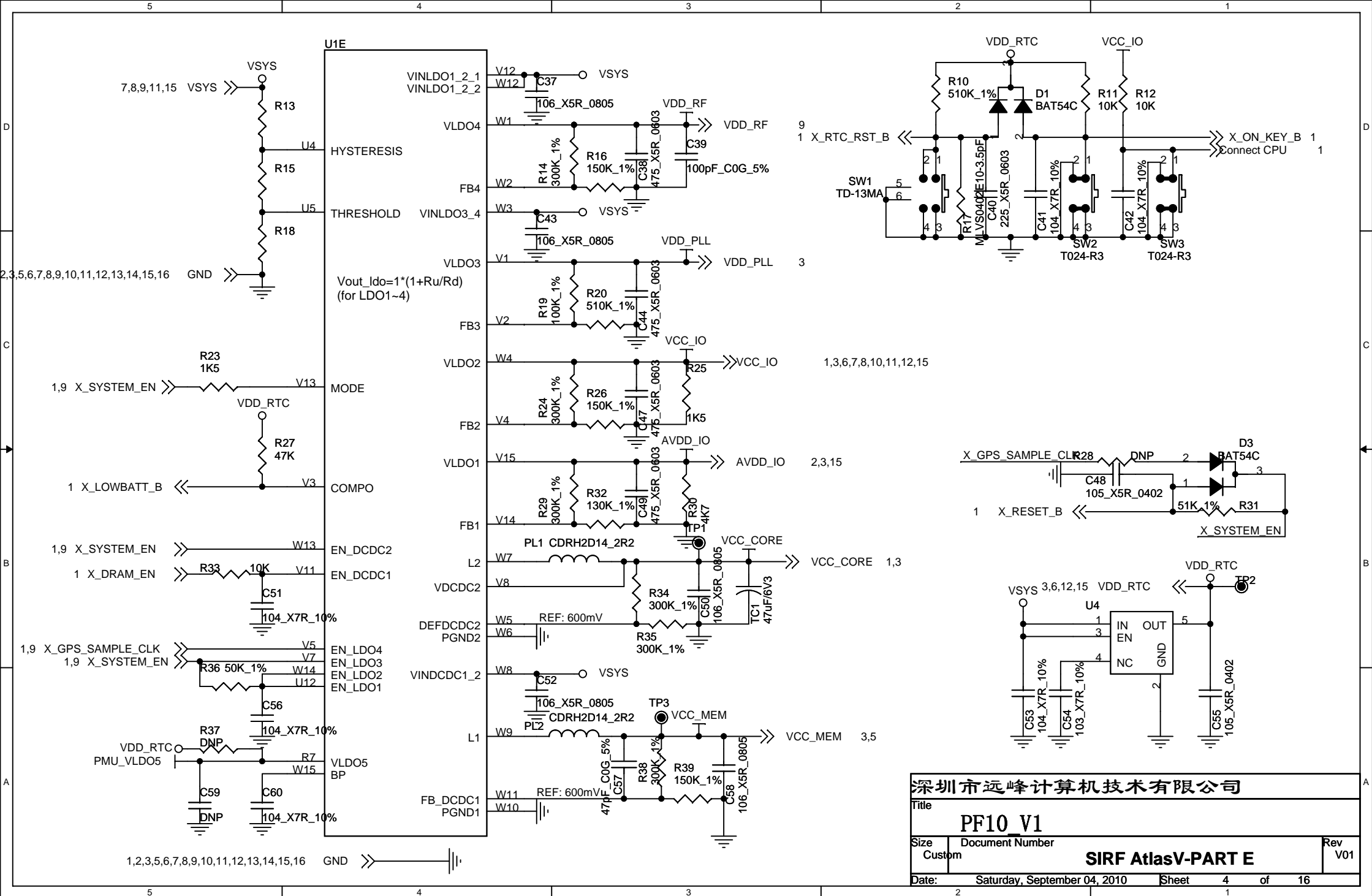
E9	VSS1
F6	VSS2
F7	VSS3
F9	VSS4
H6	VSS5
G8	VSS6
G10	VSS7
G11	VSS8
H7	VSS9
J6	VSS10
H9	VSS11
H10	VSS12
J7	VSS13
J10	VSS14
J11	VSS15
K8	VSS16
K7	VSS17
K9	VSS18
K10	VSS19
L6	VSS20
L7	VSS21
L9	VSS22
L11	VSS23
M6	VSS24
M8	VSS25
M10	VSS26
M11	VSS27
N7	VSS28
N8	VSS29
N9	VSS30
N10	VSS31
P8	VSS32
P9	VSS33
R9	VSS34
R8	VSS35
T7	VSS36
T8	VSS37
T9	VSS38
T10	VSS39
U7	VSS40
U8	VSS41
U9	VSS42
V9	VSS43
U15	VDDIO_RTC
R12	VDD_RTC

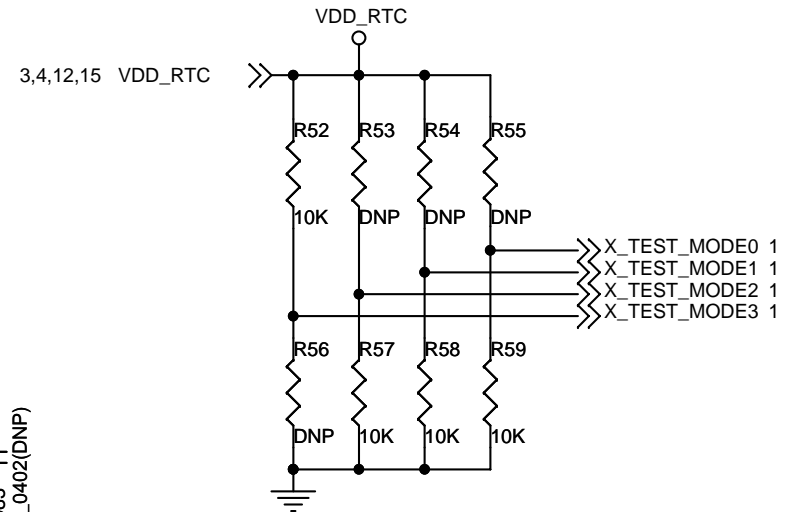
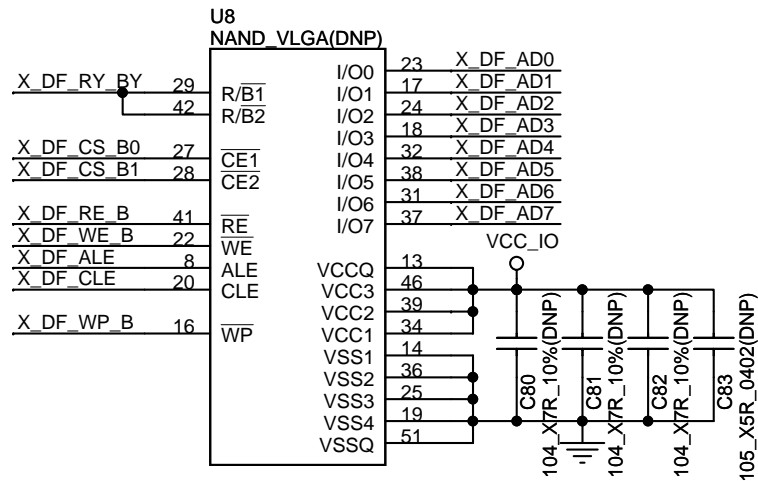
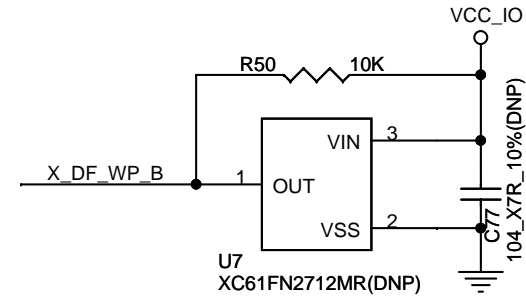
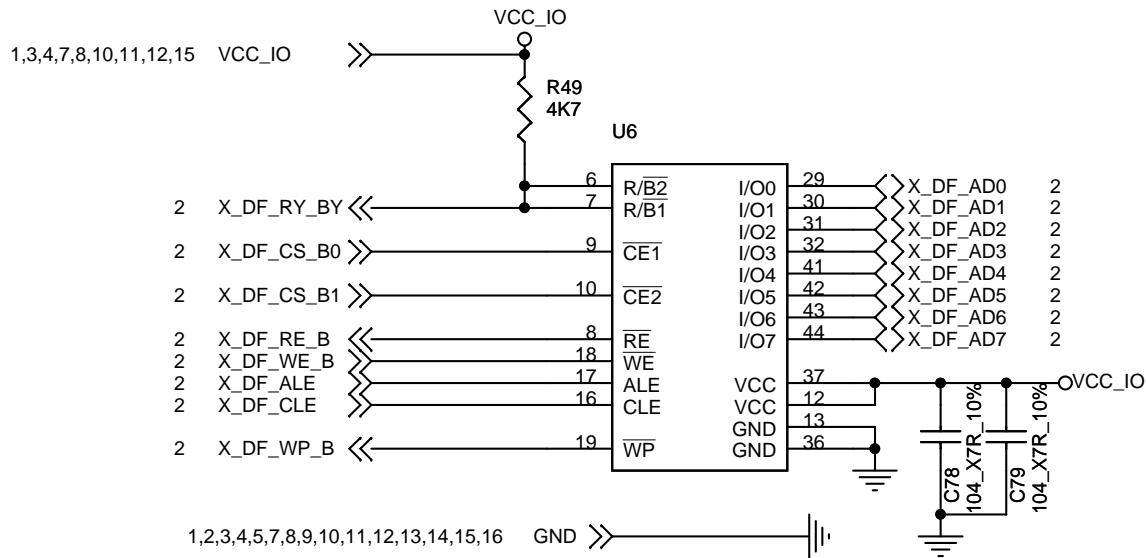


VDDIO_MEM1	G9
VDDIO_MEM2	H11
VDDIO_MEM3	J9
VDDIO_MEM4	K11
VDDIO_MEM5	L10
VDDIO_MEM6	M9
VDDIO_MEM7	F10
VDD_CORE10	F11
VDD_CORE9	L8
VDD_CORE8	M7
VDD_CORE7	K6
VDD_CORE6	N11
VDD_CORE5	J8
VDD_CORE4	P11
VDD_CORE3	H8
VDD_CORE2	F11
VDD_CORE1	F10
VDD_TSC	P12
VDD_USB	J5
VDDIO1	E6
VDDIO2	F7
VDDIO3	P6
VDDIO4	N6
VDDIO_N	E8
VDDIO_L	F8
VDDIO_OSC	L3
VDDA3V3_TSC	N13
VDDA_USB	H1
VDDIO_DAC	G6
VDD_PLL0	M1
VDD_PLL1	M2

1,2,4,5,6,7,8,9,10,11,12,13,14,15,16

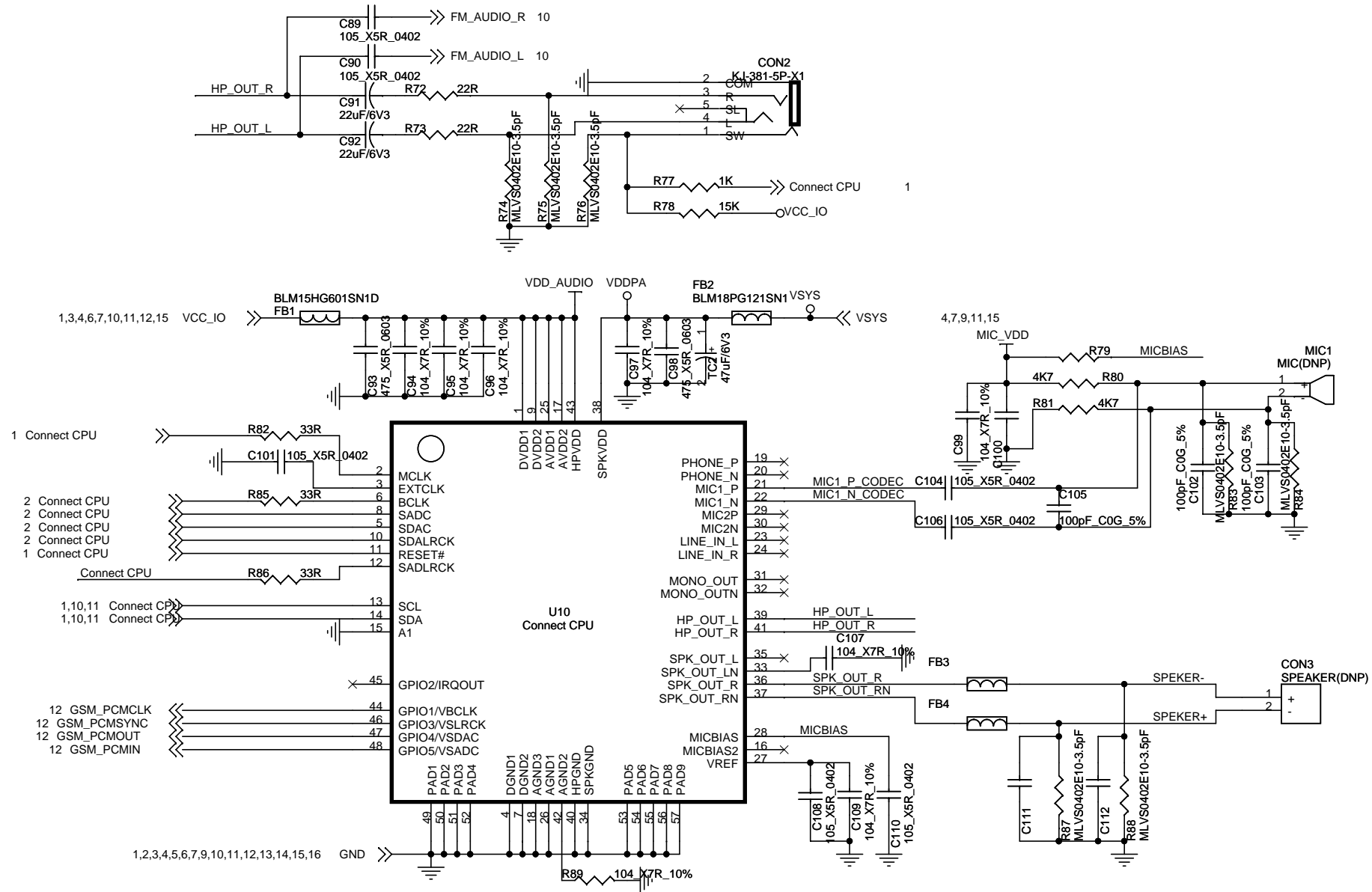






WORKING MODE	SUB MODE	FEATURE1	FEATURE0
X_TEST_MODE[5:4]	X_TEST_MODE[3:2]	X_TEST_MODE[1]	X_TEST_MODE[0]
2'B00: Normal 2'B01: Normal With ARM JTAG 2'B10: Function ATE	2'b00: Embedded ROM Nand Boot (SLC)	1'b0: 8bit	1'b0: 2KB page
		1'b1: LBA-Nand	1'b1: 4KB page
			1'bx: 2KB page
	2'b01: NAND Boot(SLC)	1'bx: Don't Care	1'b0: 512B page
			1'b1: 2KB page
			1'b0: 2KB page
			1'b1: 4KB page
			1'b0: 4KB page
	2'b10: Embedded ROM Nand Boot (MLC)	1'b0: ECC 12bit per 1KB	1'b1: 8KB page
		1'b1: ECC 24bit per 1KB	
	2'b11: Embedded ROM SD/MMC Boot	-	-

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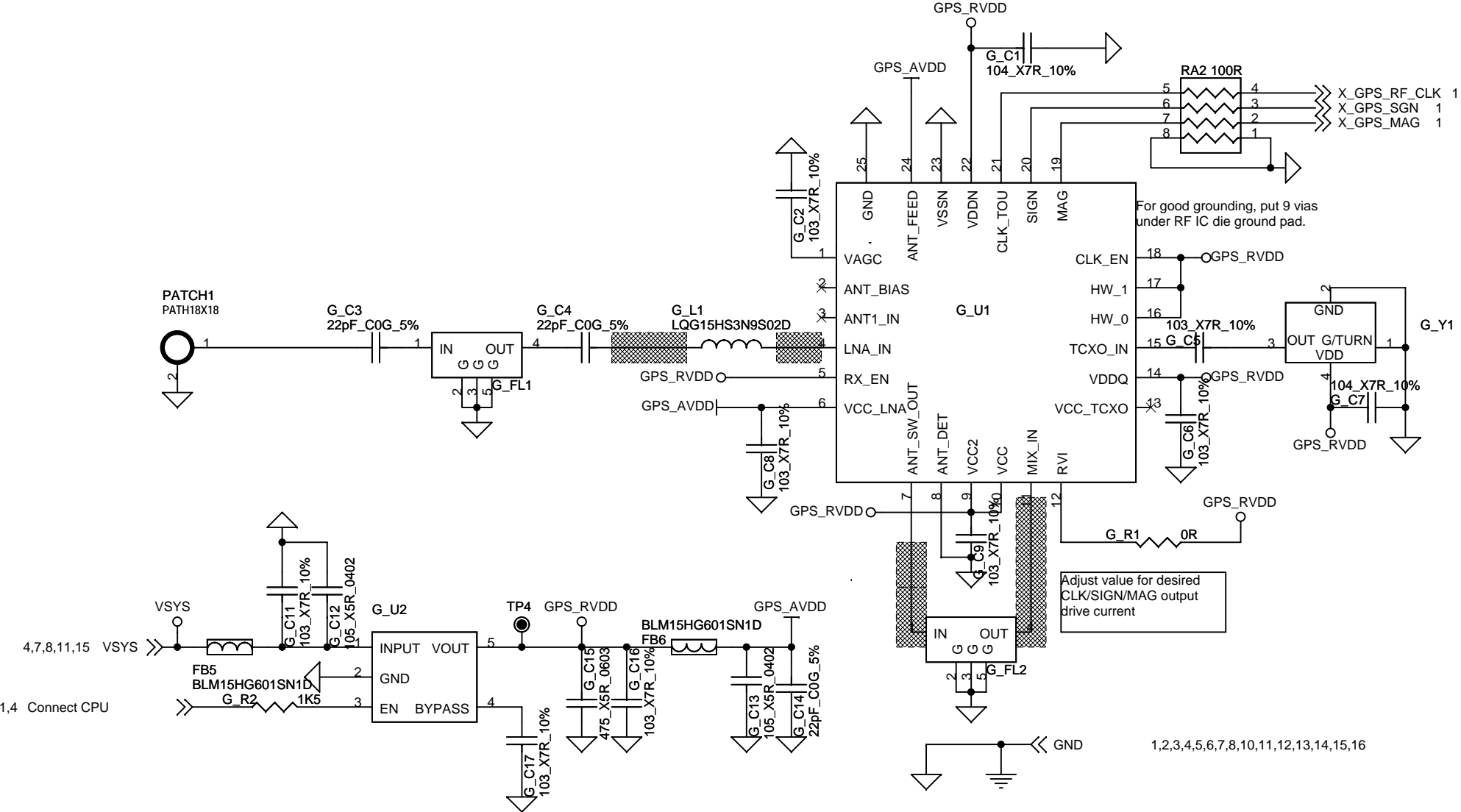
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GPS RF Receiver core
Must be placed into RF shielding case



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Table 5: Pin SW vs. Chip Supply and Clock Source

SW[1:2]	HF	Chip Mode
00	x	Disabled
11	0	XTAL/External reference 7.6MHz
11	1	XTAL/External reference 15.2MHz
10	1	XTAL/External reference 32768Hz

