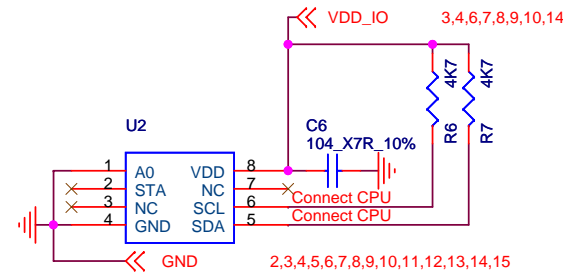
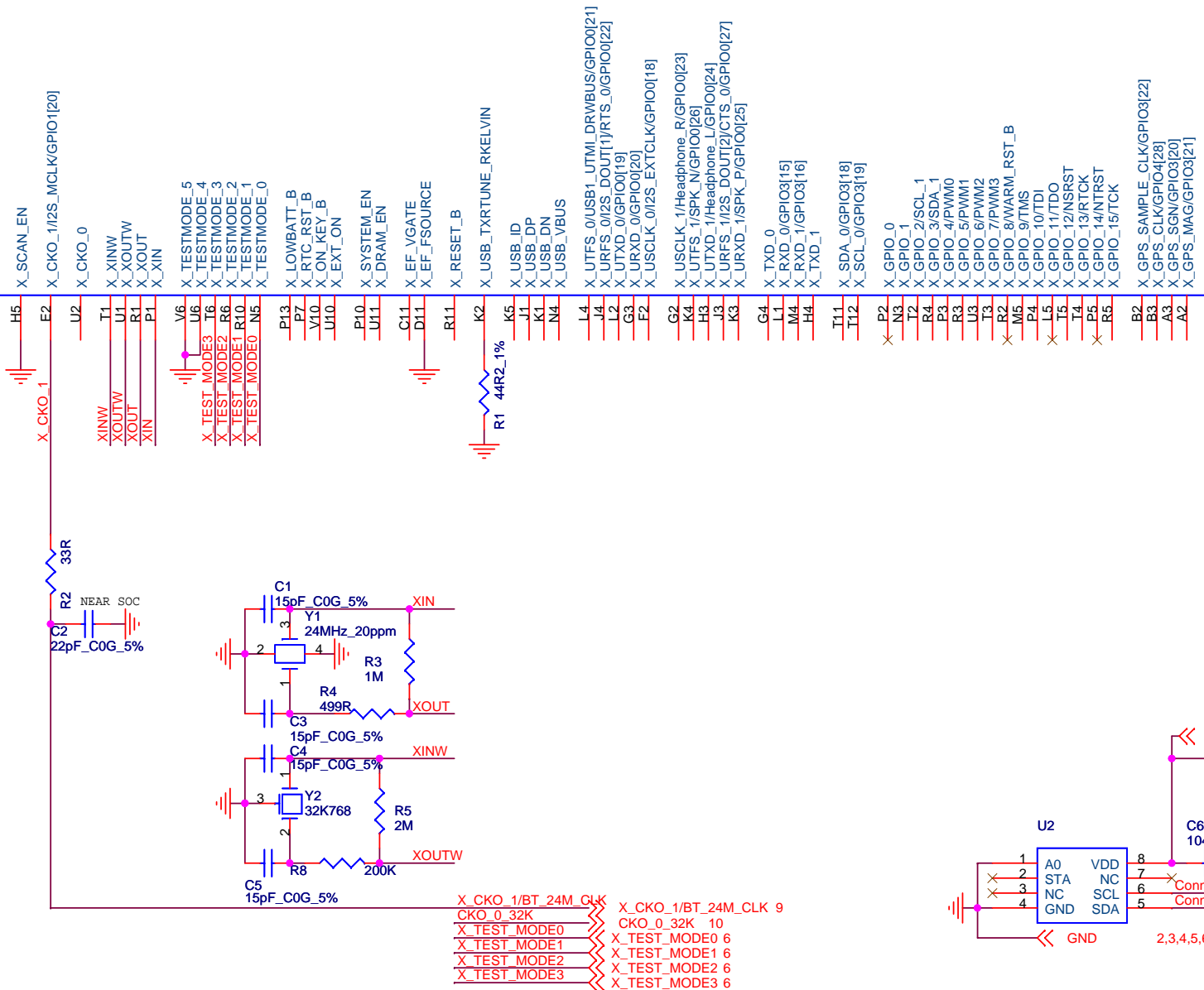


U1A



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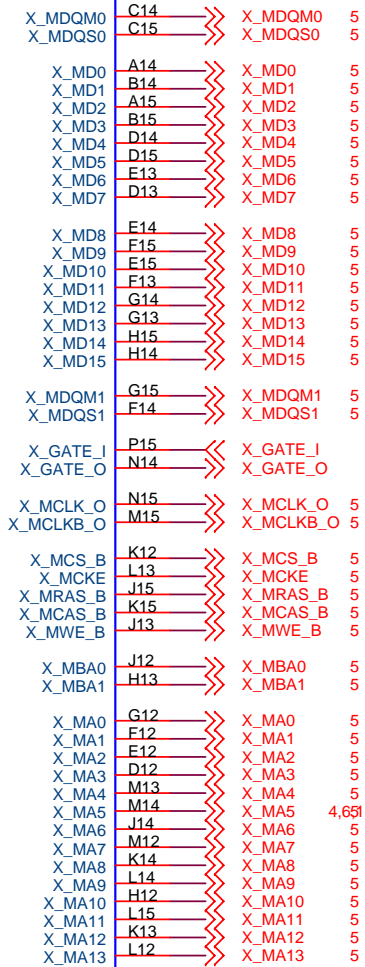
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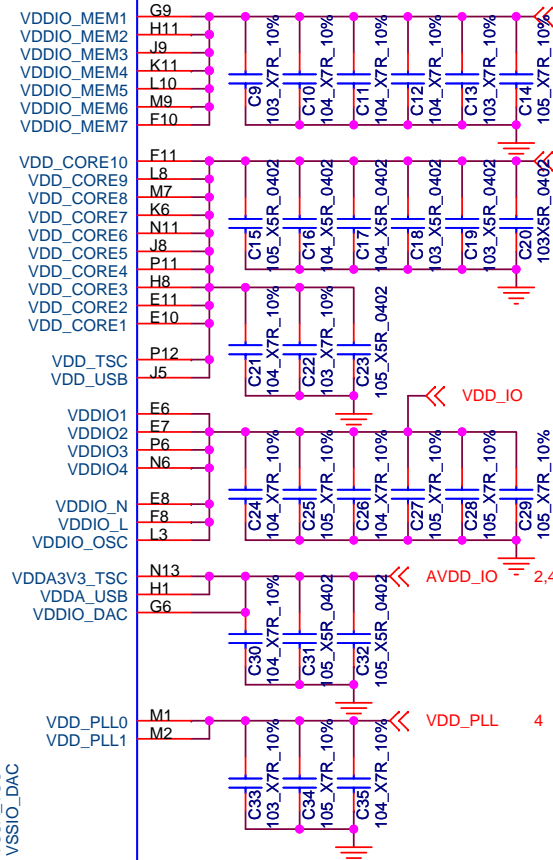
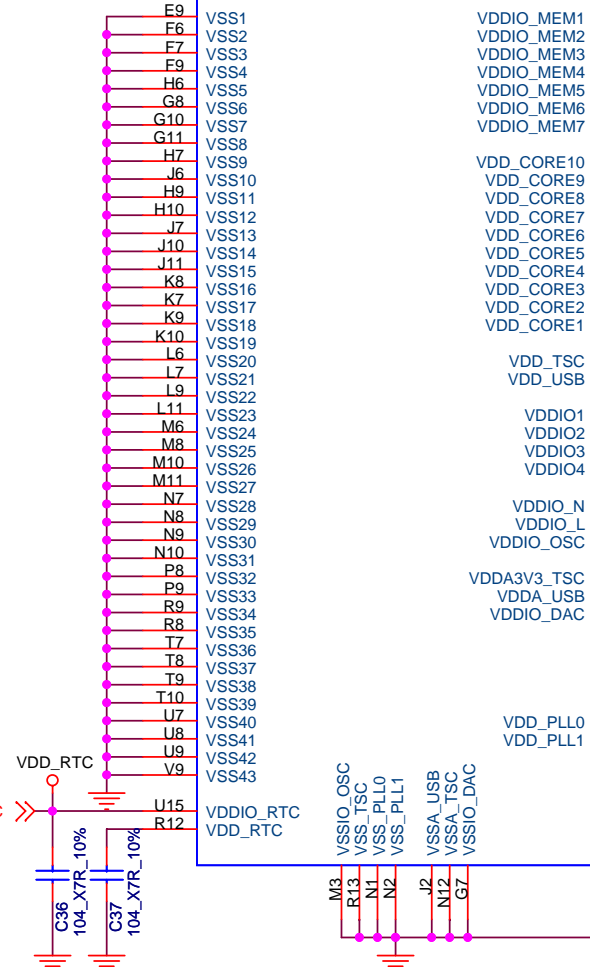
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U1C



U1D



VDD_MEM 4,5

VDD_CORE 1,4

VDD_IO 1,4,6,7,8,9,10,14

AVDD_IO 2,4,8,14

VDD_PLL 4

GND 1,2,4,5,6,7,8,9,10,11,12,13,14,15

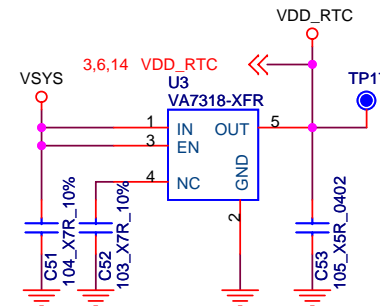
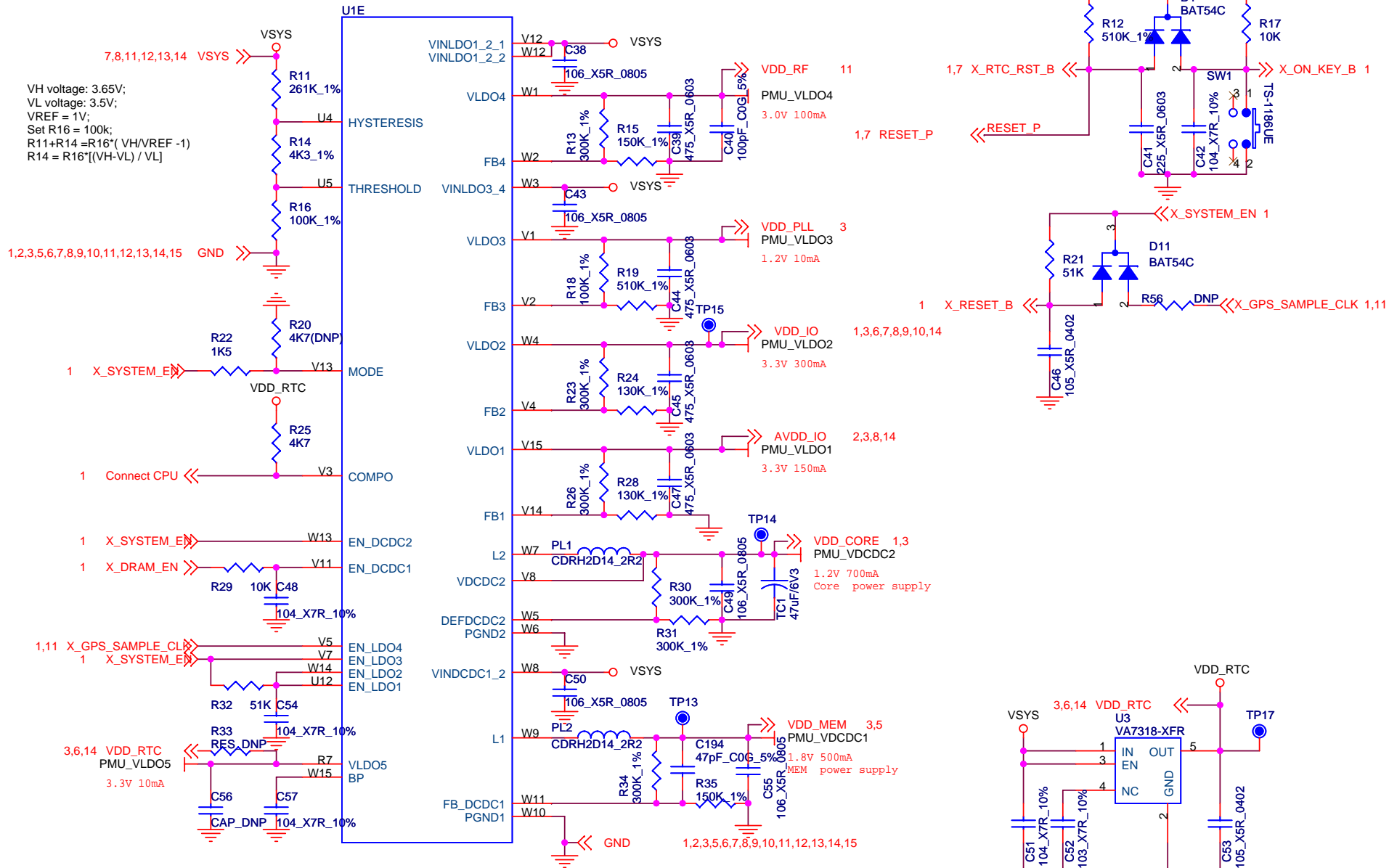
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VH voltage: 3.65V;
VL voltage: 3.5V;
VREF = 1V;
Set R16 = 100k;
 $R11+R14 = R16 * (VH/VREF - 1)$
 $R14 = R16 * [(VH-VL) / VL]$



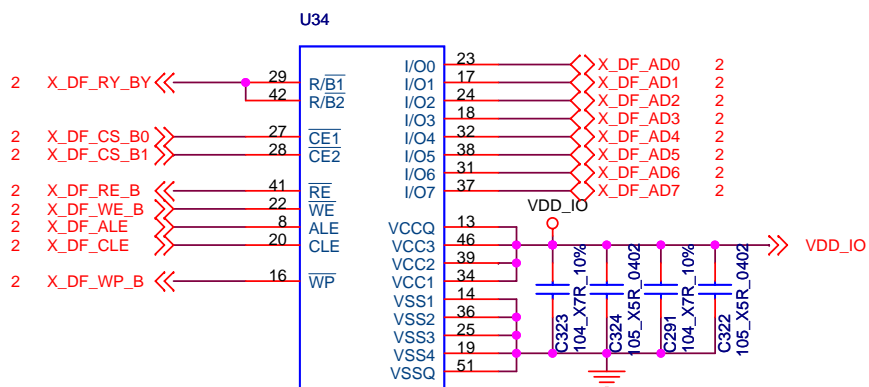
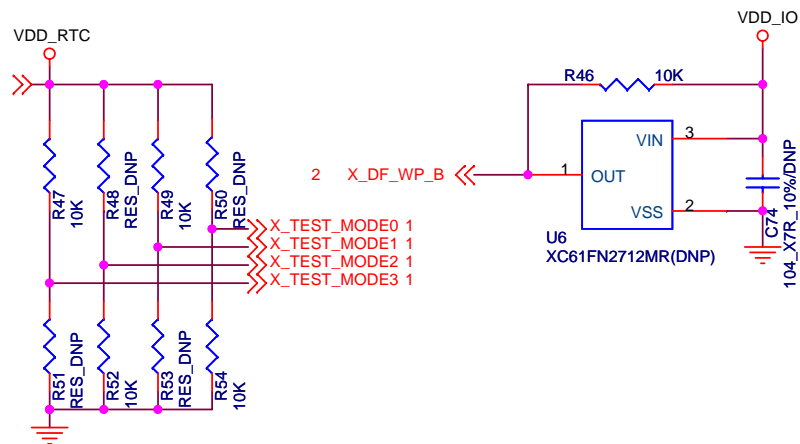
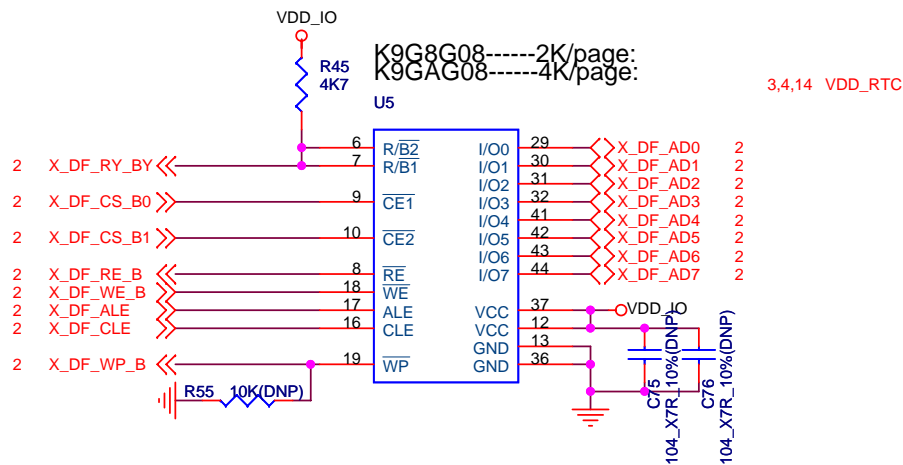
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Size Document Number
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X_TEST_MODE[5:4]	X_TEST_MODE[3:2]	X_TEST_MODE[1]	X_TEST_MODE[0]
2B00: Normal 2B01: Normal With ARM JTAG 2B10: Function ATE	2'b00: Embedded ROM NAND boot (SLC)	1'b0: 8-bit	1'b0: 2KB page
		1'b1: LBA-NAND	1'b1: 4KB page
	2'b01: NAND boot (SLC)	1'bx: Don't Care	1'bx: 2KB page
		1'b0: 512B page	1'b1: 2KB page
	2'b10: Embedded ROM NAND boot (MLC)	1'b0: ECC 12-bit per 1KB	1'b0: 2KB page
		1'b1: ECC 24-bit per 1KB	1'b1: 4KB page
			1'b1: 8KB page

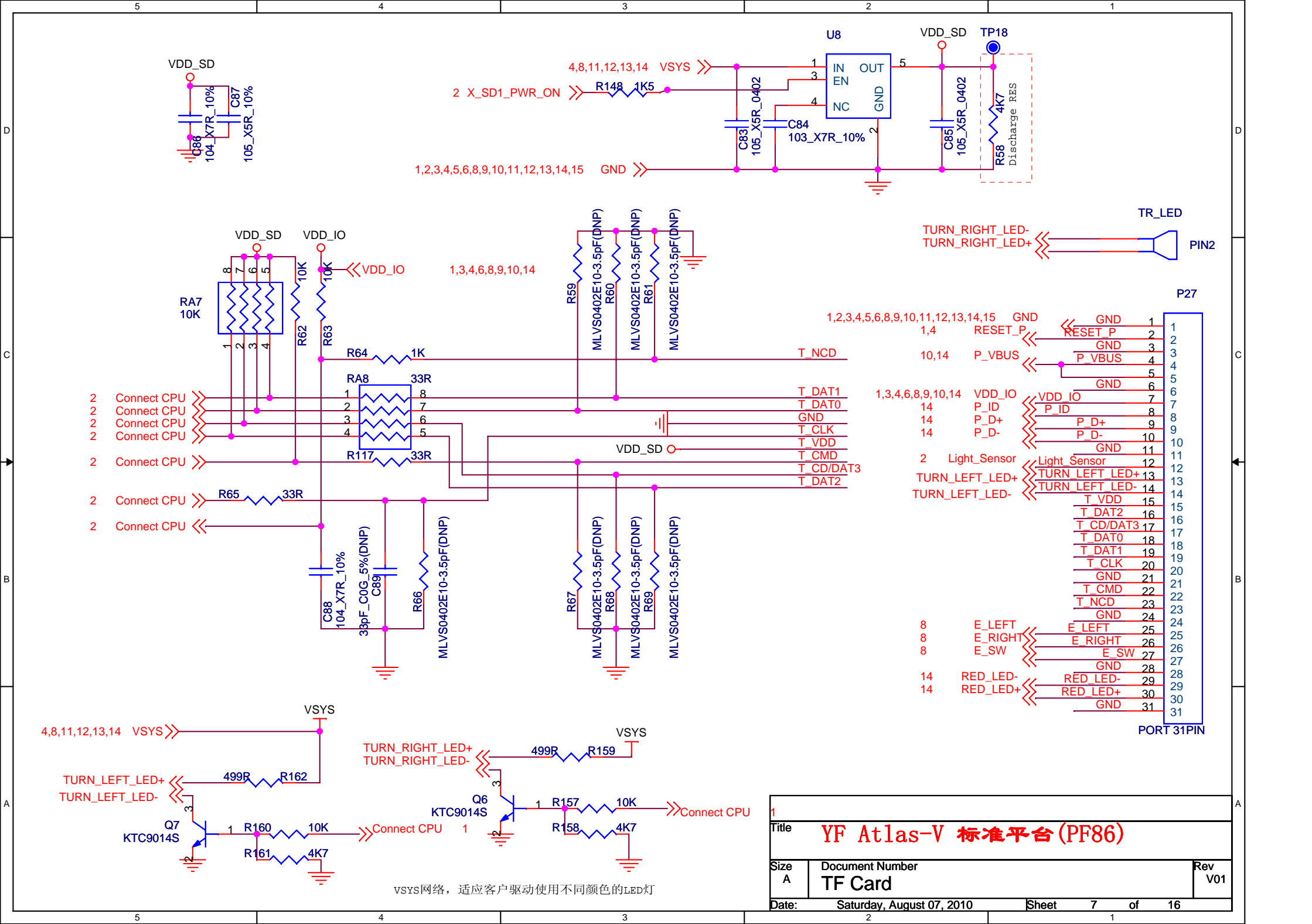
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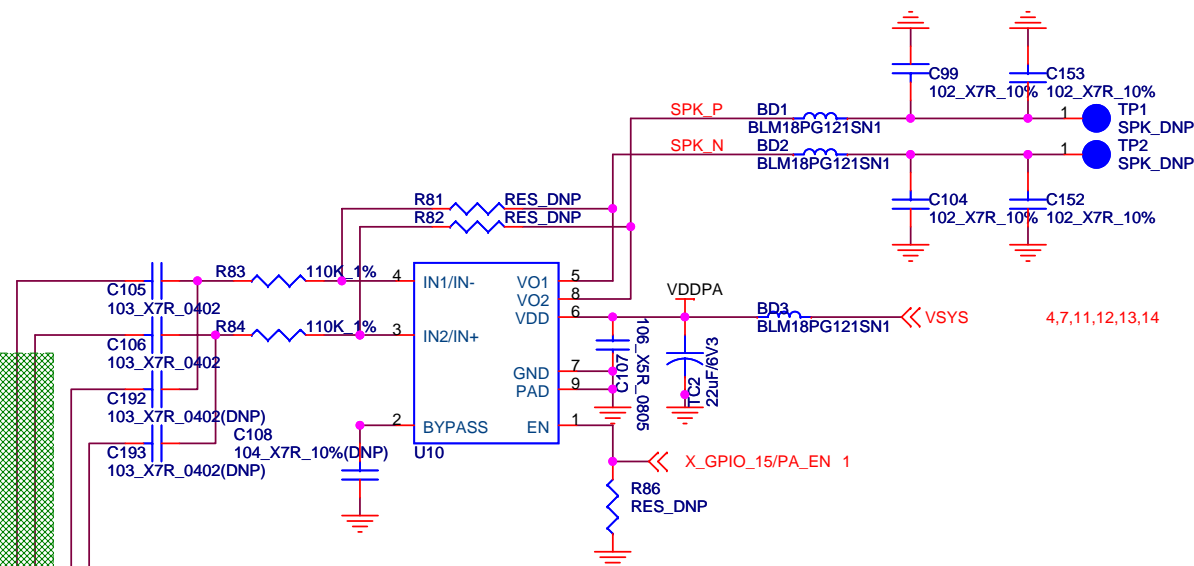
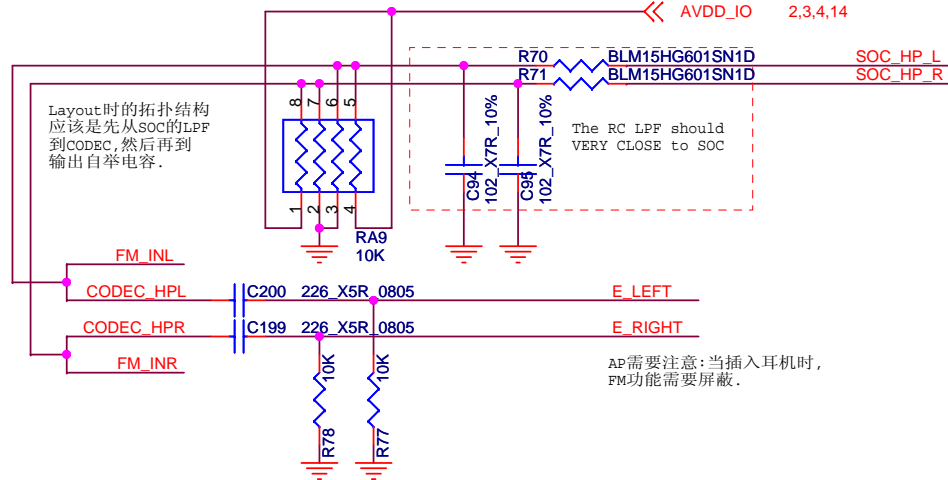
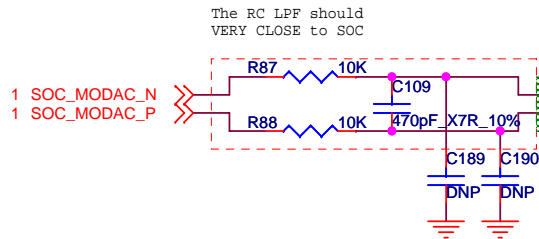
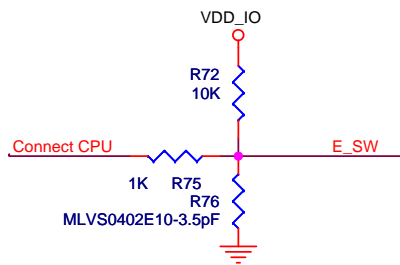
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Size Document Number
Custom MLC/iNAND

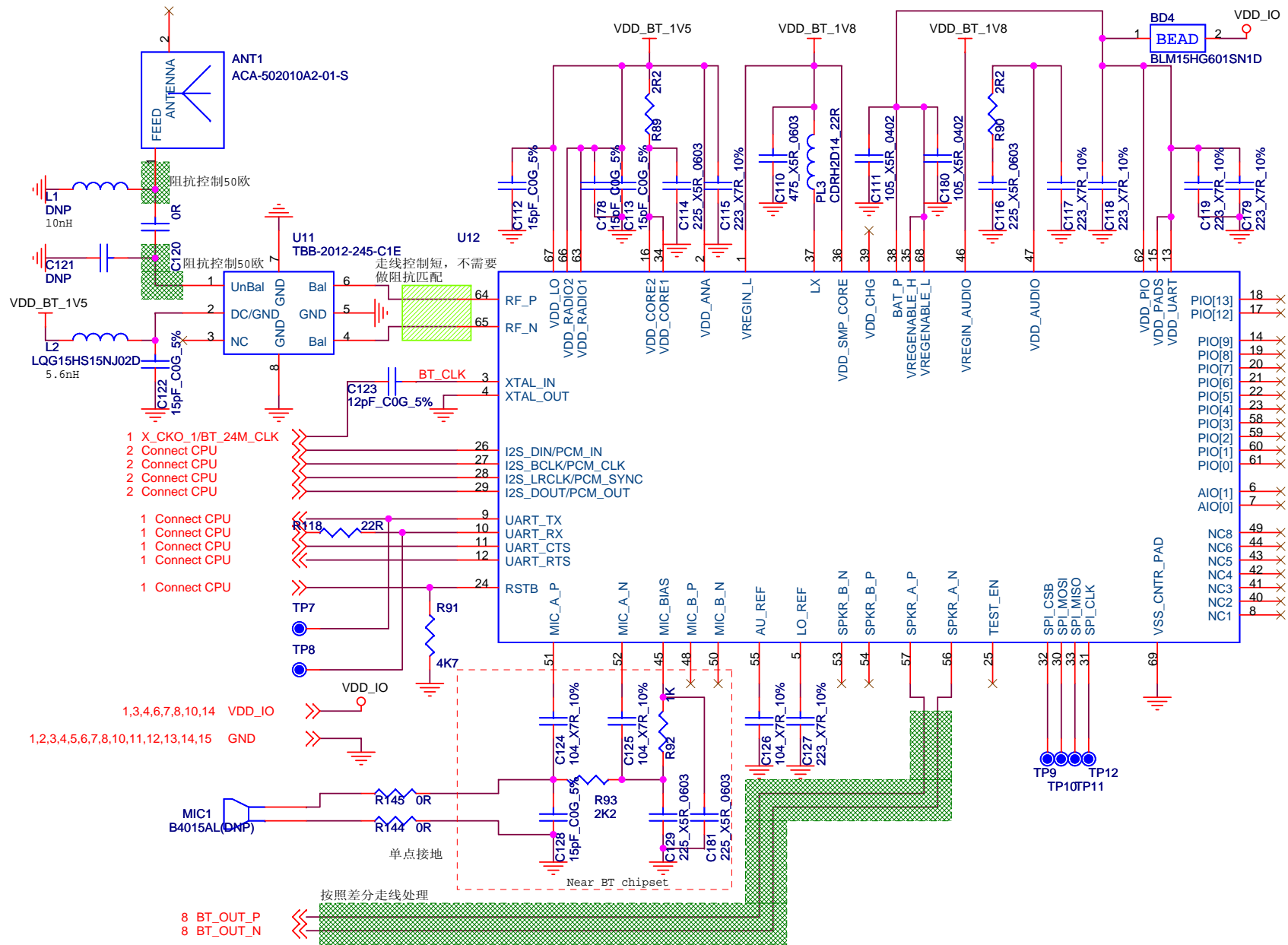
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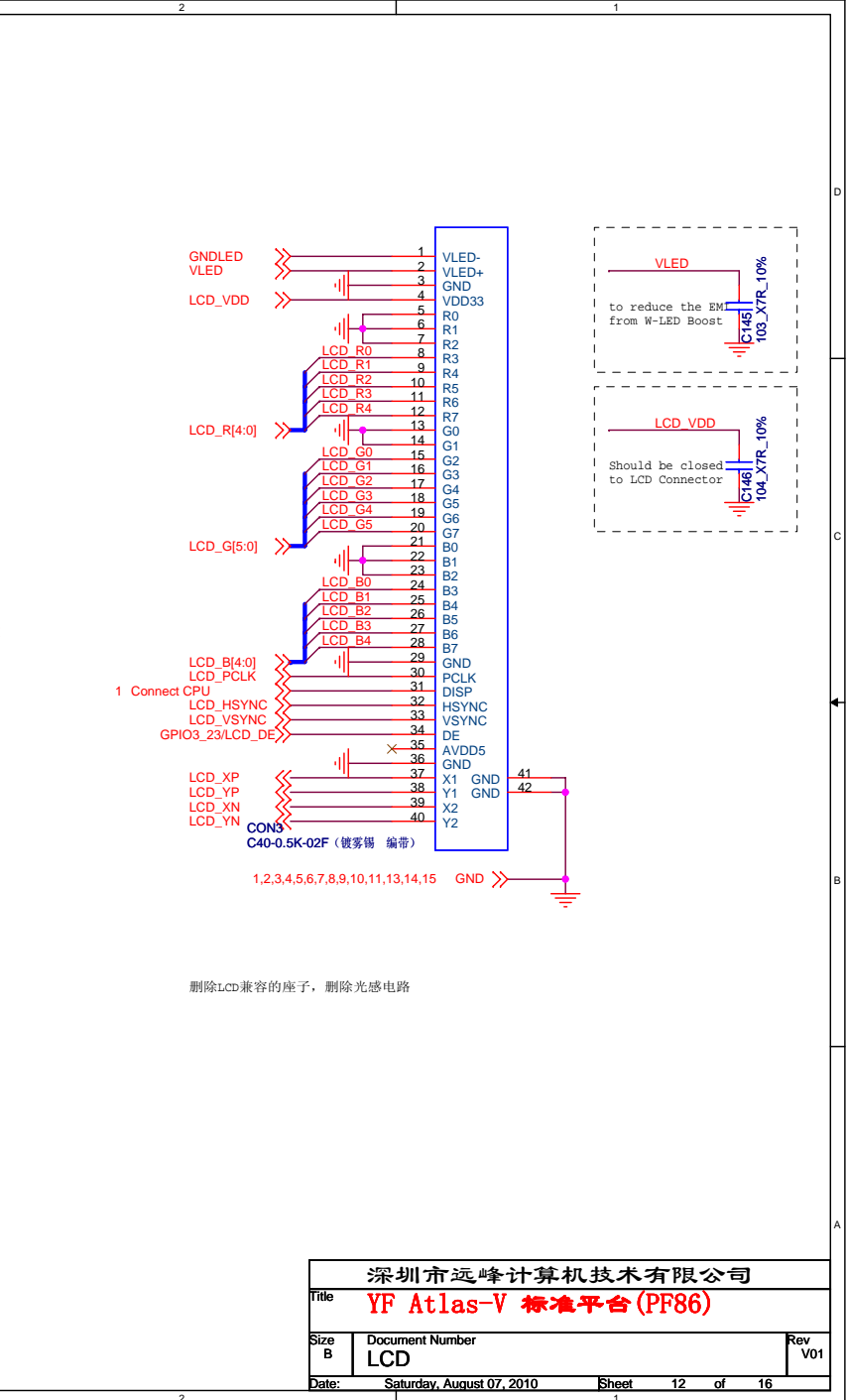
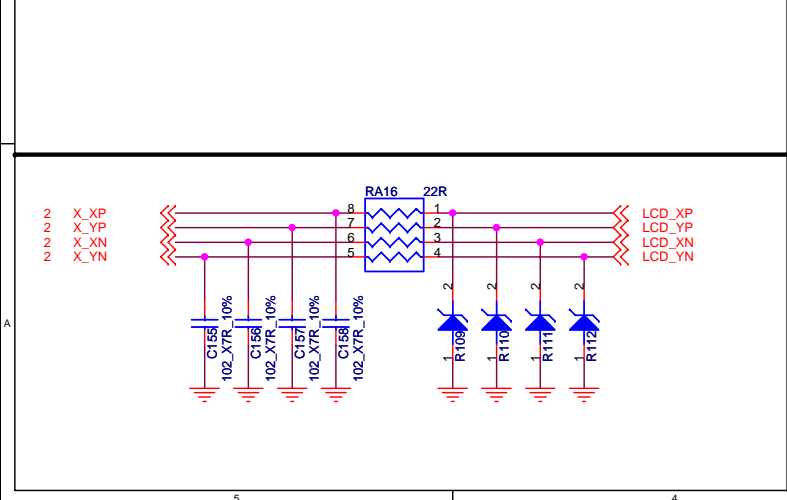
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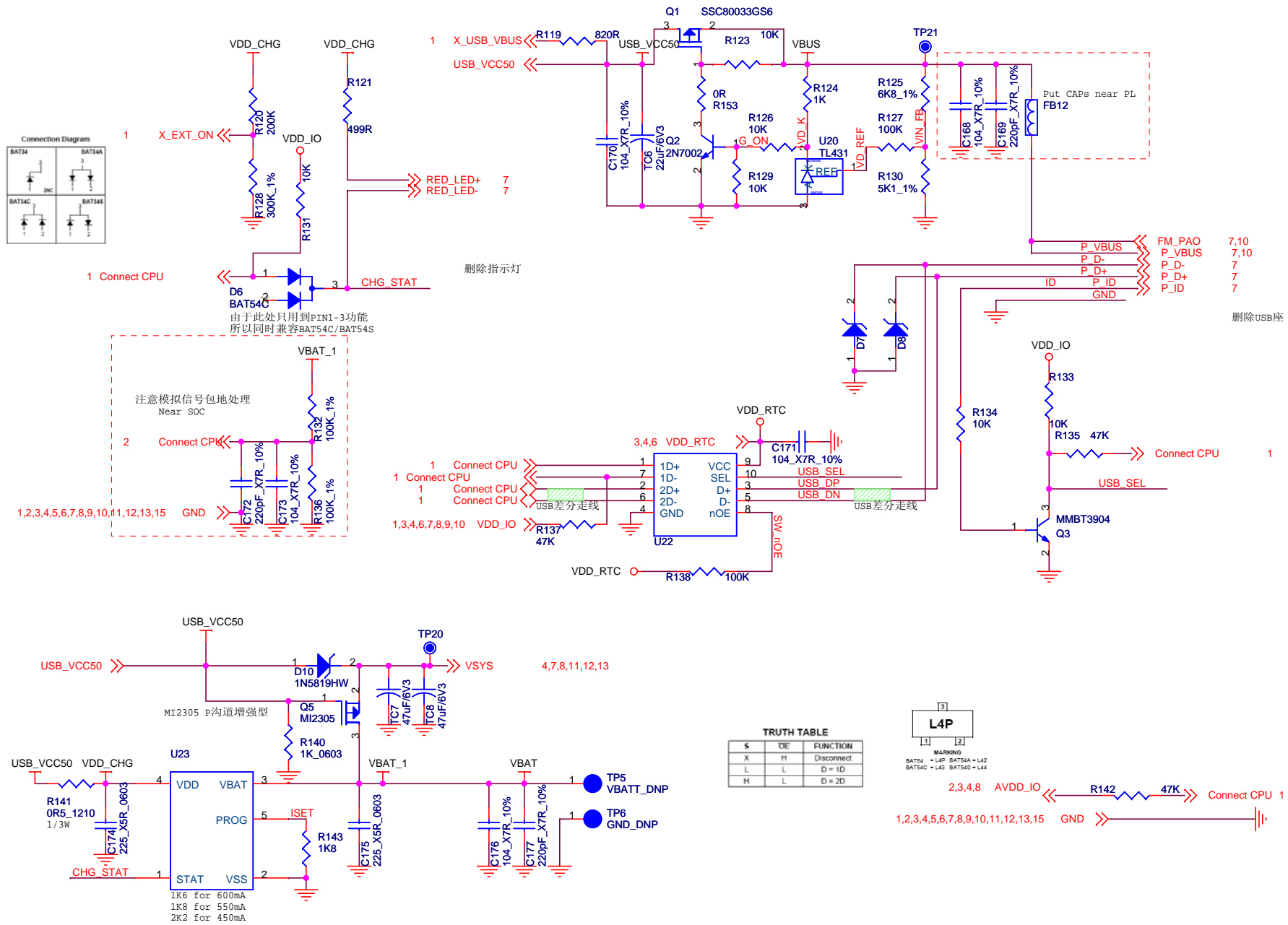
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S	OE	FUNCTION
X	H	Disconnect
L	L	D = 1D
H	L	D = 2D



MARKING

BATES4 - L4P BATES4A - L
 BATES4C - L43 BATES4S - L