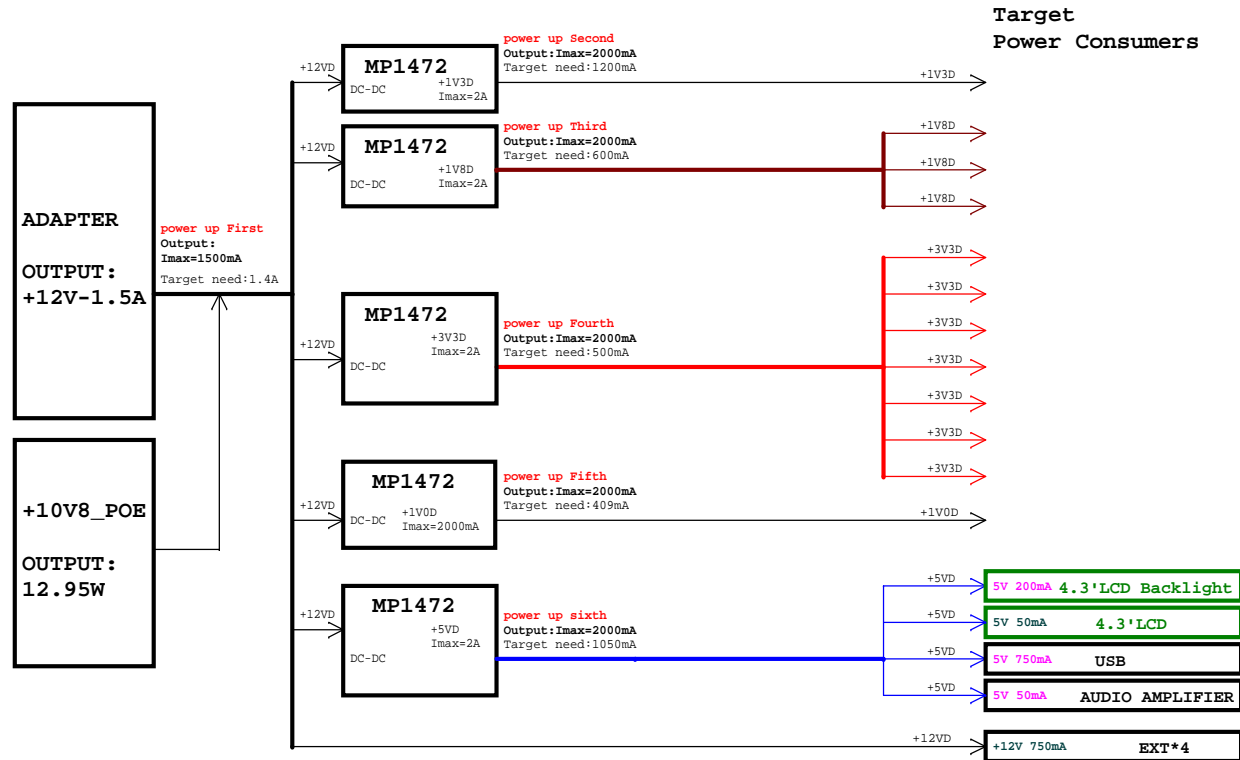
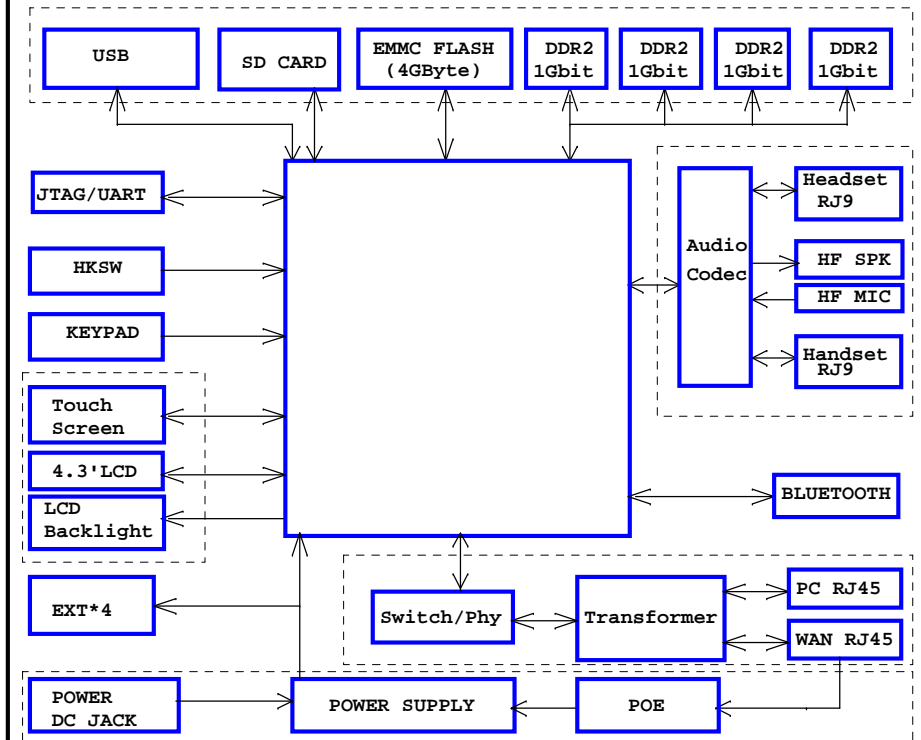



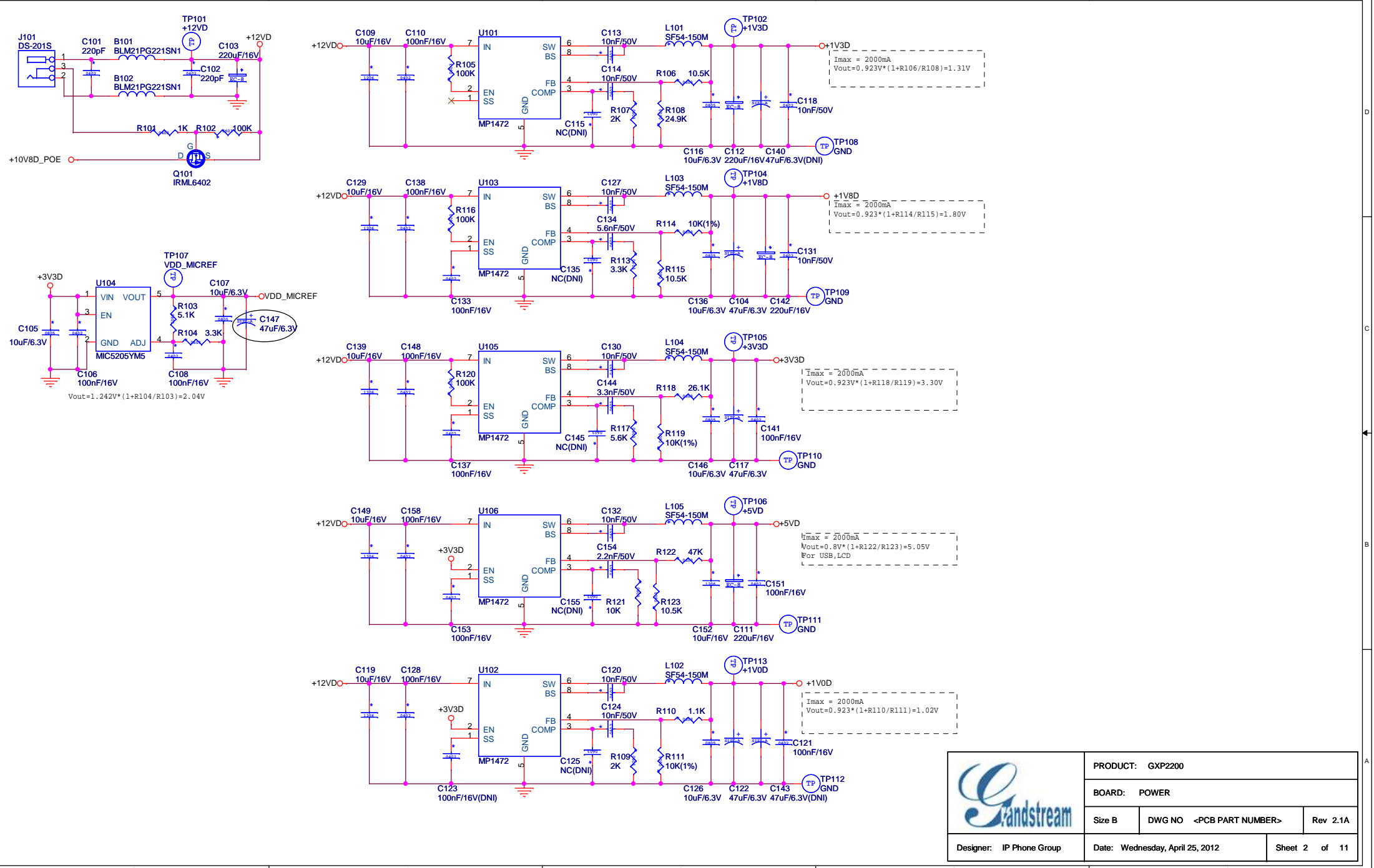
FRAMEWORK-POWER




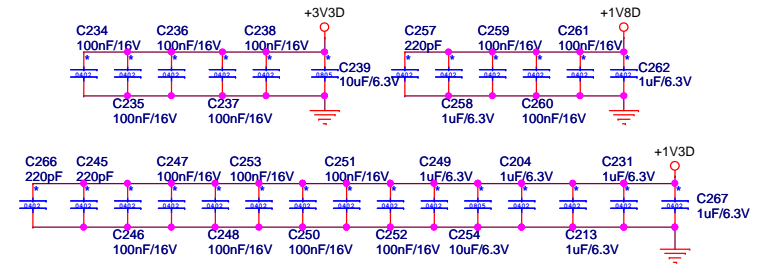
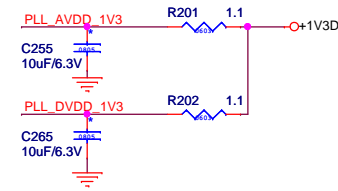
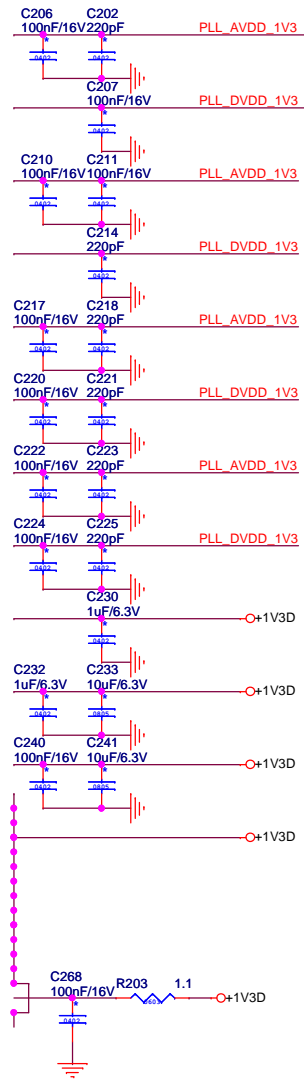
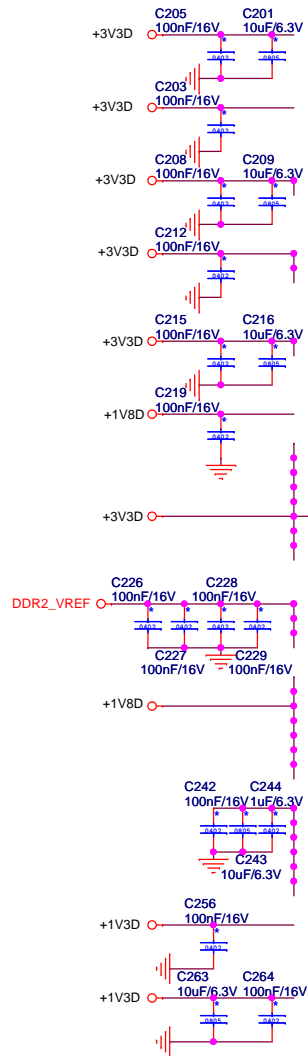
FRAMEWORK-SYSTEM




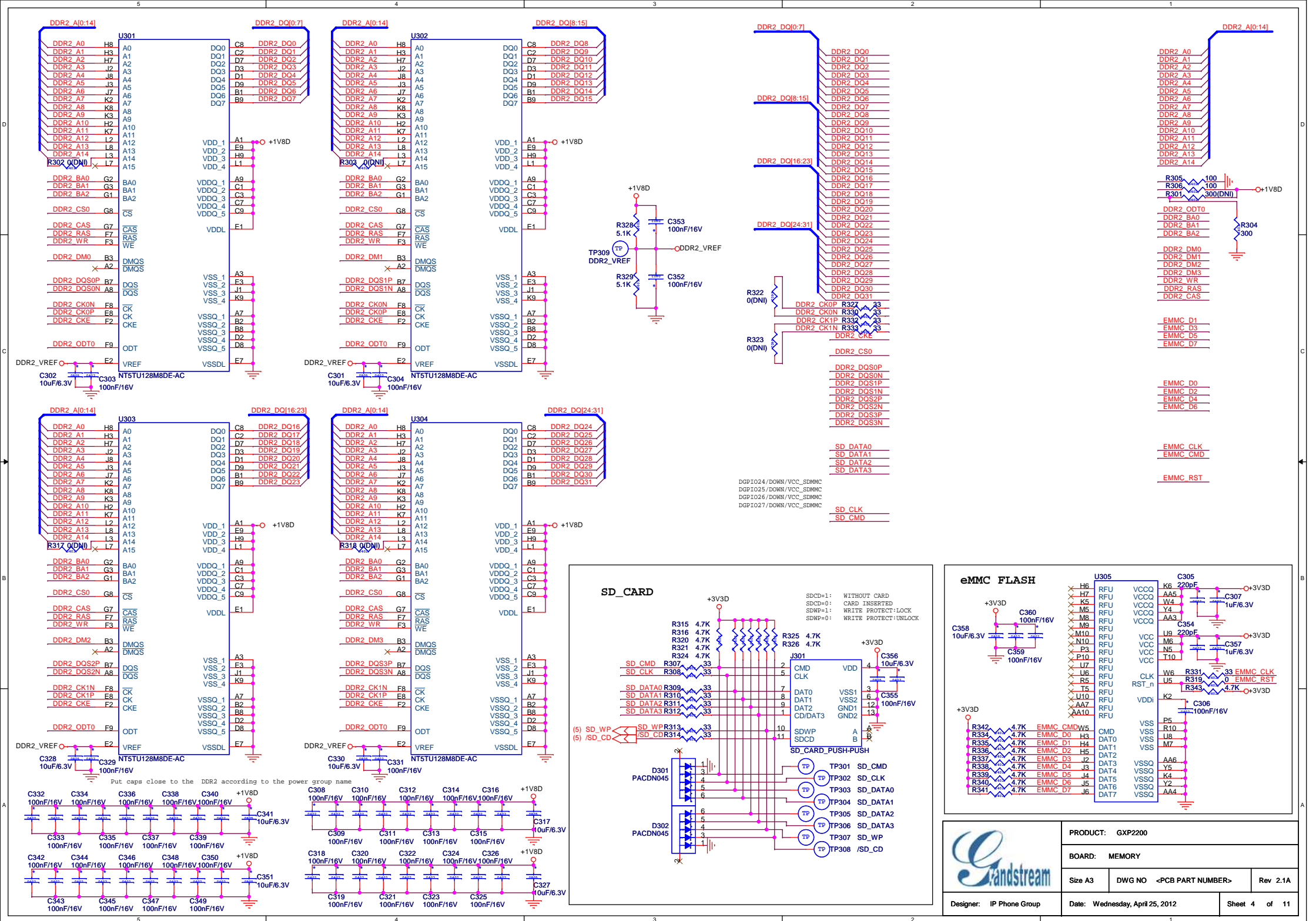
	PRODUCT: GXP2200		
	BOARD: FRAMEWORK		
	Size B	DWG NO <PCB PART NUMBER>	Rev 2.1A
	Designer: IP Phone Group	Date: Wednesday, April 25, 2012	Sheet 1 of 11

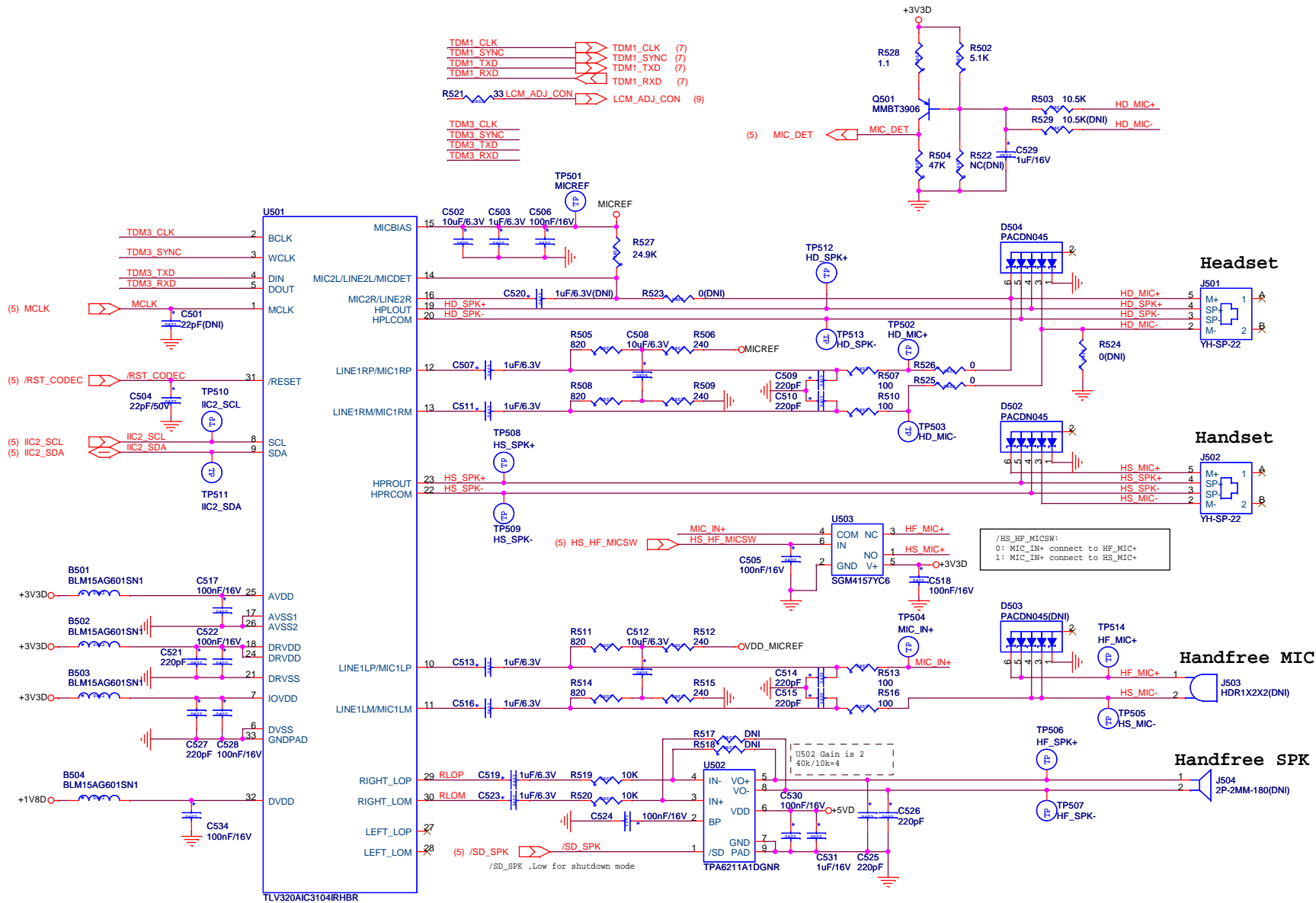


	PRODUCT: GXP2200		
	BOARD: POWER		
	Size B	DWG NO <PCB PART NUMBER>	Rev 2.1A
Designer: IP Phone Group	Date: Wednesday, April 25, 2012		Sheet 2 of 11

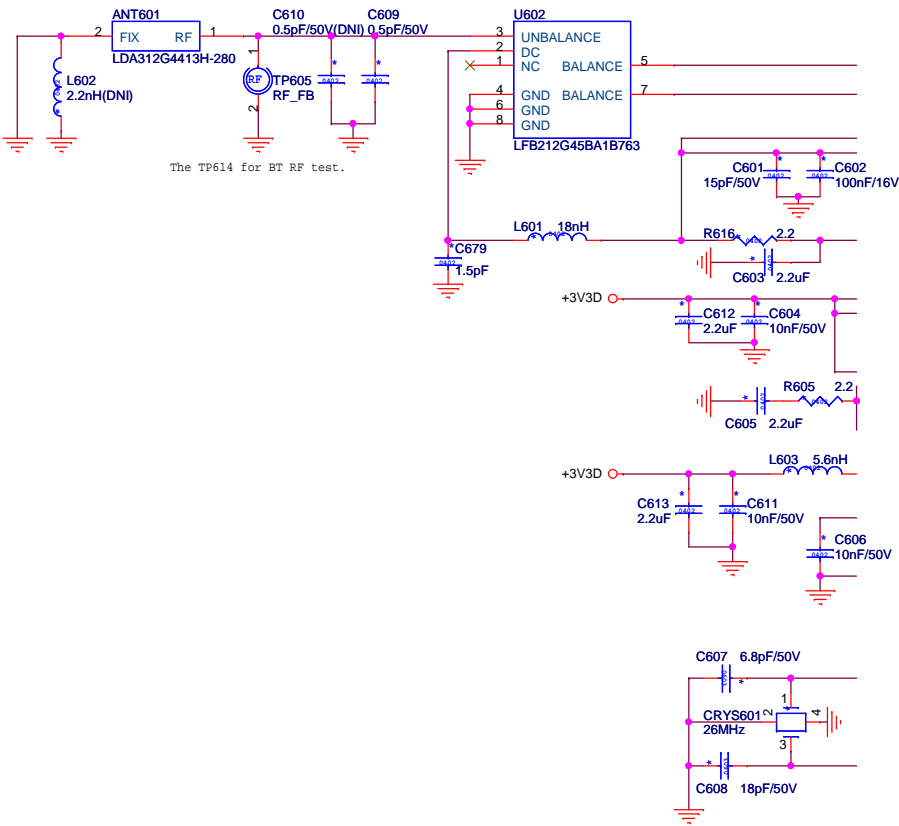


	PRODUCT: GXP2200		
	BOARD:		
	Size B	DWG NO <PCB PART NUMBER>	Rev 2.1A
	Designer: IP Phone Group	Date: Wednesday, April 25, 2012	Sheet 3 of 11



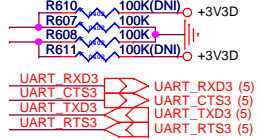
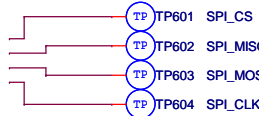


Bluetooth



R609 100K

■ PIO[4] = pulled low: UART mode is selected (Casira default setting).
■ PIO[4] = driven high: SDIO or CSPI host interface is selected.



CLK	CMD	UART Protocol
0	0	BCSP
0	1	H4
1	0	H4DS
1	1	H5

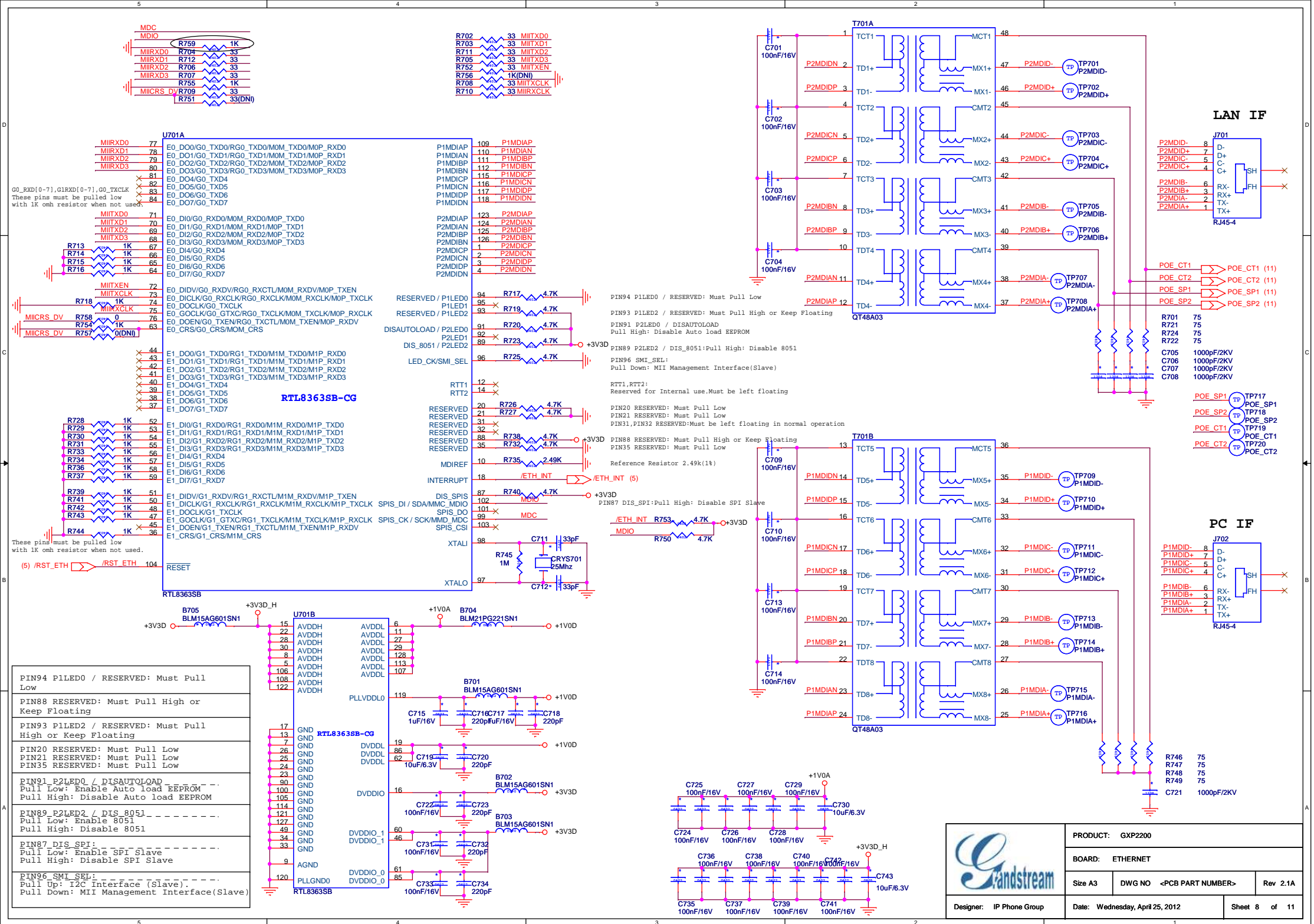


Reset if low. Input debounced so must be low for > 5ms to cause a reset

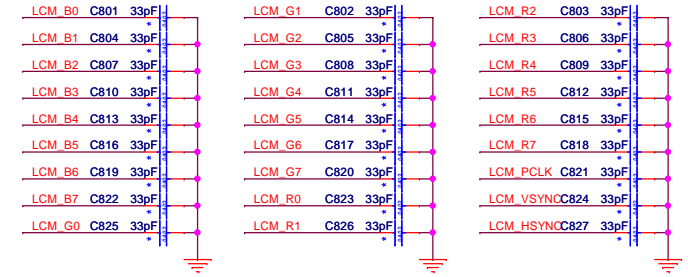
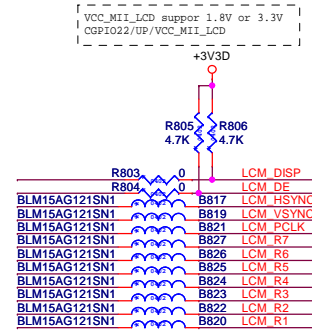
■ To select BCSP, connect 100kΩ pull-downs to both SDIO_CLK and SDIO_CMD.



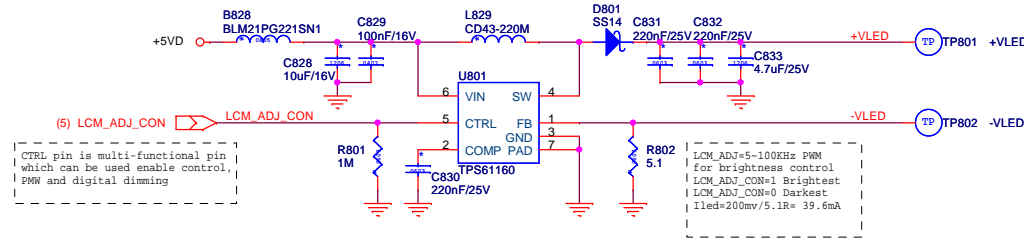
PRODUCT: GXP2200			
BOARD: BLUETOOTH			
Size B	DWG NO	<PCB PART NUMBER>	Rev 2.1A
Designer: IP Phone Group	Date: Wednesday, April 25, 2012		Sheet 7 of 11



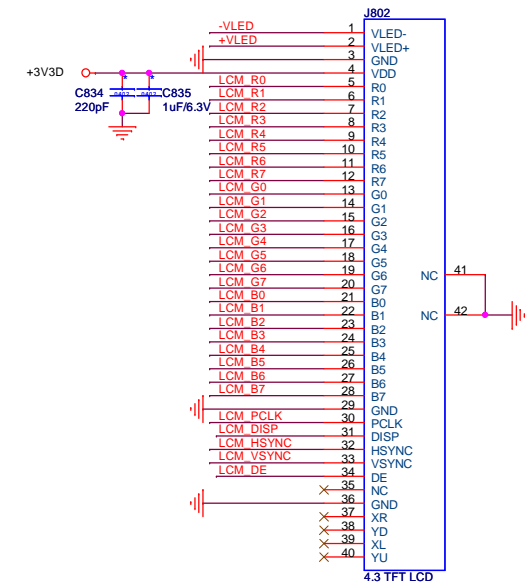
LCM_B0	B801	BLM15AG121SN1
LCM_B1	B802	BLM15AG121SN1
LCM_B2	B803	BLM15AG121SN1
LCM_B3	B804	BLM15AG121SN1
LCM_B4	B805	BLM15AG121SN1
LCM_B5	B806	BLM15AG121SN1
LCM_B6	B807	BLM15AG121SN1
LCM_B7	B808	BLM15AG121SN1
LCM_G0	B809	BLM15AG121SN1
LCM_G1	B810	BLM15AG121SN1
LCM_G2	B811	BLM15AG121SN1
LCM_G3	B812	BLM15AG121SN1
LCM_G4	B813	BLM15AG121SN1
LCM_G5	B814	BLM15AG121SN1
LCM_G6	B815	BLM15AG121SN1
LCM_G7	B816	BLM15AG121SN1
LCM_R0	B818	BLM15AG121SN1



BACKLIGHT



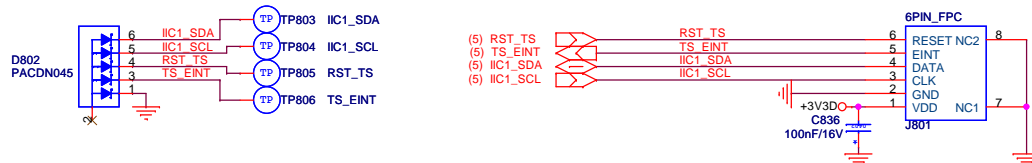
4.3" TFT Digital LCD Interface



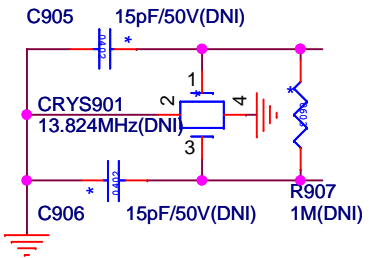
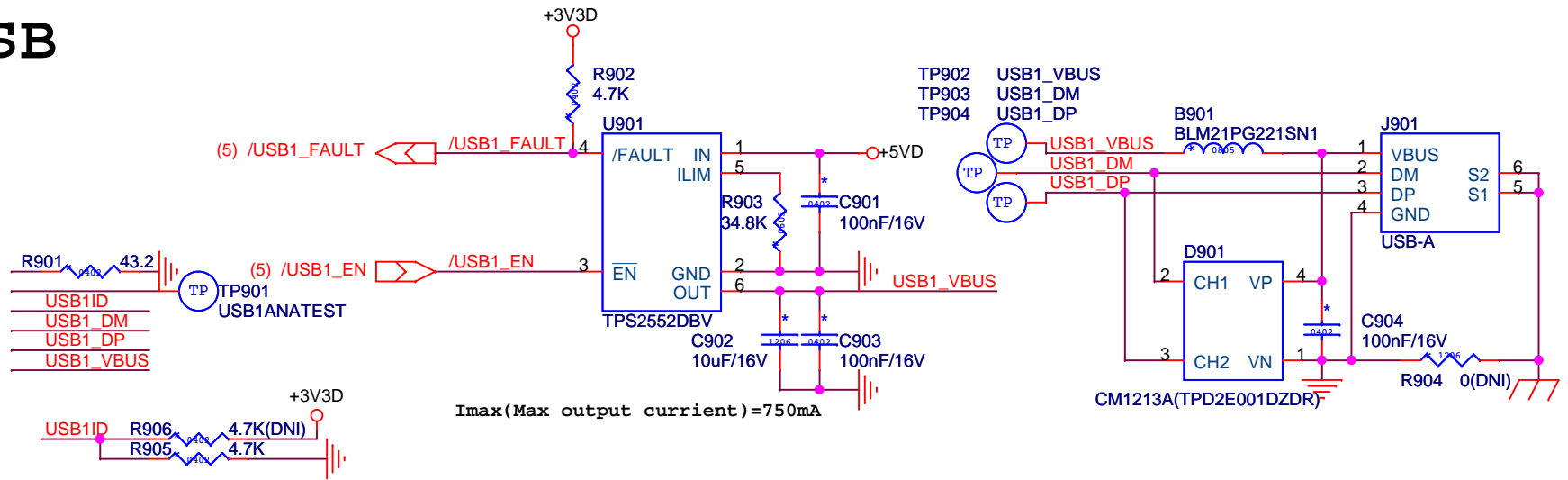
TOUCH PANEL(capacitance)

DISP:	Display on/off signal.(this pin is pulled high internally)
DE:	Input data enable control.internally pulled low.
PCLK:	Clock signal to sample each data.
HSYNC:	Horizontal synchronizing signal.
VSNC:	Vertical synchronizing signal.

Touch Screen Controller



HOST USB



UCFG1 (5)
UCFG2 (5)
UCFG3 (5)
UCFG0 (5)



PRODUCT: GXP2200

BOARD: USB

Size A

DWG NO <PCB PART NUMBER>

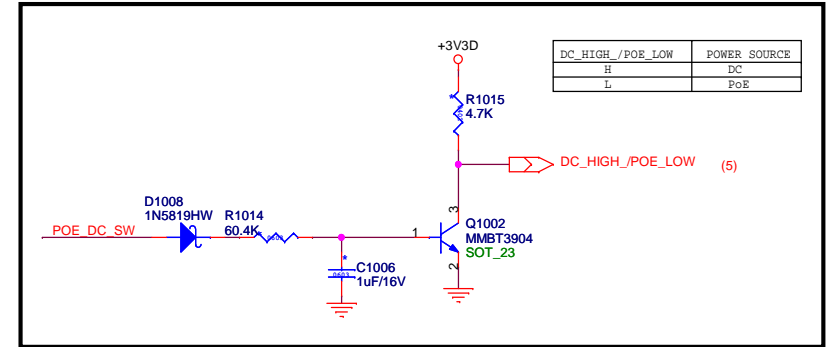
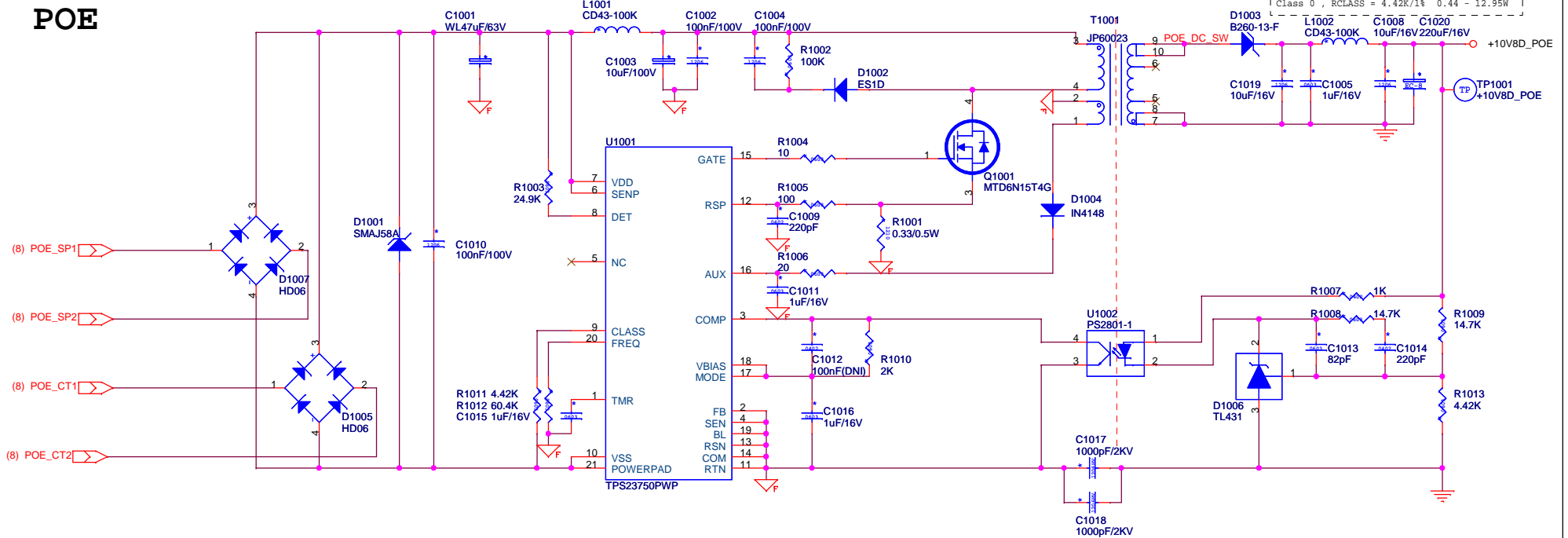
Rev 2.1A

Designer: IP Phone Group

Date: Wednesday, April 25, 2012

Sheet 10 of 11

POE



$$V_{out_poe} = 2.5 * (1 + R1009/R1013) = 10.8V$$

$$Class 0, R_{CLASS} = 4.42K/1\Omega \quad 0.44 - 12.95W$$



PRODUCT: GXP2200			
BOARD: POE			
Size B	DWG NO	<PCB PART NUMBER>	Rev 2.1A
Designer: IP Phone Group		Date: Wednesday, April 25, 2012	Sheet 11 of 11