WL1835MODCOM8A WLAN MIMO and BT Module Evaluation Board for TI Sitara™ Platform

User's Guide



Literature Number: SWRU359A September 2013–Revised October 2013



Contents

Prefac	e		3
1		etion	
	1.1	Features	
	1.2	Applications	5
	1.3	TI Module Key Benefits	
2	Board P	in Assignment	6
	2.1	Pin Descriptions	7
3	Electrica	al Characteristics	
4	Antenna	Characteristics	9
	4.1	VSWR	9
	4.2	Efficiency	10
5	Antenna	Characteristics	
	5.1	Radio Pattern	10
6	Circuit [Design	14
	6.1	Schematic	14
	6.2	Bill of Materials (BOM)	15
7	Layout (Guidelines	
	7.1	Board Layout	



Read This First

About This Manual

This user's guide describes how to use the TI WL1835MODCOM8A board to evaluate the performance of the TI WL1835MODGA module.

Related Documentation From Texas Instruments

- TI WiLink8 Single-Band Combo Module Wi-Fi, BT, and BLE (SWRS152)
- WiLink 8 Wiki: http://www.ti.com/wilink8wiki

If You Need Assistance

The primary sources of WL1835MODGA information are the device-specific data sheets and user's guides. For the most up-to-date version of the user's guide and data sheets, go to http://www.ti.com/product/wl1835mod.

Warning

The WL1835MODCOM8A board is tested to comply with ETSI/R&TTE over temperatures from 0 to +70°C. The WL1835MODCOM8A board is FCC and IC certified.

This board should not be modified to operate in other frequency bands other than what they are designed for.

FCC/IC Regulatory compliance (WL1835MODCOM8A board only)

FCC Part 15 Class A Compliant

IC ICES-003 Class A Compliant



WL1835MODCOM8A WLAN MIMO and BT Module Evaluation Board for TI Sitara™ Platform

1 Introduction

The WL1835MODCOM8A device is a WiFi® MIMO, *Bluetooth*®, and *Bluetooth* Low Energy (BLE) module board with the TI WL1835MODGA module. WL1835MODGA is built-in TI WL1835 IEEE 802.11 b/g/n and *Bluetooth* 4.0 solutions to provide the best WiFi and *Bluetooth* coexistence interoperability and power-saving technologies from TI.



Figure 1. WL1835MODCOM8A Top View

1.1 Features

- WLAN, Bluetooth, BLE on a module board
- 100-pin board card
- Dimension 76.0 mm(L) x 31.0 mm(W)
- WLAN 2.4 GHz SISO (20- and 40-MHz channels), 2.4-GHz MIMO (20-MHz channels)
- Support for BLE dual mode
- · Seamless integration with TI Sitara and other application processors
- Design for TI AM335X general-purpose EVM
- WLAN and *Bluetooth*, BLE cores are software and hardware compatible with prior WL127x, WL128x and CC256x offerings, for smooth migration to device.
- Shared HCI transport for Bluetooth and BLE over UART and SDIO for WLAN.
- WiFi / Bluetooth single antenna co-existence
- · Built-in chip antenna
- Optional U.FL RF connector for external 2.4-GHz band antenna
- Direct connection to battery using external switching mode power supply supporting 4.8-V to 2.9-V operation
- VIO in the 1.8-V domain



www.ti.com Introduction

1.2 Applications

- Internet of Things Multimedia
- · Home Electronics
- Home Appliances and White Goods
- Industrial and Home Automation
- · Smart Gateway and Metering
- Video Conferencing
- Video Camera and Security

1.3 TI Module Key Benefits

- Reduces Design Overhead: Single WiLink8™ Module Scales Across Wi-Fi and Bluetooth.
- WLAN High Throughput: 80 Mbps (TCP), 100 Mbps (UDP)
- Bluetooth 4.0 + BLE (Smart Ready)
- WiFi-Bluetooth Single Antenna Coexistence
- Low Power (30–50% Less than Previous Generation)
- Available as Easy-to-Use FCC, ETSI, and Telec Certified Module
- Lower Manufacturing Costs, Saving Board Space and Minimizing RF Expertise
- AM335x Linux® and Android™ Reference Platform Accelerates Customer Development and Time to Market



Board Pin Assignment www.ti.com

2 **Board Pin Assignment**

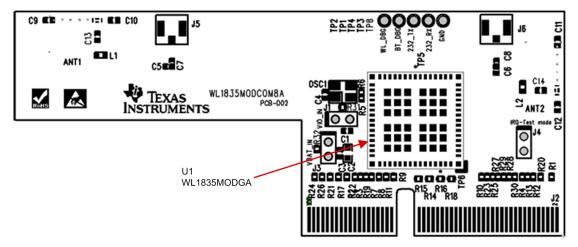


Figure 2. Board Top View

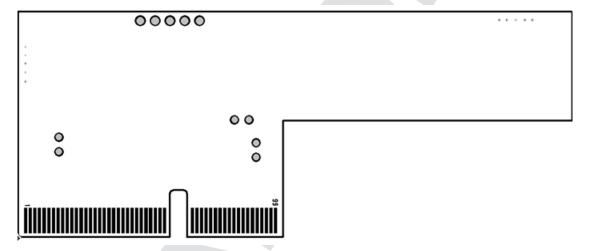


Figure 3. Board Bottom View



2.1 Pin Descriptions

No.	Name	Туре	Description	
1	SLOW_CLK	I	Slow clock input	
2	GND	G	Ground	
3	GND	G	Ground	
4	WL_EN	ı	WLAN Enable	
5	VBAT	Р	Power supply input	
6	GND	G	Ground	
7	VBAT	Р	Power supply input	
8	VIO	Р	Power supply input for I/O pin	
9	GND	G	Ground	
10	N.C.		No connection	
11	WL_RS232_TX	0	WLAN tool RS232 output	
12	N.C.		No connection	
13	WL_RS232_RX	I	WLAN tool RS232 input	
14	N.C.		No connection	
15	WL_UART_DBG	0	WLAN Logger output	
16	N.C.		No connection	
17	N.C.		No connection	
18	GND	G	Ground	
19	GND	G	Ground	
20	SDIO_CLK	1	WLAN SDIO clock	
21	N.C.		No connection	
22	GND	G	Ground	
23	N.C.		No connection	
24	SDIO_CMD	I/O	WLAN SDIO command	
25	N.C.		No connection	
26	SDIO_D0	I/O	WLAN SDIO data bit 0	
27	N.C.	7	No connection	
28	SDIO_D1	I/O	WLAN SDIO data bit 1	
29	N.C.		No connection	
30	SDIO_D2	I/O	WLAN SDIO data bit 2	
31	N.C.		No connection	
32	SDIO_D3	I/O	WLAN SDIO data bit 3	
33	N.C.		No connection	
34	WLAN_IRQ	0	WLAN SDIO interrupt out	
35	N.C.		No connection	
36	N.C.		No connection	
37	GND	G	Ground	
38	N.C.		No connection	
39	N.C.		No connection	
40	N.C.		No connection	
41	N.C.		No connection	
42	GND	G	Ground	
43	N.C.		No connection	
44	N.C.		No connection	
45	N.C.		No connection	
46	N.C.		No connection	
47	GND	G	Ground	



Board Pin Assignment www.ti.com

No.	Name	Type	Description
48	N.C.		No connection
49	N.C.		No connection
50	N.C.		No connection
51	N.C.		No connection
52	PCM_IF_CLK	I/O	Bluetooth PCM clock input or output
53	N.C.		No connection
54	PCM_IF_FSYNC	I/O	Bluetooth PCM frame sync input or output
55	N.C.		No connection
56	PCM_IF_DIN	I	Bluetooth PCM data input
57	N.C.		No connection
58	PCM_IF_DOUT	0	Bluetooth PCM data output
59	N.C.		No connection
60	GND	G	Ground
61	N.C.		No connection
62	N.C.		No connection
63	GND	G	Ground
64	GND	G	Ground
65	N.C.		No connection
66	BT_UART_IF_TX	0	Bluetooth HCI UART transmit output
67	N.C.		No connection
68	BT_UART_IF_RX	1	Bluetooth HCI UART receive input
69	N.C.	1	No connection
70		1	
71	BT_UART_IF_CTS N.C.	1	Bluetooth HCI UART Clear to Send input
72		0	No connection
73	BT_UART_IF_RTS N.C.	U	Bluetooth HCI UART Request to Send output
74	BT_FUNC1	0	No connection BT_HOST_WAKE_UP Signal to wake up the host from <i>Bluetooth</i>
75	N.C.		No connection
		0	Bluetooth Logger UART output
76	BT_UART_DEBUG GND	G	
77	GPIO9	I/O	Ground
78		1/0	General-purpose I/O
79	N.C.		No connection
80	N.C.	4	No connection
81	N.C.		No connection
82	N.C.		No connection
83	GND	G	Ground
84	N.C.		No connection
85	N.C.		No connection
86	N.C.		No connection
87	GND	G	Ground
88	N.C.		No connection
89	BT_EN	I	Bluetooth Enable
90	N.C.		No connection
91	N.C.		No connection
92	GND	G	Ground
93	BT_FUNC2	I	BT_WAKE_UP Bluetooth wakeup from host
94	N.C.		No connection
95	GND	G	Ground
96	GPIO11	I/O	General-purpose I/O



www.ti.com Electrical Characteristics

No.	Name	Туре	Description
97	GND	G	Ground
98	GPIO12	I/O	General-purpose I/O
99	N.C.		General-purpose I/O
100	GPIO10	I/O	General-purpose I/O

3 Electrical Characteristics

Refer to the detailed data in the WL1835MODGA data sheet for electrical characteristics.

4 Antenna Characteristics

4.1 VSWR

Figure 4 shows the antenna VSWR.

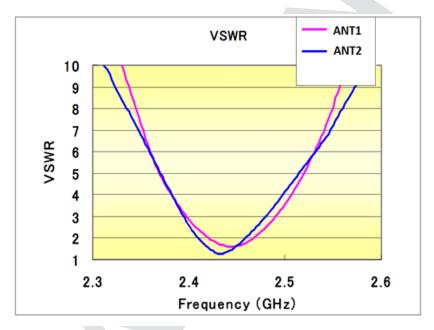


Figure 4. Antenna VSWR



Antenna Characteristics www.ti.com

4.2 **Efficiency**

Figure 5 shows the antenna efficiency.

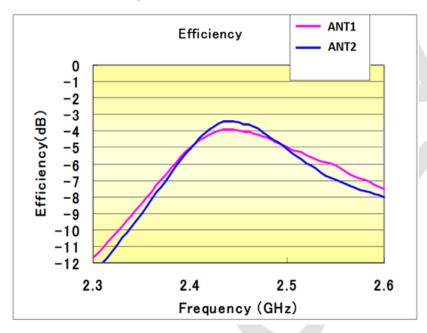


Figure 5. Antenna Efficiency

5 **Antenna Characteristics**

5.1 Radio Pattern

Figure 6 shows the radio pattern of the WL1835MODCOM8A device.

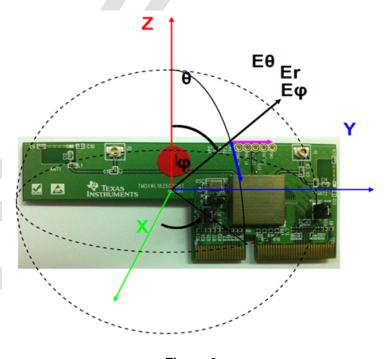


Figure 6.



www.ti.com Antenna Characteristics

5.1.1 ANT1

Figure 7 shows the ANT1 polarization of the WL1835MODCOM8A device.

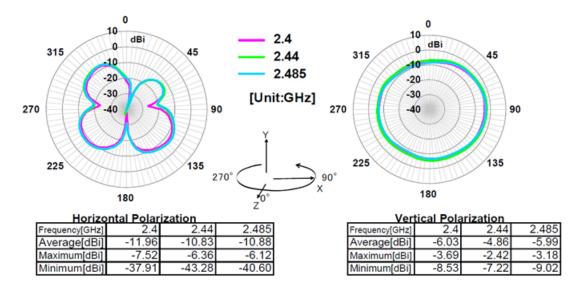


Figure 7.

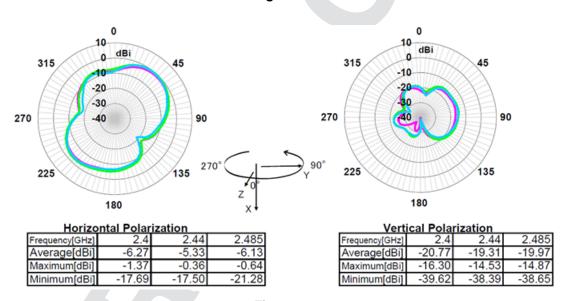


Figure 8.



Antenna Characteristics www.ti.com

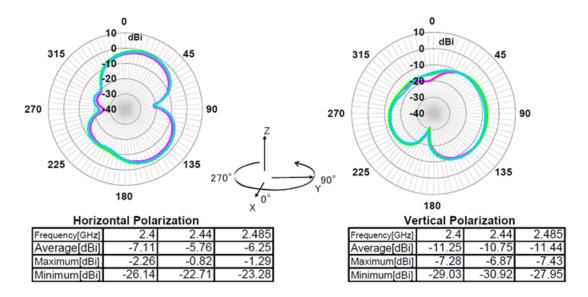


Figure 9.

ANT2 5.1.2

Figure 10 shows the ANT2 polarization of the WL1835MODCOM8A device.

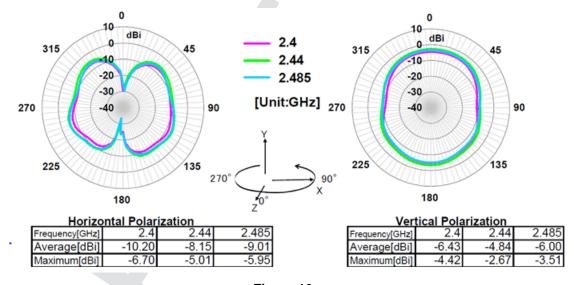


Figure 10.



www.ti.com Antenna Characteristics

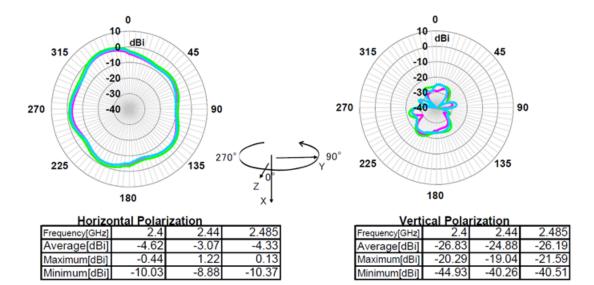


Figure 11.

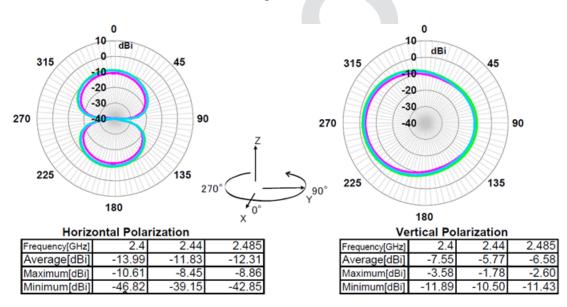


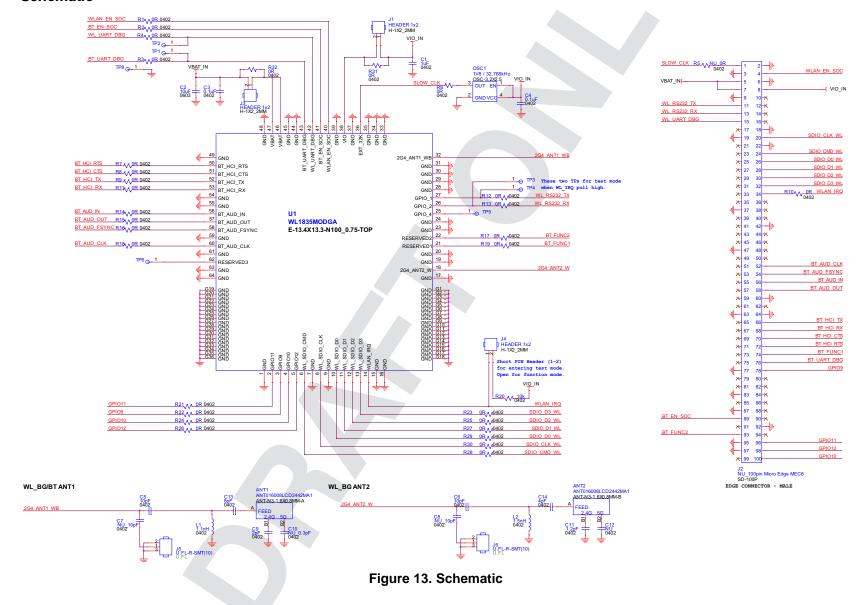
Figure 12.



Circuit Design www.ti.com

6 Circuit Design

6.1 Schematic



¹⁴ WL1835MODCOM8A WLAN MIMO and BT Module Evaluation Board for TI Sitara™ Platform



www.ti.com Circuit Design

6.2 Bill of Materials (BOM)

Table 1 lists the bill of materials.

Table 1. BOM

1	TI WL1835 WiFi/Bluetooth Module	WL1835MODGA	U1
2	XOSC 3225 / 32.768 kHz / 1.8 V / ±50 ppm	7XZ3200005	OSC1
3	ANT / Chip / 2.4 GHz, 5 GHz / Peak Gain >5 dBi	ANT016008LCD2442MA1	ANT1, ANT2
4	CON Male 1x2 / Pitch	P301-SGP-040/028-02	J1, J3, J4
5	DC JUMPER / PITCH 2.0 mm	CMJ-20BB	J1, J3
6	Mini RF Header Receptacle	U.FL-R-SMT-1(10)	J5, J6
7	IND 0402 / 1.1 nH / ±0.05 nH / SMD	LQP15MN1N1W02	L1
8	IND 0402 / 1.5 nH / ±0.05 nH / SMD	LQP15MN1N5W02	L2
9	CAP 0402 / 1.2 pF / 50 V / C0G / ±0.1 pF	GJM1555C1H1R2BB01	C11
10	CAP 0402 / 2.2 pF / 50 V / C0G / ±0.1 pF	GJM1555C1H2R2BB01	C9
11	CAP 0402 / 4 pF / 50 V / C0G / ±0.1 pF	GJM1555C1H4R0BB01	C14
12	CAP 0402 / 8 pF / 50 V / C0G / ±0.1 pF	GJM1555C1H8R0BB01	C13
13	CAP 0402 / 10 pF / 50 V / NPO / ±5%	0402N100J500LT	C7, C8
14	CAP 0402 / 0.1 µF / 6.3 V / X7R / ±10%	0402B104K100CT	C3, C4
15	CAP 0402 / 1 µF / 6.3 V / X5R / ±10% / HF	GRM155R60J105KE19D	C1
16	CAP 0603 / 10 μF / 6.3 V / X5R / ±20%	C1608X5R0J106M	C2
17	RES 0402 / 0R / ±5%	WR04X000 PTL	R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, R21, R22, R23, R24, R25, R26, R27, R28, R29, R30, R31, R32
18	RES 0402 / 10K / ±5%	WR04X103 JTL	R20



Layout Guidelines www.ti.com

7 **Layout Guidelines**

Board Layout 7.1

Figure 14 shows the WL1835MODCOM8A 4-layer board. Table 2, Figure 15, Figure 16, Figure 17, Figure 18, and Figure 19 show instances of good layout practices.

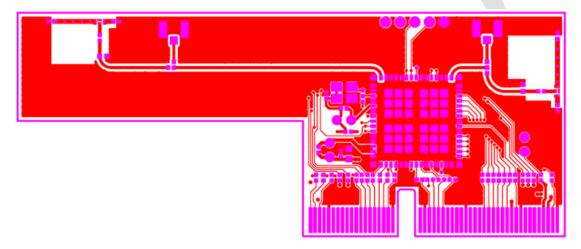


Figure 14. Layer 1

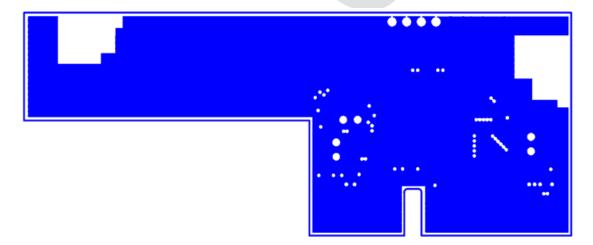


Figure 15. Layer 2



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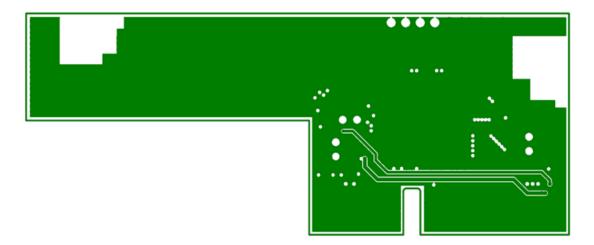


Figure 16. Layer 3

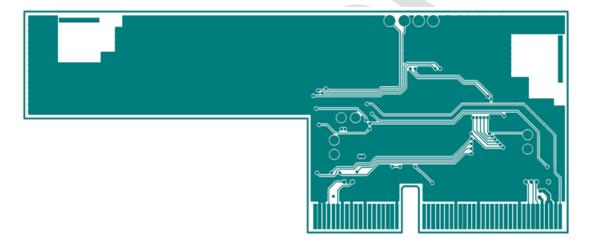


Figure 17. Layer 4

Table 2. Module Layout Guidelines

Reference	Guideline Description				
1	The proximity of ground vias must be close to the pad.				
2	Signal traces must not be run underneath the module on the layer where the module is mounted.				
3	Have a complete ground pour in layer 2 for thermal dissipation.				
4	Have a solid ground plane and ground vias under the module for stable system and thermal dissipation.				
5	Increase the ground pour in the first layer and have all of the traces from the first layer on the inner layers, if possible.				
6	Signal traces can be run on a third layer under the solid ground layer, which is below the module mounting layer.				



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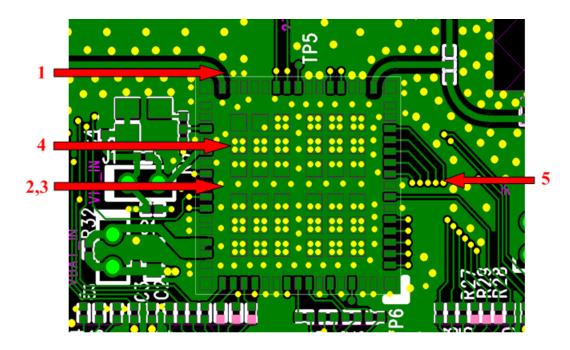


Figure 18. Module Layout Guidelines (Top Layer)

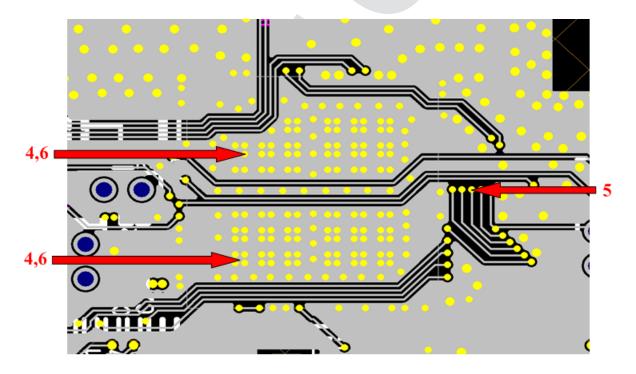


Figure 19. Module Layout Guidelines (Bottom Layer)

Figure 20 shows the trace design for the PCB. A $50-\Omega$ impedance match on the trace to the antenna should be used. Also, $50-\Omega$ traces are recommended for the PCB layout.



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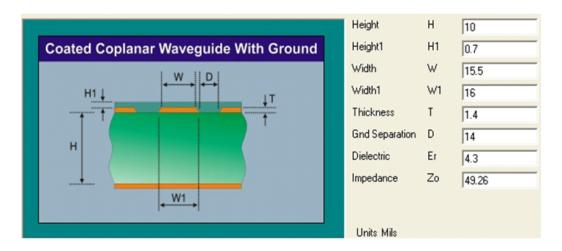


Figure 20. Trace Design for the PCB Layout

Figure 21 shows layer 1 with the trace to the antenna over ground layer 2.

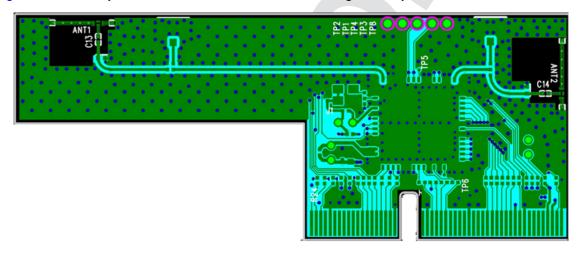


Figure 21. Layer 1 Combined With Layer 2

Table 3, Figure 22, and Figure 23 describe instances of good layout practices for the antenna and RF trace routing.

Table 3. Antenna and RF Trace Routing Layout Guidelines

Reference	Guideline Description				
1	The RF trace antenna feed must be as short as possible beyond the ground reference. At this point, the trace starts to radiate.				
2	The RF trace bends must be gradual with an approximate maximum bend of 45 degrees with trace mitered. RF traces must not have sharp corners.				
3	RF traces must have via stitching on the ground plane beside the RF trace on both sides				
4	RF traces must have constant impedance (microstrip transmission line).				
5	For best results, the RF trace ground layer must be the ground layer immediately below the RF trace. The ground layer must be solid.				
6	There must be no traces or ground under the antenna section.				
7	RF traces must be as short as possible. The antenna, RF traces, and modules must be on the edge of the PCB product. The proximity of the antenna to the enclosure and the enclosure material must also be considered.				



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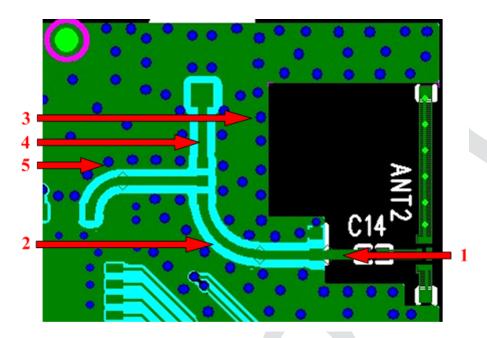


Figure 22. Top Layer - Antenna and RF Trace Routing Layout Guidelines

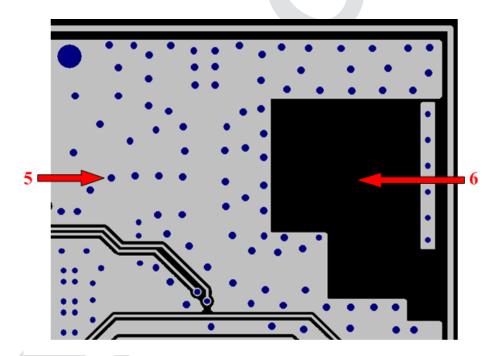


Figure 23. Bottom Layer – Antenna and RF Trace Routing Layout Guidelines



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Figure 24 describes the MIMO antenna spacing. The distance of ANT1 and ANT2 must be greater than half of wavelength (62.5 mm @ 2.4 GHz).

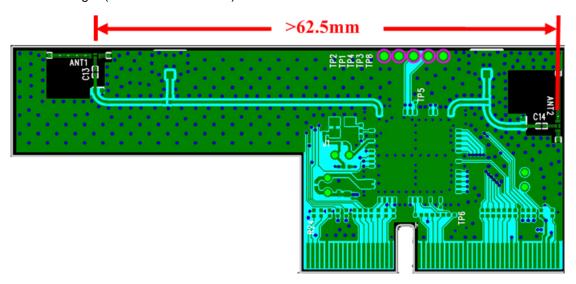


Figure 24. MIMO Antenna Spacing

The supply routing guidelines are as follows:

- For power supply routing, the power trace for V_{BAT} must be at least 40 mil wide.
- The 1.8-V trace must be at least 18 mil wide.
- Make V_{BAT} traces as wide as possible to ensure reduced inductance and trace resistance.
- If possible, shield V_{BAT} traces with ground above, below, and beside the traces.

The digital signals routing guidelines are as follows:

- SDIO signals traces (CLK, CMD, D0, D1, D2, and D3) should be routed in parallel to each other and
 as short as possible (less than 12 cm). In addition, every trace length must be the same as the others.
 There should be enough space between traces greater than 1.5 times the trace width or ground to
 ensure signal quality, especially for the SDIO_CLK trace. Remember to keep them away from the
 other digital or analog signal traces. TI recommends adding ground shielding around these buses.
- SDIO Clock, PCM clock... These digital clock signals are a source of noise. Keep the traces of these signals as short as possible. Whenever possible, maintain a clearance around them.



Revision History www.ti.com

This user's guide revision history highlights the technical changes made to the SWRU359 device-specific user's guide.

Revision History

Revision	Date	Description / Changes
SWRS359A	October 2013	Changed all references of the device name from WL1835MODCOM8 to WL1835MODCOM8A.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

