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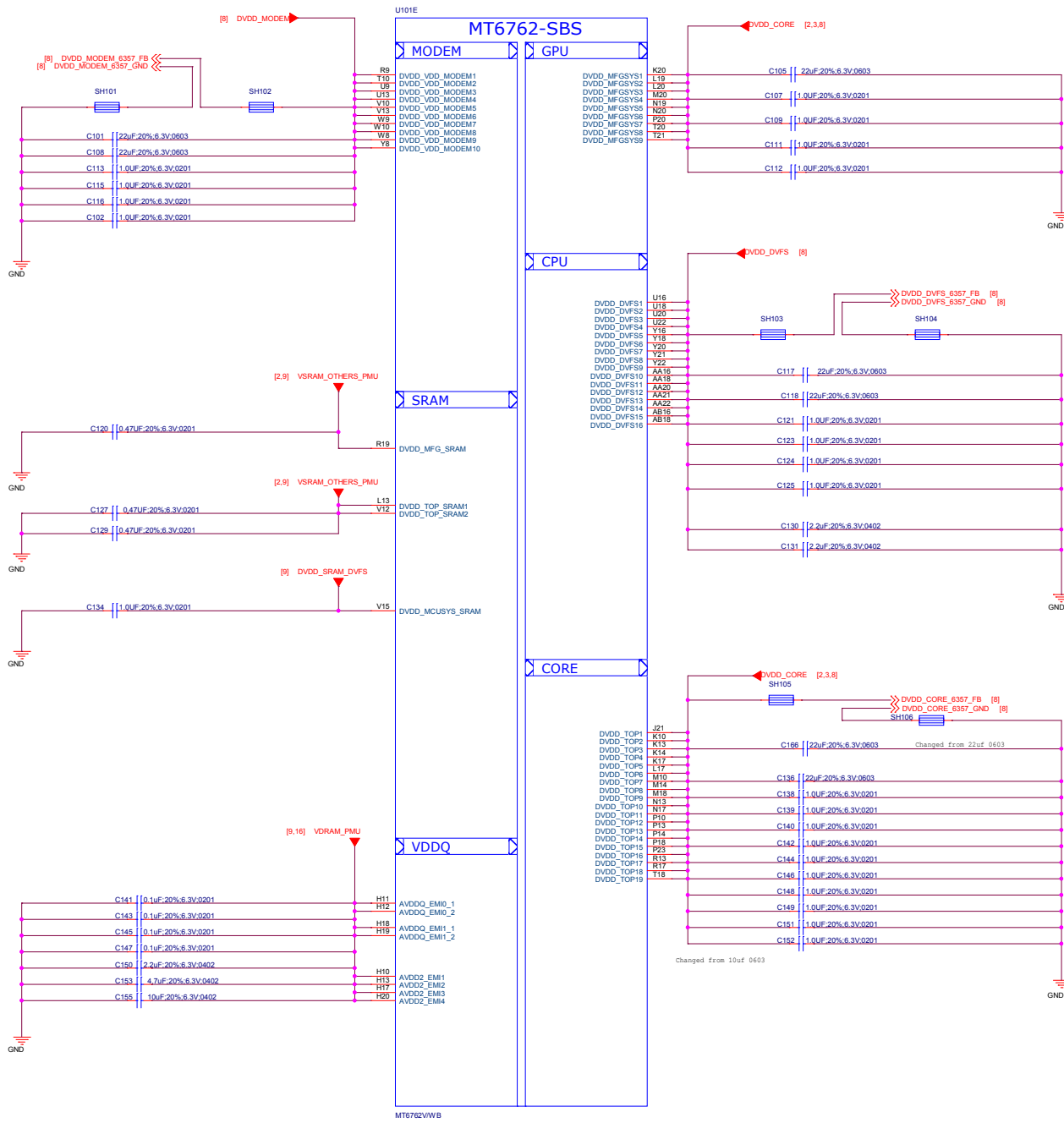
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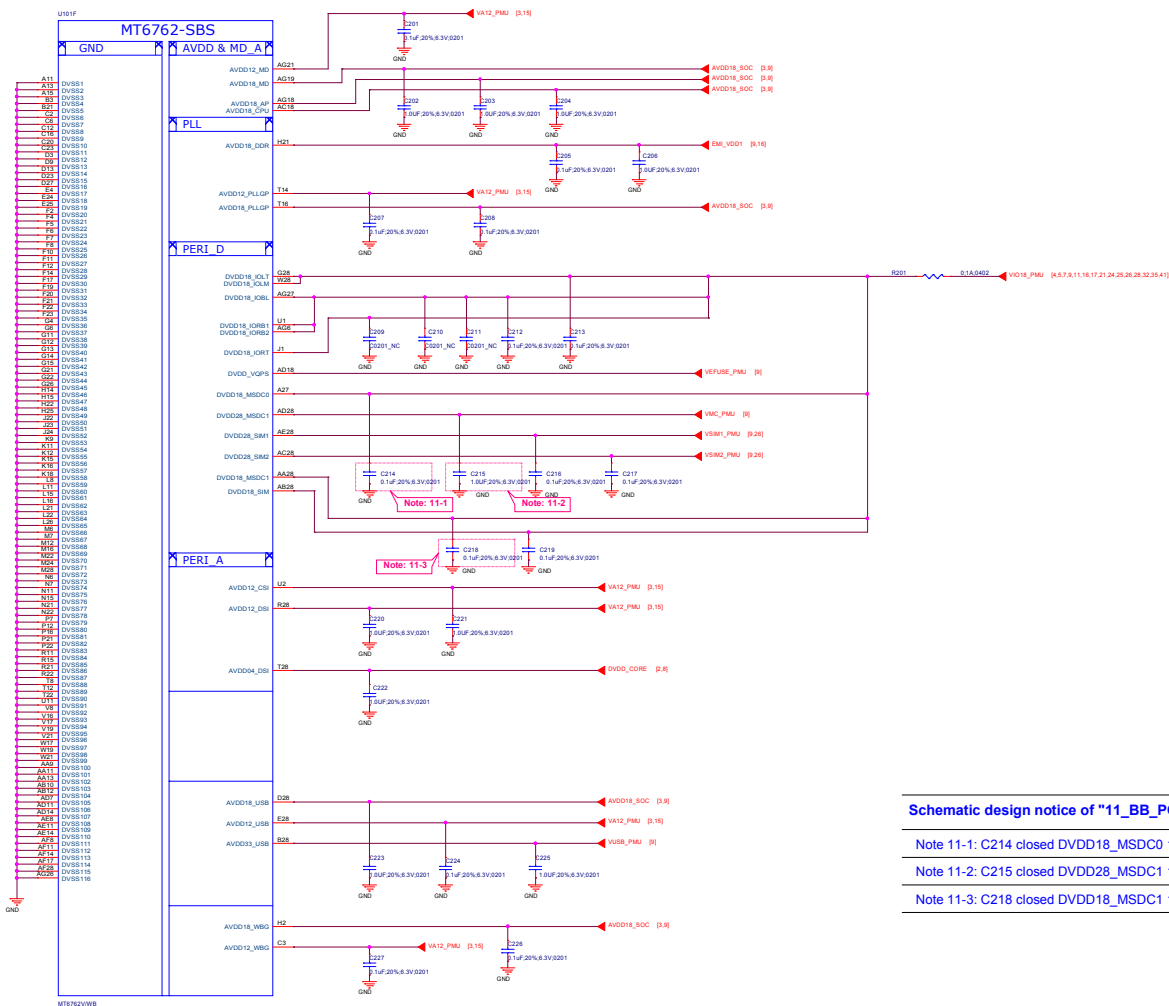
Revision History

D	REV	DATE	DESCRIPTION
	A1	20181203	Refer to MTK DVT1.1 Reference design
	A1	20181205	Change from K4 Sch 1. Change PA from 87318 to 87319 2.Change Charger IC from SM5414 to ETA6793 3.Change P-L sensor from STK3331 to Spring board STK3332 4. Delete LCM I2C switch 5. Delete USB switch 6.Delete KEY Pressed force download circuit 7.Change CAM I2C connection 8.Change BAT CONN
C			

B

A



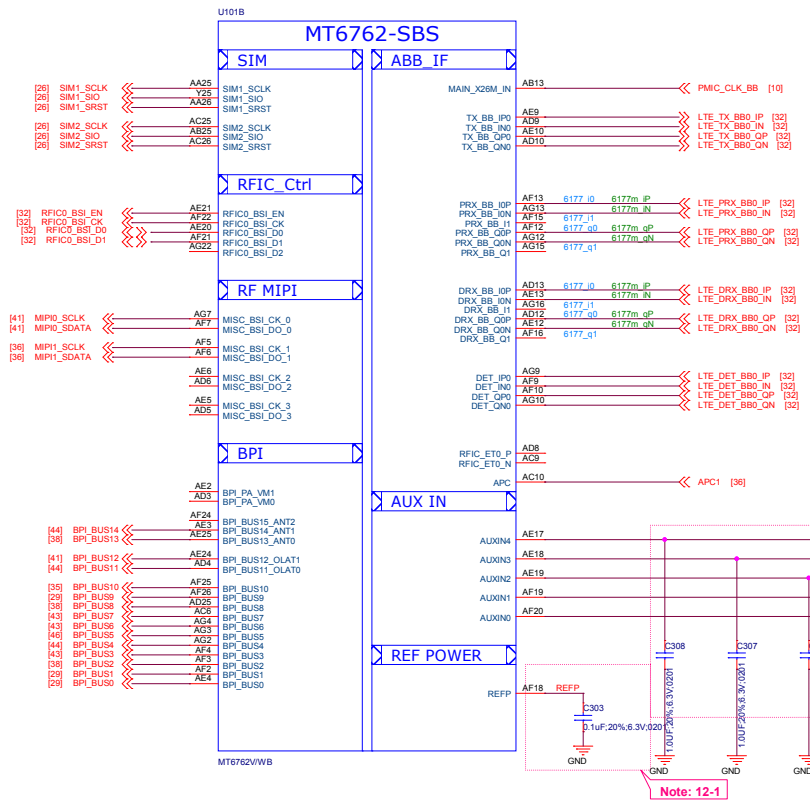
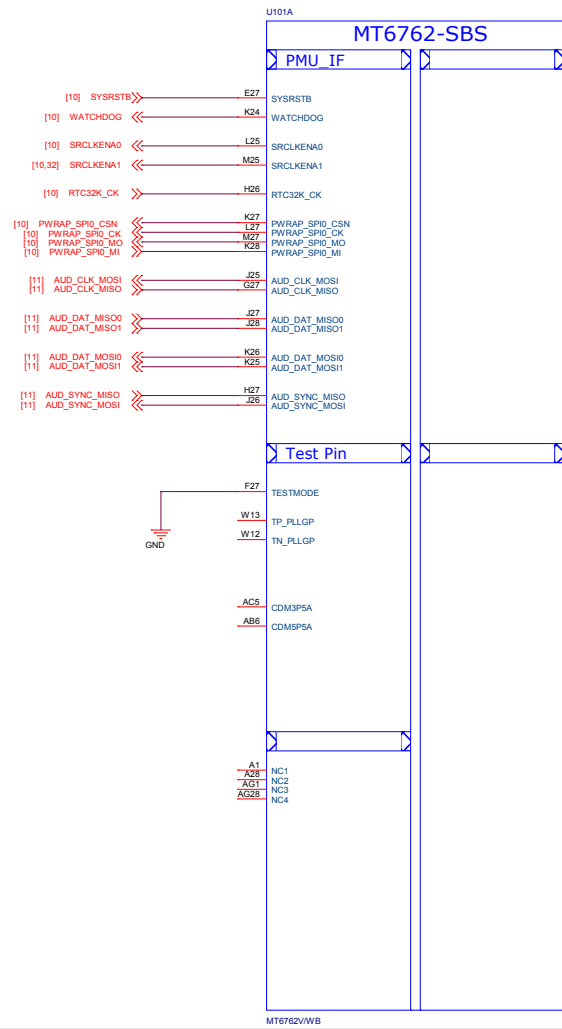


Schematic design notice of "11_BB_POWER_IO" page.

Note 11-1: C214 closed DVDD18_MSDC0 150mI

Note 11-2: C215 closed DVDD28_MSDC1 150mI

Note 11-3: C218 closed DVDD18_MSDC1 150mI



Note: 12-5

Note: 12-1

Note: 12-2

Schematic design notice of "12_BB_1" page.

Note 12-1: The de-coupling cap. for REFP (AF18 ball) have to be placed as close to BB as possible.

Note 12-2: To shunt a 1uF capacitor in the AUXIN ADC input to prevent noise coupling. It should be placed as close to BB as possible. Connect the unused AUX ADC input to GND.

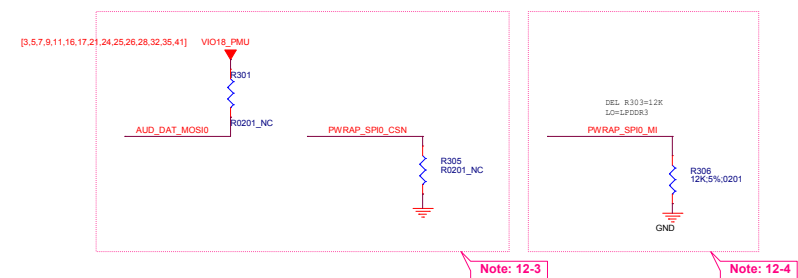
Note 12-3: "PWRAP_SPI0_CSN" and "AUD_DAT_MOSI0" are bootstrap pin to select which interface will be the JTAG pin out.

PWRAP_SPI0_CSN	AUD_DAT_MOSI0	JTAG Function	
default=PU	default=PD	AP_JTAG	MD_JTAG
HI	LO	N/A	N/A
HI	HI (by ext. PU)	SPI0+EINT8	SPI1+SPI3
LO (by ext. PD)	LO	SPI0+EINT8	N/A
LO (by ext. PD)	HI (by ext. PU)	MSDC1	N/A

Note 12-4: PWRAP_SPI0_MI is DDR type feature in bootstrap

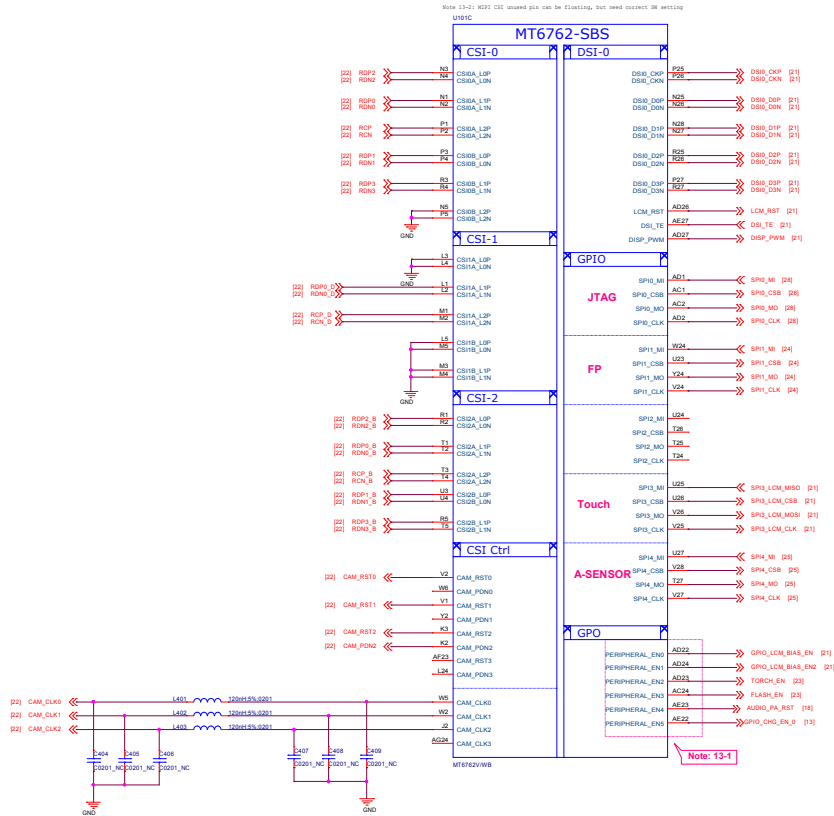
PWRAP_SPI0_MI	Booting interface
default=PU	DDR
LO (by ext. PD)	LPDDR3 follow LP3 Ref SCH.
HI	LPDDR4X follow LP4X Ref SCH.

Note 12-5: Please set unused IQ pins in NC



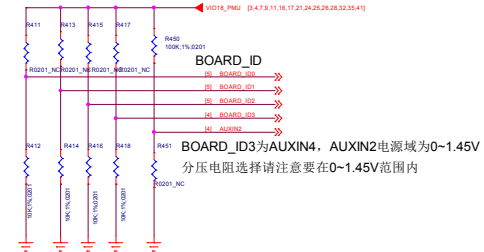
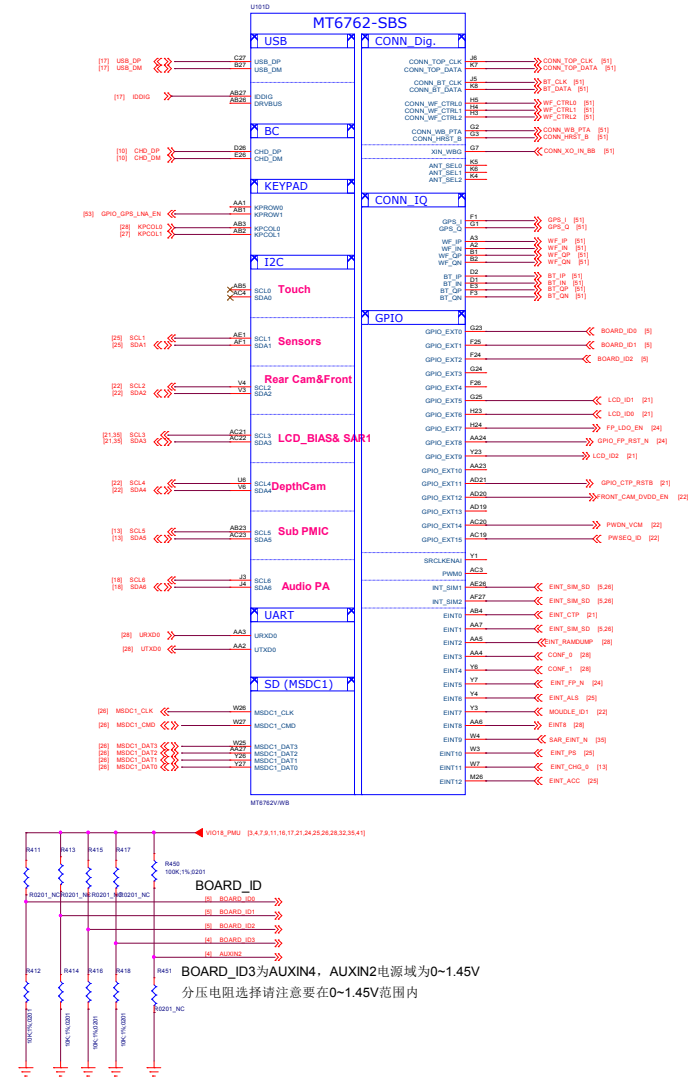
Note: 12-3

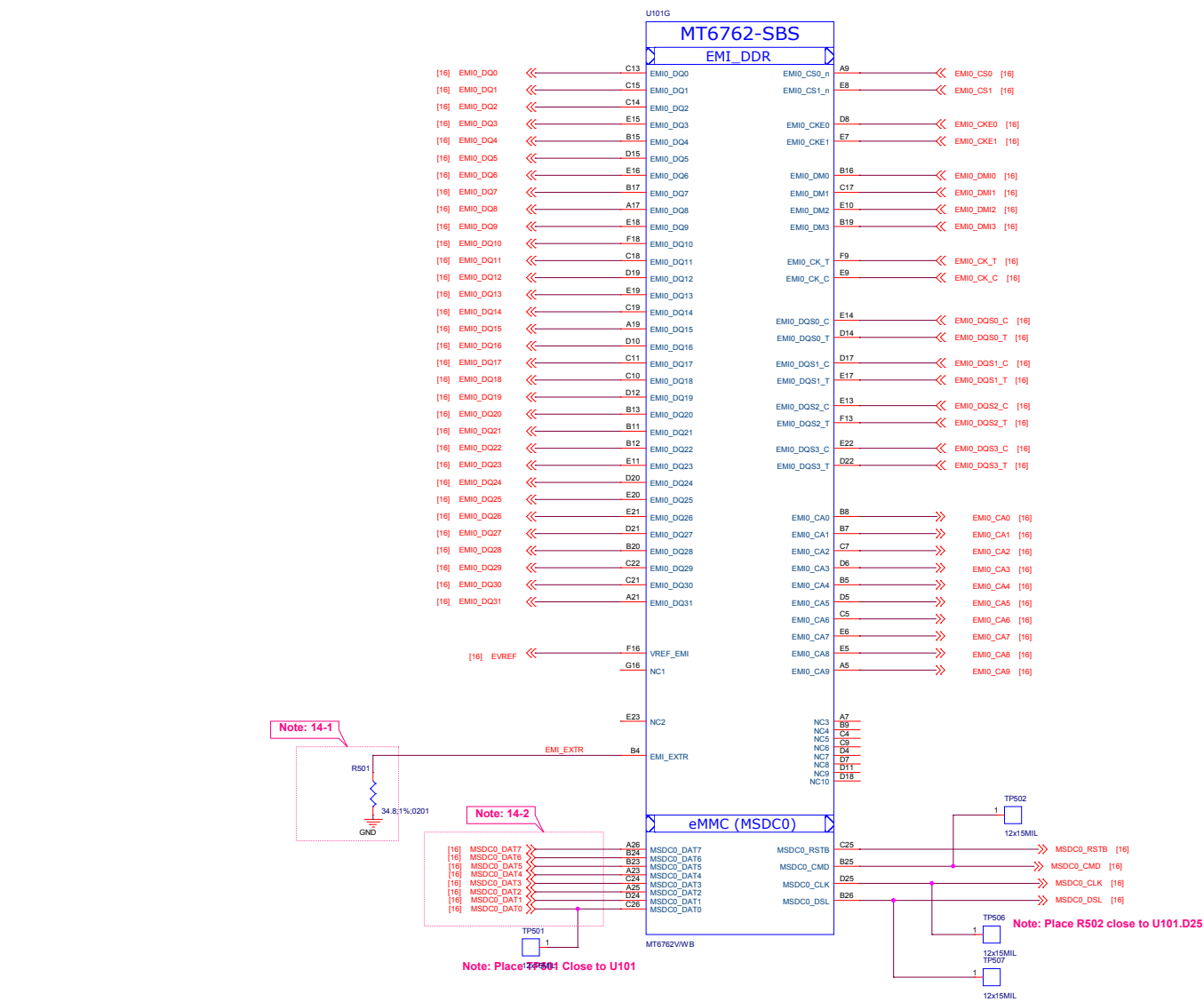
Note: 12-4



Schematic design notice of "13_BB_2" page.

Note 13-1: The enable pin of acoustic or optoelectronic devices (e.g. SPK AMP/Backlight/Charger OCP/OVP) suggest to use Peripheral_EN[0:5]
If use other GPIOs as enable pin, suggest to reserve 0201 NC to GND






Schematic design notice of "14_BB_3" page.

Note 14-1: R501 please select 34.8 ohm (1%) resistor

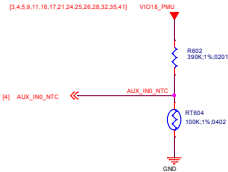
Note 14-2: Please check eMCP LP3 and eMCP LP4X pin mux

Title		05_BB_3_EMMC		REV: V10	
DOCUMENT NO.:		Design Name		Size A2	
DEPARTMENT:		WINGTECH-SH		DESIGNER: LIUFENGLEI	
					
Date:		Monday, April 08, 2019		Sheet 6 of 53	

The pull up ressisiter need to be 1% accuracy
NTC=100K

Thermistor to sense CHARGER
temperature

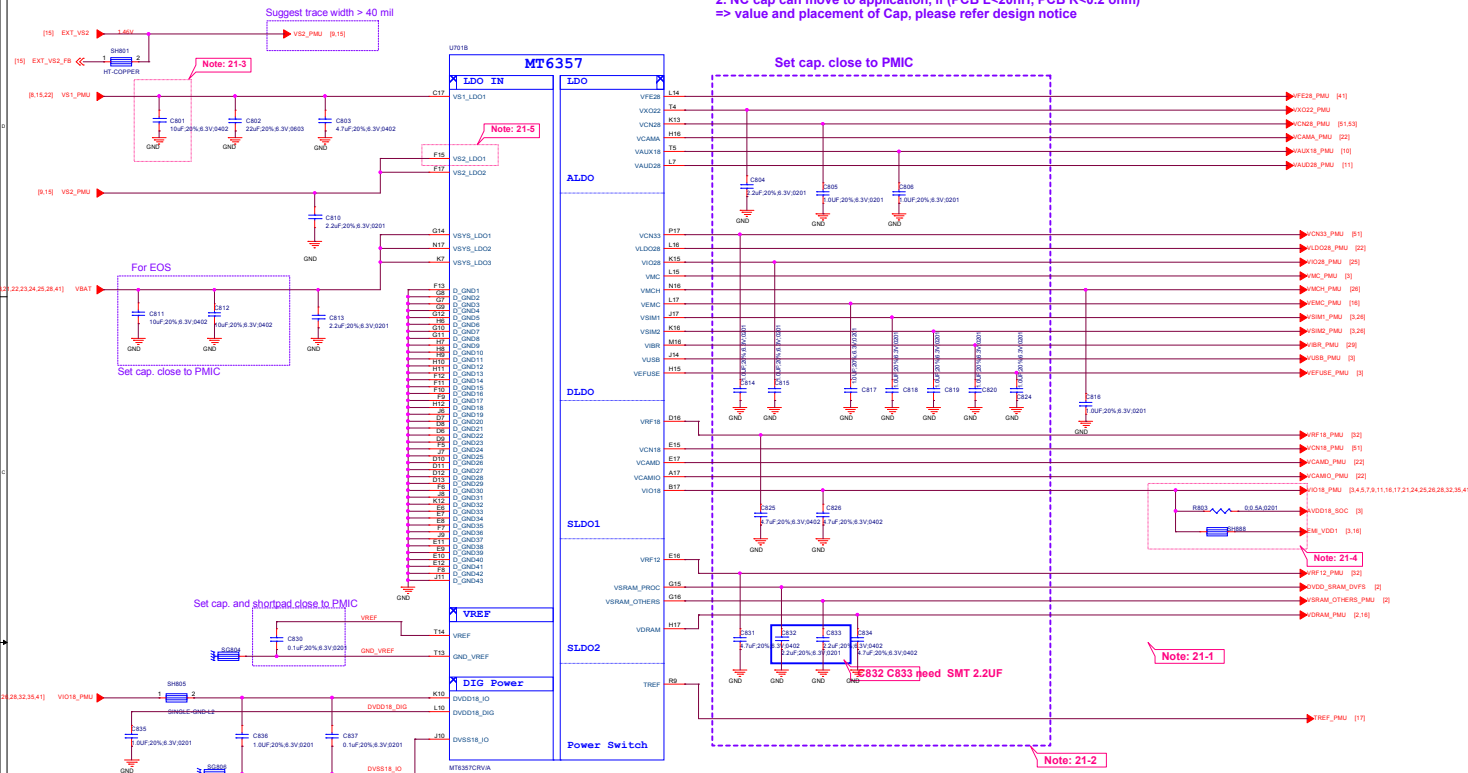
Huawei NOTE:1. NTC100k must keep a distance about 3-5 mm away from Charger IC and far from other heat sources 5-10 mm at least.



Thermistor to sense AP
temperature

- 1. RT604must keep a distance about 6-8 mm away from AP and far from other heat sources 10 mm at least.
- 2. The distance is the shortest distance from package edge to edge.

1. "Typical Cap" defined in design notice is the minimum cap. to LDO Cout.
2. NC cap can move to application, if (PCB L<20nH, PCB R<0.2 ohm)
=> value and placement of Cap, please refer design notice



Schematic design notice of "21_POWER_MT6357_LDO"

Note 21-1: If these power trace can meet LDO layout constraint, these CAP can be NC or removed. Please refer to MT6357 design notice.


Note 21-2: Output cap range please follow MT6357/CRV LDO design notice

Note 21-3: Ext Buck BOM option	Ext. buck option	
	w/ EXT VS2 Buck	w/o EXT VS2 Buck
C801	10uF	22uF

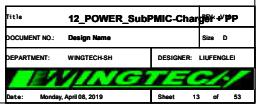
Note 21-4: Please set R803 and R803 close to C826, making star connection among VIO18_PMU, AVDD18_SOC, and EMI_VDD1 near to LDO cap. C826


Please also refer to MT6357 design notice for further detail design information

Note 21-5: Please connect VS2_LDO1(F15) to VS1_PMU if voltage applied to VCAMD(E17) >= 1.3 V

Title		11_POWER_SubPMIC-Gen(III)	V10
DOCUMENT NO.:	Design Name	Size D	
DEPARTMENT:	WINGTECHSH	DESIGNER:	LUFENGLEI
			
Date:	Monday, April 08, 2019	Sheet	12 of 53

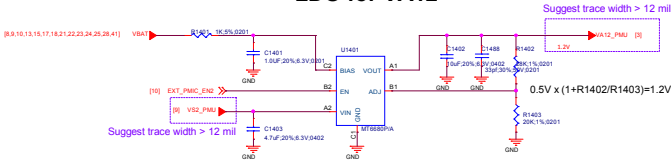
Vovp=6.3V when R1207=511K R1208=120K +-3%



Title: 13_POWER_SubPMIC-HV powers		REV: V10
DOCUMENT NO.: Design Name		Size D
DEPARTMENT: WINGTECHSH	DESIGNER: LUFENGLEI	
		
Date: Monday, April 08, 2019	Sheet	14 of 53

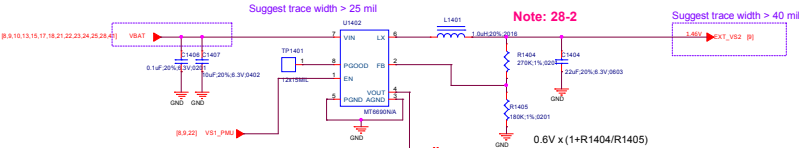
LDO for VA12

Note: 28-1



Ext. Bulk for VS2

Note: 28-2



NOTE: Do not use VCAMD 1.3/1.5/1.8 when VS2 BUCK applied

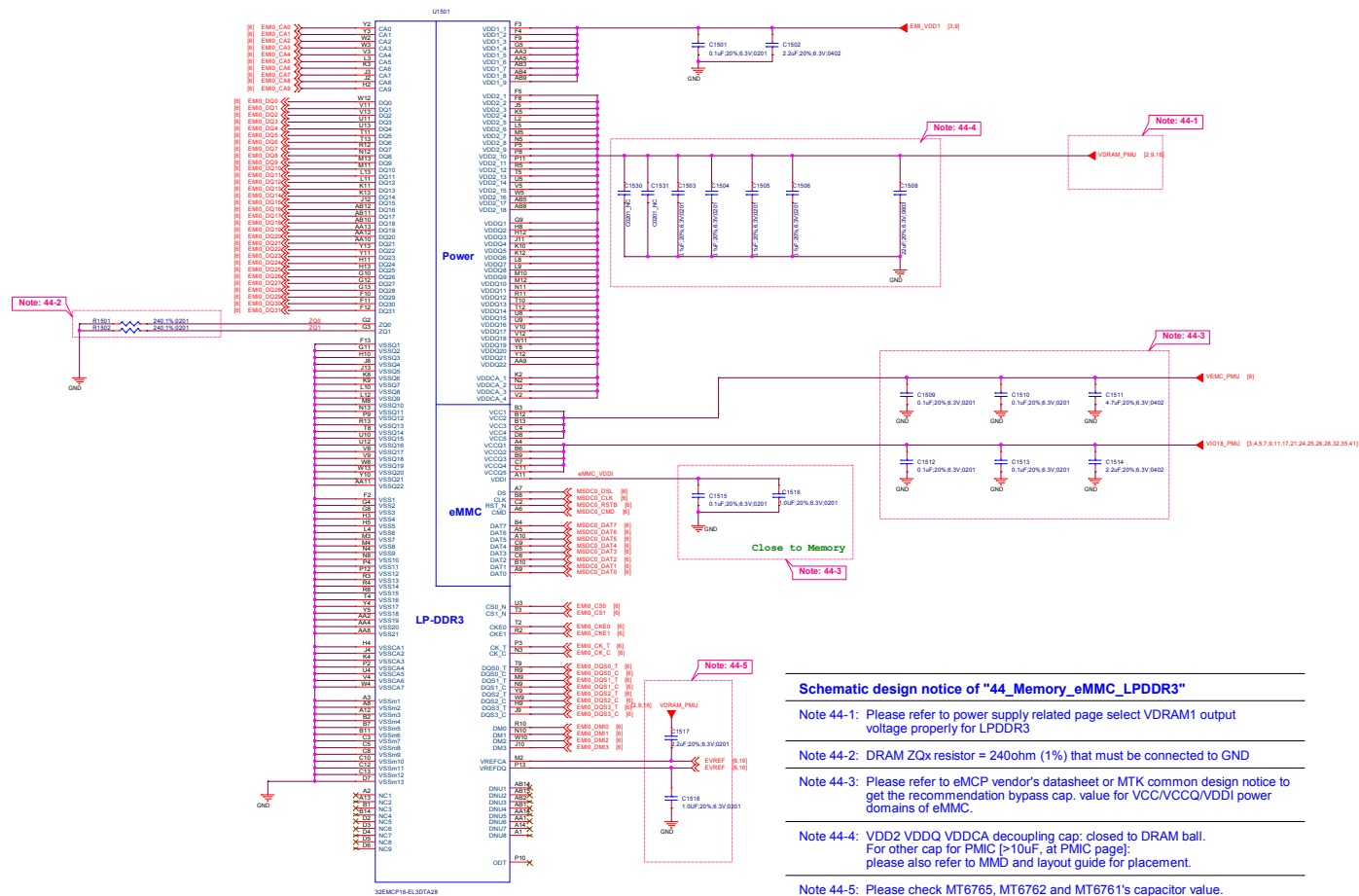
Schematic design notice of "28_POWER_ThirdParty-Power"

Note 28-1: VA12 Layout placement please close to AP

Note 28-2: VS2 Buck Layout placement please close to PMIC MT6357

Note 28-3: VCN33 LDO Layout placement please close to MT6631

LPDDR3



Schematic design notice of "44_Memory_eMMC_LPDDR3"

Note 44-1: Please refer to power supply related page select VDRAM1 output voltage properly for LPDDR3

Note 44-2: DRAM ZQx resistor = 240ohm (1%) that must be connected to GND

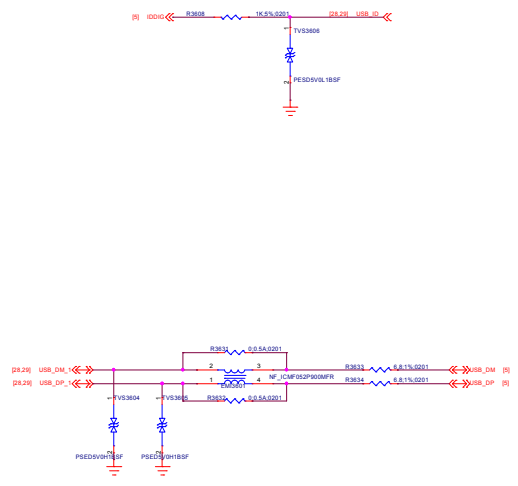
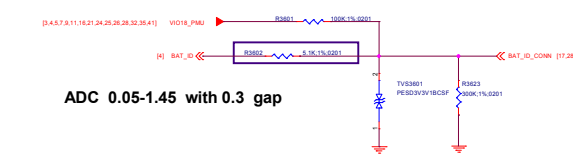
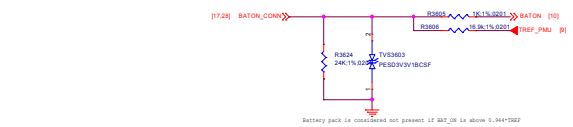
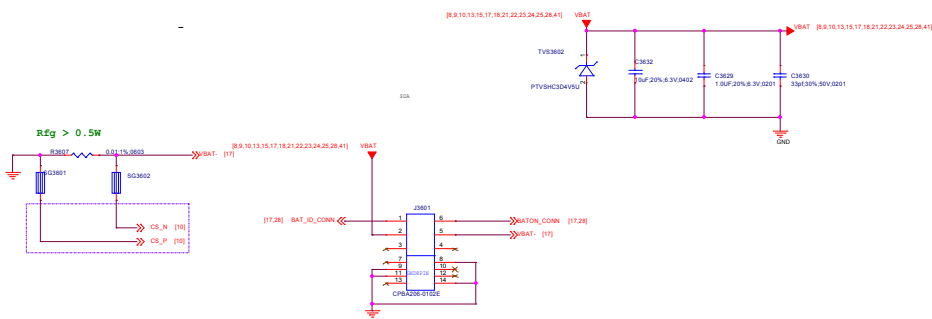
Note 44-3: Please refer to eMCP vendor's datasheet or MTK common design notice to get the recommendation bypass cap. value for VCC/VCCQ/VDDI power domains of eMMC.

Note 44-4: VDD2 VDDQ VDDCA decoupling cap: closed to DRAM ball.
For other cap for PMIC >10uF, at PMIC page:
please also refer to MMD and layout guide for placement.

Note 44-5: Please check MT6765, MT6762 and MT6761's capacitor value.

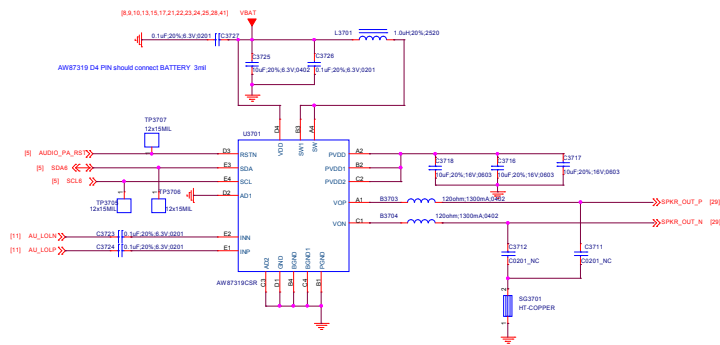
Project	C1517	C1518
MT6765	2.2uF	1uF
MT6762	2.2uF	1uF
MT6761	0.1uF	0.1uF

BATTERY CONNECTOR

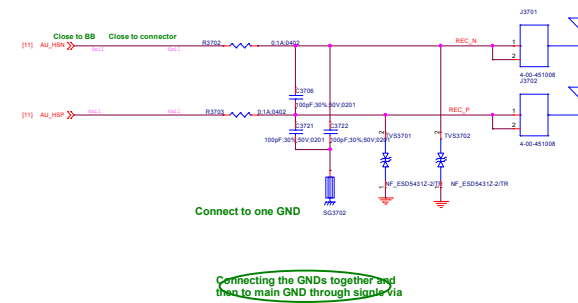


ADC 0.05-1.45 with 0.3 gap

SPK



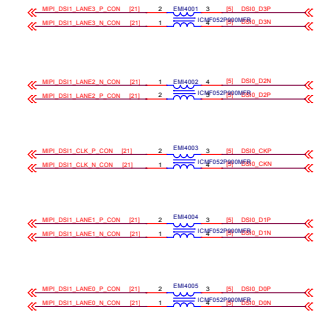
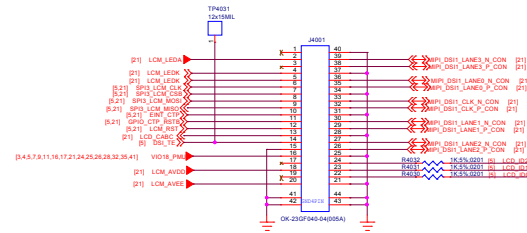
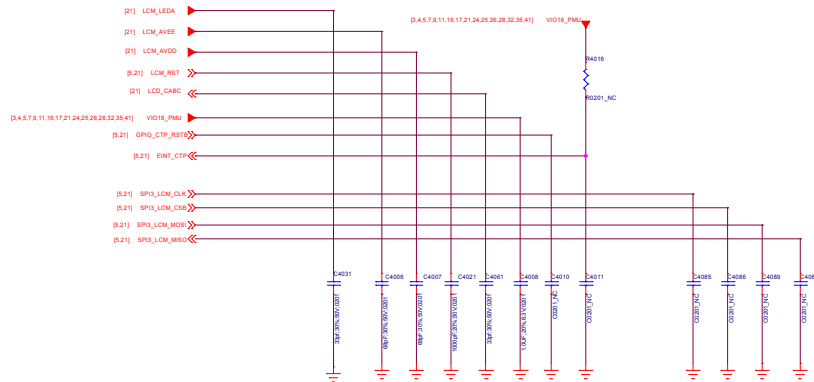
Receiver



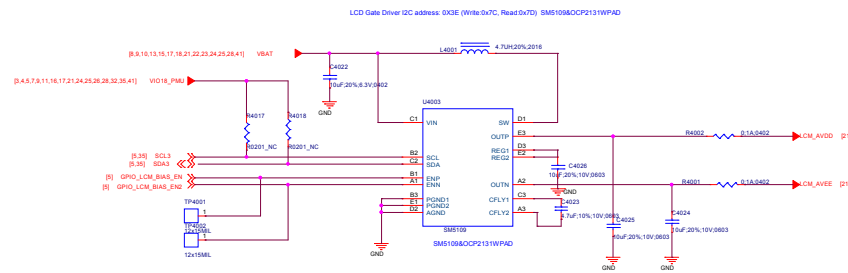
main GND



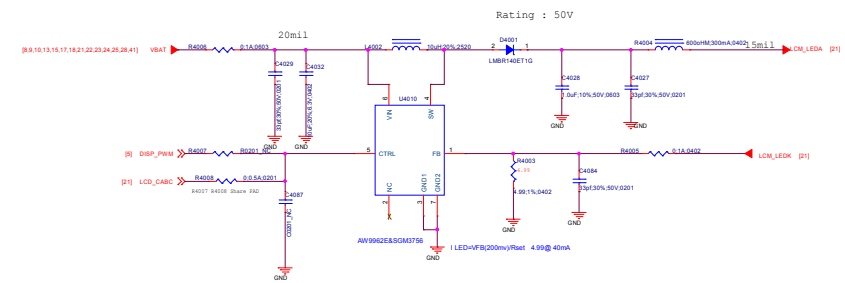
Common Mode Filter

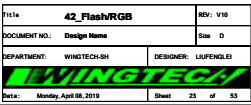


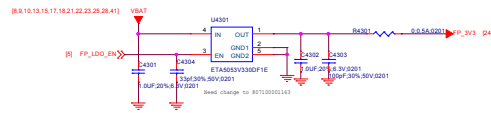
LCD Gate Drive



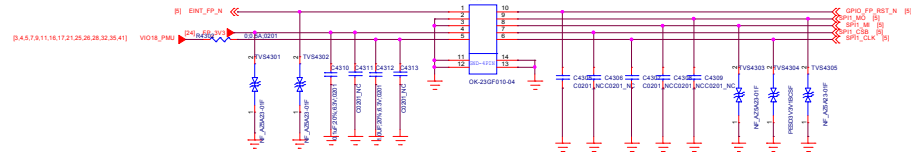
LCD Backlight LED Driver



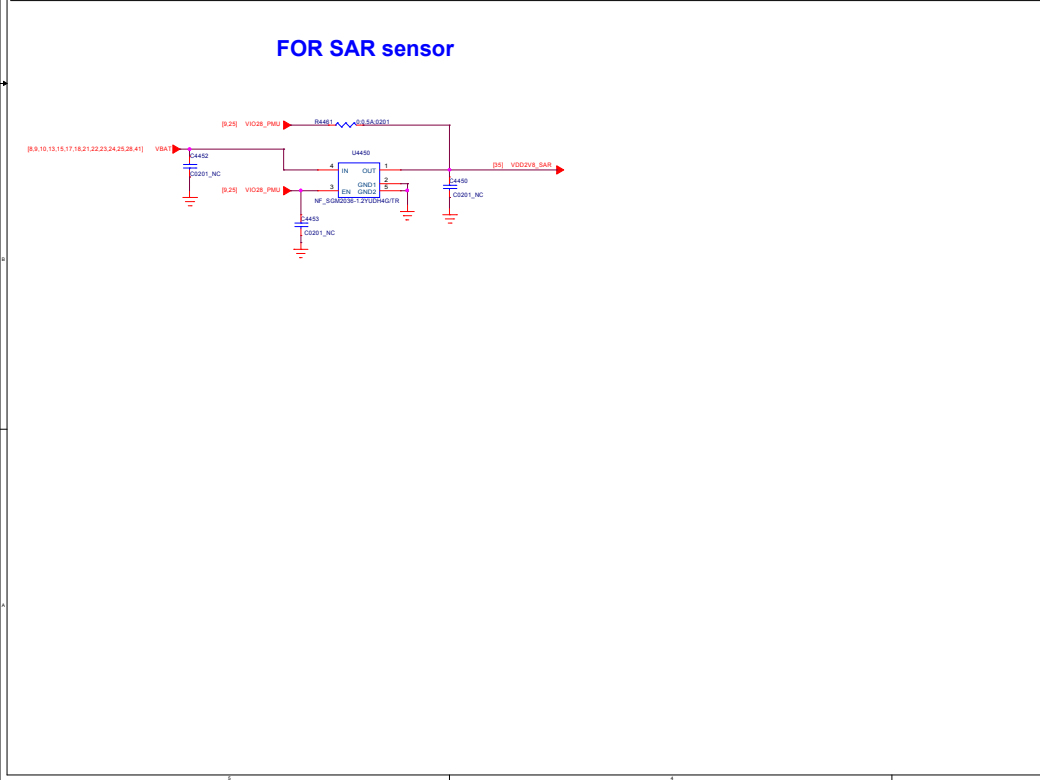




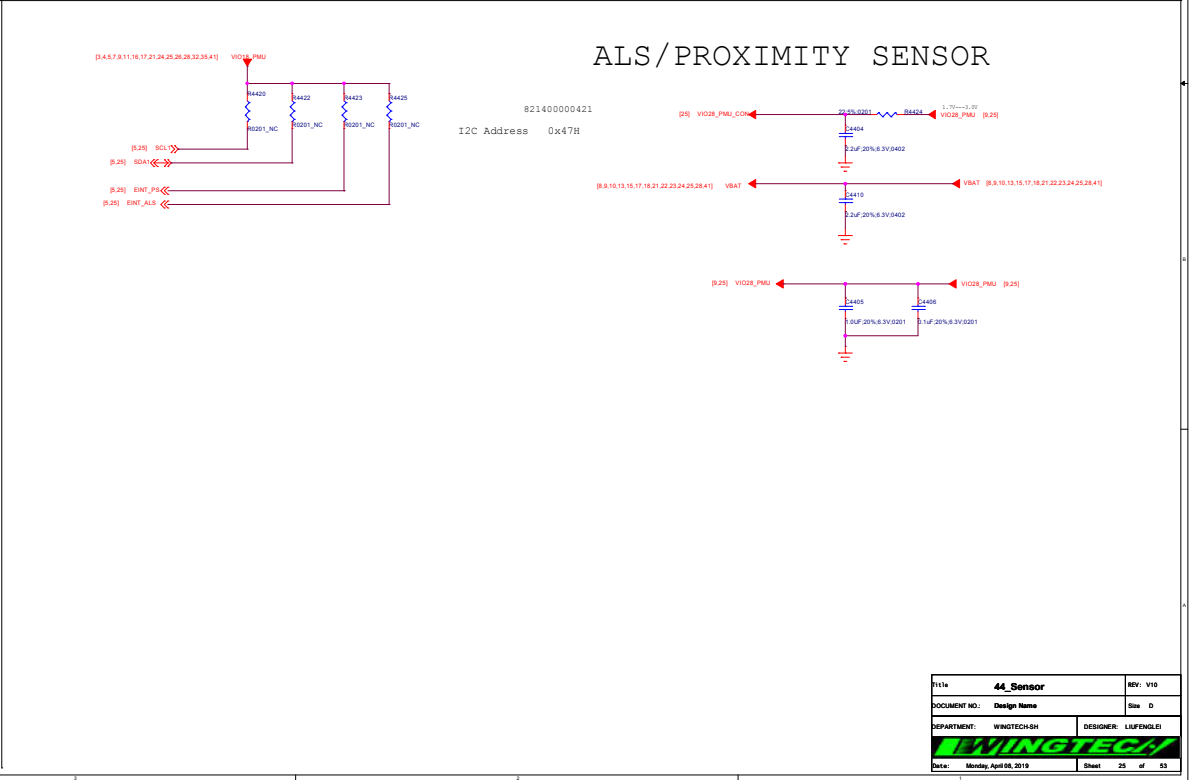
Fingerprint



Fingerprint

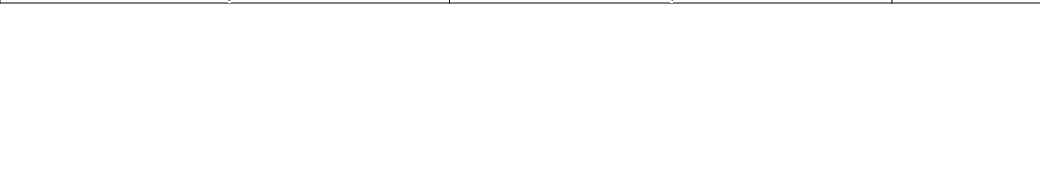
[illegible]

ALP-Sensor



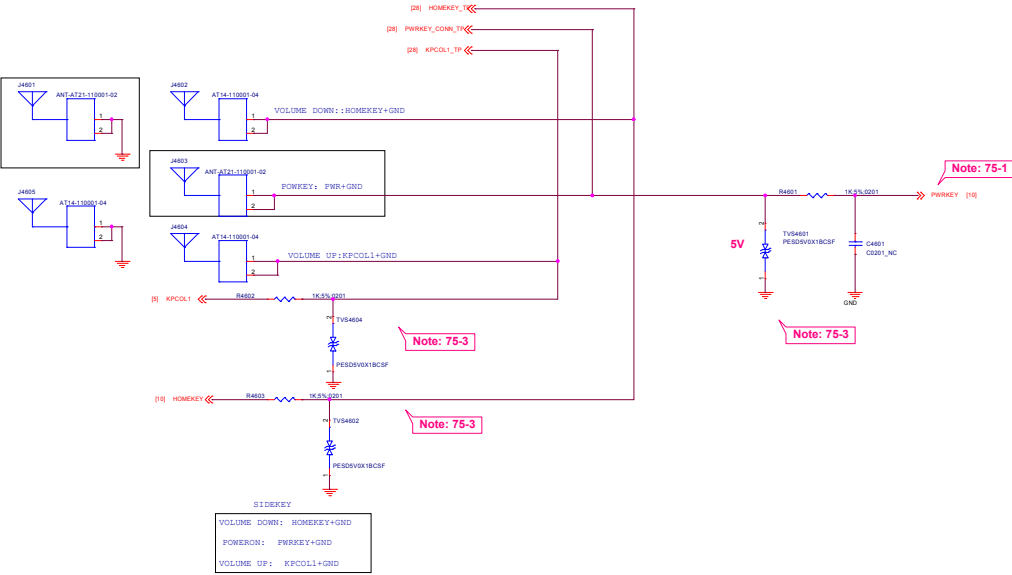
Accerometer

FOR SAR sensor

[illegible]

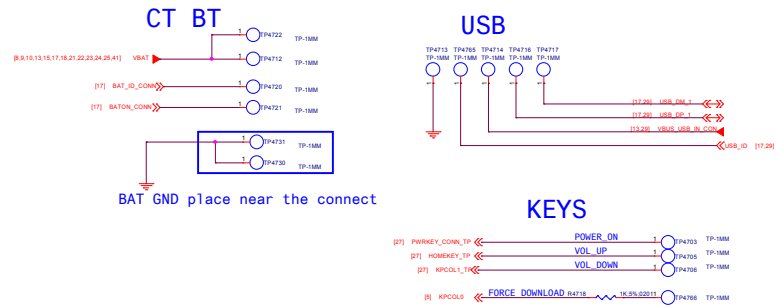
Power Key / Key Pad

DO NOT put pull-up resistor on PWRKEY



Note 75-1: DO NOT put pull-up resistor on PWRKEY
Note 75-2: Volume Up: HOME KEY+GND
Volume Down: KPCOLL+GND

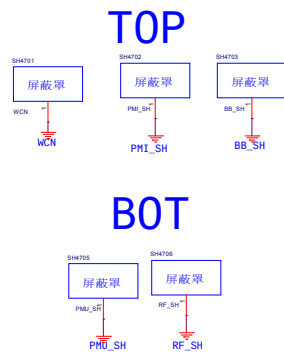
DEVICE MODE CONF



Debug



SHIELDING



MARK

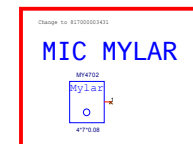


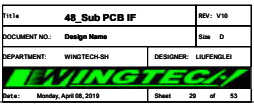
Waterproof

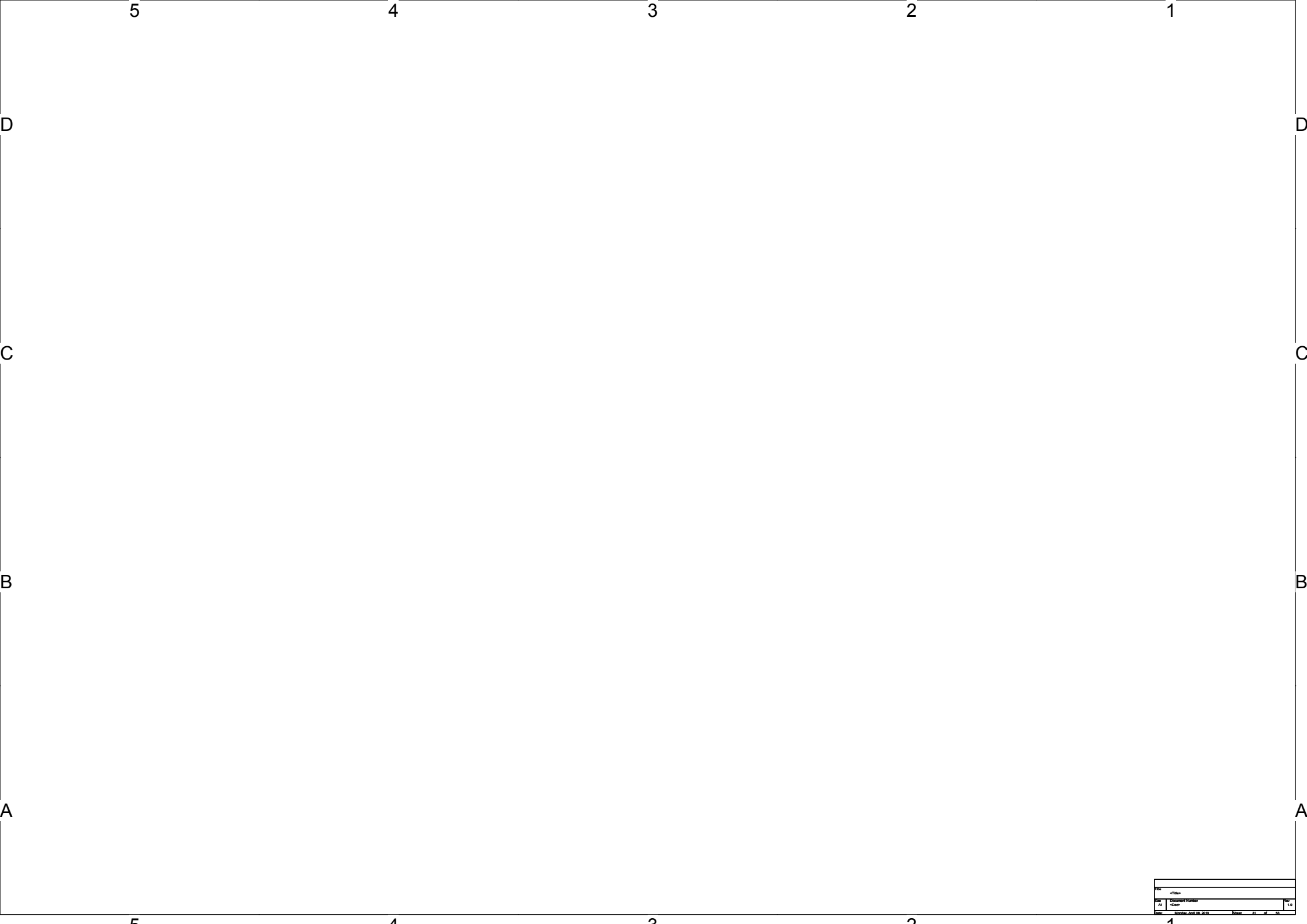
SN Label

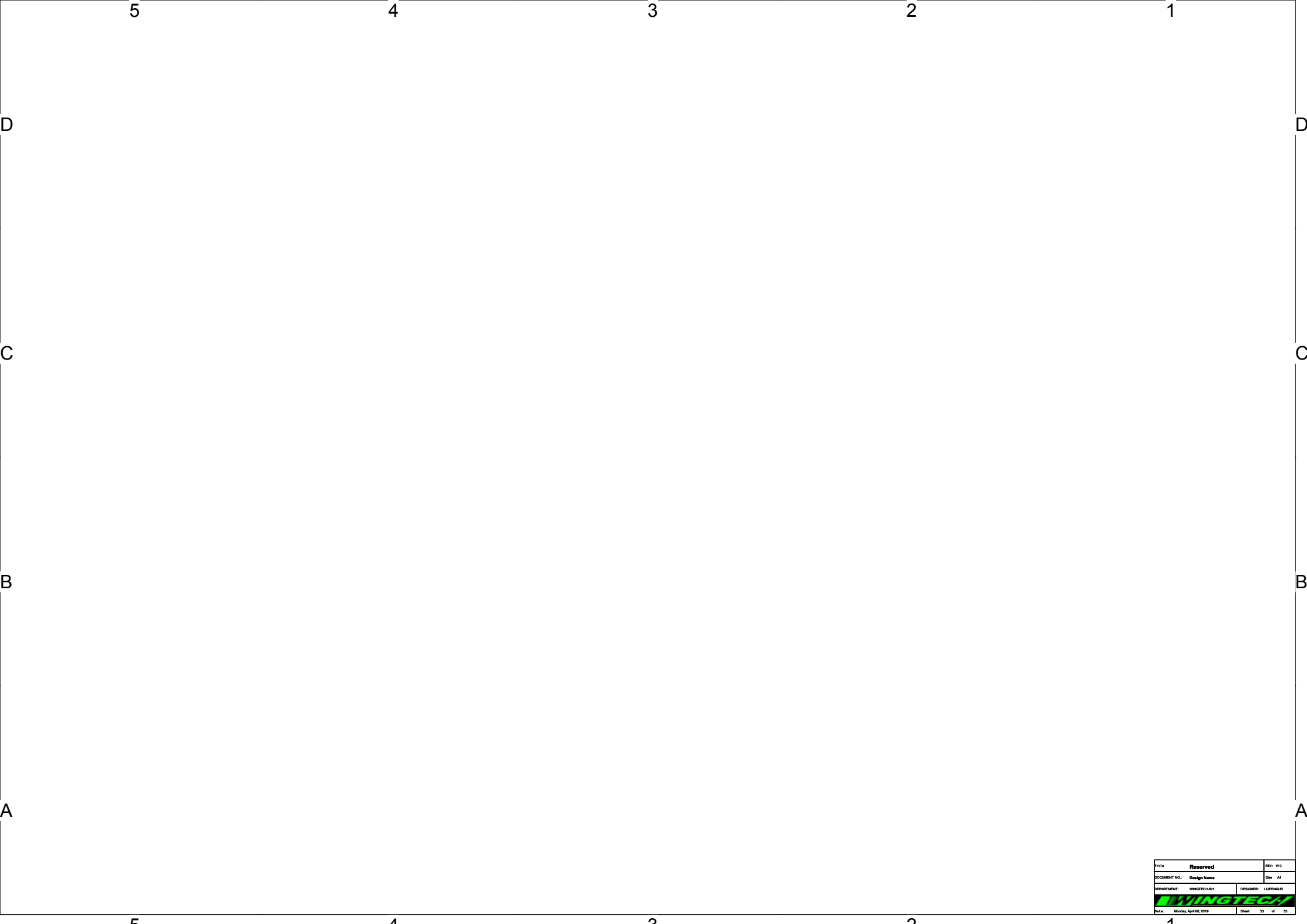


PCB









D

D

C

C

B

B

A

A

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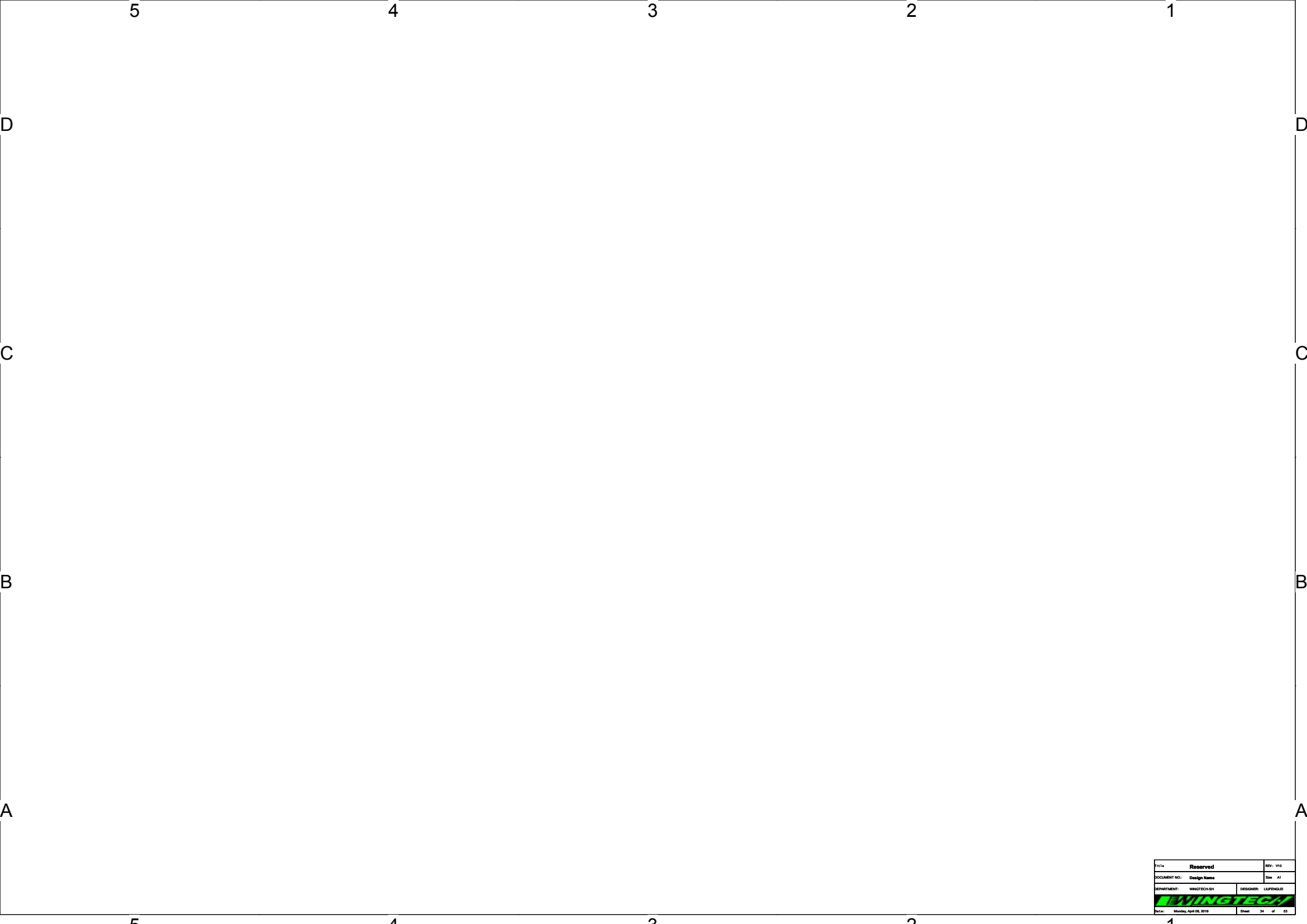
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Title: Reserved		REV: V10
DOCUMENT NO.: Design Name		Rev: A1
DEPARTMENT: WINGTECH-SH		DESIGNER: LUPENGLEB
		
Date: Monday, April 08, 2019	Sheet	33 of 33



D

D

C

C

B

B

A

A

5

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3

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1


5

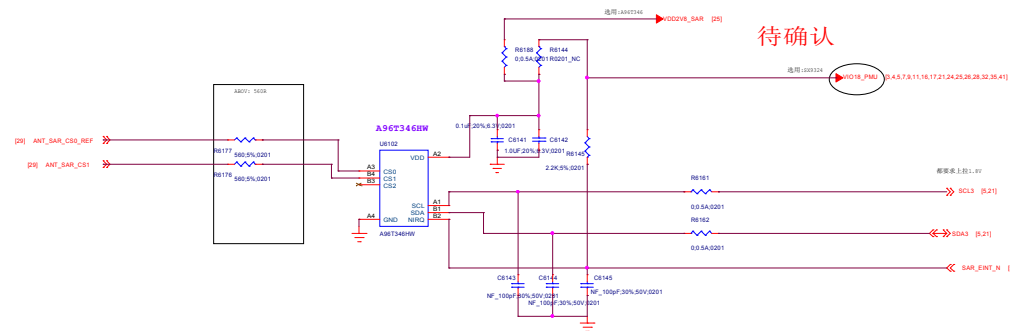
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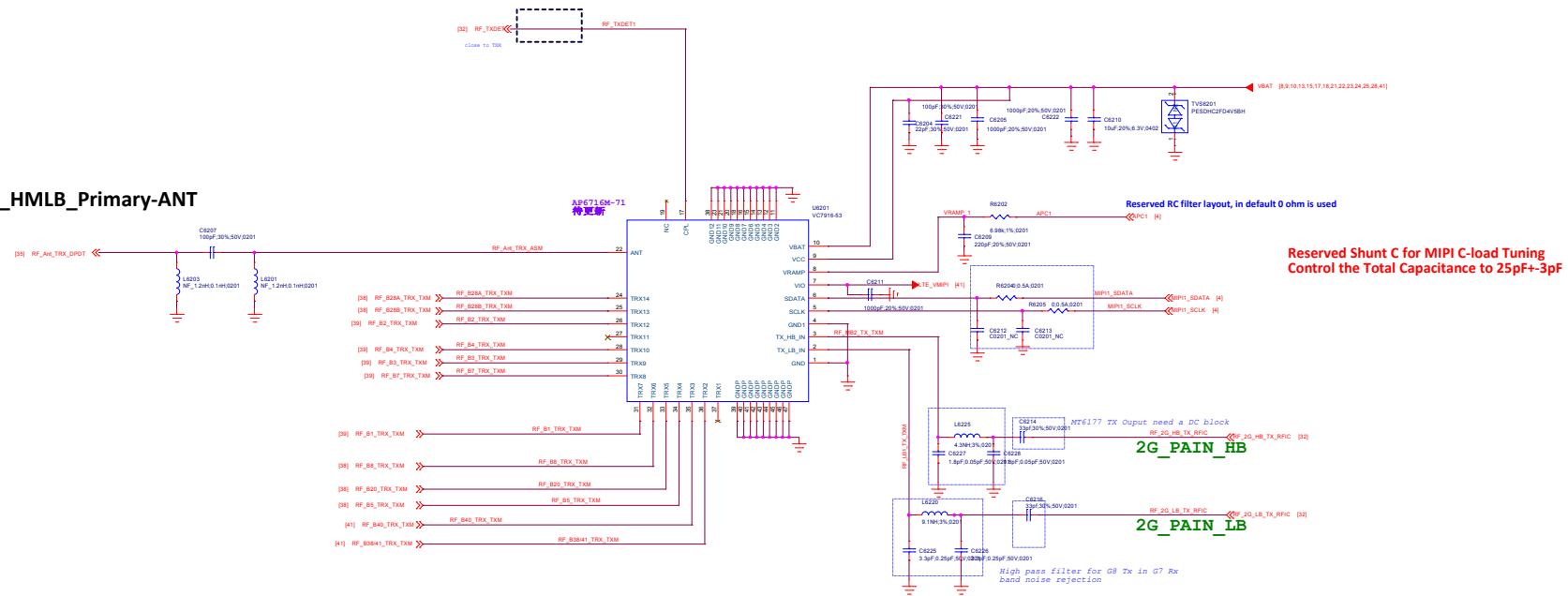
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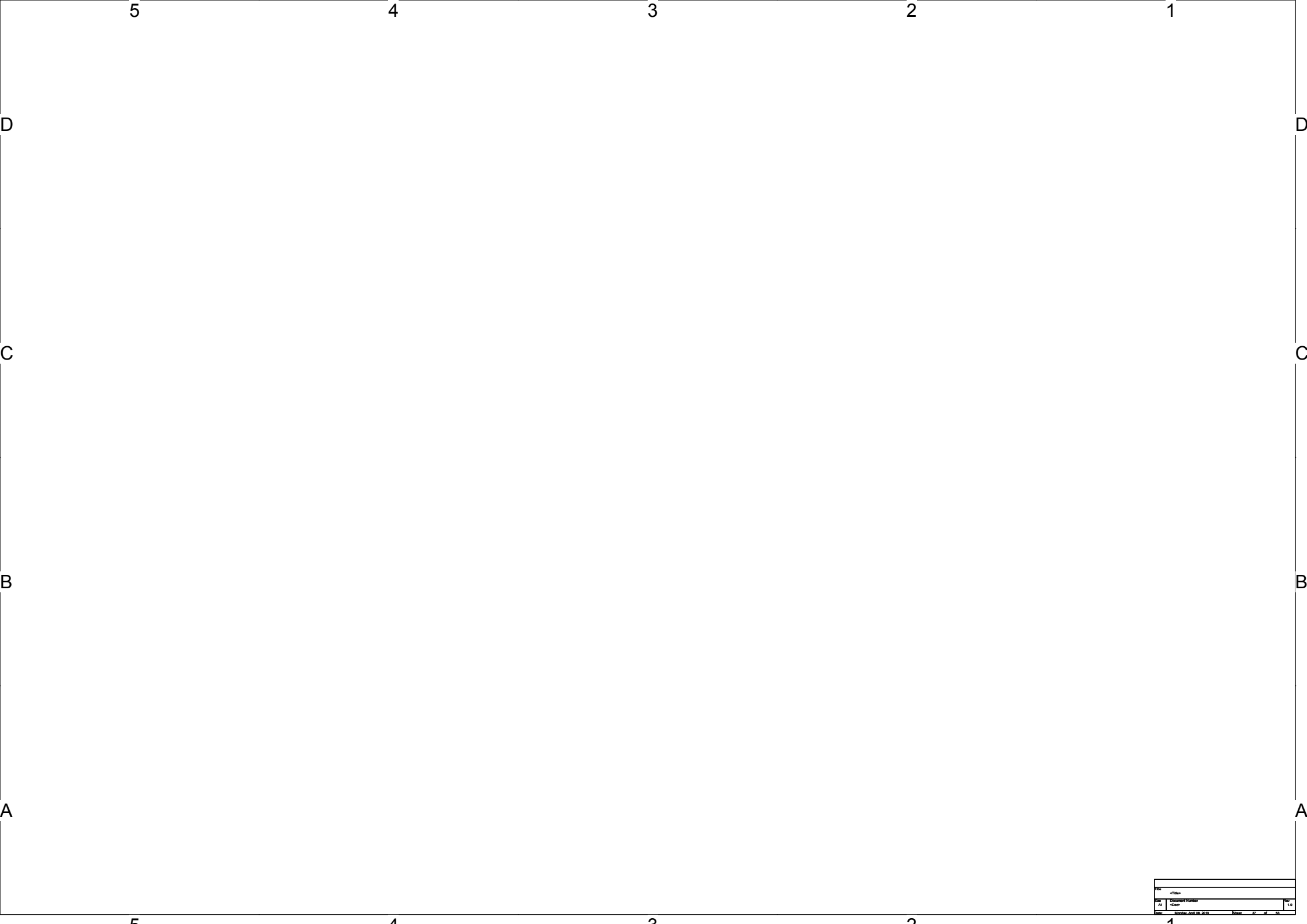
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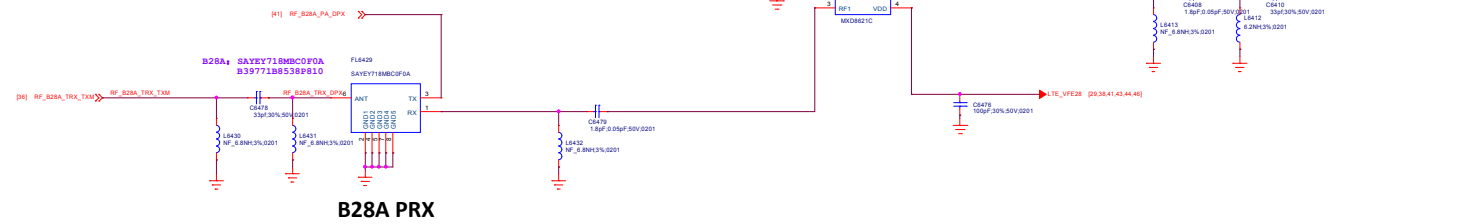
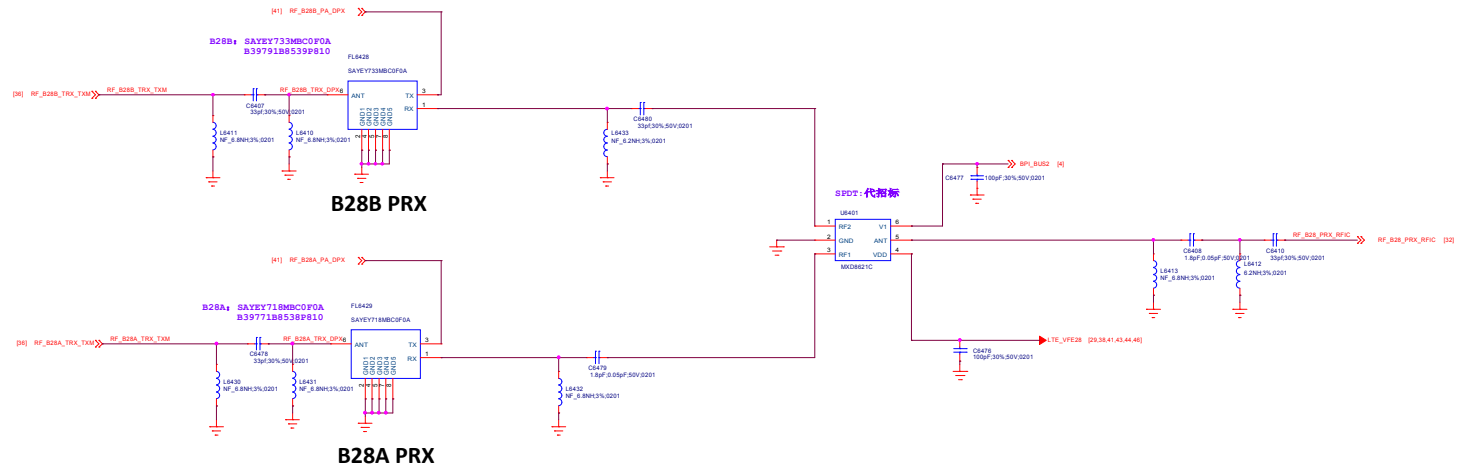
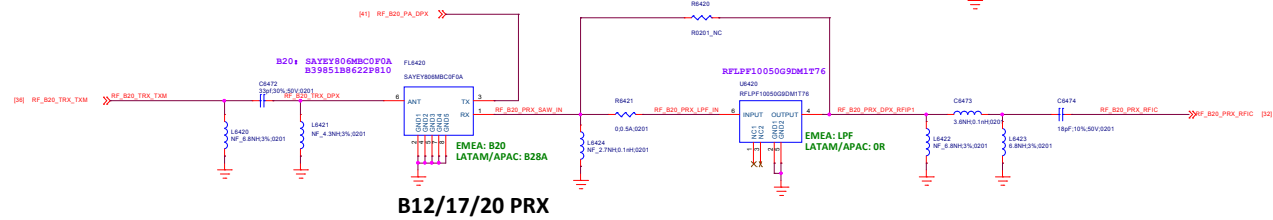
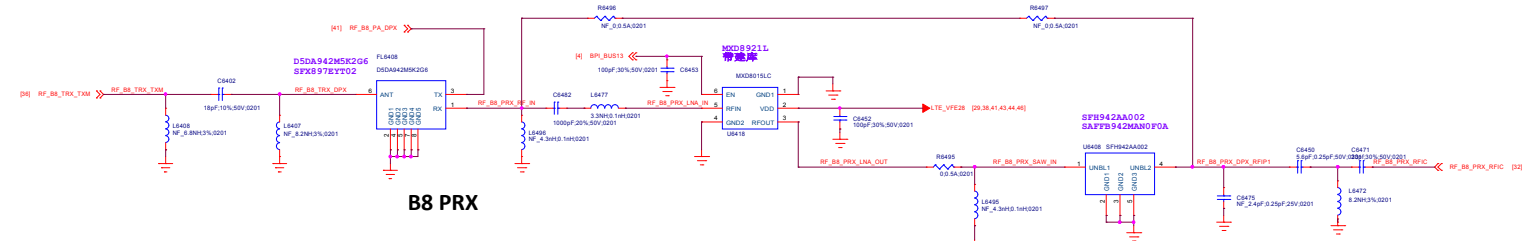
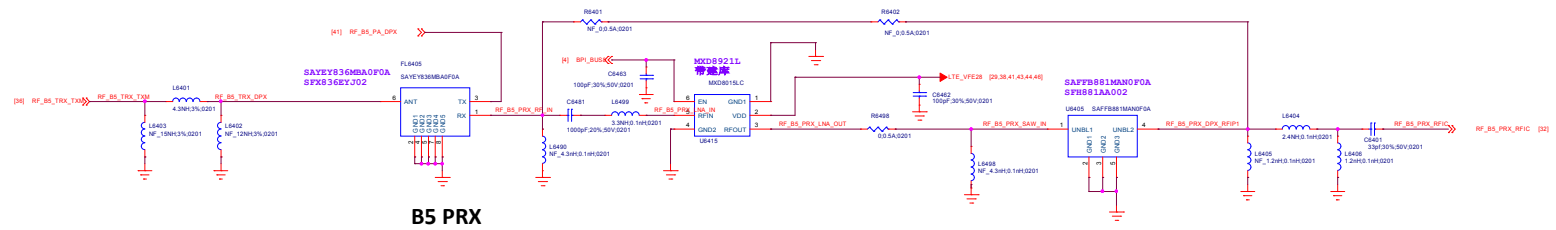
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DOCUMENT NO.: Design Name		Rev: A1
DEPARTMENT: WINGTECH-SH		DESIGNER: LUPENGLEB
		
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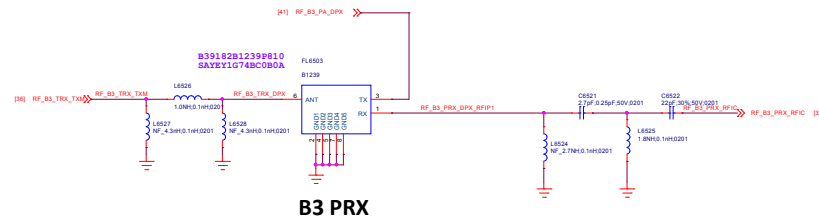
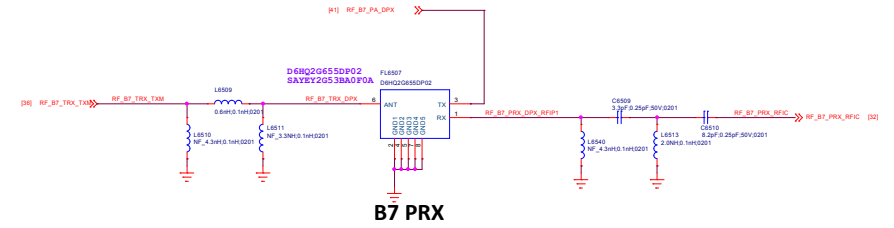
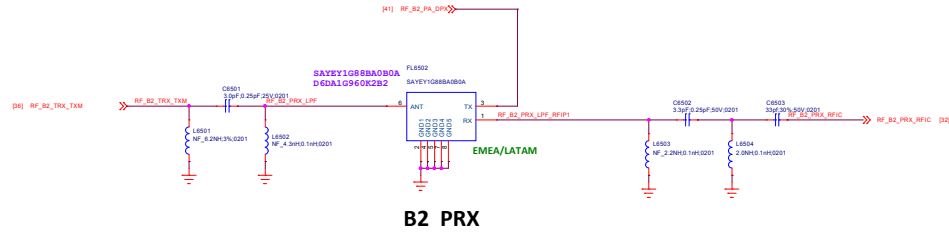
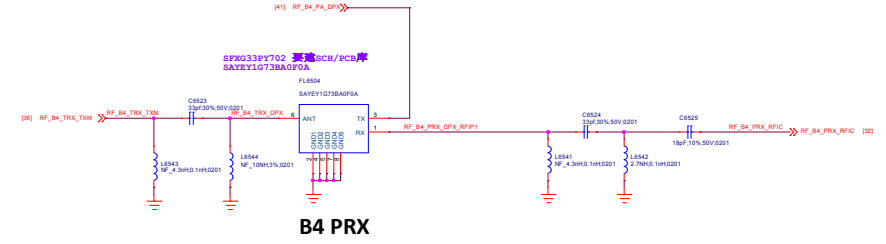
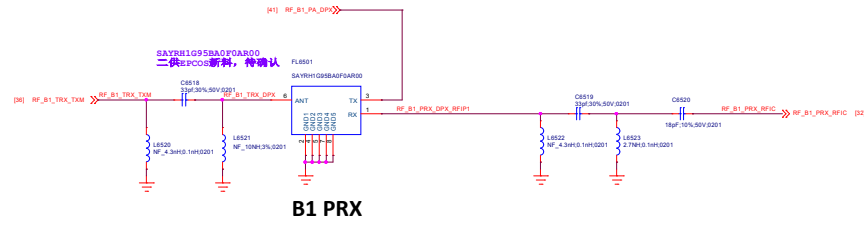


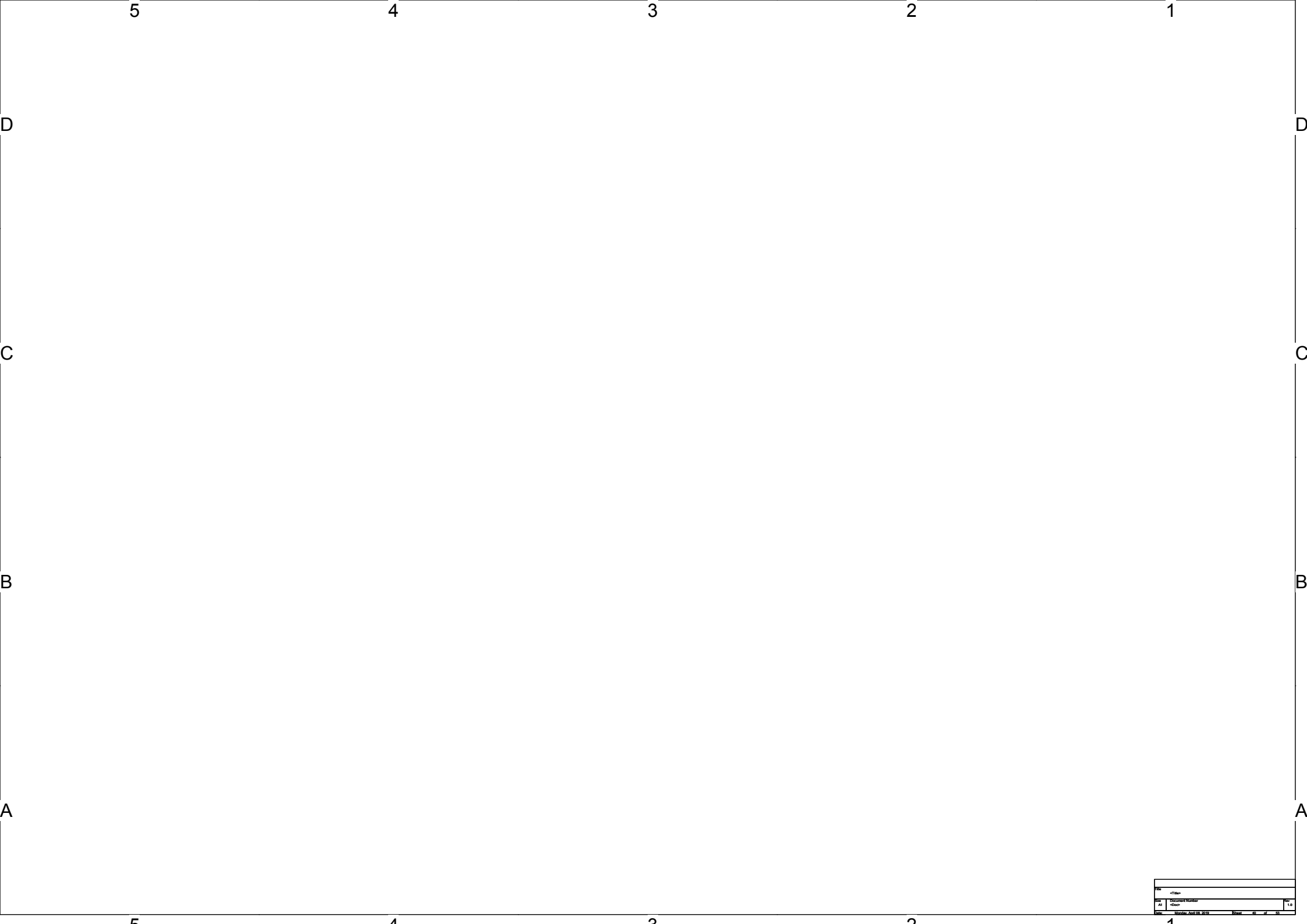
TO_HMLB_Primary-ANT

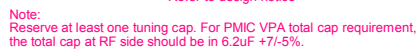


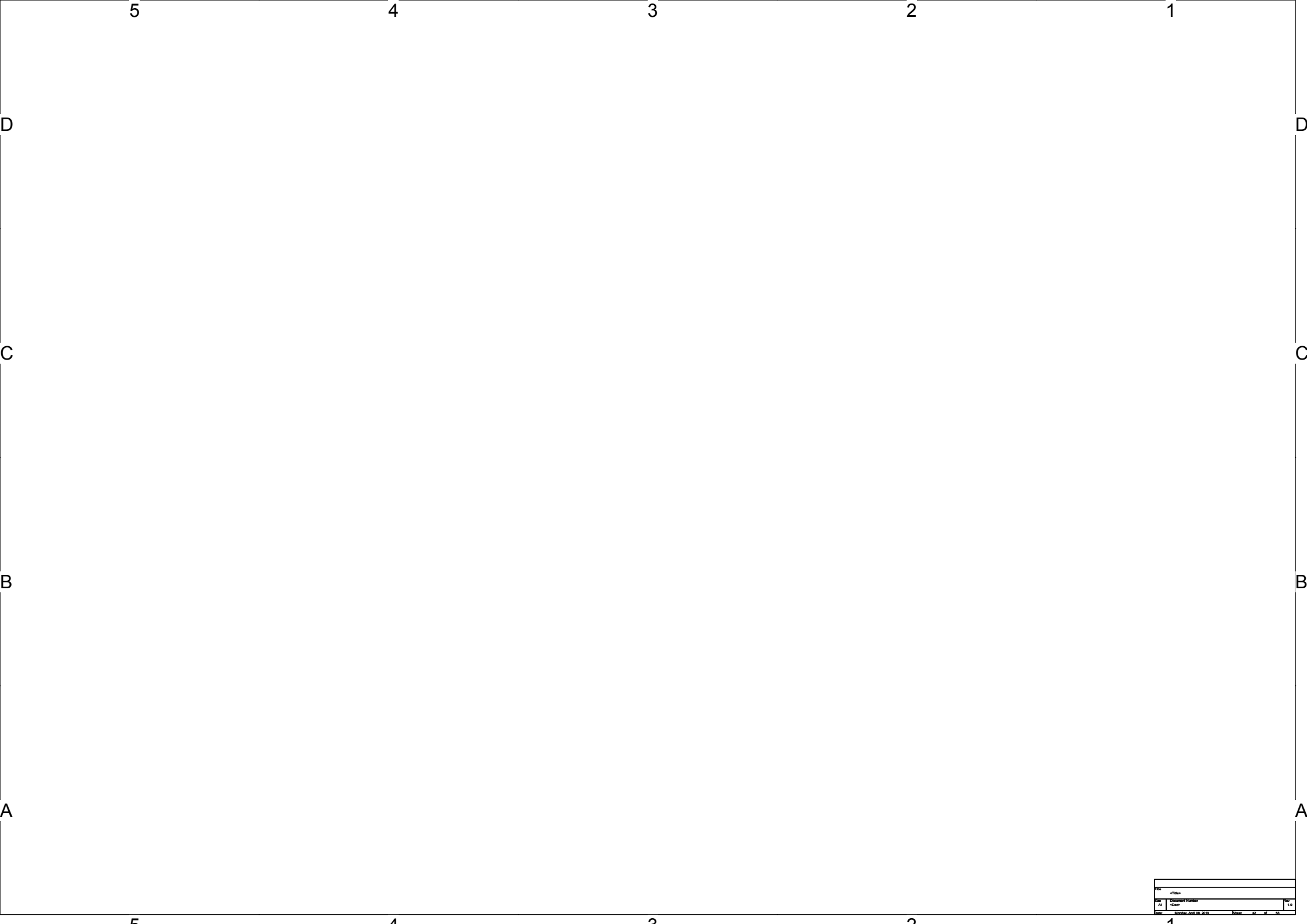


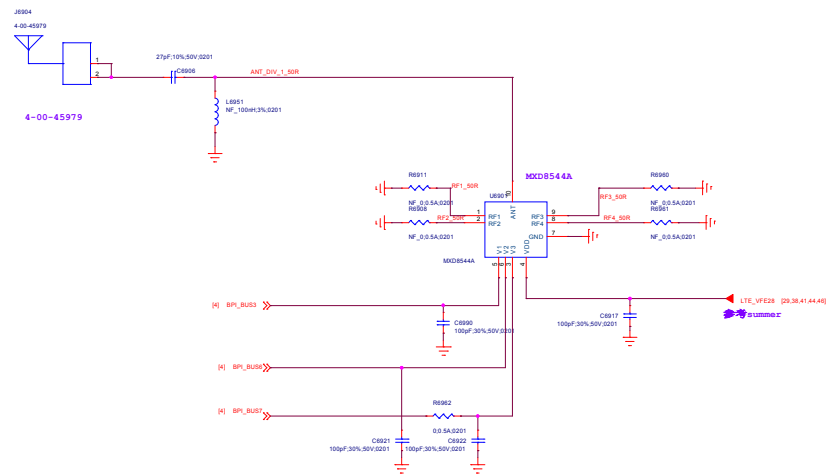
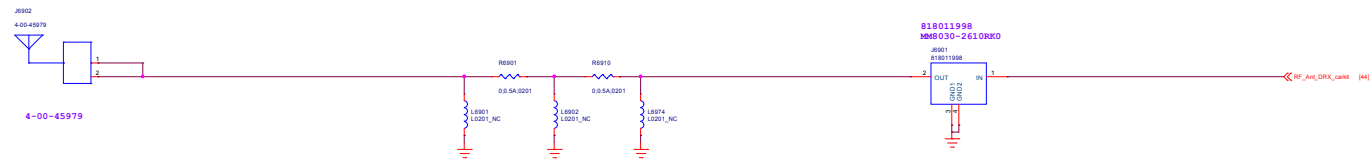


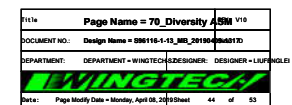


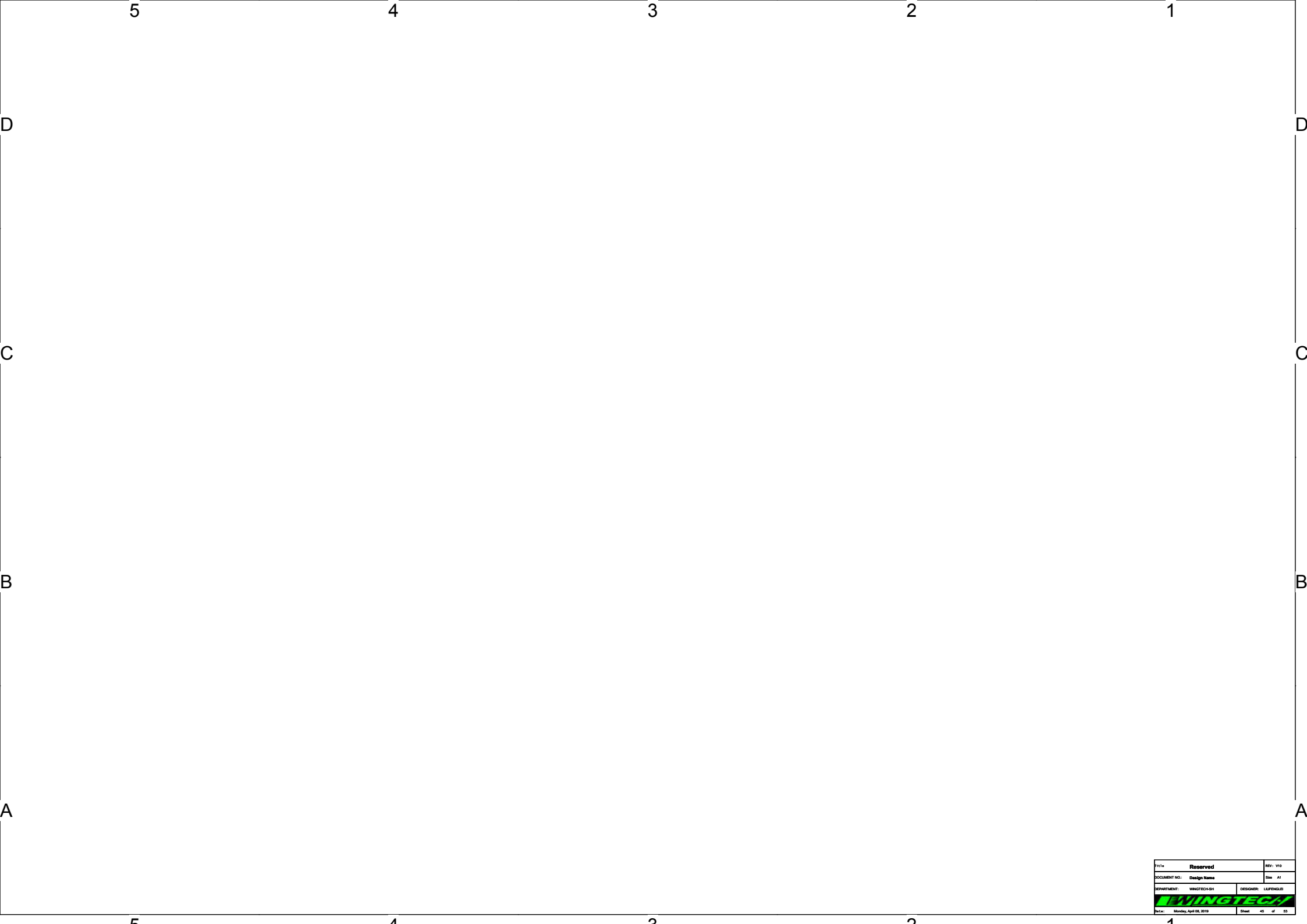




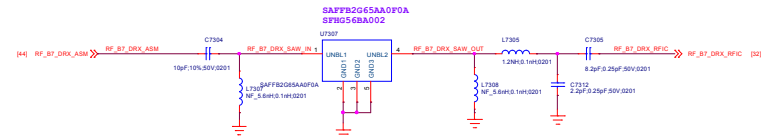




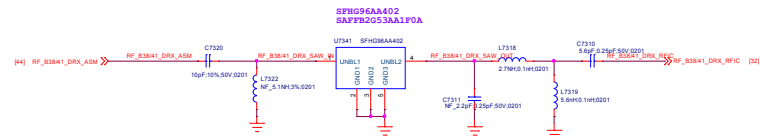




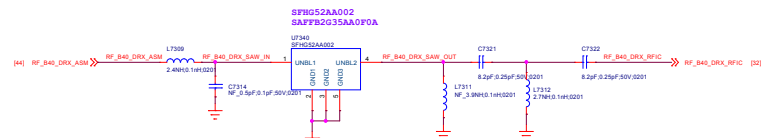
Title: Reserved		REV: V10
DOCUMENT NO.: Design Name		Rev: A1
DEPARTMENT: WINGTECH-SH		DESIGNER: LUPENGLEB
		
Date: Monday, April 08, 2019	Sheet	45 of 53



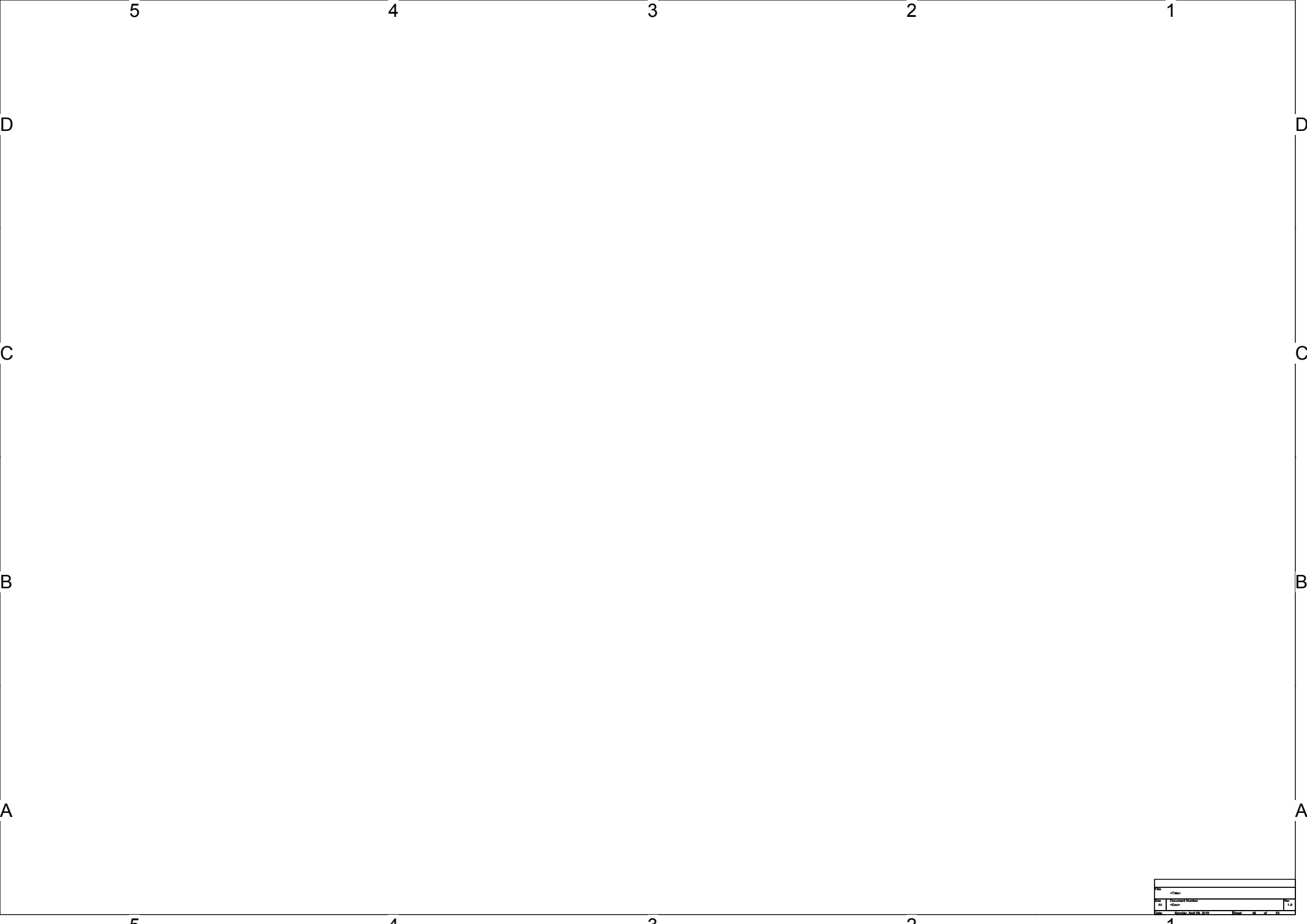
B7 DRX

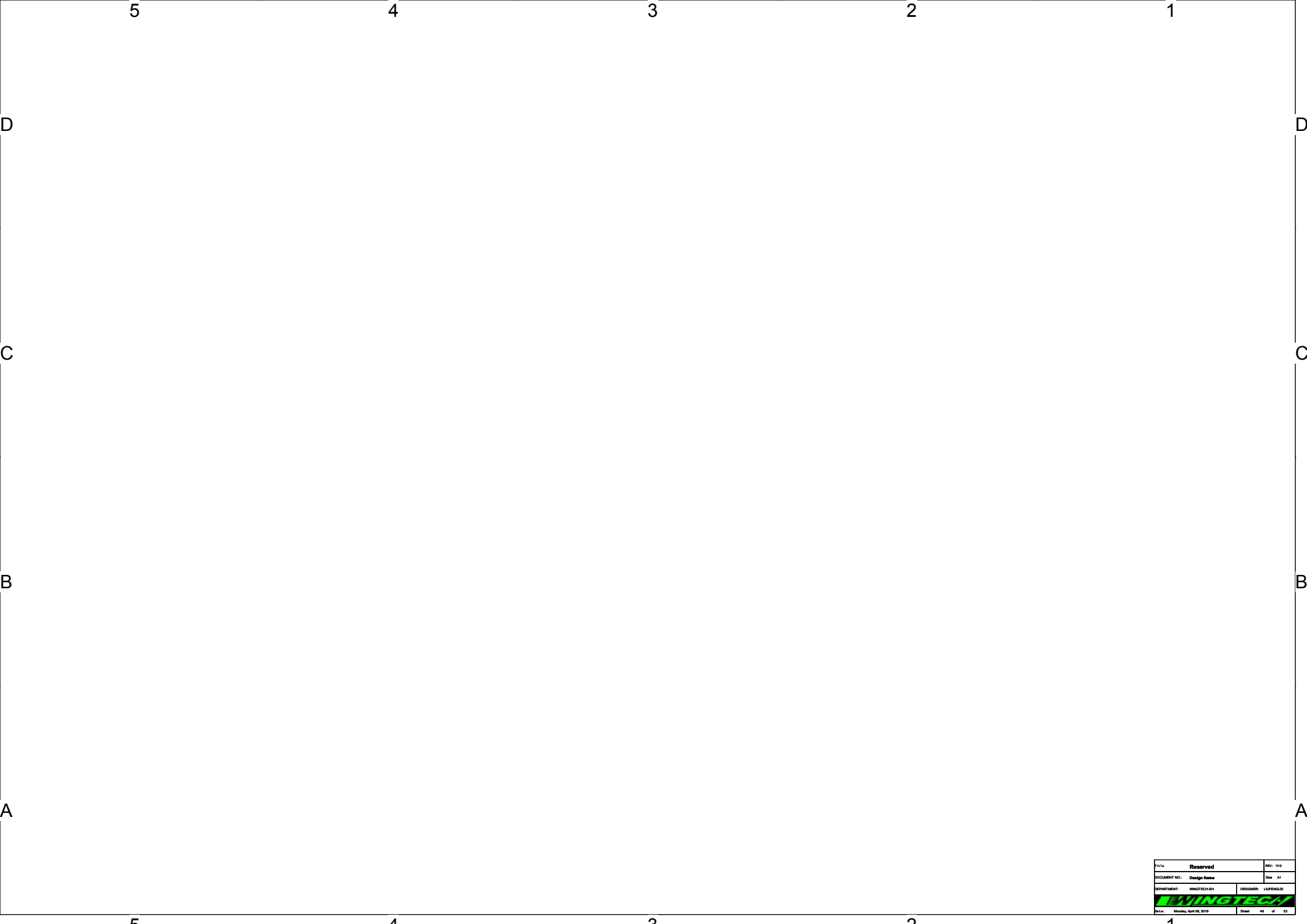


B38/41 DRX

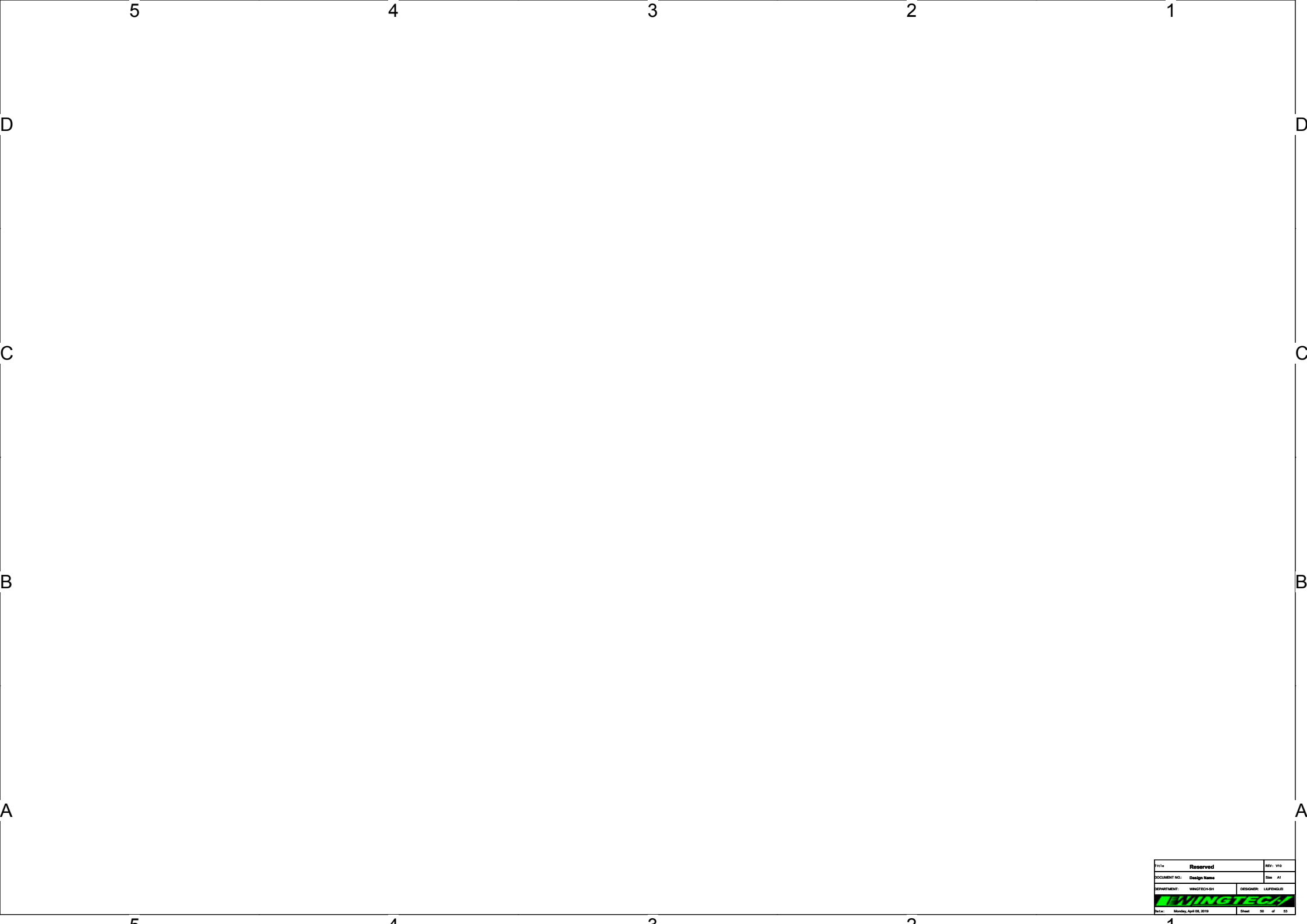


B40 DRX





Title: Reserved		REV: V10
DOCUMENT NO.: Design Name		Rev: A1
DEPARTMENT: WINGTECH-SH		DESIGNER: LUPENGLEB
		
Date: Monday, April 08, 2019	Sheet	40 of 53



D

D

C

C

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A

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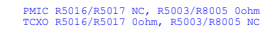
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1

Title: Reserved		REV: V10
DOCUMENT NO.: Design Name		Rev: A1
DEPARTMENT: WINGTECH-SH		DESIGNER: LUPENGLEB
		
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Note 51-1: For R5015 size, please select 0402 size or larger one

Note 51-3: If WiFi 5G not support, connect pin 34(WF_RF_5G) to GND

Note 51-5: If WiFi 5G were no need, VCN33 could be chosen from PMIC output (VCN33



