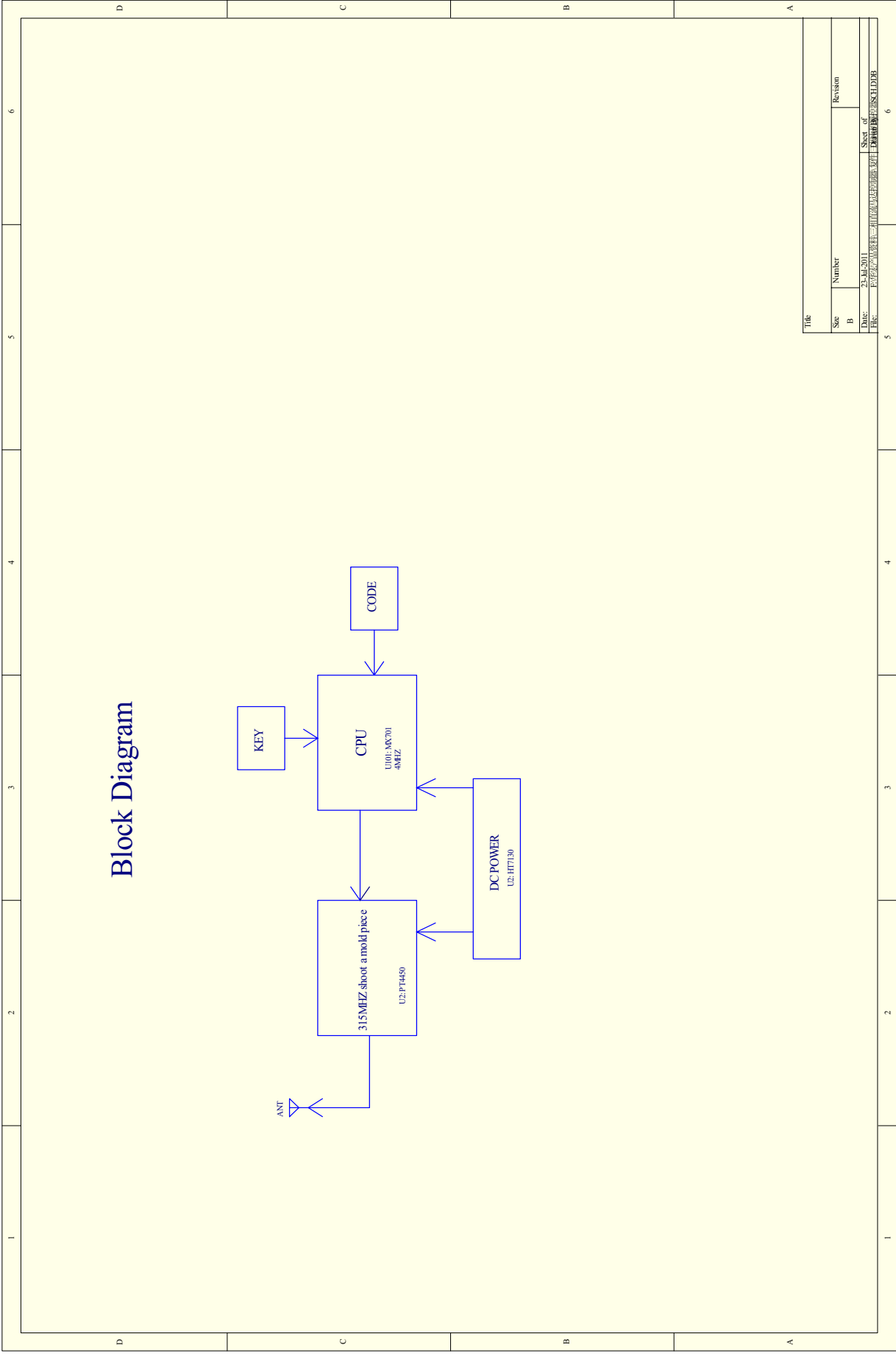


Block Diagram

```
graph TD; ANT[ANT] --> U2_PT4450["315MHz shoot a mold piece<br/>U2: PT4450"]; U2_PT4450 --> CPU["CPU<br/>U00: 3MX701<br/>4MHz"]; CPU --> CODE[CODE]; KEY[KEY] --> CPU; DC_POWER["DC POWER<br/>U2: HT7130"] --> U2_PT4450; DC_POWER --> CPU;
```

[illegible]