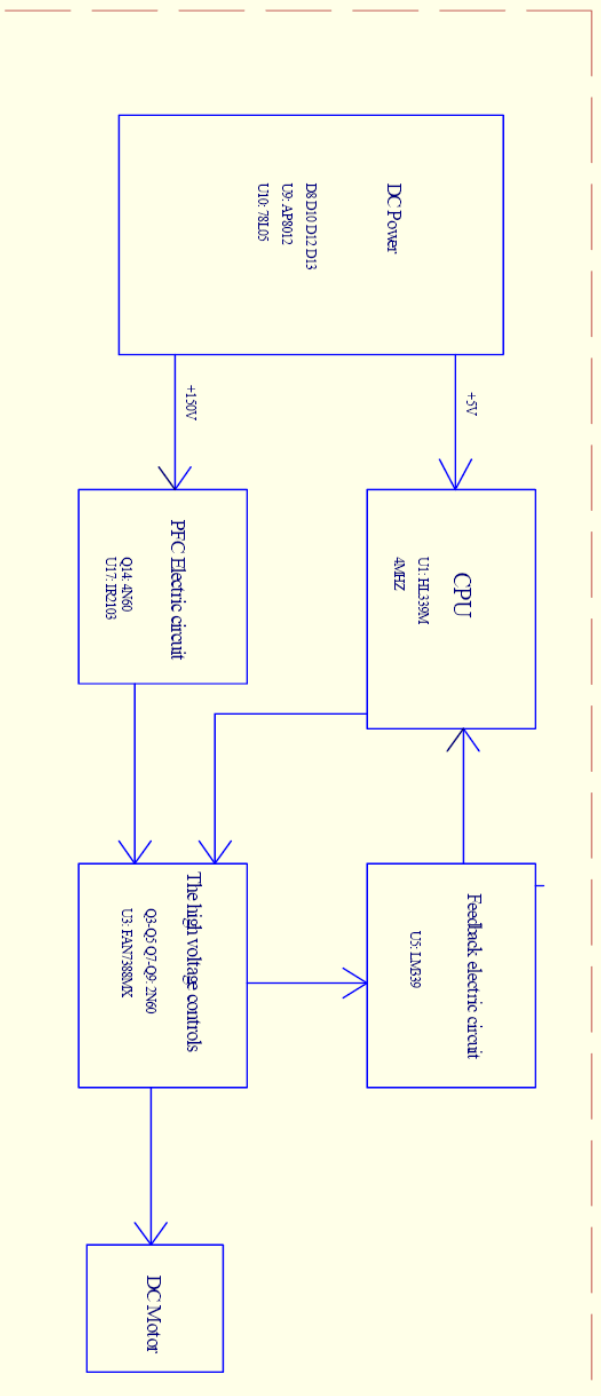


```

graph TD
    AC120V[AC120V] --> DCPOWER[DC POWER]
    DCPOWER --> ANT[ANT]
    DCPOWER --> CPU[CPU]
    CPU --> Receive[315MHz Receive module]
    Receive --> CPU
    CPU --> LampPower[Lamp Power]
    LampPower --> Lamp[Lamp]
    CPU --> TOUT[TOUT]
    
```

The diagram illustrates the system architecture. It starts with an AC120V input connected to a DC POWER block. The DC POWER block is connected to an ANT (Antenna) and a CPU block. The CPU block is connected to a 315MHz Receive module, which in turn is connected back to the CPU. The CPU block is also connected to a Lamp Power block, which is connected to a Lamp. The CPU block has a TOUT output.



Title		
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