Microprocessors & Interfacing

Analog Input/Output (III)

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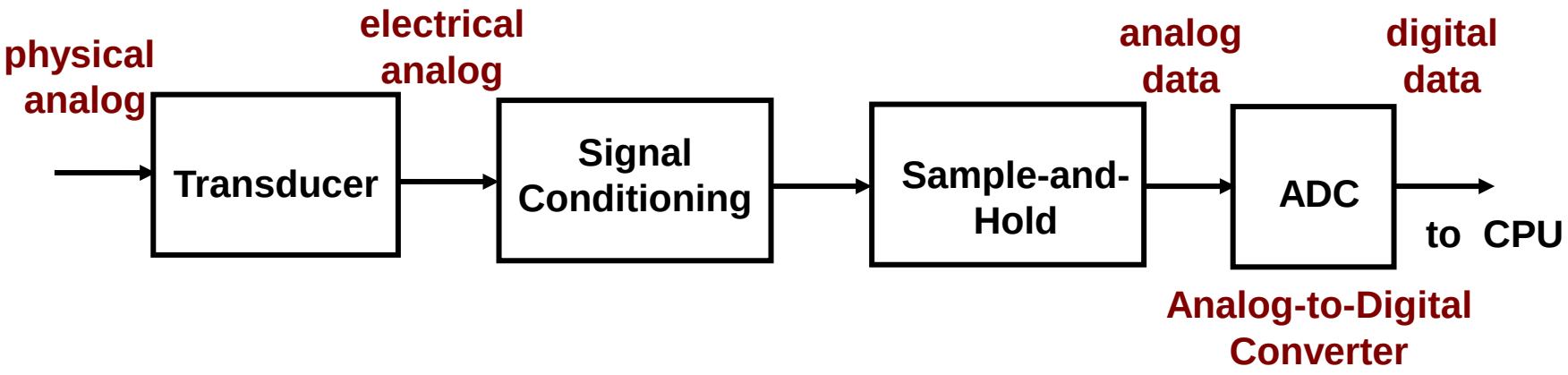
Lecture Overview

- Analog input
  - Analog-to-Digital (A/D) Conversion
  - AVR ADC*
    - extended topic (new)

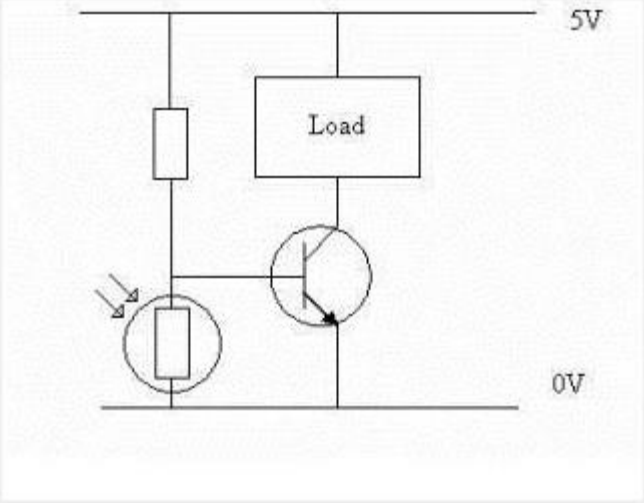
A/D Conversion



Sensor*

- **Example**
  - **LDR (Light Dependent Resistor)**

A typical LDR



LDR controlled transistor circuit

Data Acquisition and Conversion

- A transducer converts physical values to electrical signals, either voltages or currents.
- Signal conditioner performs the following tasks:
  - Isolation and buffering 隔离和缓冲
    - The input to ADC may need to be protected from dangerous voltages such as static charges or reversed polarity voltages.
  - Amplification 放大
    - To ensure the full-scale signal from the analog results in a full-scale signal to ADC.
  - Bandwidth limiting
    - The signal conditioning provides a low-pass filter to limit the range of frequencies that can be digitized.

Data Acquisition and Conversion (cont.)

- The sample-and-hold circuit samples the signal and holds it steady for A/D conversion.
  - What is the sample frequency?
- The ADC converts the sampled signal to digital data
  - The output of ADC connected to CPU through three-state buffers.

Shannon's Sampling Theorem

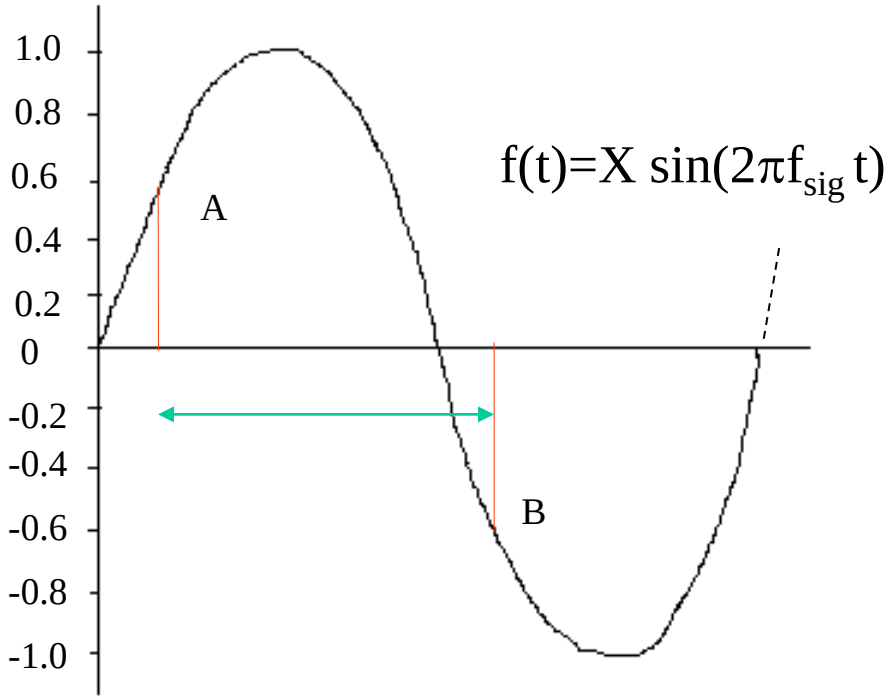
- To preserve the full information in the signal, it is necessary to sample at the frequency *at least twice the maximum frequency of the signal*.
  - This minimum sampling frequency is known as the *Nyquist rate*.
  - A signal can be exactly reproduced if it is sampled at a frequency greater than or equal to its Nyquist rate.

Aliasing

- If the sampling frequency is less than Nyquist rate, the waveform is said to be undersampled.
- Undersampled signal, when converted back into a continuous time signal, will exhibit a phenomenon called ***aliasing***.

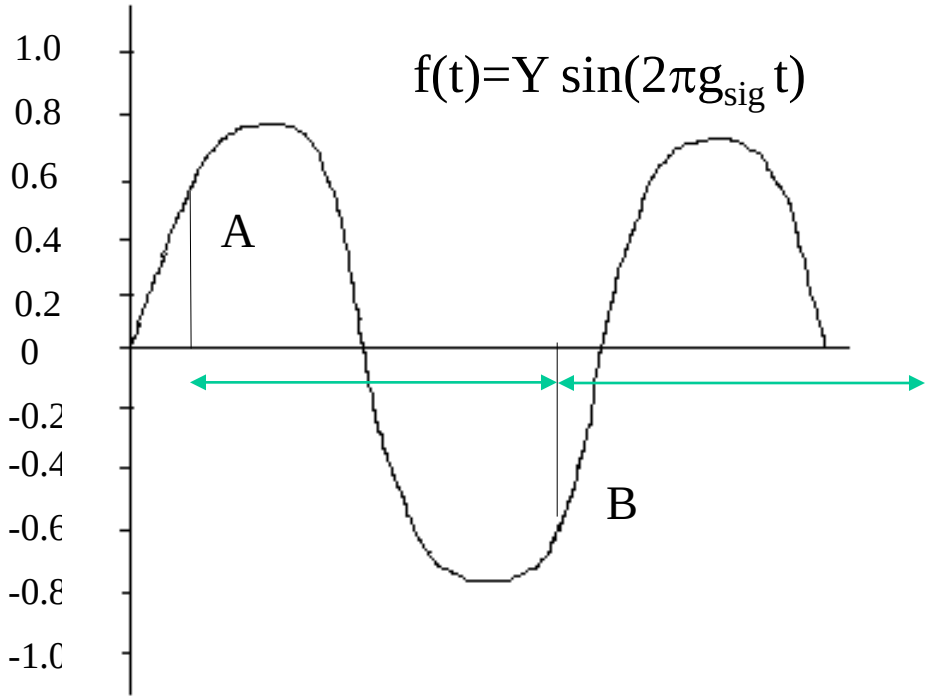
Sample Examples

- Sampled at twice of the signal frequency.



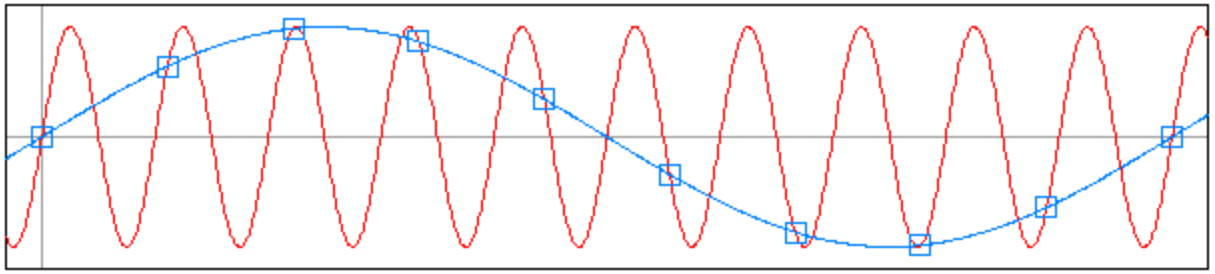
Sample Examples

- Undersampled, with sample frequency less than twice of the signal frequency

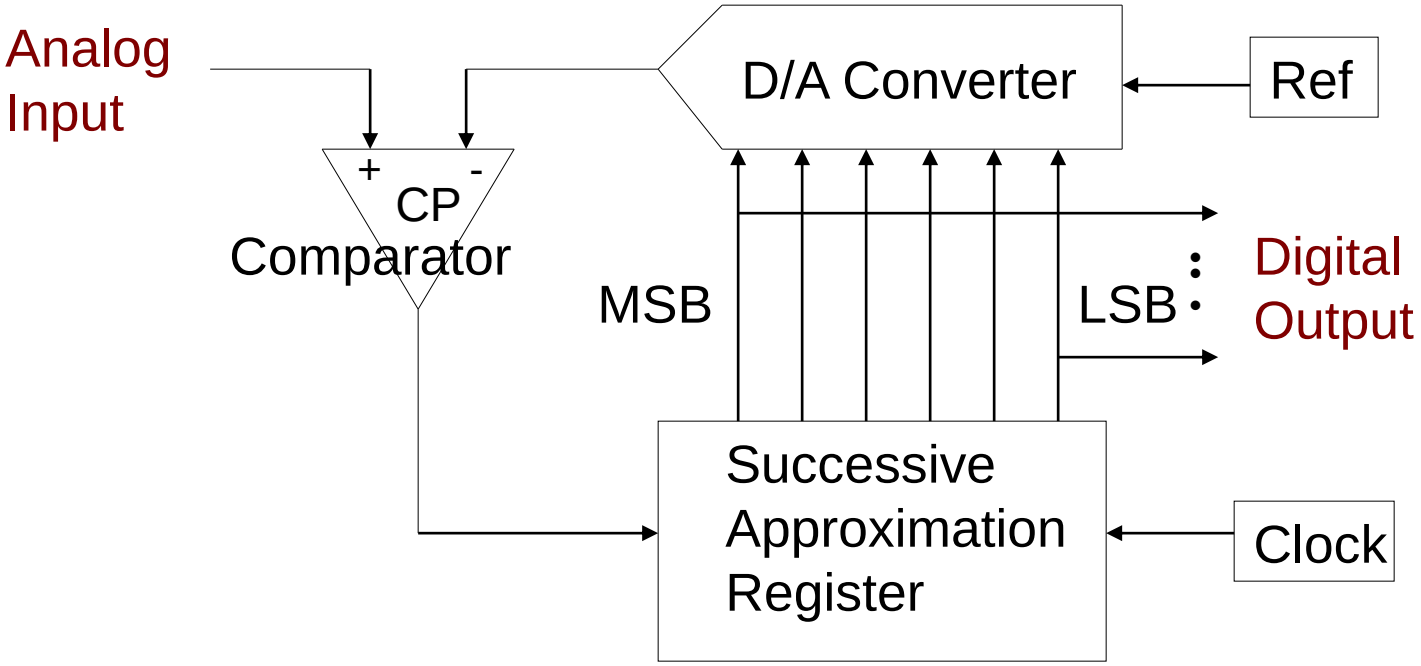


Aliasing (cont.)

- Aliasing
  - the presence of unwanted components in the reconstructed signal. These components were not present when the original signal was sampled.
  - See the demonstration below



Successive Approximation Converter

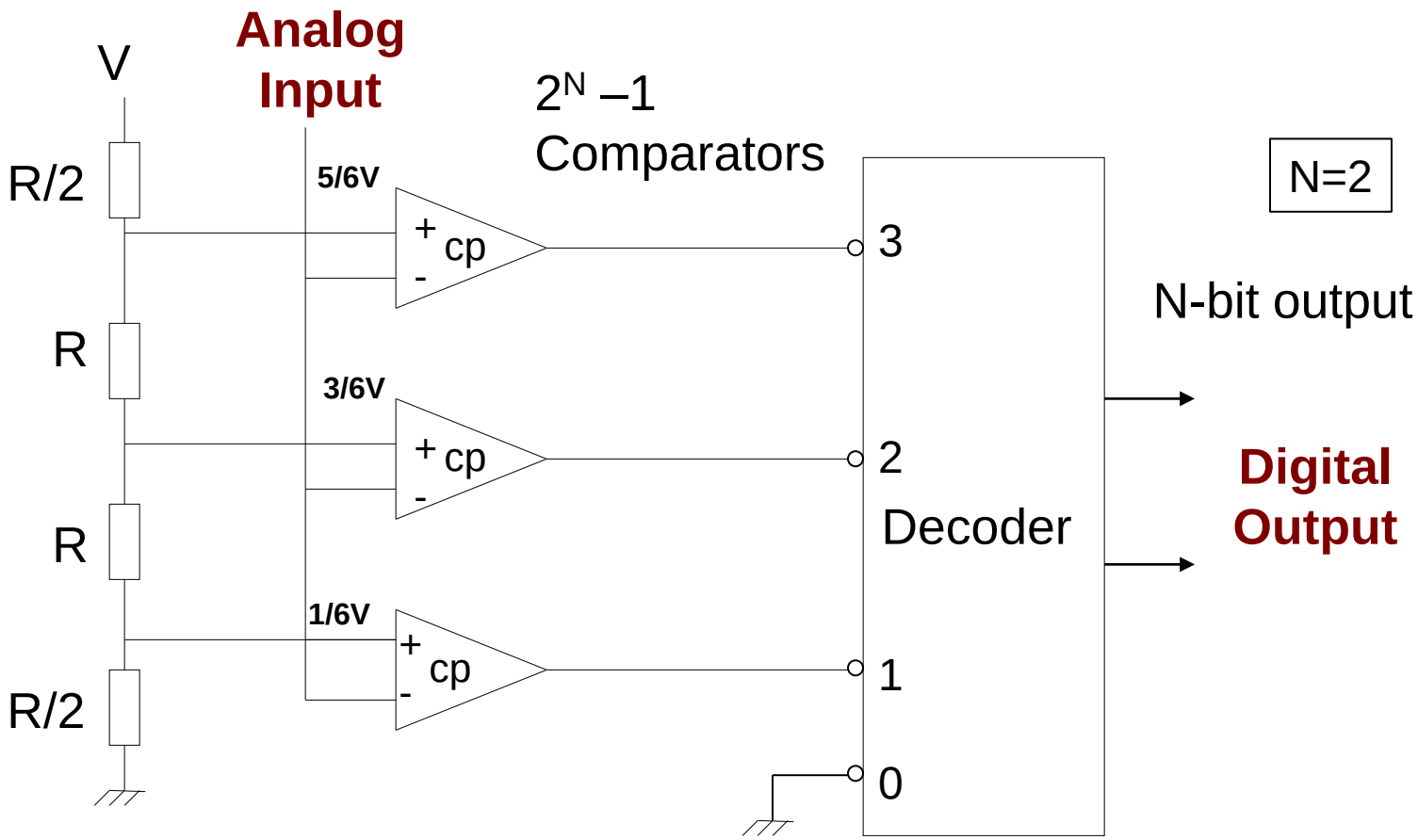


- MSB: most significant bit
- LSB: least significant bit

Successive Approximation A/D Converter (cont.)

- Each bit in the *successive approximation register* is tested, starting at the most significant bit and working toward the least significant bit.
  - As each bit is set, the output of the D/A converter is compared (by the comparator) with the analog input.
  - If the D/A output is lower than the input signal, the bit remains set and the next bit is tried.
- For an N-bit output, such a bit test needs to be performed N times.

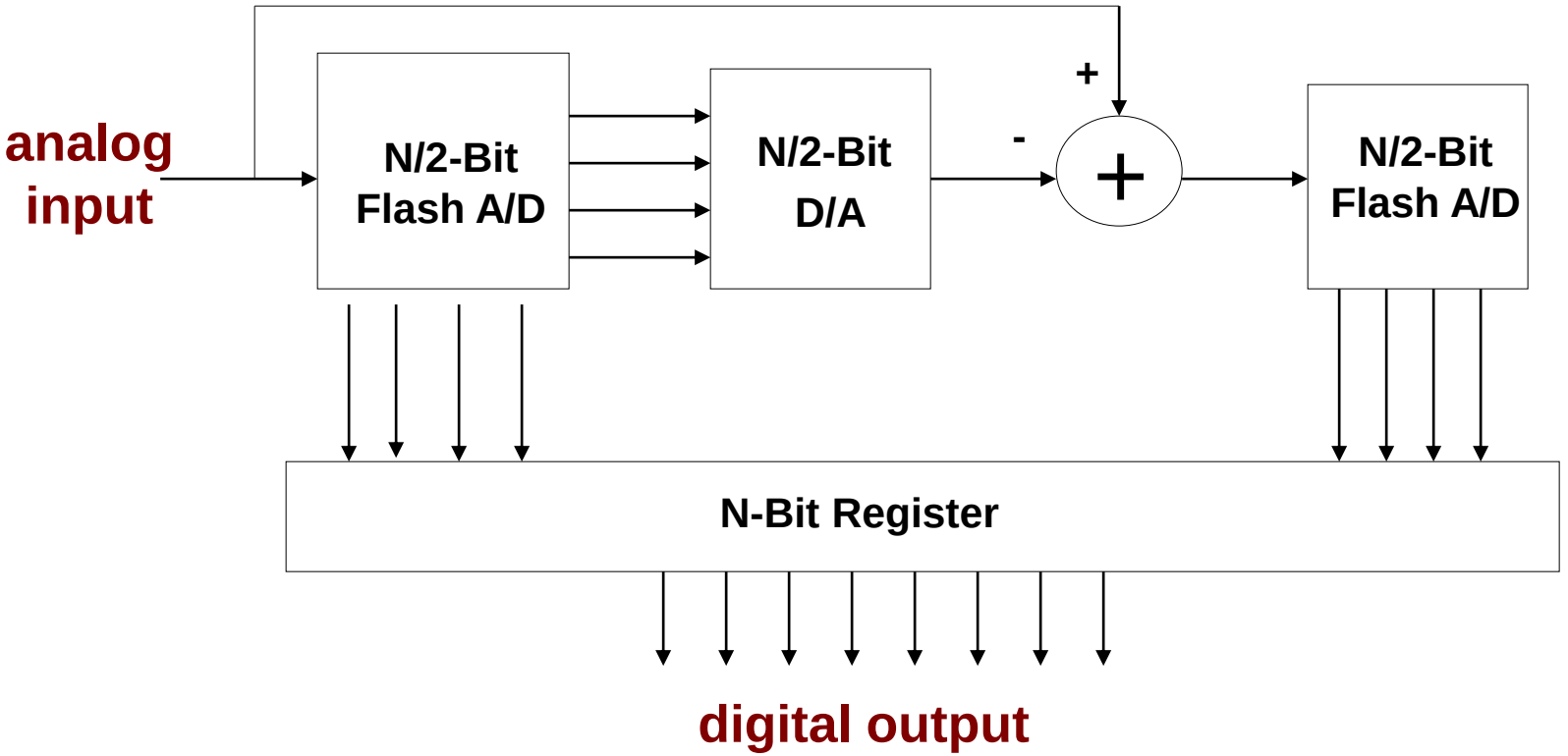
Parallel A/D Converter



Parallel A/D Converter (cont.)

- For an N-bit output, the ADC consists of
  - an array of 2^N-1 comparators
    - produces a (2^N-1)-bit code
  - a 2^N-to-N decoder
    - converts 2^N-bit input code to N-bit binary value
- The design is
  - fast
    - hence called **flash ADC**
  - but more costly than the successive approximation ADC

Two-Stage Parallel A/D Converter*



Two-Stage Parallel A/D Converter*

- The input signal is converted in two steps:
  - First, a coarse estimate is found by the first parallel A/D converter. This digital value is sent to the D/A converter and the adder, where it is subtracted from the original analog value.
  - Next, the difference is converted by the second parallel converter and the result combined with that from the first ADC gives the digitized value.

Two-Stage Parallel A/D Converter*

- The two-stage ADC has nearly the performance of the parallel converter but without the need of 2^N –1 comparators.
- It offers high resolution and high-speed conversion for applications like video signal processing.

A/D Converter Specifications

- Conversion time
  - The time required to complete a conversion of the input signal.
  - Determines the upper signal frequency limit that can be sampled without aliasing.

$$f_{MAX}=1/(2*\text{conversion time})$$

- Resolution
  - the smallest analog input signal that can be digitized
  - is determined by the number of bits used by DAC

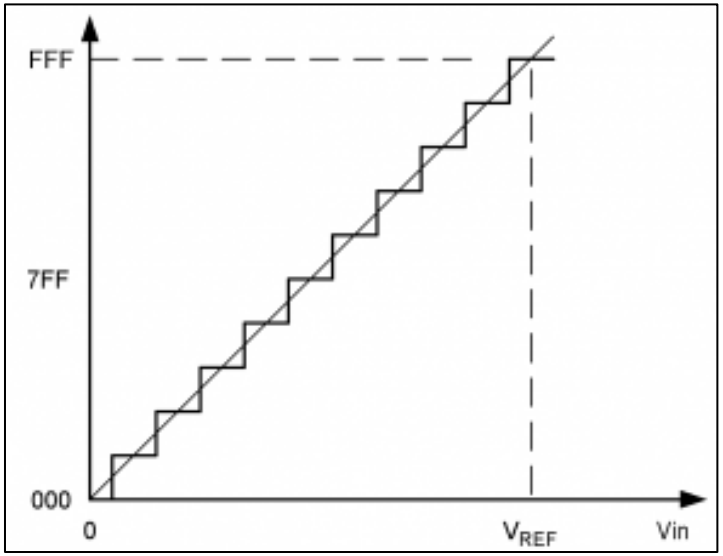
A/D Converter Specifications (cont.)

- Accuracy
  - Describes how close the digital output is to the theoretically expected digital output for a given analog input.
  - Determines how many bits in the digital output code represent useful information about the input signal.

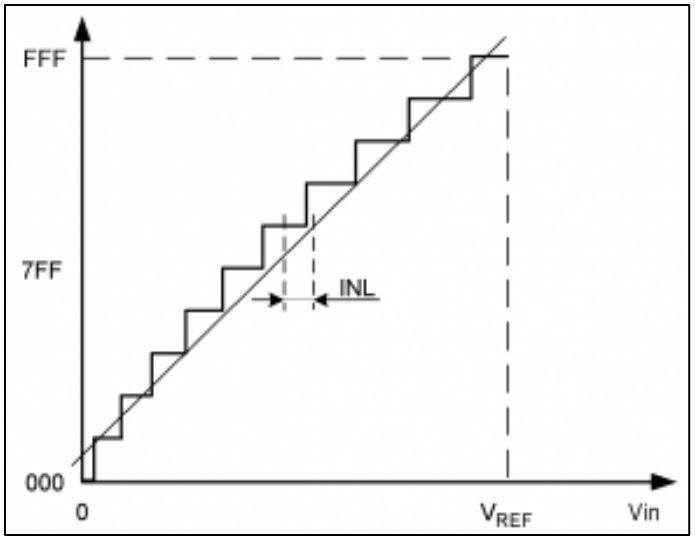
An n-bit ADC may have less than n bits of accuracy!

A/D Converter Specifications (cont.)

- Linearity
  - The derivation in output codes from the real value



Linear



Non-linear

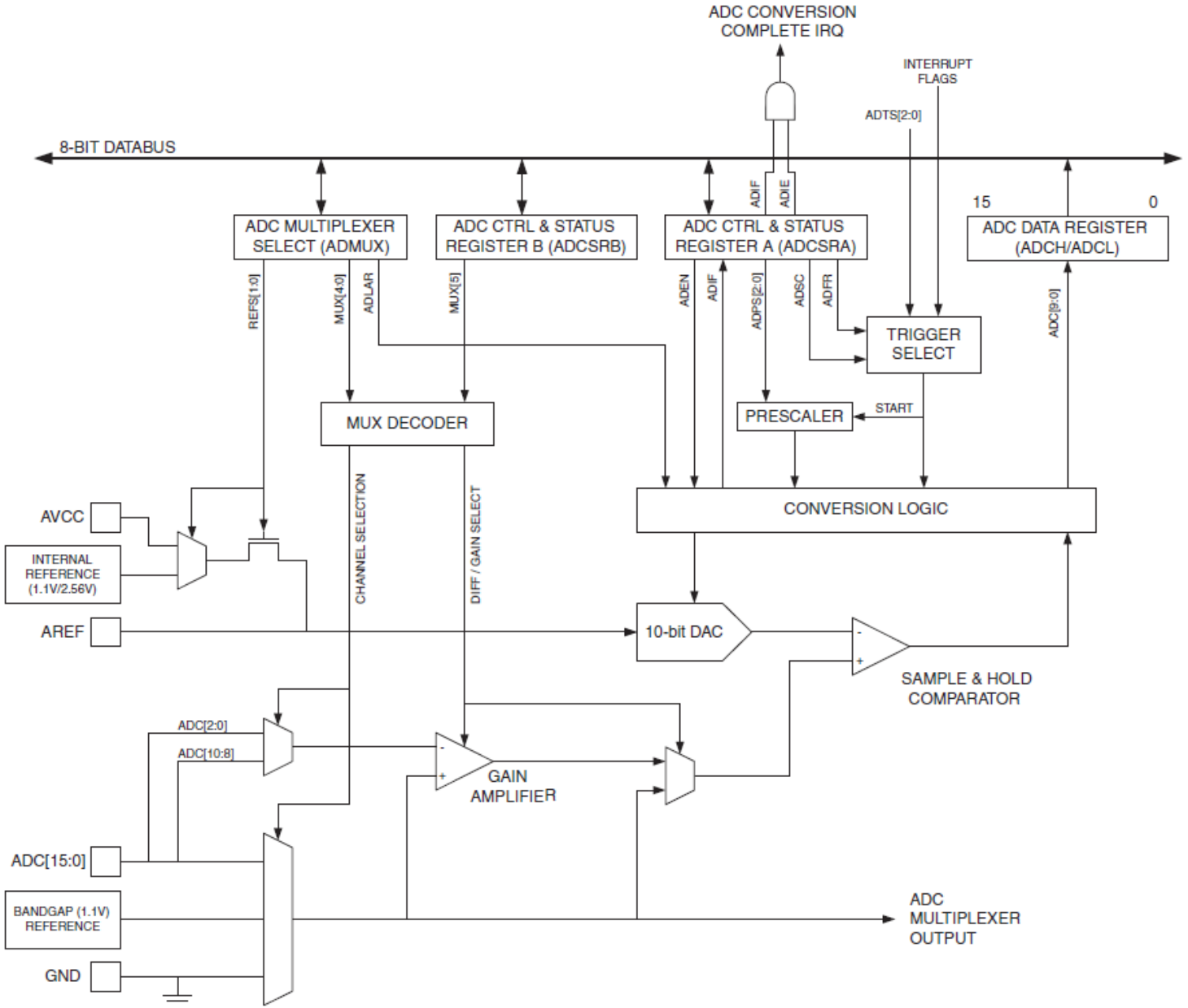
A/D Converter Specifications (cont.)

- Aperture time
  - The time that the A/D converter is “looking” at the input signal.
  - It is usually equal to the conversion time.

ADC on AVR MCU

- 10-bit successive approximation ADC
- Multiple channels
  - Allowing 8/16 single-ended voltage inputs
    - Each refers to 0V (GND)
- Multiple choices of supply voltage
- A brief description of its operation is presented in the next slides.
  - More information can be found from the MCU datasheet.

ADC Structural Diagram



ADMUX

- ADC Multiplexor Section Register
  - ADLAR (bit 5): ADC Left Adjust Result
    - When the bit is set, the conversion result in ADCH:ADCL aligned to the left; otherwise right
  - MUX4:0: Analog Channel Selection
    - Determine which analog channels are connected to ADC

Bit	7	6	5	4	3	2	1	0
(0x7C)	REFS1	REFS0	ADLAR	MUX4	MUX3	MUX2	MUX1	MUX0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

ADMUX (cont.)

- ADC Multiplexor Section Register
  - REFS1-0: voltage reference selection

Bit	7	6	5	4	3	2	1	0
(0x7C)	REFS1	REFS0	ADLAR	MUX4	MUX3	MUX2	MUX1	MUX0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

Table 26-3. Voltage Reference Selections for ADC

REFS1	REFS0	Voltage Reference Selection[1]
0	0	AREF, Internal V_{REF} turned off
0	1	AVCC with external capacitor at AREF pin
1	0	Internal 1.1V Voltage Reference with external capacitor at AREF pin
1	1	Internal 2.56V Voltage Reference with external capacitor at AREF pin

ADCSA

- ADC Control and Status Register
  - ADEN: ADC Enable
    - 1: enable; 0: disable
  - ADSC: Start Conversion
  - ADIE: ADC Interrupt Enable

Bit	7	6	5	4	3	2	1	0
(0x7A)	ADEN	ADSC	ADATE	ADIF	ADIE	ADPS2	ADPS1	ADPS0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

ADCSA (cont.)

- ADC Control and Status Register
  - ADPS2:0: ADC Prescaler Select Bits

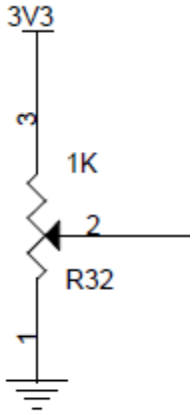
Bit	7	6	5	4	3	2	1	0
(0x7A)	ADEN	ADSC	ADATE	ADIF	ADIE	ADPS2	ADPS1	ADPS0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

Table 26-5. ADC Prescaler Selections

ADPS2	ADPS1	ADPS0	Division Factor
0	0	0	2
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

Example

- Convert an analog voltage input from POT to digital value and display the value on LEDs.
  - POT: potentiometer



Example (cont.)

```
.include "m2560def.inc"

.def temp=r16

    ser temp
    out DDRC, temp

    ; Vref=AVcc
    ldi temp, 1<<REFS0
    sts ADMUX, temp
    ;set prescaller to 128 and enable ADC
    ldi temp, (1<<ADPS2)|(1<<ADPS1)|(1<<ADPS0)|(1<<ADEN)
    sts ADCSRA, temp

    ; Left-adjust, Ref. = AVCC, Single-ended on ADC0 is default
    ldi temp, (1<<ADLAR) | (1<<REFS0)
    sts ADMUX, temp
```

Example (cont.)

```
 new_conversion:
    ; start conversion, with the single conversion mode
    lds temp, ADCSRA
    ori temp, (1<<ADSC)
    sts ADCSRA, temp

    ;wait until the conversion is complete
loop:
    lds temp, ADCSRA
    sbrc temp, ADSC ; also the two lines can be used.
    jmp loop


    ; on completion of the conversion, display the digital output on Port C
    lds temp, ADCH
    out PORTC, temp

    rjmp new_conversion
```

Reading Material

- Chapter 13: Analog Input and Output. Microcontrollers and Microcomputers by Fredrick M. Cady.
- AVR Mega2560 Data Sheet.
  - ADC

Homework

1. The A/D converter conversion time is 100 us. What is the maximum frequency of a signal that can be digitalized without aliasing occurring?

Homework

2. Assume the successive approximation converter shown below is to convert a signal in the range of 0~5 volts into 3 bit binary integer. What is the output value from the converter if the input is 3.2 volts?